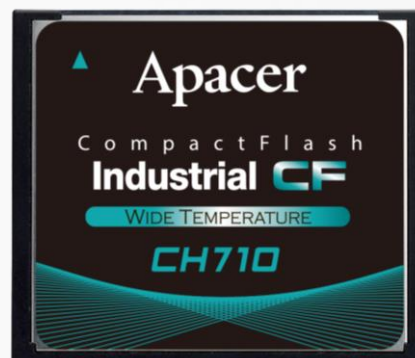


Halogen-free & RoHS Recast Compliant **CH710-CF** Industrial CF Product Specifications



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Version 1.4



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Specifications Overview:

- **CompactFlash Association Specification Revision 6.1 Standard Interface**
 - ATA command set compatible
 - ATA transfer mode supports: PIO Mode 6, Multiword DMA Mode 4, Ultra DMA Mode 6 in True-IDE mode
- **Capacity**
 - 8, 16, 32, 64 GB
- **Performance***
 - Sequential read: Up to 115 MB/sec
 - Sequential write: Up to 80 MB/sec
 - Random read (4K): Up to 3,100 IOPS
 - Random write (4K): Up to 2,100 IOPS
- **Flash Management**
 - Global Wear Leveling
 - Built-in BCH ECC capable of correcting up to 96 bits in 1KB data
 - Supports S.M.A.R.T commands
 - Flash Block Management
 - Flash Translation Layer: Page Mapping
 - Power Failure Management
 - SLC-liteX
- **Reliability**
 - Supply voltage power-down detection for full power-down robustness
- **NAND Flash Type: 3D TLC (BiC3)**
- **MTBF: >3,000,000 hours**
- **Endurance (in drive writes per day: DWPD)**
 - 8 GB: 20.47 DWPD
 - 16 GB: 9.87 DWPD
 - 32 GB: 10.54 DWPD
 - 64 GB: 8.84 DWPD
- **Temperature Range**
 - Operating:
 - Standard: 0°C to 70°C
 - Wide: -40°C to 85°C
 - Storage: -40°C to 100°C
- **Supply Voltage**
 - 3.3V ± 5%
 - 5.0V ± 10%
- **Power Consumption***

Operating Voltage: 3.3V

 - Active mode: 185 mA
 - Standby mode: 10 mA

Operating Voltage: 5.0V

 - Active mode: 190 mA
 - Standby mode: 10 mA
- **Connector Type**
 - 50 pins female
- **Form Factor**
 - 36.4mm x 42.8mm x 3.3mm
 - Net Weight: 9.95g ± 5%
- **Halogen Free**
- **RoHS Recast Compliant**
 - Complies with 2011/65/EU Standard

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

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1. General Descriptions

Apacer's value-added Industrial CompactFlash Card offers high performance, high reliability and power-efficient storage. Regarding standard compliance, this CompactFlash Card complies with CompactFlash specification revision 6.1, supporting transfer modes up to Programmed Input Output (PIO) Mode 6, Multi-word Direct Memory Access (DMA) Mode 4, Ultra DMA Mode 6 in True-IDE Mode.

Apacer's value-added CFC provides complete PCMCIA – ATA functionality and compatibility. Apacer's CompactFlash technology is designed for applications in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications such as the new generation of Digital Single Lens Reflex (DSLR) cameras.

1.1 Intelligent Endurance Design

1.1.1 Error Correction Code (ECC)

The CompactFlash card is programmed with BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms capable of correcting up to 96 random bits in 1KB bytes data.

High performance is achieved through hardware-based error detection and correction.

1.1.2 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global Wear leveling is an important mechanism that levels out the wearing of blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

1.1.3 S.M.A.R.T. Technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

| Code | SMART Subcommand |
|------|-----------------------------------|
| D0h | READ DATA |
| D1h | READ ATTRIBUTE THRESHOLDS |
| D2h | ENABLE/DISABLE ATTRIBUTE AUTOSAVE |
| D4h | EXECUTE OFF-LINE IMMEDIATE |
| D5h | SMART READ LOG |
| D6h | SMART WRITE LOG |
| D8h | ENABLE OPERATIONS |

| Code | SMART Subcommand |
|------|--------------------|
| D9h | DISABLE OPERATIONS |
| DAh | RETURN STATUS |

General SMART attribute structure

| Byte | Description |
|-------|-------------|
| 0 | ID (Hex) |
| 1 – 2 | Status Flag |
| 3 | Value |
| 4 | Worst |
| 5*-11 | Raw Data |

*Byte 5: LSB

SMART attribute ID list

| ID (Hex) | Attribute Name |
|------------|-------------------------|
| 12 (0x0C) | Power Cycle Count |
| 160 (0xA0) | Initial Bad Block Count |
| 161 (0xA1) | Bad Block Count |
| 162 (0xA2) | Spare Block Count |
| 163 (0xA3) | Max. Erase Count |
| 164 (0xA4) | Avg. Erase Count |
| 241 (0xF1) | Total LBAs Written |
| 242 (0xF2) | Total LBAs Read |

1.1.4 Flash Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

1.1.5 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

1.1.6 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

1.1.7 SLC-liteX

SLC-liteX is based on 3D NAND technology. The firmware is carefully tweaked by our engineering team so as to offer the greatest number of P/E cycles in this format – 30,000, which is 10 times more than MLC or industrial 3D TLC. The longest lifespans are therefore available at reasonable cost.

2. Functional Block

The CompactFlash Card (CFC) includes a controller and flash media, as well as the CompactFlash standard interface. Figure 2-1 shows the functional block diagram.

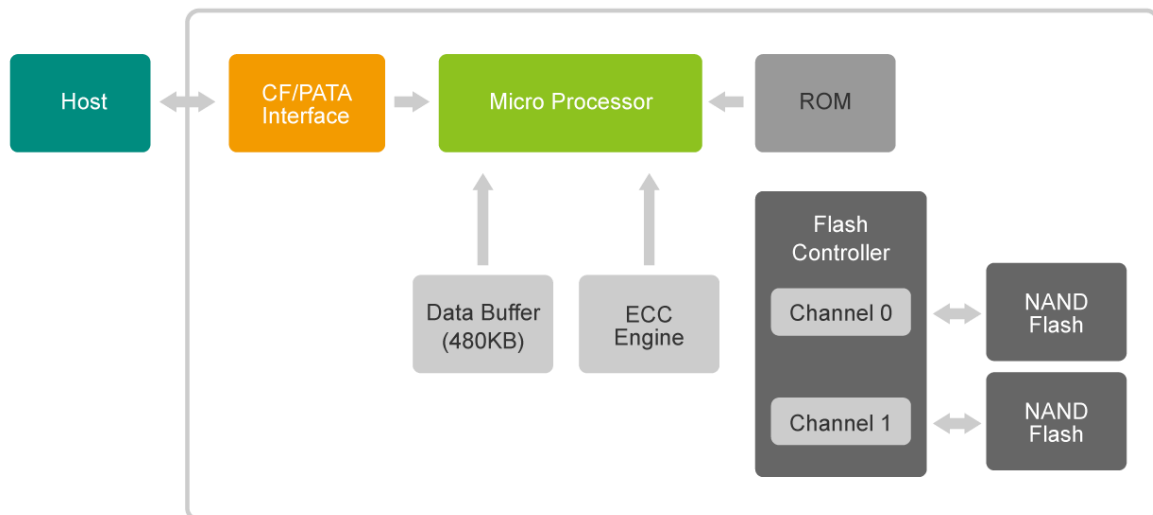


Figure 2-1 Functional Block Diagram

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A “#” suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1 Pin Assignments

| Pin No. | Memory card mode | | I/O card mode | | True IDE mode | |
|---------|------------------|--------------|---------------|--------------|--------------------|--------------|
| | Signal name | Pin I/O type | Signal name | Pin I/O type | Signal name | Pin I/O type |
| 1 | GND | - | GND | - | GND | - |
| 2 | D3 | I/O | D3 | I/O | D3 | I/O |
| 3 | D4 | I/O | D4 | I/O | D4 | I/O |
| 4 | D5 | I/O | D5 | I/O | D5 | I/O |
| 5 | D6 | I/O | D6 | I/O | D6 | I/O |
| 6 | D7 | I/O | D7 | I/O | D7 | I/O |
| 7 | #CE1 | I | #CE1 | I | #CS0 | I |
| 8 | A10 | I | A10 | I | A10 ¹ | I |
| 9 | #OE | I | #OE | I | #ATA SEL | I |
| 10 | A9 | I | A9 | I | A9 ¹ | I |
| 11 | A8 | I | A8 | I | A8 ¹ | I |
| 12 | A7 | I | A7 | I | A7 ¹ | I |
| 13 | VCC | - | VCC | - | VCC | - |
| 14 | A6 | I | A6 | I | A6 ¹ | I |
| 15 | A5 | I | A5 | I | A5 ¹ | I |
| 16 | A4 | I | A4 | I | A4 ¹ | I |
| 17 | A3 | I | A3 | I | A3 ¹ | I |
| 18 | A2 | I | A2 | I | A2 | I |
| 19 | A1 | I | A1 | I | A1 | I |
| 20 | A0 | I | A0 | I | A0 | I |
| 21 | D0 | I/O | D0 | I/O | D0 | I/O |
| 22 | D1 | I/O | D1 | I/O | D1 | I/O |
| 23 | D2 | I/O | D2 | I/O | D2 | I/O |
| 24 | WP | O | #IOIS16 | O | #IOCS16 | O |
| 25 | #CD2 | O | #CD2 | O | #CD2 | O |
| 26 | #CD1 | O | #CD1 | O | #CD1 | O |
| 27 | D11 | I/O | D11 | I/O | D11 | I/O |
| 28 | D12 | I/O | D12 | I/O | D12 | I/O |
| 29 | D13 | I/O | D13 | I/O | D13 | I/O |
| 30 | D14 | I/O | D14 | I/O | D14 | I/O |
| 31 | D15 | I/O | D15 | I/O | D15 | I/O |
| 32 | #CE2 | I | #CE2 | I | #CS1 | I |
| 33 | #VS1 | O | #VS1 | O | #VS1 | O |
| 34 | #IORD | I | #IORD | I | #IORD | I |
| 35 | #IOWR | I | #IOWR | I | #IOWR | I |
| 36 | #WE | I | #WE | I | #WE | I |
| 37 | RDY/-BSY | O | #IREQ | O | INTRQ | O |
| 38 | VCC | - | VCC | - | VCC | - |
| 39 | #CSEL | I | #CSEL | I | #CSEL | I |
| 40 | #VS2 | O | #VS2 | O | #VS2 | O |
| 41 | RESET | I | RESET | I | #RESET | I |
| 42 | #WAIT | O | #WAIT | O | IORDY | O |
| 43 | #INPACK | O | #INPACK | O | DMARQ ² | O |
| 44 | #REG | I | #REG | I | DMACK ² | I |
| 45 | BVD2 | O | #SPKR | O | #DASP | I/O |
| 46 | BVD1 | O | #STSCHG | O | #PDIAG | I/O |

| Pin No. | Memory card mode | | I/O card mode | | True IDE mode | |
|---------|------------------|--------------|---------------|--------------|---------------|--------------|
| | Signal name | Pin I/O type | Signal name | Pin I/O type | Signal name | Pin I/O type |
| 47 | D8 | I/O | D8 | I/O | D8 | I/O |
| 48 | D9 | I/O | D9 | I/O | D9 | I/O |
| 49 | D10 | I/O | D10 | I/O | D10 | I/O |
| 50 | GND | - | GND | - | GND | - |

1. The signal should be grounded by the host.
2. Connection required when UDMA is in use.

4. Product Specifications

4.1 Capacity

Capacity specifications of the CompactFlash Card series (CFC) are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

| Capacity | Total bytes* | Cylinders | Heads | Sectors | Total LBA |
|----------|----------------|-----------|-------|---------|-------------|
| 8 GB | 8,012,390,400 | 15,525 | 16 | 63 | 15,649,200 |
| 16 GB | 16,013,942,784 | 16,383 | 16 | 63 | 31,277,232 |
| 32 GB | 32,017,047,552 | 16,383 | 16 | 61 | 62,533,296 |
| 64 GB | 64,023,257,088 | 16,383 | 16 | 63 | 125,045,424 |

Note:

Display of total bytes varies from operating systems.

Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.

Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of the CompactFlash Card is listed in Table 4-2.

Table 4-2 Performance Specifications

| Performance | Capacity | 8 GB | 16 GB | 32 GB | 64 GB |
|---------------------------------|--------------------------------|-------|-------|-------|-------|
| | Sequential Read* (MB/s) | | 90 | 115 | 115 |
| Sequential Write* (MB/s) | | 38 | 75 | 80 | 80 |
| Random Read IOPS** (4K) | | 3,100 | 3,100 | 3,100 | 3,000 |
| Random Write IOPS** (4K) | | 1,300 | 1,900 | 2,000 | 2,100 |

Note:

Results may differ from various flash configurations or host system setting.

*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

**Random performance measured using IOMeter with Queue Depth 32.

4.3 Environmental Specifications

Environmental specifications of the CompactFlash Card are shown in Table 4-3.

Table 4-3 Environmental Specifications

| Item | Specifications |
|-------------------------|--|
| Operating temp. | 0°C to 70°C (Standard); -40°C to 85°C (Wide) |
| Non-operating temp. | -40°C to 100°C |
| Operating vibration | 7.69 GRMS, 20~2000 Hz/random (compliant with MIL-STD-810G) |
| Non-operating vibration | 4.02 GRMS, 15 ~ 2000 Hz/sine (compliant with MIL-STD-810G) |
| Operating shock | 50G, 11ms, half-sine wave |
| Non-operating shock | 1,500G, 0.5ms, half-sine wave |

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in the CompactFlash card. The prediction result for the CompactFlash card is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

The CompactFlash Card complies with the following global standards:

- CE
- FCC
- Halogen-free
- EMC
- RoHS Recast (2011/65/EU)

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Drive Writes Per Day

| Capacity | Drive Writes Per Day |
|----------|----------------------|
| 8 GB | 20.47 |
| 16 GB | 9.87 |
| 32 GB | 10.54 |
| 64 GB | 8.84 |

Note:

- This estimation complies with JEDEC JESD-219, enterprise endurance workload of sequential data with payload size distribution.
- Flash vendor guaranteed 3D TLC SLC-liteX P/E cycle: 30K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024 GB
- DWPD (Drive Write Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (SLC-liteX warranty: 5 years)

5. Software Interface

5.1 CF-ATA Command Set

Table 5-1 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 5-1 CFC-ATA Command Set

| Command Set | Command | Code | Protocol |
|------------------------------|------------------------------|------------|-------------------|
| CFA Feature Set | Request Sense | 03h | Non-data |
| | Write Sectors Without Erase | 38h | PIO data-out |
| | Erase Sectors | C0h | Non-data |
| | Write Multiple Without Erase | CDh | PIO data-out |
| | Translate Sector | 87h | PIO data-in |
| | Write Multiple w/o erase | CDh | PIO |
| | Write sector(s) w/o erase | 38h | PIO |
| General Feature Set | Execute Drive Diagnostic | 90h | Device diagnostic |
| | Flush Cache | E7h | Non-data |
| | Identify Device | ECh | PIO data-in |
| | Read DMA | C8h | DMA |
| | Read Multiple | C4h | PIO data-in |
| | Read Sector(s) | 20h or 21h | PIO data-in |
| | Read Verify Sector(s) | 40h or 41h | Non-data |
| | Set Feature | EFh | Non-data |
| | Set Multiple Mode | C6h | Non-data |
| | Write DMA | CAh | DMA |
| | Write Multiple | C5h | PIO data-out |
| | Write Sector(s) | 30h or 31h | PIO data-out |
| | NOP | 00h | Non-data |
| | Read Buffer | E4h | PIO data-in |
| | Write Buffer | E8h | PIO data-out |
| | Set Feature | EFh | Non-data |
| Power Management Feature Set | Check Power Mode | E5h or 98h | Non-data |
| | Idle | E3h or 97h | Non-data |
| | Idle Immediate | E1h or 95h | Non-data |
| | Set sleep mode | E6h or 99h | Non-data |
| | Sleep | E6h or 99h | Non-data |
| | Standby | E2h or 96h | Non-data |

| Command Set | Command | Code | Protocol |
|---------------------------------|----------------------------------|------------|--------------|
| | Standby Immediate | E0h or 94h | Non-data |
| Security Mode Feature Set | Security Set Password | F1h | PIO data-out |
| | Security Unlock | F2h | PIO data-out |
| | Security Erase Prepare | F3h | Non-data |
| | Security Erase Unit | F4h | PIO data-out |
| | Security Freeze Lock | F5h | Non-data |
| | Security Disable Password | F6h | PIO data-out |
| | Media Lock | DEh | Non-data |
| | Media Unlock | DFh | Non-data |
| SMART Feature Set | SMART Disable Operations | B0h | Non-data |
| | SMART Enable/Disable Autosave | B0h | Non-data |
| | SMART Enable Operations | B0h | Non-data |
| | SMART Return Status | B0h | Non-data |
| | SMART Execute Off-line Immediate | B0h | Non-data |
| | SMART Read Data | B0h | PIO data-in |
| Host Protected Area Feature Set | Data Set Management | 06h | DMA |
| | Read Native Max Address | F8h | Non-data |
| | Read native max addr Ext | 27h | Non-data |
| | Set Max Address | F9h | Non-data |
| Others | Format Track | 50h | PIO data-out |
| | Initialize Drive Parameters | 91h | Non-data |
| | Recalibrate | 1Xh | Non-data |
| | Seek | 7Xh | Non-data |
| | Write Verify | 3Ch | PIO data-out |
| | Download Microcode | 92h | PIO data-in |
| | Download Microcode DMA | 93h | DMA |
| 48-bit Address Feature Set | Read Sector Ext | 24h | PIO data-in |
| | Read DMA Ext | 25h | DMA |
| | Read Multiple Ext | 29h | PIO data-in |
| | Write Sector Ext | 34h | PIO data-out |
| | Write DMA Ext | 35h | DMA |
| | Read Verify Sector Ext | 42h | Non-data |
| | Write Multiple FUA Ext | CEh | PIO data-out |
| | Flush Cache Ext | EAh | Non-data |
| | Read Log Ext | 2Fh | PIO |
| Read Log DMA Ext | 57h | DMA | |

| Command Set | Command | Code | Protocol |
|-------------|---------------------|------|----------|
| | Write DMA FUA Ext | 3Dh | DMA |
| | Write Log Ext | 3Fh | PIO |
| | Write Log DMA Ext | 57h | DMA |
| | Write Multiple Ext | 39h | PIO |
| | Set max address Ext | 37h | Non-data |

6. Electrical Specifications

6.1 Operating Voltage

Table 6-1 lists the supply voltage for the CompactFlash Card.

Table 6-1 Operating Range

| Item | Range |
|------------------------|------------------|
| Supply voltage at 3.3V | 3.135 to 3.465 V |
| Supply voltage at 5V | 4.75 to 5.25 V |

6.2 Power Consumption

Table 6-2 and 6-3 list the power consumption for the CompactFlash Card.

Table 6-2 Power Consumption @3.3V

| Capacity Mode | 8 GB | 16 GB | 32 GB | 64 GB |
|------------------|------|-------|-------|-------|
| Active (mA) | 150 | 175 | 180 | 185 |
| Standby (mA) | 10 | 10 | 10 | 10 |

Table 6-3 Power Consumption @5V

| Capacity Mode | 8 GB | 16 GB | 32 GB | 64 GB |
|------------------|------|-------|-------|-------|
| Active (mA) | 150 | 180 | 190 | 190 |
| Standby (mA) | 10 | 10 | 10 | 10 |

Note:

*All values are typical and may vary depending on flash configurations or host system settings.

**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

6.3 AC/DC Characteristics

The following section provides general AC/DC characteristics of this CompactFlash card.

6.3.1 DC Characteristics

- Absolute Maximum Ratings**

| Parameter | Remark |
|--|----------------------|
| Supply voltage on 3.3V supply pins | -0.5V to 3.63V |
| Supply voltage on 1.2V supply pins | -0.5V to 1.32V |
| Voltage on CF/PATA pins with respect to ground | -0.5V to 6.7V |
| Voltage on flash pins with respect to ground | -0.5V to VDDF + 0.5V |
| Voltage on GPIO8..15 pins with respect to ground | -0.5V to + 0.5V |
| Voltage on other pins with respect to ground | -0.5V to VCC + 0.5V |
| Storage temperature | -40°C to 125°C |

- DC Parameters**

| Parameter | Remark |
|----------------------------|----------------------------|
| Supply Voltage VCC, AVCC | 3.30V ± 5% |
| Supply Voltage VDDF | 3.30V ± 5%, 1.80V ± 5% |
| Supply Voltage VDDC, AVDDC | 1.2V ± 5% |
| Temperature (ambient) | -40°C to 85°C (industrial) |

- General DC characteristics**

| Symbol | Parameter | Min | Max | Unit | Remark |
|---------------------|--------------------------|----------------------|-----------------------|------|--|
| V _{IL, H} | Input LOW Voltage | -0.3 | 0.8 | V | CF/PATA host interface |
| V _{IH, H} | Input HIGH Voltage | 2.0 | 5.5 | V | |
| V _{IL} | Input LOW Voltage | -0.3 | 0.3*V _{DD} | V | V _{DD} is VDDF (flash IF) or VCC (other pins) |
| V _{IH} | Input HIGH Voltage | 0.7*V _{DD} | *V _{DD} +0.3 | V | |
| V _{OL} | Output LOW Voltage | | 0.4 | V | at 4mA (12mA for DASP) |
| V _{OH, H} | Output HIGH Voltage | VCC-0.51 | | V | at 6mA, CF/PATA pins |
| V _{OH} | Output HIGH Voltage | V _{DD} -0.4 | | V | at 4mA, other pins |
| I _{LI} | Input Leakage Current | -5 | 5 | µA | if not pull-up/pull-down |
| I _{LO} | Output Leakage Current | -5 | 5 | µA | if not pull-up/pull-down |
| I _{PURB33} | Pull-Up Current | 1.5 | 2.5 | mA | F _n RB0..3 pins, at 3.3V |
| I _{PURB18} | Pull-Up Current | 0.6 | 1.4 | mA | F _n RB0..3 pins, at 1.8V |
| I _{PU} | Pull-Up Current | 15 | 110 | µA | other pins |
| I _{PD} | Pull-Down Current | 20 | 160 | µA | |
| C _{IO} | Input/Output Capacitance | | 10 | pF | |
| ESD | ESD Protection | 2 | | kV | HBM |

● **Operating Currents**

| Symbol | Parameter | Typ | Max | Unit | Remark |
|--------------------|---------------|-----|------|------|---|
| I _{VCC} | VCC current | | | | |
| | Sleep mode | 3.0 | 4.5 | mA | |
| | Operating | 15 | 85 | mA | in UDMA6 mode |
| I _{VDDC} | VDDC current | | | | at 25°C |
| | Sleep mode | 1 | 6 | mA | |
| | Operating | 50 | 80 | mA | at 160 MHz CPU clock |
| I _{VDDF} | VDDF current | | | | at 80 MHz flash clock, typical CF card PCB |
| | at 1.8V | 8 | 25 | mA | |
| | at 3.3V | 15 | 60 | mA | |
| I _{AVCC} | AVCC current | 0.4 | 0.6 | mA | |
| I _{AVDDC} | AVDDC current | | | | |
| | Sleep mode | 20 | 200 | μA | |
| | Operating | 4.5 | 14.0 | mA | typ for 400 MHz PLL |

● **Voltage Regulator Parameters**

1.2V switching regulator (supply for VDDC)

| Symbol | Parameter | Min | Typ | Max | Unit | Remark |
|------------------|----------------------------|------|------|------|------|--------------|
| V _I | Input voltage (CIN) | 3.00 | 3.30 | 3.60 | V | |
| V _O | Output voltage | 1.15 | 1.20 | 1.25 | V | |
| I _O | Average load current | | | 600 | mA | |
| V _{R20} | Output ripple 20 MHz BW | | | 15 | mV | |
| T _{on} | Startup time | | 50 | | μS | |
| L _O | Output filtering inductor | | 2.2 | | μH | |
| C _O | Output filtering capacitor | | 2x10 | | μF | 2 capacitors |
| ESR | Output capacitor ESR | 2 | | 200 | mΩ | |
| ESL | Output capacitor ESL | | | 4 | nH | |

1.8V linear regulator (supply for VDDF)

| Symbol | Parameter | Min | Typ | Max | Unit | Remark |
|-----------------|----------------------------|------|------|------|------|--------|
| V _I | Input voltage (FIN) | 3.00 | 3.30 | 3.60 | V | |
| V _O | Output voltage (FOUT) | 1.72 | 1.80 | 1.88 | V | |
| I _O | Average load current | | | 150 | mA | |
| T _{on} | Startup time | | 10 | | μS | |
| C _O | Output filtering capacitor | | 2.2 | | μF | |
| ESR | Output capacitor ESR | 4 | | 200 | mΩ | |
| ESL | Output capacitor ESL | | | 4 | nH | |

● **SLEVCC Switchable ISO7816 Power Supply Output Parameters**

| Symbol | Parameter | Min | Typ | Max | Unit | Remark |
|------------------|-------------------------|-------------|-----|-----|------|--------------|
| V _{SLE} | SLEVCC Output Voltage | VCC -0.2 | | VCC | V | When enabled |
| I _{SLE} | SLEVCC Output Current | | | 30 | mA | |
| T _{SLE} | SLEVCC Ramp Up Time | | 10 | | μS | |
| C _{SLE} | SLEVCC Output Capacitor | | 0.1 | | μF | |

● **Supply Voltage Monitor Parameters**

| Symbol | Parameter | Min | Typ | Max | Unit | Remark |
|---------------------|------------------------------|------|------|------|------|--------------------------|
| ReS _{1.2R} | 1.2V Reset rising threshold | | 95 | | % | of 1.2V regulator output |
| ReS _{3.3R} | 3.3V Reset rising threshold | 2.23 | 2.35 | 2.47 | V | at VCC pin |
| ReS _{3.3F} | 3.3V Reset falling threshold | 2.15 | 2.20 | 2.25 | V | at VCC pin |
| S _{5VH} | 5V sense high threshold | 4.31 | 4.40 | 4.49 | V | at SENSE5V pin |
| S _{5VL} | 5V sense low threshold | 3.01 | 3.07 | 3.13 | V | at SENSE5V pin |
| S _{3V} | 3.3V sense threshold | 2.84 | 2.90 | 2.96 | V | at SENSE3V pin |

The ReS_{1.2R} and ReS_{3.3R} thresholds are used by the reset logic to release the internal reset signal on a system power-on. The ReS_{3.3L} threshold is used to assert the internal reset signal on a system power down.

The S_{3V} and S_{5V} threshold comparators generate interrupts to the firmware. The S_{3V} comparator normally monitors the 3.3V VCC supply, the S_{5V} comparator normally monitors the 5V or 3.3V module supply. The S_{3V} interrupt can be used to stop accesses to the flash memory early on a system power down event. The S_{5V} interrupt can be used to implement a supply hold-up functionality when a backup energy source is available.

In packages that do not have the SENSE3V pin, SENSE3V is internally connected to VCC.

6.3.2 AC Characteristics

The AC Characteristics reference the timing diagrams of the CompactFlash Specification Revision 4.1 and the symbols in these timing diagrams. The AC characteristics are valid for a supply voltage of 3.3V ± 5%.

● **Attribute Memory Read and Write Characteristics**

See figures 25 and 26 in the CF Specification Revision 4.1.

| Symbol | Parameter | Min | Max | Unit |
|------------|-------------------------------------|-----|-----|------|
| tc(R) | Read cycle time | 250 | | ns |
| ta(A) | Address access time | | 250 | ns |
| ta(CE) | Card Enable access time | | 250 | ns |
| ta(OE) | Output Enable access time | | 125 | ns |
| tdis(CE) | Output disable time from CE | | 100 | ns |
| tdis(OE) | Output disable time from OE | | 100 | ns |
| ten(CE) | Output enable time from CE | 5 | | ns |
| ten(OE) | Output enable time from OE | 5 | | ns |
| tv(A) | Data valid time from address change | 0 | | ns |
| tsu(A) | Address setup time | 30 | | ns |
| tc(W) | Write cycle time | 250 | | ns |
| tw(WE) | Write pulse time | 150 | | ns |
| trec(WE) | Address hold time from WE | 30 | | ns |
| tsu(D-WEH) | Data setup time for WE | 80 | | ns |
| th(D) | Data hold time | 30 | | ns |

● **Common Memory Read and Write Characteristics**

See figures 27 and 28 in the CF Specification Revision 4.1. The wait functionality is not used.

| Symbol | Parameter | Min | Max | Unit |
|------------|-------------------------------|-----|-----|------|
| tc | Cycle time | 80 | | ns |
| ta(OE) | Output Enable access time | | 45 | ns |
| tdis(OE) | Output disable time from OE | | 45 | ns |
| tsu(A) | Address setup time | 10 | | ns |
| th(A) | Address hold time | 10 | | ns |
| tsu(CE) | Card Enable setup time | 0 | | ns |
| th(CE) | Card Enable hold time | 10 | | ns |
| tw(WE) | Write pulse time | 55 | | ns |
| tsu(A) | Address setup time for WE | 10 | | ns |
| tsu(CE) | Card Enable setup time for WE | 0 | | ns |
| tsu(D-WEH) | Data setup time for WE | 30 | | ns |
| th(D) | Data hold time | 10 | | ns |
| trec(WE) | Write recovery time | 15 | | ns |

● **I/O Access Read and Write Characteristics**

See figures 29 and 30 in the CF Specification Revision 4.1. The wait functionality is not used.

| Symbol | Parameter | Min | Max | Unit |
|-----------------|-----------------------------------|-----|-----|------|
| td(IORD) | Data delay after IORD | | 45 | ns |
| th(IORD) | Data hold following IORD | 5 | | ns |
| tw(IORD) | IORD pulse width | 55 | | ns |
| tsuA(IORD) | Address setup time for IORD | 15 | | ns |
| thA(IORD) | Address hold time from IORD | 10 | | ns |
| tsuCE(IORD) | Card Enable setup time for IORD | 5 | | ns |
| thCE(IORD) | Card Enable hold time from IORD | 10 | | ns |
| tsuREG(IORD) | REG setup time for IORD | 5 | | ns |
| thREG(IORD) | REG hold time from IORD | 0 | | ns |
| tdfINPACK(IORD) | INPACK delay falling from IORD | 0 | 45 | ns |
| tdrINPACK(IORD) | INPACK delay rising from IORD | | 45 | ns |
| tdfIOIS16(ADR) | IOIS16 delay falling from address | | 35 | ns |
| tdrIOIS16(ADR) | IOIS16 delay rising from address | | 35 | ns |
| tsu(IOWR) | Data setup time for IOWR | 15 | | ns |
| th(IOWR) | Data hold time from IOWR | 5 | | ns |
| tw(IOWR) | IOWR pulse width | 55 | | ns |
| tsuA(IOWR) | Address setup time for IOWR | 15 | | ns |
| thA(IOWR) | Address hold time from IOWR | 10 | | ns |
| tsuCE(IOWR) | Card Enable setup time for IOWR | 5 | | ns |
| thCE(IOWR) | Card Enable hold time from IOWR | 10 | | ns |
| tsuREG(IOWR) | REG setup time for IOWR | 5 | | ns |
| thREG(IOWR) | REG hold time from IOWR | 0 | | ns |

- **True-IDE PIO Mode Read and Write Characteristics**

See figure 31 in the CF Specification Revision 4.1. The IORDY functionality is not used.

| Symbol | Parameter | Min | Max | Unit |
|--------|----------------------------------|-----|-----|------|
| t0 | Cycle time | 80 | | ns |
| t1 | Address setup time for IORD/IOWR | 10 | | ns |
| t9 | Address hold time from IORD/IOWR | 10 | | ns |
| t2 | IORD/IOWR pulse width | 55 | | ns |
| t2i | IORD/IOWR recovery time | 20 | | ns |
| t5 | Data setup time for IORD | 10 | | ns |
| t6 | Data hold following IORD | 5 | | ns |
| t6z | Output disable time from IORD | | 20 | ns |
| t3 | Data setup time for IOWR | 15 | | ns |
| t4 | Data hold following IOWR | 5 | | ns |

- **True-IDE MDMA Mode Read and Write Characteristics**

See figure 32 in the CF Specification Revision 4.1.

| Symbol | Parameter | Min | Max | Unit |
|----------|-----------------------------------|-----|-----|------|
| tO | Cycle time | 80 | | ns |
| tD | IORD/IOWR pulse width | 55 | | ns |
| tE | IORD data access | | 45 | ns |
| tF | Data hold following IORD | 5 | | ns |
| tG | Data setup time for IORD/IOWR | 10 | | ns |
| tH | Data hold following IOWR | 5 | | ns |
| tI | DMACK setup time for IORD/IOWR | 0 | | ns |
| tJ | DMACK hold following IORD/IOWR | 5 | | ns |
| tKR, tKW | IORD/IOWR recovery time | 20 | | ns |
| tLR, tLW | IORD/IOWR to DMARQ delay | | 35 | ns |
| tM | CS0, CS1 setup for IORD/IOWR | 5 | | ns |
| tN | CS0, CS1 hold following IORD/IOWR | 10 | | ns |
| tZ | Output disable time from DMACK | | 25 | ns |

- **True-IDE UDMA Mode Read and Write Characteristics**

The interface timing in the True-IDE UDMA modes is not only depending on the interface hardware, but also on the correct setup of the UDMA registers in the firmware, according to the UDMA transfer mode selected by the host. With a correct register setup, the interface timing complies to the UDMA Mode 0 to Mode 7 timing specifications of the CF Specification Revision 6.1, and to the UDMA Mode 0 to Mode 6 timing specifications of the ATA/ATAPI-7 Standard.

- **Toggle Mode Flash Memory Interface Characteristics**

The AC Characteristics for the flash memory interface are based on the F9 flash interface clock cycle time. τ is $\frac{1}{2}$ of the flash interface clock cycle time configured in the preformat. In Toggle mode, the valid range for τ is 5ns to 10ns. The table lists the flash memory interface timing based on τ , valid for a load of not more than 45pF on the flash interfacepins.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|-----------------------------------|-------------|-----|-------------|------|
| t _{CALS} | CLE, ALE setup time | 6 τ - 2 | | | ns |
| t _{CALH} | CLE, ALE hold time | 1.5 τ - 2 | | | ns |
| t _{CS} | CE# setup time | 6 τ - 2 | | | ns |
| t _{CH} | CE# hold time | 1.5 τ - 2 | | | ns |
| t _{CAS} | Data (command/address) setup time | 2.5 τ - 2 | | | ns |
| t _{CAH} | Data (command/address) hold time | 1.5 τ - 2 | | | ns |
| t _{WC} | Write cycle time | 7.5 τ | | | ns |
| t _{WP} | WE# low pulse width | 4 τ - 2 | | | ns |
| t _{WH} | WE# high pulse width | 4 τ - 2 | | | ns |
| t _{DSC} | DQS cycle time | | 2 τ | | ns |
| t _{DQSH} | DQS high time | 0.94 τ | | | ns |
| t _{DQSL} | DQS low time | 0.94 τ | | | ns |
| t _{DS} | Data output setup time to DQS | 0.5 τ - 1.5 | | | ns |
| t _{DH} | Data output hold time from DQS | 0.5 τ - 1.5 | | | ns |
| t _{RC} | Read cycle time | | 2 τ | | ns |
| t _{RP} | RE# low pulse width | 0.94 τ | | | ns |
| t _{REH} | RE# high pulse width | 0.94 τ | | | ns |
| t _{DQSQ} | DQS to input data skew | | | 0.5 τ - 1.6 | ns |
| t _{QH} | Input data hold from DQS | 0.5 τ + 0.8 | | | ns |

● **ONFI-2 Mode Flash Memory Interface Characteristics**

The AC Characteristics for the flash memory interface are based on the F9 flash interface clock cycle time. τ is ½ of the flash interface clock cycle time configured in the preformat. In ONFI-2 mode, the valid range for τ is 5ns to 10ns. The table lists the flash memory binterface timing based on τ, valid for a load of not more than 45pF on the flash interface pins.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|-----------------------------------|-------------|-----|-------------|------|
| t _{CK} | Average clock cycle time | | 2 τ | | ns |
| t _{CKH} | Clock high time | 0.94 τ | | 1.06 τ | ns |
| t _{CKL} | Clock low time | 0.94 τ | | 1.06 τ | ns |
| t _{CALS} | ALE, CLE, W/R# setup time to CLK | τ - 3 | | | ns |
| t _{CALH} | ALE, CLE, W/R# hold time from CLK | τ - 3 | | | ns |
| t _{CS} | CE# setup time to CLK | 5 τ - 3 | | | ns |
| t _{CH} | CE# hold time from CLK | τ - 3 | | | ns |
| t _{CAS} | Data output setup time to CLK | τ - 3 | | | ns |
| t _{CAH} | Data output hold time from CLK | τ - 3 | | | ns |
| t _{DQSS} | DQS phase | 2 τ - 2 | | 2 τ + 2 | ns |
| t _{DQSH} | DQS high time | 0.94 τ | | 1.06 τ | ns |
| t _{DQSL} | DQS low time | 0.94 τ | | 1.06 τ | ns |
| t _{DS} | Data output setup time to DQS | 0.5 τ - 1.5 | | | ns |
| t _{DH} | Data output hold time from DQS | 0.5 τ - 1.5 | | | ns |
| t _{DQSQ} | DQS to input data skew | | | 0.5 τ - 1.6 | ns |
| t _{QH} | Input data hold from DQS | 0.5 τ + 0.8 | | | ns |

7. Physical Characteristics

7.1 Dimensions

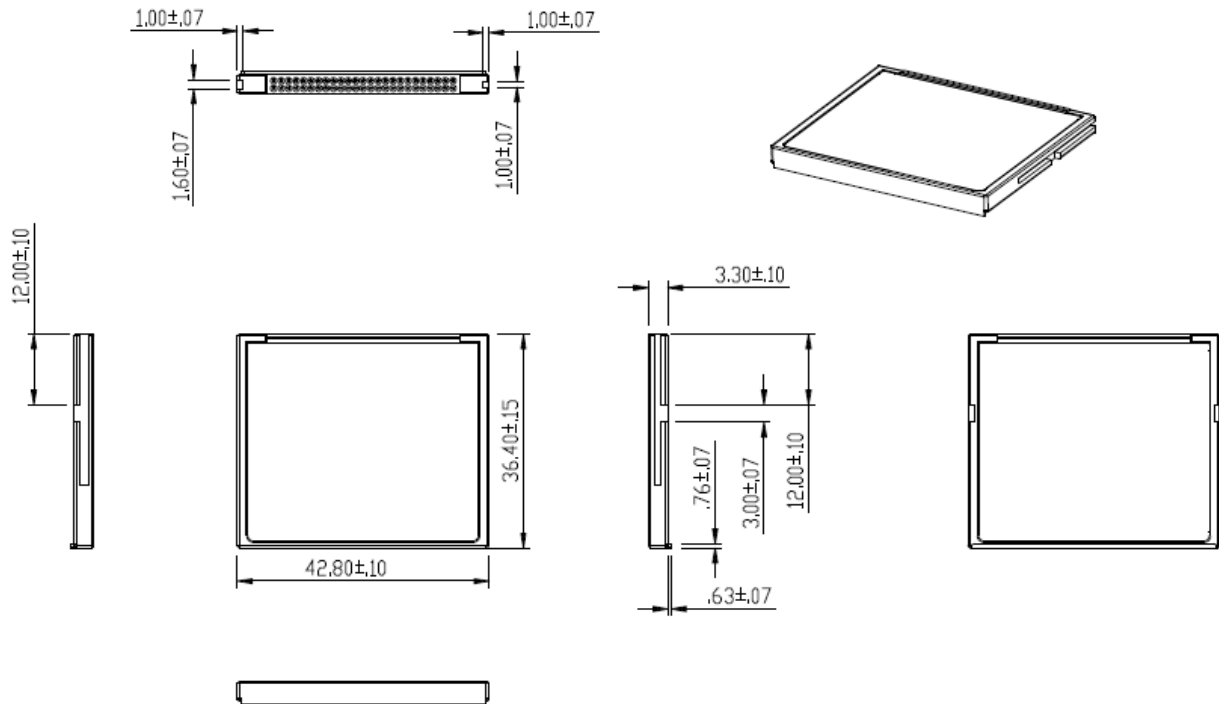


Figure 7-1 Physical Dimensions.

Unit: mm

7.2 Net Weight

Table 7-1 Net Weight

| Capacity | Net Weight (g ± 5%) |
|----------|---------------------|
| 8 GB | 8.38 |
| 16 GB | 8.92 |
| 32 GB | 9.95 |
| 64 GB | 9.95 |

8. Product Ordering Information

8.1 Product Code Designations

| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|
| | A | G | 2 | . | 7 | 1 | 8 | X | X | A | . | X | X | X | 0 | 1 |

| | |
|--|---|
| Code 1-3 (Product Line & Form Factor) | MDC+CF Card |
| Code 5-6 (Model/Solution) | CH710-CF |
| Code 7-8 (Product Capacity) | 8F: 8GB (SLC-liteX) 8G: 16GB (SLC-liteX) 8H: 32GB (SLC-liteX) 8J: 64GB (SLC-liteX) |
| Code 9 (Flash Type & Product Temp) | L: 3D SLC-liteX Standard temperature M: 3D SLC-liteX Wide temperature |
| Code 10 (Product Spec) | A: Non-Removable |
| Code 12-14 (Version Number) | Random numbers generated by system |
| Code 15-16 (Firmware Version) | 01: CFHA001C |

8.2 Valid Combinations

| Capacity | Standard Temperature | Wide Temperature |
|----------|----------------------|------------------|
| 8GB | AG2.718FLA.00101 | AG2.718FMA.00101 |
| 16GB | AG2.718GLA.00101 | AG2.718GMA.00101 |
| 32GB | AG2.718HLA.00101 | AG2.718HMA.00101 |
| 64GB | AG2.718JLA.00101 | AG2.718JMA.00101 |

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

| Revision | Description | Date |
|----------|---|-----------|
| 1.0 | Initial release | 3/19/2020 |
| 1.1 | Updated product photo on the cover page | 3/26/2020 |
| 1.2 | Removed VDDG from 6.3.1 DC Characteristics | 8/24/2020 |
| 1.3 | Updated MTBF to >3,000,000 hours on Specifications Overview page and at 4.4 Mean Time Between Failures (MTBF) | 3/17/2021 |
| 1.4 | Updated 8.1 Product Code Designations by changing the description of code 5-6 to CH710-CF | 3/19/2021 |