

IGLOOe Low Power Flash FPGAs with Flash*Freeze Technology

Features and Benefits

Low Power

- 1.2 V to 1.5 V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- Low-Power Active FPGA Operation
- Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Flash*Freeze Pin Allows Easy Entry to / Exit from Ultra-Low-Power Flash*Freeze Mode

High Capacity

- 600 k to 3 Million System Gates
- 108 to 504 kbits of True Dual-Port SRAM
- Up to 341 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Instant On Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off
- 250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance

In-System Programming (ISP) and Security

- ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532-compliant)
- FlashLock[®] Designed to Secure FPGA Contents

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Pro (Professional) I/O

- 700 Mbps DDR, LVDS-Capable I/Os
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation

- Bank-Selectable I/O Voltages—Up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7 V to 3.6 V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14 V to 1.575 V
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay
- Schmitt Trigger Option on Single-Ended Inputs
- Weak Pull-Up/Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the IGLOO[®]e Family

Clock Conditioning Circuit (CCC) and PLL

- Six CCC Blocks, Each with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

Embedded Memory

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)

ARM Processor Support in IGLOOe FPGAs

- M1 IGLOOe Devices—Cortex™-M1 Soft Processor Available with or without Debug

Table 1 • IGLOOe Product Family

| IGLOOe Devices | AGLE600 | AGLE3000 |
|---|---------|------------|
| ARM-Enabled IGLOOe Devices | | M1AGLE3000 |
| System Gates | 600,000 | 3,000,000 |
| VersaTiles (D-flip-flops) | 13,824 | 75,264 |
| Quiescent Current (typical) in Flash*Freeze Mode (µW) | 49 | 137 |
| RAM kbits (1,024 bits) | 108 | 504 |
| 4,608-Bit Blocks | 24 | 112 |
| FlashROM Kbits (1,024 bits) | 1 | 1 |
| Secure (AES) ISP | Yes | Yes |
| CCCs with Integrated PLLs | 6 | 6 |
| VersaNet Globals ¹ | 18 | 18 |
| I/O Banks | 8 | 8 |
| Maximum User I/Os | 165 | 341 |
| Package Pins FBGA | FG256 | FG484 |

Notes:

1. Refer to the [Cortex-M1 Handbook](#) for more information.
2. Six chip (main) and twelve quadrant global networks are available.
3. For devices supporting lower densities, refer to the [IGLOO Low-Power Flash FPGAs with Flash*Freeze Technology datasheet](#).

I/Os Per Package ¹

| IGLOOe Devices | AGLE600 | | AGLE3000 | |
|----------------------------|-------------------------------|------------------------|-------------------------------|------------------------|
| ARM-Enabled IGLOOe Devices | | | M1AGLE3000 | |
| Package | I/O Types | | | |
| | Single-Ended I/O ¹ | Differential I/O Pairs | Single-Ended I/O ¹ | Differential I/O Pairs |
| FG256 | 165 | 79 | – | – |
| | – | – | 341 | 168 |

Notes:

- When considering migrating your design to a lower- or higher-density device, refer to the [IGLOOe FPGA Fabric User's Guide](#) to ensure compliance with design and board migration requirements.
- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- For AGLE3000 devices, the usage of certain I/O standards is limited as follows:
 - SSTL3(I) and (II): up to 40 I/Os per north or south bank
 - LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
 - SSTL2(I) and (II) / GTL+ 2.5 V / GTL 2.5 V: up to 72 I/Os per north or south bank
- FG256 and FG484 are footprint-compatible packages.
- When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (VREF) per minibank (group of I/Os).
- When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.
- "G" indicates RoHS-compliant packages. Refer to ["IGLOOe Ordering Information"](#) on page III for the location of the "G" in the part number.

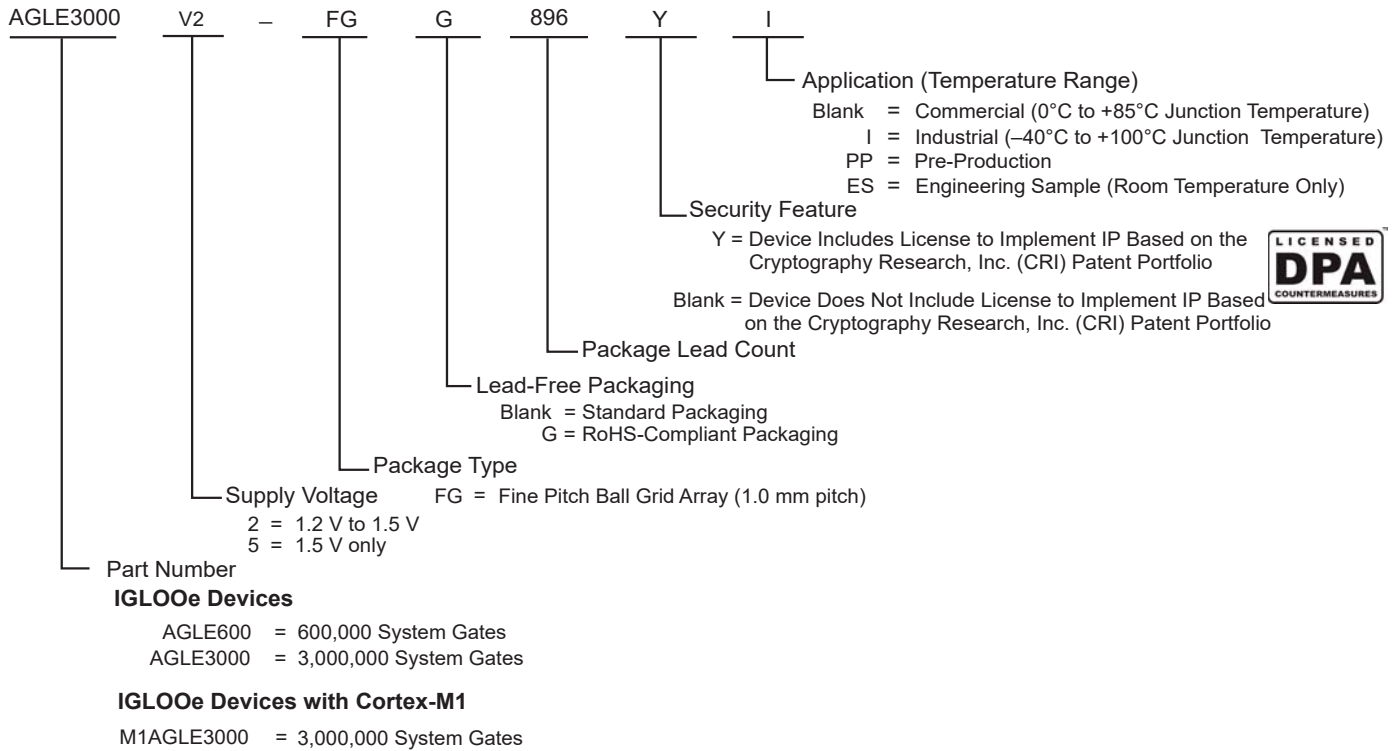
IGLOOe FPGAs Package Sizes Dimensions

| Package | FG256 | FG484 |
|---------------------------------|---------|---------|
| Length × Width (mm × mm) | 17 × 17 | 23 × 23 |
| Nominal Area (mm ²) | 289 | 529 |
| Pitch (mm) | 1 | 1 |
| Height (mm) | 1.6 | 2.23 |

IGLOOe Device Status

| IGLOOe Devices | Status | M1 IGLOOe Devices | Status |
|----------------|------------|-------------------|------------|
| AGLE600 | Production | | |
| AGLE3000 | Production | M1AGLE3000 | Production |

IGLOOe Ordering Information



Note: Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.

Temperature Grade Offerings

| Package | AGLE600 | AGLE3000 |
|---------|---------|-------------|
| | | M1AGLPE3000 |
| FG256 | C, I | – |
| FG484 | – | C, I |

Note: C = Commercial temperature range: 0°C to 85°C junction temperature.

I = Industrial temperature range: –40°C to 100°C junction temperature.

References made to IGLOOe devices also apply to ARM-enabled IGLOOe devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability:

<http://www.microsemi.com/soc/contact/default.aspx>.

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1 – IGLOOe Device Family Overview

General Description

The IGLOOe family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOOe devices enables entering and exiting an ultra-low power mode while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOOe device is completely functional in the system. This allows the IGLOOe device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOOe devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOOe is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOOe devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on 6 integrated phase-locked loops (PLLs). IGLOOe devices have up to 3 million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 341 user I/Os.

M1 IGLOOe devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low power consumption and speed when implemented in an M1 IGLOOe device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from Microsemi for use in M1 IGLOOe FPGAs.

The ARM-enabled devices have Microsemi ordering numbers that begin with M1AGLE and do not support AES decryption.

Flash*Freeze Technology

The IGLOOe device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOOe devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOOe V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOOe device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOOe devices the best fit for portable electronics.

Flash Advantages

Low Power

Flash-based IGLOOe devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOOe devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOOe devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOOe device the lowest total system power offered by any FPGA.

Security

The nonvolatile, flash-based IGLOOe devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOOe devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOOe devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOOe devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOOe devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOOe devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOOe family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOOe family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOOe device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOOe FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based IGLOOe devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOOe devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOOe device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOOe devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOOe devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOOe family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOOe family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOOe flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOOe FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOOe family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOOe family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOOe architecture provides granularity comparable to standard-cell ASICs. The IGLOOe device consists of five distinct and programmable architectural features (Figure 1-1 on page 4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOOe core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

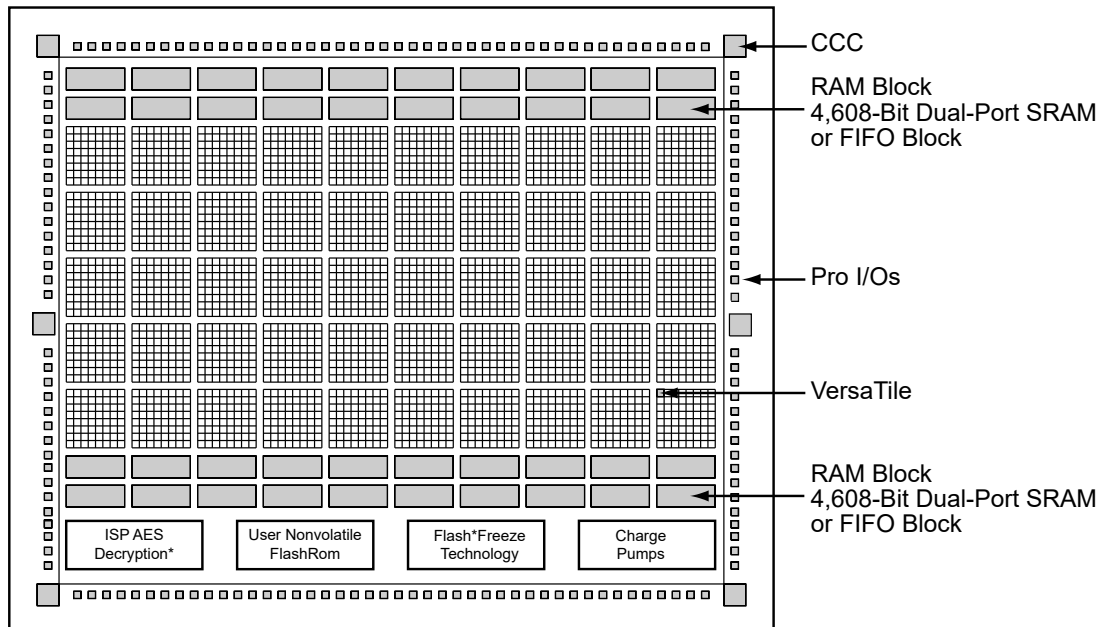


Figure 1-1 • IGLOOe Device Architecture Overview

Flash*Freeze Technology

The IGLOOe device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 μ s) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static and dynamic capabilities of the IGLOOe device. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode.

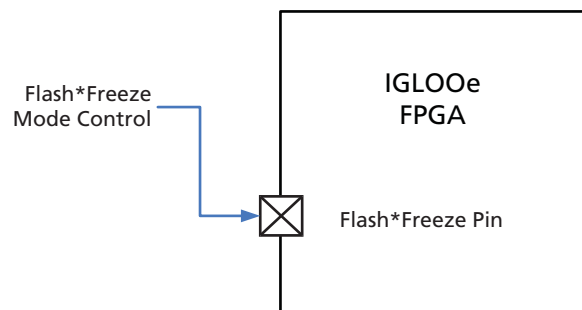


Figure 1-2 • IGLOOe Flash*Freeze Mode

VersaTiles

The IGLOOe core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The IGLOOe VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-3](#) for VersaTile configurations.

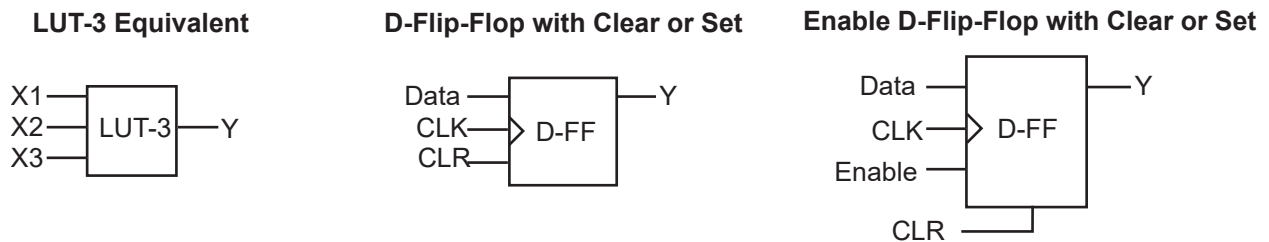


Figure 1-3 • VersaTile Configurations

User Nonvolatile FlashROM

IGLOOe devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOOe IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOOe development software solutions, Libero[®] System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

IGLOOe devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

IGLOOe devices provide designers with very flexible clock conditioning capabilities. Each member of the IGLOOe family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 μs
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

IGLOOe devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Pro I/Os with Advanced I/O Standards

The IGLOOe family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOOe FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

IGLOOe banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOOe devices support JEDEC-defined wide range I/O operation. IGLOOe devices support both the JESD8-B specification, covering 3.0 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click **PDB Configuration**. A FlashPoint – Programming File Generator window appears.
3. Click the **Specify I/O States During Programming** button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify ([Figure 1-4 on page 1-8](#)).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 – I/O is set to drive out logic High
 - 0 – I/O is set to drive out logic Low
 - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
 - Z -Tri-State: I/O is tristated

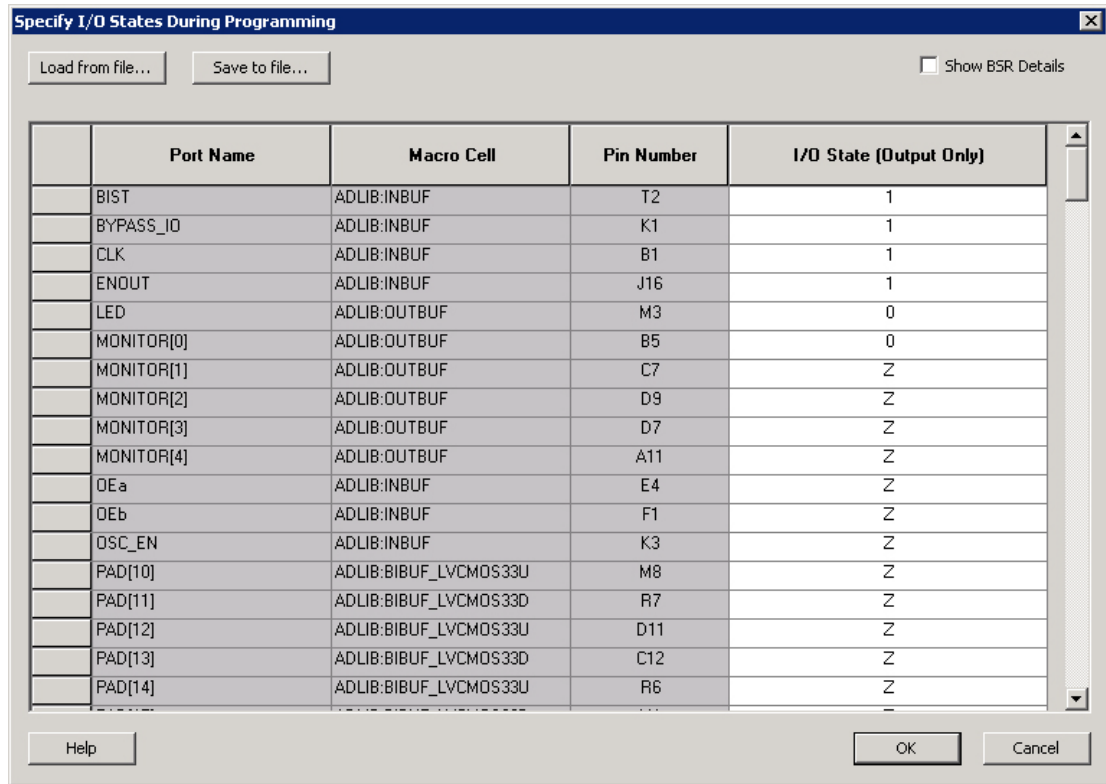


Figure 1-4 • I/O States During Programming Window

- Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – IGLOOe DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2](#) on [page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings

| Symbol | Parameter | Limits | Units |
|-------------------------------|------------------------------|---|-------|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPUMP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCI and VMV ³ | DC I/O buffer supply voltage | –0.3 to 3.75 | V |
| VI | I/O input voltage | –0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | V |
| T _{STG} ² | Storage temperature | –65 to +150 | °C |
| T _J ² | Junction temperature | +125 | °C |

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4](#) on [page 2-3](#).
2. For flash programming and retention maximum limits, refer to [Table 2-3](#) on [page 2-3](#), and for recommended operating limits, refer to [Table 2-2](#) on [page 2-2](#).
3. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on [page 3-1](#) for further information.

Table 2-2 • Recommended Operating Conditions¹

| Symbol | Parameter | Commercial | Industrial | Units | |
|---------------------------|--|---|----------------|----------------|---|
| T _J | Junction Temperature ² | 0 to + 85 | -40 to +100 | °C | |
| VCC ³ | 1.5 V DC core supply voltage ⁴ | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| | 1.2 V–1.5 V wide range DC core voltage ^{5, 6} | 1.14 to 1.575 | 1.14 to 1.575 | V | |
| VJTAG | JTAG DC voltage | 1.4 to 3.6 | 1.4 to 3.6 | V | |
| VPUMP | Programming voltage ⁶ | Programming Mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation ⁷ | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL ⁸ | Analog power supply (PLL) | 1.5 V DC core supply voltage ⁴ | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | | 1.2 V–1.5 V DC core supply voltage ⁵ | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VCCI and VMV ⁹ | 1.2 V DC supply voltage ⁵ | 1.14 to 1.26 | 1.14 to 1.26 | V | |
| | 1.2 V wide range DC supply voltage ⁵ | 1.14 to 1.575 | 1.14 to 1.575 | V | |
| | 1.5 V DC supply voltage | 1.425 to 1.575 | 1.425 to 1.575 | V | |
| | 1.8 V DC supply voltage | 1.7 to 1.9 | 1.7 to 1.9 | V | |
| | 2.5 V DC supply voltage | 2.3 to 2.7 | 2.3 to 2.7 | V | |
| | 3.0 V DC supply voltage ¹⁰ | 2.7 to 3.6 | 2.7 to 3.6 | V | |
| | 3.3 V DC supply voltage | 3.0 to 3.6 | 3.0 to 3.6 | V | |
| | LVDS differential I/O | 2.375 to 2.625 | 2.375 to 2.625 | V | |
| | LVPECL differential I/O | 3.0 to 3.6 | 3.0 to 3.6 | V | |

Notes:

- All parameters representing voltages are measured with respect to GND unless otherwise specified.
- Software Default Junction Temperature Range is set to 0°C - 70°C for commercial, and -40°C - 85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using temperature custom settings for running timing and power analysis tools. For more information regarding custom settings, please refer to the New Project Dialog Box component in the Designer in Libero SOC section of the Libero User Guide.
- The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-20. VCCI should be at the same voltage within a given I/O bank.
- For IGLOOe V5 devices
- For IGLOOe V2 devices only, operating at VCCI ≥ VCC
- All IGLOOe devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.
- VPUMP can be left floating during operation (not programming mode).
- VCCPLL pins should be tied to VCC pins. See the "VCCPLA/B/C/D/E/F PLL Supply Voltage" section for further information.
- VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section for further information.
- 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature¹

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature T _{STG} (°C) ² | Maximum Operating Junction Temperature T _J (°C) ² |
|---------------|--------------------|-------------------------------------|--|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to [Table 2-1 on page 2-1](#) and [Table 2-2 for device operating conditions and absolute limits](#).

Table 2-4 • Overshoot and Undershoot Limits^{1, 3}

| VCCI | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ² | Maximum Overshoot/Undershoot ² |
|---------------|---|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

Notes:

1. Based on reliability requirements at junction temperature at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
3. This table does not provide PCI overshoot/undershoot limits.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOOe device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#) and [Figure 2-2 on page 2-5](#).

There are five regions to consider during power-up.

IGLOOe I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-1 on page 2-4](#) and [Figure 2-2 on page 2-5](#)).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper powerup behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *IGLOOe FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

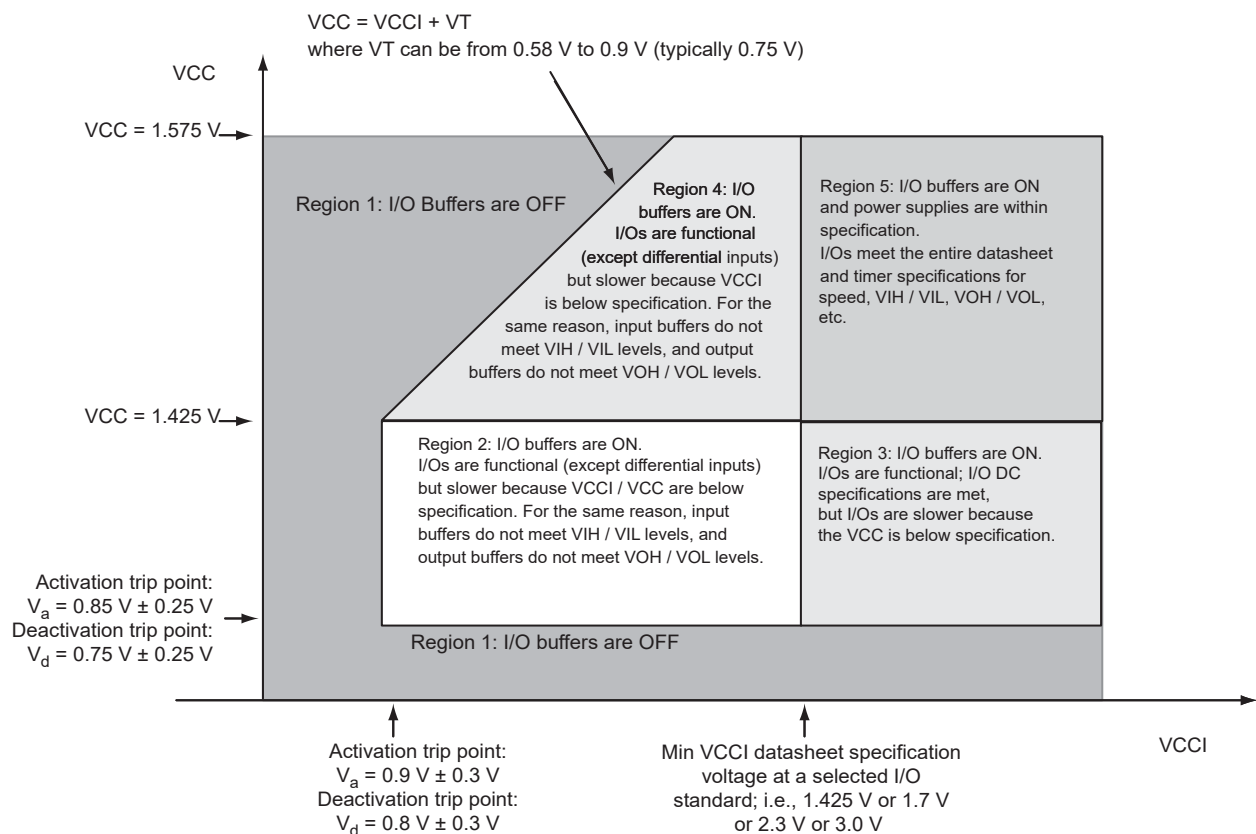


Figure 2-1 • V5 – I/O State as a Function of VCCI and VCC Voltage Levels

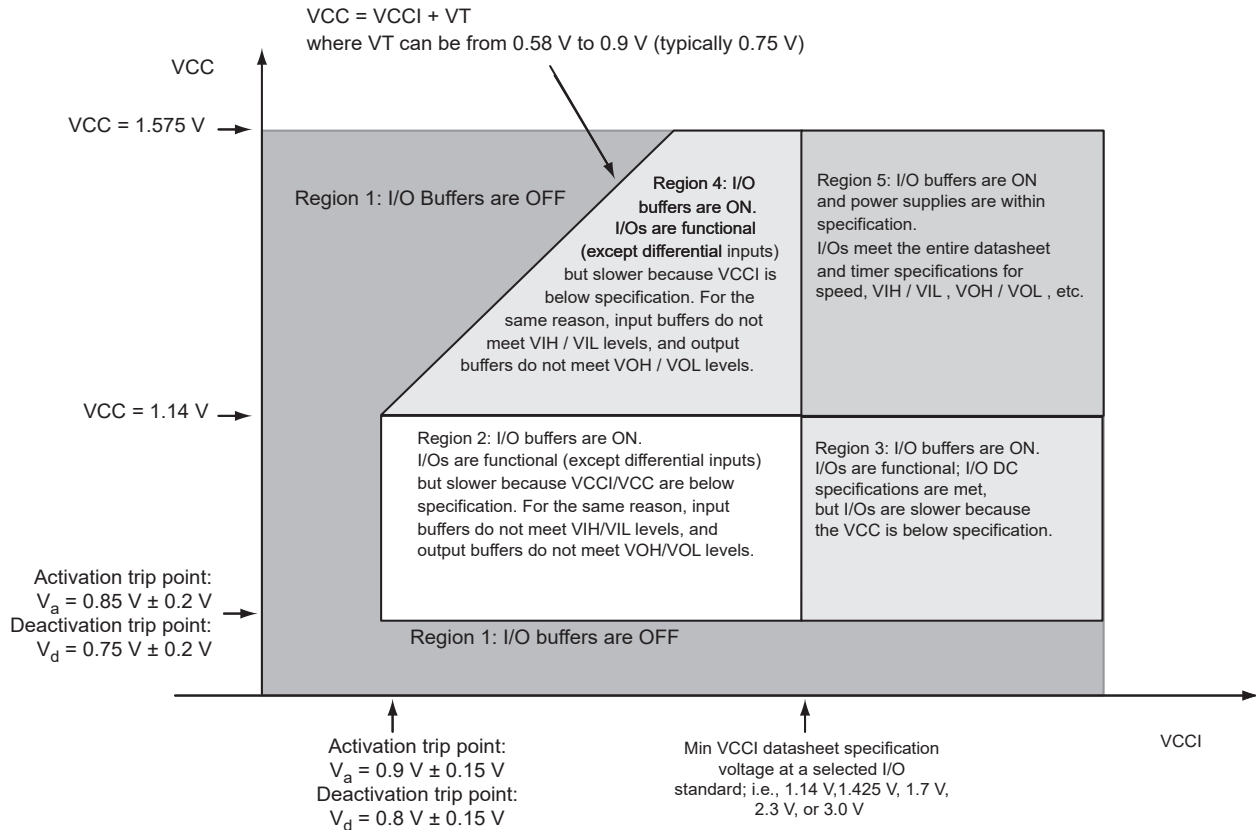


Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja}(\text{}^\circ\text{C/W)}} = \frac{100^\circ\text{C} - 70^\circ\text{C}}{13.6^\circ\text{C/W}} = 2.206 \text{ W}$$

EQ 2

Table 2-5 • Package Thermal Resistivities

| Package Type | Pin Count | θ_{jc} | θ_{ja} | | | Units |
|--|-----------|---------------|---------------|--------------|--------------|-------|
| | | | Still Air | 200 ft./min. | 500 ft./min. | |
| Plastic Quad Flat Package (PQFP) | 208 | 8.0 | 26.1 | 22.5 | 20.8 | C/W |
| Plastic Quad Flat Package (PQFP) with embedded heat spreader | 208 | 3.8 | 16.2 | 13.3 | 11.9 | C/W |
| Fine Pitch Ball Grid Array (FBGA) | 256 | 3.8 | 26.9 | 22.8 | 21.5 | C/W |
| | 484 | 3.2 | 20.5 | 17.0 | 15.9 | C/W |
| | 676 | 3.2 | 16.4 | 13.0 | 12.0 | C/W |
| | 896 | 2.4 | 13.6 | 10.4 | 9.4 | C/W |

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425 \text{ V}$)
For IGLOOe V2 or V5 devices, 1.5 V DC Core Supply Voltage

| Array Voltage VCC (V) | Junction Temperature ($^\circ\text{C}$) | | | | | |
|--------------------------|---|-------------------|--------------------|--------------------|--------------------|---------------------|
| | -40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.425 | 0.945 | 0.965 | 0.978 | 1.000 | 1.008 | 1.013 |
| 1.500 | 0.876 | 0.893 | 0.906 | 0.927 | 0.934 | 0.940 |
| 1.575 | 0.824 | 0.840 | 0.852 | 0.872 | 0.879 | 0.884 |

Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14 \text{ V}$)
For IGLOOe V2, 1.2 V DC Core Supply Voltage

| Array Voltage VCC (V) | Junction Temperature ($^\circ\text{C}$) | | | | | |
|--------------------------|---|-------------------|--------------------|--------------------|--------------------|---------------------|
| | -40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.14 | 0.968 | 0.978 | 0.991 | 1.000 | 1.006 | 1.010 |
| 1.20 | 0.864 | 0.873 | 0.885 | 0.893 | 0.898 | 0.902 |
| 1.26 | 0.793 | 0.803 | 0.813 | 0.821 | 0.826 | 0.829 |

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power modes usage. Microsemi recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • Power Supply State per Mode

| Modes/power supplies | Power Supply Configurations | | | | |
|----------------------|-----------------------------|--------|------|-------|-----------------|
| | VCC | VCCPLL | VCCI | VJTAG | VPUMP |
| Flash*Freeze | On | On | On | On | On/off/floating |
| Sleep | Off | Off | On | Off | Off |
| Shutdown | Off | Off | Off | Off | Off |
| No Flash*Freeze | On | On | On | On | On/off/floating |

Note: Off: Power supply level = 0 V

Table 2-9 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode*

| | Core Voltage | AGLE600 | AGLE3000 | Units |
|----------------|--------------|---------|----------|-------|
| Typical (25°C) | 1.2 V | 34 | 95 | μA |
| | 1.5 V | 72 | 310 | μA |

Note: *IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in [Table 2-13 on page 2-9](#) and [Table 2-14 on page 2-10](#) (PDC6 and PDC7).

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Sleep Mode*

| | Core Voltage | AGLE600 | AGLE3000 | Units |
|---|---------------|---------|----------|-------|
| VCCI/VJTAG = 1.2 V (per bank) Typical (25°C) | 1.2 V | 1.7 | 1.7 | μA |
| VCCI/VJTAG = 1.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.8 | 1.8 | μA |
| VCCI/VJTAG = 1.8 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.9 | 1.9 | μA |
| VCCI/VJTAG = 2.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.2 | 2.2 | μA |
| VCCI/VJTAG = 3.3 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.5 | 2.5 | μA |

Note: *IDD = $N_{BANKS} \times ICCI$. Values do not include I/O static contribution, which is shown in [Table 2-13 on page 2-9](#) and [Table 2-14 on page 2-10](#) (PDC6 and PDC7).

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode*

| | Core Voltage | AGLE600 | AGLE3000 | Units |
|----------------|---------------|---------|----------|-------|
| Typical (25°C) | 1.2 V / 1.5 V | 0 | 0 | μA |

Table 2-12 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode¹

| | Core Voltage | AGLE600 | AGLE3000 | Units |
|---|---------------|---------|----------|-------|
| ICCA Current² | | | | |
| Typical (25°C) | 1.2 V | 28 | 89 | μA |
| | 1.5 V | 82 | 320 | μA |
| ICCI or IJTAG Current³ | | | | |
| VCCI/VJTAG = 1.2 V (per bank) Typical (25°C) | 1.2 V | 1.7 | 1.7 | μA |
| VCCI/VJTAG = 1.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.8 | 1.8 | μA |
| VCCI/VJTAG = 1.8 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.9 | 1.9 | μA |
| VCCI/VJTAG = 2.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.2 | 2.2 | μA |
| VCCI/VJTAG = 3.3 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.5 | 2.5 | μA |

Notes:

1. $IDD = N_{BANKS} \times ICCI + ICCA$. JTAG counts as one bank when powered.
2. Includes VCC and VPUMP and VCCPLL currents.
3. Values do not include I/O static contribution (PDC6 and PDC7).

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings

| | VCCI (V) | Static Power PDC6 (mW) ¹ | Dynamic Power PAC9 (μW/MHz) ² |
|--|-------------|--|---|
| Single-Ended | | | |
| 3.3 V LVTTTL/LVCMOS | 3.3 | – | 16.34 |
| 3.3 V LVTTTL/LVCMOS – Schmitt trigger | 3.3 | – | 24.49 |
| 3.3 V LVCMOS Wide Range ³ | 3.3 | – | 16.34 |
| 3.3 V LVCMOS Wide Range – Schmitt trigger ³ | 3.3 | – | 24.49 |
| 2.5 V LVCMOS | 2.5 | – | 4.71 |
| 2.5 V LVCMOS | 2.5 | – | 6.13 |
| 1.8 V LVCMOS | 1.8 | – | 1.66 |
| 1.8 V LVCMOS – Schmitt trigger | 1.8 | – | 1.78 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.01 |
| 1.5 V LVCMOS (JESD8-11) – Schmitt trigger | 1.5 | – | 0.97 |
| 1.2 V LVCMOS ⁴ | 1.2 | – | 0.60 |
| 1.2 V LVCMOS – Schmitt trigger ⁴ | 1.2 | – | 0.53 |
| 1.2 V LVCMOS Wide Range ⁴ | 1.2 | – | 0.60 |
| 1.2 V LVCMOS Wide Range – Schmitt trigger ⁴ | 1.2 | – | 0.53 |
| 3.3 V PCI | 3.3 | – | 17.76 |
| 3.3 V PCI – Schmitt trigger | 3.3 | – | 19.10 |
| 3.3 V PCI-X | 3.3 | – | 17.76 |
| 3.3 V PCI-X – Schmitt trigger | 3.3 | – | 19.10 |
| Voltage-Referenced | | | |
| 3.3 V GTL | 3.3 | 2.90 | 7.14 |
| 2.5 V GTL | 2.5 | 2.13 | 3.54 |
| 3.3 V GTL+ | 3.3 | 2.81 | 2.91 |
| 2.5 V GTL+ | 2.5 | 2.57 | 2.61 |
| HSTL (I) | 1.5 | 0.17 | 0.79 |
| HSTL (II) | 1.5 | 0.17 | .079 |
| SSTL2 (I) | 2.5 | 1.38 | 3.26 |
| SSTL2 (II) | 2.5 | 1.38 | 3.26 |
| SSTL3 (I) | 3.3 | 3.21 | 7.97 |
| SSTL3 (II) | 3.3 | 3.21 | 7.97 |
| Differential | | | |
| LVDS | 2.5 | 2.26 | 0.89 |
| LVPECL | 3.3 | 5.71 | 1.94 |

Notes:

1. PDC6 is the static power (where applicable) measured on VCCI.
2. PAC9 is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.
4. Applicable for IGLOOe V2 devices only.

Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹

| | C _{LOAD} (pF) | V _{CCI} (V) | Static Power PDC7 (mW) ² | Dynamic Power PAC10 (μW/MHz) ³ |
|--------------------------------------|---------------------------|-------------------------|--|--|
| Single-Ended | | | | |
| 3.3 V LVTTTL/LVCMOS | 5 | 3.3 | – | 148.00 |
| 3.3 V LVCMOS Wide Range ⁴ | 5 | 3.3 | – | 148.00 |
| 2.5 V LVCMOS | 5 | 2.5 | – | 83.23 |
| 1.8 V LVCMOS | 5 | 1.8 | – | 54.58 |
| 1.5 V LVCMOS (JESD8-11) | 5 | 1.5 | – | 37.05 |
| 1.2 V LVCMOS (JESD8-11) | 5 | 1.2 | – | 17.94 |
| 1.2 V LVCMOS (JESD8-11) – Wide Range | | | | 17.94 |
| 3.3 V PCI | 10 | 3.3 | – | 204.61 |
| 3.3 V PCI-X | 10 | 3.3 | – | 204.61 |
| Voltage-Referenced | | | | |
| 3.3 V GTL | 10 | 3.3 | – | 24.08 |
| 2.5 V GTL | 10 | 2.5 | – | 13.52 |
| 3.3 V GTL+ | 10 | 3.3 | – | 24.10 |
| 2.5 V GTL+ | 10 | 2.5 | – | 13.54 |
| HSTL (I) | 20 | 1.5 | 7.08 | 26.22 |
| HSTL (II) | 20 | 1.5 | 13.88 | 27.18 |
| SSTL2 (I) | 30 | 2.5 | 16.69 | 105.56 |
| SSTL2 (II) | 30 | 2.5 | 25.91 | 116.60 |
| SSTL3 (I) | 30 | 3.3 | 26.02 | 114.67 |
| SSTL3 (II) | 30 | 3.3 | 42.21 | 131.69 |
| Differential | | | | |
| LVDS | – | 2.5 | 7.70 | 89.62 |
| LVPECL | – | 3.3 | 19.42 | 167.86 |

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PDC7 is the static power (where applicable) measured on VCCI.
3. PAC10 is the total dynamic power measured on VCCI.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

Power Consumption of Various Internal Resources

Table 2-15 • Different Components Contributing to the Dynamic Power Consumption in IGLOOe Devices For IGLOOe V2 or V5 Devices, 1.5 V DC Core Supply Voltage

| Parameter | Definition | Device-Specific Dynamic Contributions ($\mu\text{W}/\text{MHz}$) | |
|-----------|--|--|----------|
| | | AGLE600 | AGLE3000 |
| PAC1 | Clock contribution of a Global Rib | 19.7 | 12.77 |
| PAC2 | Clock contribution of a Global Spine | 4.16 | 1.85 |
| PAC3 | Clock contribution of a VersaTile row | 0.88 | |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.11 | |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.057 | |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.207 | |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | 0.207 | |
| PAC8 | Average contribution of a routing net | 0.7 | |
| PAC9 | Contribution of an I/O input pin (standard-dependent) | See Table 2-13 on page 2-9. | |
| PAC10 | Contribution of an I/O output pin (standard-dependent) | See Table 2-14 on page 2-10. | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | |
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 | |
| PAC13 | Dynamic contribution for PLL | 2.70 | |

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC software.

Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO Devices For IGLOOe V2 or V5 Devices, 1.5 V DC Core Supply Voltage

| Parameter | Definition | Device Specific Static Power (mW) | |
|-----------|--|-----------------------------------|----------|
| | | AGLE600 | AGLE3000 |
| PDC1 | Array static power in Active mode | See Table 2-12 on page 2-8. | |
| PDC2 | Array static power in Static (Idle) mode | See Table 2-11 on page 2-7. | |
| PDC3 | Array static power in Flash*Freeze mode | See Table 2-9 on page 2-7. | |
| PDC4 | Static PLL contribution | 1.84 | |
| PDC5 | Bank quiescent power (VCCI-dependent) | See Table 2-12 on page 2-8. | |
| PDC6 | I/O input pin static power (standard-dependent) | See Table 2-13 on page 2-9. | |
| PDC7 | I/O output pin static power (standard-dependent) | See Table 2-14 on page 2-10. | |

Table 2-17 • Different Components Contributing to the Dynamic Power Consumption in IGLOOe Devices For IGLOOe V2 Devices, 1.2 V DC Core Supply Voltage

| Parameter | Definition | Device-Specific Dynamic Contributions ($\mu\text{W}/\text{MHz}$) | |
|-----------|--|--|----------|
| | | AGLE600 | AGLE3000 |
| PAC1 | Clock contribution of a Global Rib | 12.61 | 8.17 |
| PAC2 | Clock contribution of a Global Spine | 2.66 | 1.18 |
| PAC3 | Clock contribution of a VersaTile row | 0.56 | |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.071 | |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.045 | |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.186 | |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | 0.109 | |
| PAC8 | Average contribution of a routing net | 0.449 | |
| PAC9 | Contribution of an I/O input pin (standard-dependent) | See Table 2-9 on page 2-7. | |
| PAC10 | Contribution of an I/O output pin (standard-dependent) | See Table 2-10 on page 2-7 and Table 2-11 on page 2-7. | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | |
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 | |
| PAC13 | Dynamic PLL contribution | 2.10 | |

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC software.

Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices For IGLOOe V2 Devices, 1.2 V DC Core Supply Voltage

| Parameter | Definition | Device Specific Static Power (mW) | |
|-----------|--|-----------------------------------|----------|
| | | AGLE600 | AGLE3000 |
| PDC1 | Array static power in Active mode | See Table 2-12 on page 2-8. | |
| PDC2 | Array static power in Static (Idle) mode | See Table 2-11 on page 2-7. | |
| PDC3 | Array static power in Flash*Freeze mode | See Table 2-9 on page 2-7. | |
| PDC4 | Static PLL contribution | 0.90 | |
| PDC5 | Bank quiescent power (VCCI-dependent) | See Table 2-12 on page 2-8. | |
| PDC6 | I/O input pin static power (standard-dependent) | See Table 2-13 on page 2-9. | |
| PDC7 | I/O output pin static power (standard-dependent) | See Table 2-14 on page 2-10. | |

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-19 on page 2-15](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-20 on page 2-15](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-20 on page 2-15](#). The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = (PDC1 \text{ or } PDC2 \text{ or } PDC3) + N_{BANKS} * PDC5 + N_{INPUTS} * PDC6 + N_{OUTPUTS} * PDC7$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOOe FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOOe FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19 on page 2-15](#).

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19](#) on page 2-15.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19](#) on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-19](#) on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-19](#) on page 2-15.

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-20](#) on page 2-15.

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in [Table 2-20](#) on page 2-15.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-20](#) on page 2-15.

PLL Contribution— P_{PLL}

$$P_{PLL} = PDC4 + PAC13 * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.¹

1. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($PAC13 * F_{CLKOUT}$ product) to the total PLL contribution.

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-19 • Toggle Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|------------|----------------------------------|-----------|
| α_1 | Toggle rate of VersaTile outputs | 10% |
| α_2 | I/O buffer toggle rate | 10% |

Table 2-20 • Enable Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|-----------|--------------------------------------|-----------|
| β_1 | I/O output buffer enable rate | 100% |
| β_2 | RAM enable rate for read operations | 12.5% |
| β_3 | RAM enable rate for write operations | 12.5% |

User I/O Characteristics

Timing Model

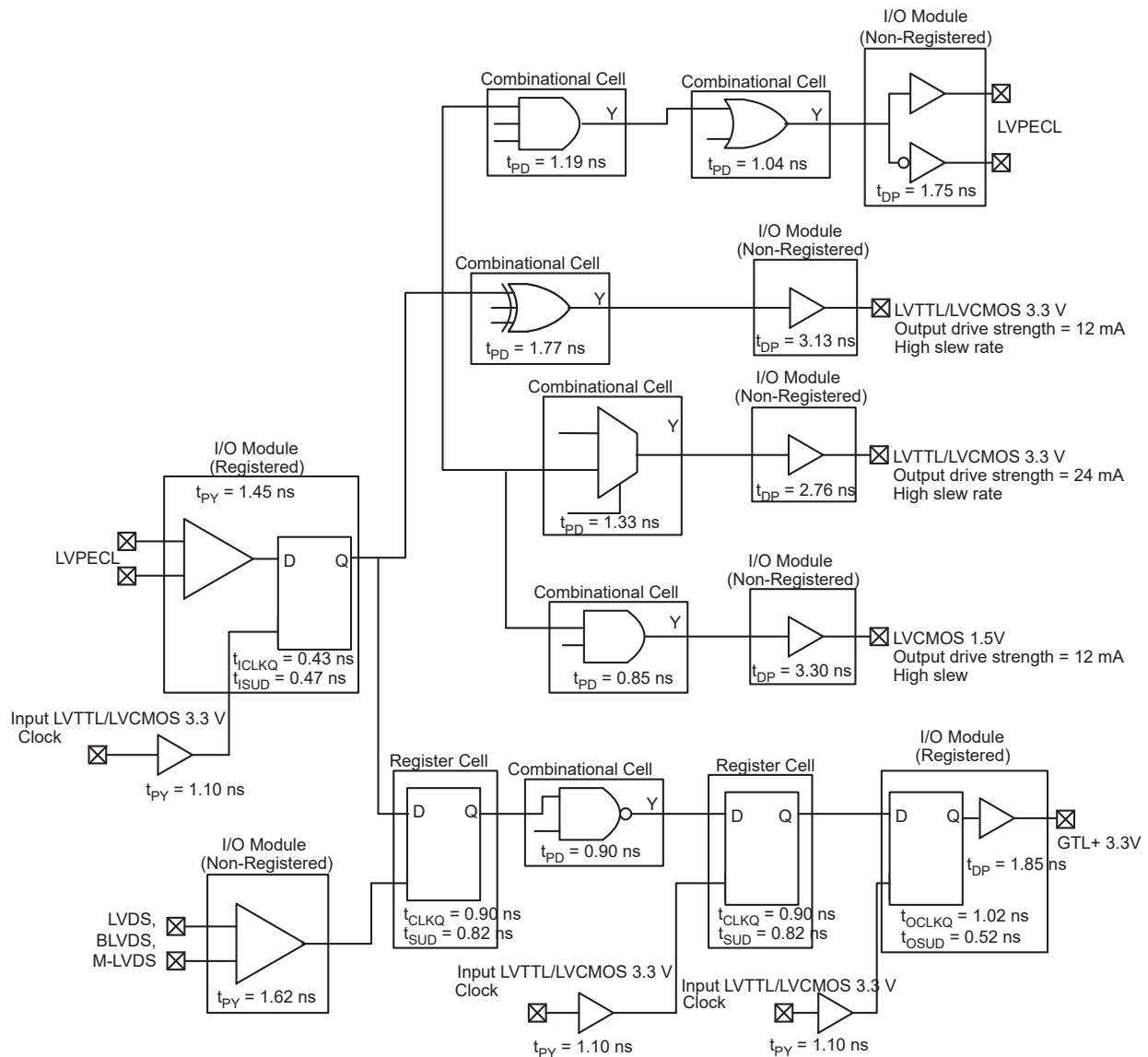


Figure 2-3 • Timing Model

Operating Conditions: Std. Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$), Worst-Case VCC = 1.425 V, Applicable to 1.5 V DC Core Voltage, V2 and V5 devices

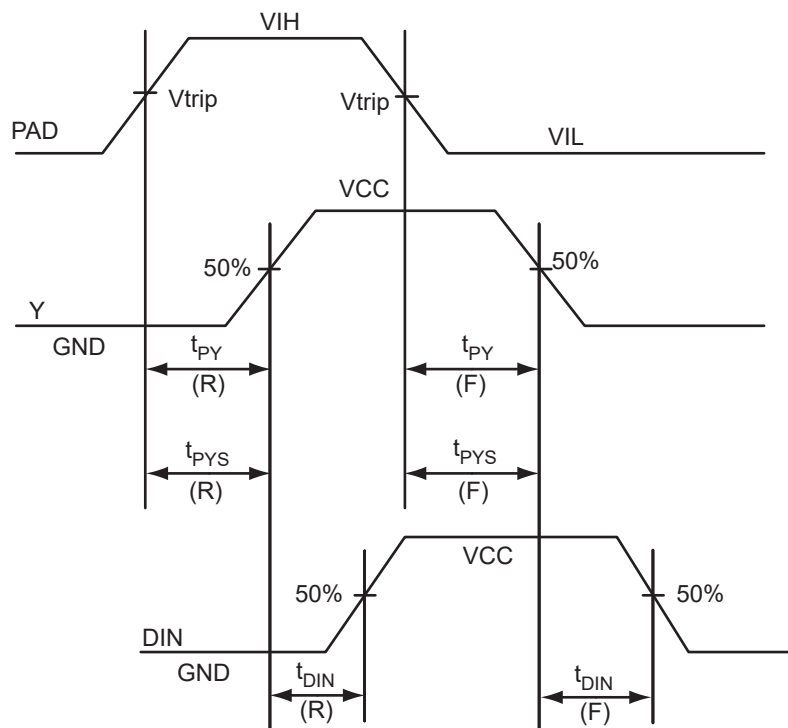
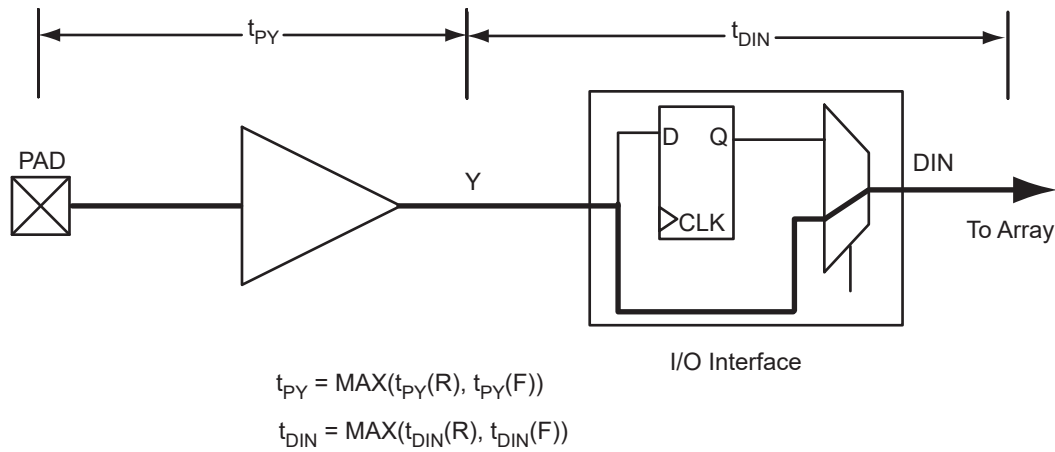


Figure 2-4 • Input Buffer Timing Model and Delays (example)

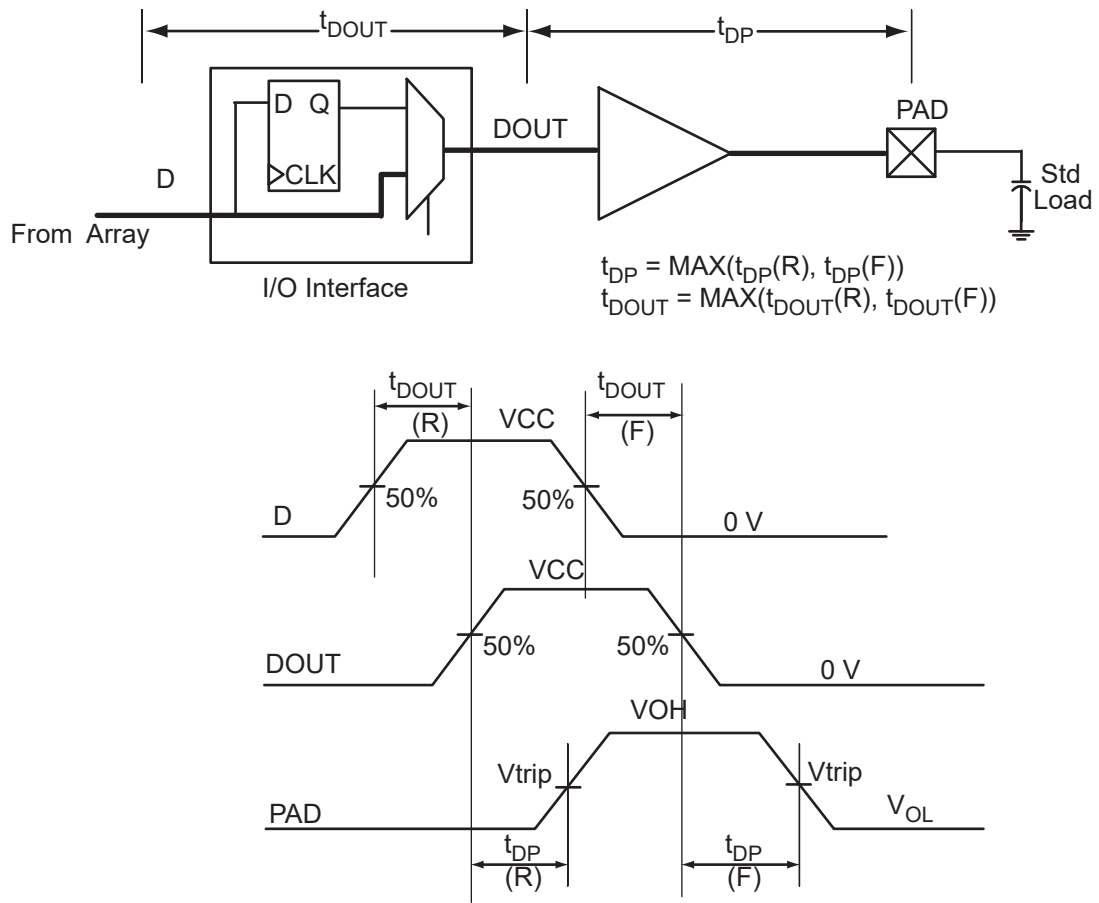


Figure 2-5 • Output Buffer Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels
Applicable to Commercial and Industrial Conditions**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength ² | Slew Rate | VIL | | VIH | | VOL | VOH | IOL ¹ | IOH ¹ |
|--------------------------------------|-------------------------|---|-----------|--------|-------------|-------------|--------|-------------|-------------|------------------|------------------|
| | | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 mA | 12 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 3.3 V LVCMOS Wide Range ³ | 100 μ A | 12 mA | High | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI - 0.2 | 0.1 | 0.1 |
| 2.5 V LVCMOS | 12 mA | 12 mA | High | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | 12 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | 12 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 1.2 V LVCMOS | 2 mA | 2 mA | High | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 |
| 1.2 V LVCMOS Wide Range ⁴ | 100 μ A | 2 mA | High | -0.3 | 0.3 * VCCI | 0.7 * VCCI | 3.6 | 0.1 | VCCI - 0.1 | 0.1 | 0.1 |
| 3.3 V PCI | Per PCI Specification | | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X Specification | | | | | | | | | | |
| 3.3 V GTL | 20 mA ⁵ | 20 mA ⁵ | High | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 |
| 2.5 V GTL | 20 mA ⁵ | 20 mA ⁵ | High | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 |
| 3.3 V GTL+ | 35 mA | 35 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 35 | 35 |
| 2.5 V GTL+ | 33 mA | 33 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 33 | 33 |
| HSTL (I) | 8 mA | 8 mA | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 8 | 8 |

Notes:

1. Currents are measured at 85°C junction temperature.
2. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-12 specification.
4. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
5. Output drive strength is below JEDEC specification.
6. Output Slew Rates can be extracted from IBIS Models, <http://www.microsemi.com/soc/download/ibis/default.aspx>.

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels (continued)
Applicable to Commercial and Industrial Conditions

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength ² | Slew Rate | VIL | | VIH | | VOL | VOH | IOL ¹ | IOH ¹ |
|--------------|--------------------|---|-----------|--------|------------|------------|--------|--------|-------------|------------------|------------------|
| | | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| HSTL (II) | 15 mA ⁵ | 15 mA ⁵ | High | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 15 | 15 |
| SSTL2 (I) | 15 mA | 15 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI - 0.62 | 15 | 15 |
| SSTL2 (II) | 18 mA | 18 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI - 0.43 | 18 | 18 |
| SSTL3 (I) | 14 mA | 14 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI - 1.1 | 14 | 14 |
| SSTL3 (II) | 21 mA | 21 mA | High | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI - 0.9 | 21 | 21 |

Notes:

1. Currents are measured at 85°C junction temperature.
2. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-12 specification.
4. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
5. Output drive strength is below JEDEC specification.
6. Output Slew Rates can be extracted from IBIS Models, <http://www.microsemi.com/soc/download/ibis/default.aspx>.

**Table 2-22 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial and Industrial Conditions**

| DC I/O Standards | Commercial ¹ | | Industrial ² | |
|--------------------------------------|-------------------------|------------------|-------------------------|------------------|
| | IIL ³ | IIH ⁴ | IIL ³ | IIH ⁴ |
| | μA | μA | μA | μA |
| 3.3 V LVTTTL / 3.3 V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V LVCMOS Wide Range | 10 | 10 | 15 | 15 |
| 2.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.2 V LVCMOS ⁵ | 10 | 10 | 15 | 15 |
| 1.2 V LVCOMS Wide Range ⁵ | 10 | 10 | 15 | 15 |
| 3.3 V PCI | 10 | 10 | 15 | 15 |
| 3.3 V PCI-X | 10 | 10 | 15 | 15 |
| 3.3 V GTL | 10 | 10 | 15 | 15 |
| 2.5 V GTL | 10 | 10 | 15 | 15 |
| 3.3 V GTL+ | 10 | 10 | 15 | 15 |
| 2.5 V GTL+ | 10 | 10 | 15 | 15 |
| HSTL (I) | 10 | 10 | 15 | 15 |
| HSTL (II) | 10 | 10 | 15 | 15 |
| SSTL2 (I) | 10 | 10 | 15 | 15 |
| SSTL2 (II) | 10 | 10 | 15 | 15 |
| SSTL3 (I) | 10 | 10 | 15 | 15 |
| SSTL3 (II) | 10 | 10 | 15 | 15 |

Notes:

1. Commercial range ($0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)
2. Industrial range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$)
3. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
4. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
5. Applicable to V2 devices operating at $V_{CCI} \geq V_{CC}$.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-23 • Summary of AC Measuring Points

| Standard | Input Reference Voltage (VREF_TYP) | Board Termination Voltage (VTT_REF) | Measuring Trip Point (Vtrip) |
|-----------------------------|------------------------------------|-------------------------------------|------------------------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | – | – | 1.4 V |
| 3.3 V LVCMOS Wide Range | – | – | 1.4 V |
| 2.5 V LVCMOS | – | – | 1.2 V |
| 1.8 V LVCMOS | – | – | 0.90 V |
| 1.5 V LVCMOS | – | – | 0.75 V |
| 1.2 V LVCMOS* | – | – | 0.6 V |
| 1.2 V LVCMOS – Wide Range* | – | – | 0.6 V |
| 3.3 V PCI | – | – | 0.285 * VCCI (RR) |
| | – | – | 0.615 * VCCI (FF)) |
| 3.3 V PCI-X | – | – | 0.285 * VCCI (RR) |
| | – | – | 0.615 * VCCI (FF) |
| 3.3 V GTL | 0.8 V | 1.2 V | VREF |
| 2.5 V GTL | 0.8 V | 1.2 V | VREF |
| 3.3 V GTL+ | 1.0 V | 1.5 V | VREF |
| 2.5 V GTL+ | 1.0 V | 1.5 V | VREF |
| HSTL (I) | 0.75 V | 0.75 V | VREF |
| HSTL (II) | 0.75 V | 0.75 V | VREF |
| SSTL2 (I) | 1.25 V | 1.25 V | VREF |
| SSTL2 (II) | 1.25 V | 1.25 V | VREF |
| SSTL3 (I) | 1.5 V | 1.485 V | VREF |
| SSTL3 (II) | 1.5 V | 1.485 V | VREF |
| LVDS | – | – | Cross point |
| LVPECL | – | – | Cross point |

Note: *Applicable to V2 devices ONLY operating in the 1.2 V core range.

Table 2-24 • I/O AC Parameter Definitions

| Parameter | Definition |
|------------|---|
| t_{DP} | Data to Pad delay through the Output Buffer |
| t_{PY} | Pad to Data delay through the Input Buffer with Schmitt trigger disabled |
| t_{DOUT} | Data to Output Buffer delay through the I/O interface |
| t_{EOUT} | Enable to Output Buffer Tristate Control delay through the I/O interface |
| t_{DIN} | Input Buffer to Data delay through the I/O interface |
| t_{PYS} | Pad to Data delay through the Input Buffer with Schmitt trigger enabled |
| t_{HZ} | Enable to Pad delay through the Output Buffer—HIGH to Z |
| t_{ZH} | Enable to Pad delay through the Output Buffer—Z to HIGH |
| t_{LZ} | Enable to Pad delay through the Output Buffer—LOW to Z |
| t_{ZL} | Enable to Pad delay through the Output Buffer—Z to LOW |
| t_{ZHS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH |
| t_{ZLS} | Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW |

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings
 Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case V_{CCI} (per standard)

| I/O Standard | Drive Strength (mA) | Equivalent Software Default Drive Strength Option ¹ (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | t_{DOUT} (ns) | t_{DP} (ns) | t_{DIN} (ns) | t_{PY} (ns) | t_{PYS} (ns) | t_{EOUT} (ns) | t_{ZL} (ns) | t_{ZH} (ns) | t_{LZ} (ns) | t_{HZ} (ns) | t_{ZLS} (ns) | t_{ZHS} (ns) | Units |
|---|---------------------|---|-----------|----------------------|--------------------------------|-----------------|---------------|----------------|---------------|----------------|-----------------|---------------|---------------|---------------|---------------|----------------|----------------|-------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 | 12 | High | 5 | – | 0.97 | 2.12 | 0.18 | 1.08 | 1.34 | 0.66 | 2.17 | 1.69 | 2.71 | 3.08 | 5.76 | 5.28 | ns |
| 3.3 V LVCMOS Wide Range ^{1, 2} | 100 μA | 12 | High | 5 | – | 0.97 | 2.96 | 0.18 | 1.42 | 1.84 | 0.66 | 2.98 | 2.28 | 3.86 | 4.36 | 6.58 | 5.87 | ns |
| 2.5 V LVCMOS | 12 | 12 | High | 5 | – | 0.97 | 2.15 | 0.18 | 1.31 | 1.41 | 0.66 | 2.20 | 1.85 | 2.78 | 2.98 | 5.80 | 5.45 | ns |
| 1.8 V LVCMOS | 12 | 12 | High | 5 | – | 0.97 | 2.37 | 0.18 | 1.27 | 1.59 | 0.66 | 2.42 | 2.03 | 3.07 | 3.57 | 6.02 | 5.62 | ns |
| 1.5 V LVCMOS | 12 | 12 | High | 5 | – | 0.97 | 2.69 | 0.18 | 1.47 | 1.77 | 0.66 | 2.75 | 2.30 | 3.24 | 3.67 | 6.35 | 5.89 | ns |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25 ³ | 0.97 | 2.38 | 0.18 | 0.96 | 1.42 | 0.66 | 2.43 | 1.80 | 2.72 | 3.08 | 6.03 | 5.39 | ns |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25 ³ | 0.97 | 2.38 | 0.19 | 0.92 | 1.34 | 0.66 | 2.43 | 1.80 | 2.72 | 3.08 | 6.03 | 5.39 | ns |
| 3.3 V GTL | 20 ⁴ | – | High | 10 | 25 | 0.97 | 1.78 | 0.19 | 2.35 | – | 0.66 | 1.80 | 1.78 | – | – | 5.39 | 5.38 | ns |
| 2.5 V GTL | 20 ⁴ | – | High | 10 | 25 | 0.97 | 1.85 | 0.19 | 1.98 | – | 0.66 | 1.89 | 1.82 | – | – | 5.49 | 5.42 | ns |
| 3.3 V GTL+ | 35 | – | High | 10 | 25 | 0.97 | 1.80 | 0.19 | 1.32 | – | 0.66 | 1.84 | 1.77 | – | – | 5.44 | 5.36 | ns |
| 2.5 V GTL+ | 33 | – | High | 10 | 25 | 0.97 | 1.92 | 0.19 | 1.26 | – | 0.66 | 1.96 | 1.80 | – | – | 5.56 | 5.40 | ns |
| HSTL (I) | 8 | – | High | 20 | 50 | 0.97 | 2.67 | 0.18 | 1.72 | – | 0.66 | 2.72 | 2.67 | – | – | 6.32 | 6.26 | ns |
| HSTL (II) | 15 | – | High | 20 | 25 | 0.97 | 2.55 | 0.18 | 1.72 | – | 0.66 | 2.60 | 2.34 | – | – | 6.20 | 5.93 | ns |
| SSTL2 (I) | 15 | – | High | 30 | 50 | 0.97 | 1.86 | 0.19 | 1.12 | – | 0.66 | 1.90 | 1.68 | – | – | 5.50 | 5.28 | ns |
| SSTL2 (II) | 18 | – | High | 30 | 25 | 0.97 | 1.89 | 0.19 | 1.12 | – | 0.66 | 1.93 | 1.62 | – | – | 5.53 | 5.22 | ns |
| SSTL3 (I) | 14 | – | High | 30 | 50 | 0.97 | 2.00 | 0.19 | 1.06 | – | 0.66 | 2.04 | 1.67 | – | – | 5.64 | 5.27 | ns |
| SSTL3 (II) | 21 | – | High | 30 | 25 | 0.97 | 1.81 | 0.19 | 1.06 | – | 0.66 | 1.85 | 1.55 | – | – | 5.45 | 5.14 | ns |
| LVDS | 24 | – | High | – | – | 0.97 | 1.73 | 0.19 | 1.62 | – | – | – | – | – | – | – | – | ns |
| LVPECL | 24 | – | High | – | – | 0.97 | 1.65 | 0.18 | 1.42 | – | – | – | – | – | – | – | – | ns |

Notes:

1. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI Specifications. See [Figure 2-12 on page 2-49](#) for connectivity. This resistor is not required during normal operation.
4. Output drive strength is below JEDEC specification.
5. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings
 Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
 Worst-Case V_{CCI} (per standard)

| I/O Standard | Drive Strength (mA) | Equivalent Software Default Drive Strength Option ¹ (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | t_{pOUT} (ns) | t_{pP} (ns) | t_{pIN} (ns) | t_{pY} (ns) | t_{pYS} (ns) | t_{pEOUT} (ns) | t_{zL} (ns) | t_{zH} (ns) | t_{zLZ} (ns) | t_{zHZ} (ns) | t_{zLS} (ns) | t_{zHS} (ns) | Units |
|--|---------------------|---|-----------|----------------------|--------------------------------|-----------------|---------------|----------------|---------------|----------------|------------------|---------------|---------------|----------------|----------------|----------------|----------------|-------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 12 | 12 | High | 5 | – | 1.55 | 2.47 | 0.26 | 1.31 | 1.58 | 1.10 | 2.51 | 2.04 | 3.28 | 3.97 | 8.29 | 7.82 | ns |
| 3.3 V LVCMOS Wide Range ^{1,2} | 100 μA | 12 | High | 35 | – | 1.55 | 3.40 | 0.26 | 1.66 | 2.14 | 1.10 | 3.40 | 2.68 | 4.55 | 5.49 | 9.19 | 8.46 | ns |
| 2.5 V LVCMOS | 12 | 12 | High | 5 | – | 1.55 | 2.51 | 0.26 | 1.55 | 1.77 | 1.10 | 2.54 | 2.22 | 3.36 | 3.85 | 8.33 | 8.00 | ns |
| 1.8 V LVCMOS | 12 | 12 | High | 5 | – | 1.55 | 2.75 | 0.26 | 1.53 | 1.96 | 1.10 | 2.78 | 2.40 | 3.68 | 4.56 | 8.57 | 8.19 | ns |
| 1.5 V LVCMOS | 12 | 12 | High | 5 | – | 1.55 | 3.10 | 0.26 | 1.72 | 2.16 | 1.10 | 3.15 | 2.70 | 3.86 | 4.68 | 8.93 | 8.49 | ns |
| 1.2 V LVCMOS | 2 | 2 | High | 5 | – | 1.55 | 4.06 | 0.26 | 2.09 | 2.95 | 1.10 | 3.92 | 3.46 | 4.01 | 3.79 | 9.71 | 9.24 | ns |
| 1.2 V LVCMOS Wide Range ^{1,3} | 100 μA | 2 | High | 5 | – | 1.55 | 4.06 | 0.26 | 2.09 | 2.95 | 1.10 | 3.92 | 3.46 | 4.01 | 3.79 | 9.71 | 9.24 | ns |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25 ⁴ | 1.55 | 2.76 | 0.26 | 1.19 | 1.63 | 1.10 | 2.79 | 2.16 | 3.29 | 3.97 | 8.58 | 7.94 | ns |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25 ⁴ | 1.55 | 2.76 | 0.25 | 1.22 | 1.58 | 1.10 | 2.79 | 2.16 | 3.29 | 3.97 | 8.58 | 7.94 | ns |
| 3.3 V GTL | 20 ⁵ | – | High | 10 | 25 | 1.55 | 2.08 | 0.25 | 2.76 | – | 1.10 | 2.09 | 2.08 | – | – | 7.88 | 7.87 | ns |
| 2.5 V GTL | 20 ⁵ | – | High | 10 | 25 | 1.55 | 2.17 | 0.25 | 2.35 | – | 1.10 | 2.20 | 2.13 | – | – | 7.99 | 7.91 | ns |
| 3.3 V GTL+ | 35 | – | High | 10 | 25 | 1.55 | 2.12 | 0.25 | 1.62 | – | 1.10 | 2.14 | 2.07 | – | – | 7.93 | 7.85 | ns |
| 2.5 V GTL+ | 33 | – | High | 10 | 25 | 1.55 | 2.25 | 0.25 | 1.55 | – | 1.10 | 2.27 | 2.10 | – | – | 8.06 | 7.89 | ns |
| HSTL (I) | 8 | – | High | 20 | 50 | 1.55 | 3.09 | 0.25 | 1.95 | – | 1.10 | 3.11 | 3.09 | – | – | 8.90 | 8.88 | ns |
| HSTL (II) | 15 | – | High | 20 | 25 | 1.55 | 2.94 | 0.25 | 1.95 | – | 1.10 | 2.98 | 2.74 | – | – | 8.77 | 8.53 | ns |
| SSTL2 (I) | 15 | – | High | 30 | 50 | 1.55 | 2.18 | 0.25 | 1.40 | – | 1.10 | 2.21 | 2.03 | – | – | 7.99 | 7.82 | ns |
| SSTL2 (II) | 18 | – | High | 30 | 25 | 1.55 | 2.21 | 0.25 | 1.40 | – | 1.10 | 2.24 | 1.97 | – | – | 8.03 | 7.76 | ns |
| SSTL3 (I) | 14 | – | High | 30 | 50 | 1.55 | 2.33 | 0.25 | 1.33 | – | 1.10 | 2.36 | 2.02 | – | – | 8.15 | 7.81 | ns |
| SSTL3 (II) | 21 | – | High | 30 | 25 | 1.55 | 2.13 | 0.25 | 1.33 | – | 1.10 | 2.16 | 1.89 | – | – | 7.94 | 7.67 | ns |

Notes:

1. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-12 on page 2-49](#) for connectivity. This resistor is not required during normal operation.
5. Output drive strength is below JEDEC specification.
6. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings (continued)
 Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
 Worst-Case V_{CCI} (per standard)

| I/O Standard | Drive Strength (mA) | Equivalent Software Default Drive Strength Option ¹ (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | t_{POUT} (ns) | t_{PP} (ns) | t_{PIN} (ns) | t_{PY} (ns) | t_{PYS} (ns) | t_{EOUT} (ns) | t_{ZL} (ns) | t_{ZH} (ns) | t_{LZ} (ns) | t_{HZ} (ns) | t_{ZLS} (ns) | t_{ZHS} (ns) | Units |
|--------------|---------------------|---|-----------|----------------------|--------------------------------|-----------------|---------------|----------------|---------------|----------------|-----------------|---------------|---------------|---------------|---------------|----------------|----------------|-------|
| LVDS | 24 | – | High | – | – | 1.55 | 2.26 | 0.25 | 1.95 | – | – | – | – | – | – | – | – | ns |
| LVPECL | 24 | – | High | – | – | 1.55 | 2.17 | 0.25 | 1.70 | – | – | – | – | – | – | – | – | ns |

Notes:

1. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-12](#) on page 2-49 for connectivity. This resistor is not required during normal operation.
5. Output drive strength is below JEDEC specification.
6. For specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on page 2-6 for derating values.

Detailed I/O DC Characteristics

Table 2-27 • Input Capacitance

| Symbol | Definition | Conditions | Min. | Max. | Units |
|-------------|------------------------------------|-----------------------------------|------|------|-------|
| C_{IN} | Input capacitance | $V_{IN} = 0, f = 1.0 \text{ MHz}$ | | 8 | pF |
| C_{INCLK} | Input capacitance on the clock pin | $V_{IN} = 0, f = 1.0 \text{ MHz}$ | | 8 | pF |

Table 2-28 • I/O Output Buffer Maximum Resistances¹

| Standard | Drive Strength | $R_{PULL-DOWN} (\Omega)^2$ | $R_{PULL-UP} (\Omega)^3$ |
|--------------------------------------|-------------------|------------------------------|------------------------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 4 mA | 100 | 300 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 3.3 V LVCMOS Wide Range | 100 μA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 100 | 200 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 1.2 V LVCMOS ⁴ | 2 mA | 158 | 164 |
| 1.2 V LVCMOS Wide Range ⁴ | 100 μA | Same as regular 1.2 V LVCMOS | Same as regular 1.2 V LVCMOS |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at <http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$
4. Applicable to IGLOOe V2 devices operating in the 1.2 V core range ONLY.
5. Output drive strength is below JEDEC specification.

Table 2-28 • I/O Output Buffer Maximum Resistances¹ (continued)

| Standard | Drive Strength | R _{PULL-DOWN} (Ω) ² | R _{PULL-UP} (Ω) ³ |
|-----------------|-----------------------------|---|---------------------------------------|
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |
| 3.3 V GTL | 20 mA ⁵ | 11 | – |
| 2.5 V GTL | 20 mA ⁵ | 14 | – |
| 3.3 V GTL+ | 35 mA | 12 | – |
| 2.5 V GTL+ | 33 mA | 15 | – |
| HSTL (I) | 8 mA | 50 | 50 |
| HSTL (II) | 15 mA | 25 | 25 |
| SSTL2 (I) | 15 mA | 27 | 31 |
| SSTL2 (II) | 18 mA | 13 | 15 |
| SSTL3 (I) | 14 mA | 44 | 69 |
| SSTL3 (II) | 21 mA | 18 | 32 |

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at <http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$
4. Applicable to IGLOOe V2 devices operating in the 1.2 V core range ONLY.
5. Output drive strength is below JEDEC specification.

**Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| VCCI | R _(WEAK PULL-UP) ¹ (Ω) | | R _(WEAK PULL-DOWN) ² (Ω) | |
|-------------------------|---|---------|---|---------|
| | Minimum | Maximum | Minimum | Maximum |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 3.3 V (wide range I/Os) | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |
| 1.2 V | 25 k | 110 k | 25 k | 150 k |
| 1.2 V (wide range I/Os) | 19 k | 110 k | 19 k | 150 k |

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN-MIN)}$

Table 2-30 • I/O Short Currents IOSH/IOSL

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|-----------------------------|--------------------------------|---------------------------------|---------------------------------|
| 3.3 V LVTTTL / 3.3 V LVCMOS | 4 mA | 25 | 27 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 3.3 V LVCMOS Wide Range | 100 μ A | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 16 | 18 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |
| 1.2 V LVCMOS | 2 mA | 20 | 26 |
| 1.2 V LVCMOS Wide Range | 100 μ A | 20 | 26 |
| 3.3 V PCI/PCIX | Per PCI/PCI-X Specification | Per PCI Curves | |
| 3.3 V GTL | 25 mA | 268 | 181 |
| 2.5 V GTL | 25 mA | 169 | 124 |
| 3.3 V GTL+ | 35 mA | 268 | 181 |
| 2.5 V GTL+ | 33 mA | 169 | 124 |
| HSTL (I) | 8 mA | 32 | 39 |
| HSTL (II) | 15 mA | 66 | 55 |
| SSTL2 (I) | 15 mA | 83 | 87 |
| SSTL2 (II) | 18 mA | 169 | 124 |
| SSTL3 (I) | 14 mA | 51 | 54 |
| SSTL3 (II) | 21 mA | 103 | 109 |

Note: $T_J = 100^\circ\text{C}$

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • Duration of Short Circuit Event before Failure

| Temperature | Time before Failure |
|-------------|---------------------|
| -40°C | > 20 years |
| 0°C | > 20 years |
| 25°C | > 20 years |
| 70°C | 5 years |
| 85°C | 2 years |
| 100°C | 6 months |

**Table 2-32 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers**

| Input Buffer Configuration | Hysteresis Value (typ.) |
|--|-------------------------|
| 3.3 V LVTTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode) | 240 mV |
| 2.5 V LVCMOS (Schmitt trigger mode) | 140 mV |
| 1.8 V LVCMOS (Schmitt trigger mode) | 80 mV |
| 1.5 V LVCMOS (Schmitt trigger mode) | 60 mV |
| 1.2 V LVCMOS (Schmitt trigger mode) | 40 mV |

Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability*

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|--|-----------------------------|---|------------------|
| LVTTTL/LVCMOS (Schmitt trigger disabled) | No requirement | 10 ns* | 20 years (100°C) |
| LVTTTL/LVCMOS (Schmitt trigger enabled) | No requirement | No requirement, but input noise voltage cannot exceed Schmitt hysteresis. | 20 years (100°C) |
| HSTL/SSTL/GTL | No requirement | 10 ns* | 10 years (100°C) |
| LVDS/B-LVDS/M-LVDS/LVPECL | No requirement | 10 ns* | 10 years (100°C) |

Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTTL support.

Table 2-34 • Minimum and Maximum DC Input and Output Levels

| 3.3 V LVTTTL / 3.3 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|--------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |
| 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 103 | 109 | 10 | 10 |
| 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 132 | 127 | 10 | 10 |
| 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 268 | 181 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

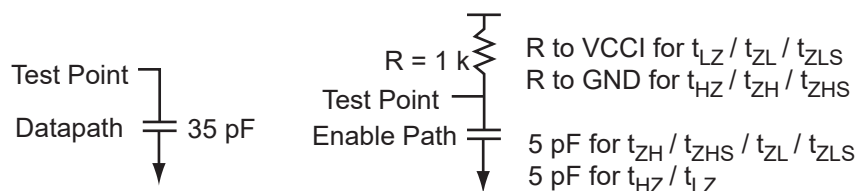


Figure 2-7 • AC Loading

Table 2-35 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 3.3 | 1.4 | – | 5 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-36 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.97 | 4.90 | 0.18 | 1.08 | 1.34 | 0.66 | 5.00 | 3.99 | 2.27 | 2.16 | 8.60 | 7.59 | ns |
| 8 mA | Std. | 0.97 | 4.05 | 0.18 | 1.08 | 1.34 | 0.66 | 4.13 | 3.45 | 2.53 | 2.65 | 7.73 | 7.05 | ns |
| 12 mA | Std. | 0.97 | 3.44 | 0.18 | 1.08 | 1.34 | 0.66 | 3.51 | 3.05 | 2.71 | 2.95 | 7.11 | 6.64 | ns |
| 16 mA | Std. | 0.97 | 3.27 | 0.18 | 1.08 | 1.34 | 0.66 | 3.34 | 2.96 | 2.74 | 3.04 | 6.93 | 6.55 | ns |
| 24 mA | Std. | 0.97 | 3.18 | 0.18 | 1.08 | 1.34 | 0.66 | 3.24 | 2.97 | 2.79 | 3.36 | 6.84 | 6.56 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-37 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 0.97 | 2.85 | 0.18 | 1.08 | 1.34 | 0.66 | 2.92 | 2.27 | 2.27 | 2.27 | 6.51 | 5.87 | ns |
| 8 mA | Std. | 0.97 | 2.39 | 0.18 | 1.08 | 1.34 | 0.66 | 2.44 | 1.88 | 2.53 | 2.76 | 6.03 | 5.47 | ns |
| 12 mA | Std. | 0.97 | 2.12 | 0.18 | 1.08 | 1.34 | 0.66 | 2.17 | 1.69 | 2.71 | 3.08 | 5.76 | 5.28 | ns |
| 16 mA | Std. | 0.97 | 2.08 | 0.18 | 1.08 | 1.34 | 0.66 | 2.12 | 1.65 | 2.75 | 3.17 | 5.72 | 5.25 | ns |
| 24 mA | Std. | 0.97 | 2.10 | 0.18 | 1.08 | 1.34 | 0.66 | 2.14 | 1.60 | 2.80 | 3.49 | 5.74 | 5.20 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-38 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 1.55 | 5.54 | 0.26 | 1.31 | 1.58 | 1.10 | 5.63 | 4.53 | 2.79 | 2.87 | 11.42 | 10.32 | ns |
| 8 mA | Std. | 1.55 | 4.60 | 0.26 | 1.31 | 1.58 | 1.10 | 4.67 | 3.94 | 3.09 | 3.45 | 10.45 | 9.73 | ns |
| 12 mA | Std. | 1.55 | 3.93 | 0.26 | 1.31 | 1.58 | 1.10 | 3.99 | 3.51 | 3.28 | 3.82 | 9.77 | 9.29 | ns |
| 16 mA | Std. | 1.55 | 3.74 | 0.26 | 1.31 | 1.58 | 1.10 | 3.79 | 3.41 | 3.32 | 3.92 | 9.58 | 9.20 | ns |
| 24 mA | Std. | 1.55 | 3.64 | 0.26 | 1.31 | 1.58 | 1.10 | 3.69 | 3.42 | 3.38 | 4.30 | 9.48 | 9.21 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-39 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 1.55 | 3.26 | 0.26 | 1.31 | 1.58 | 1.10 | 3.33 | 2.67 | 2.79 | 3.01 | 9.12 | 8.46 | ns |
| 8 mA | Std. | 1.55 | 2.77 | 0.26 | 1.31 | 1.58 | 1.10 | 2.80 | 2.24 | 3.09 | 3.59 | 8.59 | 8.03 | ns |
| 12 mA | Std. | 1.55 | 2.47 | 0.26 | 1.31 | 1.58 | 1.10 | 2.51 | 2.04 | 3.28 | 3.97 | 8.29 | 7.82 | ns |
| 16 mA | Std. | 1.55 | 2.42 | 0.26 | 1.31 | 1.58 | 1.10 | 2.46 | 2.00 | 3.33 | 4.08 | 8.24 | 7.79 | ns |
| 24 mA | Std. | 1.55 | 2.45 | 0.26 | 1.31 | 1.58 | 1.10 | 2.48 | 1.95 | 3.38 | 4.46 | 8.26 | 7.73 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

3.3 V LVCMOS Wide Range

Table 2-40 • Minimum and Maximum DC Input and Output Levels

| 3.3 V LVCMOS Wide Range | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|-------------------------|--|----------|----------|----------|---------|----------|-----------|---------------|---------------|------------------------|------------------------|----------------------------|----------------------------|
| Drive Strength | Equivalent Software Default Drive Strength Option ³ | Min. (V) | Max. (V) | Min. (V) | Max (V) | Max. (V) | Min. (V) | μA | μA | Max. (mA) ⁴ | Max. (mA) ⁴ | μA ⁵ | μA ⁵ |
| 100 μA | 2 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 μA | 4 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 μA | 6 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 μA | 8 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 μA | 12 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |
| 100 μA | 16 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 132 | 127 | 10 | 10 |
| 100 μA | 24 mA | -0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD - 0.2 | 100 | 100 | 268 | 181 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
4. Currents are measured at 85°C junction temperature.
5. All LVCMOS 3.3 V software macros supports LVCMOS 3.3 V wide range as specified in the JEDEC8a specification.
6. Software default selection highlighted in gray.

Table 2-41 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 3.3 | 1.4 | - | 5 |

Note: *Measuring point = V_{trip} . See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-42 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

| Drive Strength | Equivalent Software Default Drive Strength Option ¹ | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------------|--|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 100 μA | 4 mA | Std. | 0.97 | 7.26 | 0.18 | 1.42 | 1.84 | 0.66 | 7.28 | 5.78 | 3.18 | 2.93 | 10.88 | 9.38 | ns |
| 100 μA | 8 mA | Std. | 0.97 | 5.94 | 0.18 | 1.42 | 1.84 | 0.66 | 5.96 | 4.96 | 3.59 | 3.69 | 9.56 | 8.56 | ns |
| 100 μA | 12 mA | Std. | 0.97 | 5.00 | 0.18 | 1.42 | 1.84 | 0.66 | 5.02 | 4.34 | 3.86 | 4.16 | 8.62 | 7.94 | ns |
| 100 μA | 16 mA | Std. | 0.97 | 4.73 | 0.18 | 1.42 | 1.84 | 0.66 | 4.75 | 4.21 | 3.92 | 4.29 | 8.35 | 7.81 | ns |
| 100 μA | 24 mA | Std. | 0.97 | 4.59 | 0.18 | 1.42 | 1.84 | 0.66 | 4.61 | 4.23 | 3.99 | 4.78 | 8.21 | 7.82 | ns |

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-43 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

| Drive Strength | Equivalent Software Default Drive Strength Option ¹ | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------------|--|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 100 μA | 4 mA | Std. | 0.97 | 4.10 | 0.18 | 1.42 | 1.84 | 0.66 | 4.12 | 3.17 | 3.18 | 3.11 | 7.71 | 6.77 | ns |
| 100 μA | 8 mA | Std. | 0.97 | 3.37 | 0.18 | 1.42 | 1.84 | 0.66 | 3.39 | 2.57 | 3.59 | 3.87 | 6.99 | 6.16 | ns |
| 100 μA | 12 mA | Std. | 0.97 | 2.96 | 0.18 | 1.42 | 1.84 | 0.66 | 2.98 | 2.28 | 3.86 | 4.36 | 6.58 | 5.87 | ns |
| 100 μA | 16 mA | Std. | 0.97 | 2.90 | 0.18 | 1.42 | 1.84 | 0.66 | 2.92 | 2.22 | 3.93 | 4.49 | 6.51 | 5.82 | ns |
| 100 μA | 24 mA | Std. | 0.97 | 2.92 | 0.18 | 1.42 | 1.84 | 0.66 | 2.94 | 2.15 | 4.00 | 4.99 | 6.54 | 5.75 | ns |

Notes:

1. The minimum drive strength for any or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

1.2 V DC Core Voltage

Table 2-44 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

| Drive Strength | Equivalent Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------------|--|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 100 μA | 4 mA | Std. | 1.55 | 8.14 | 0.26 | 1.66 | 2.14 | 1.10 | 8.14 | 6.46 | 3.80 | 3.79 | 13.93 | 12.25 | ns |
| 100 μA | 8 mA | Std. | 1.55 | 6.68 | 0.26 | 1.66 | 2.14 | 1.10 | 6.68 | 5.57 | 4.25 | 4.69 | 12.47 | 11.36 | ns |
| 100 μA | 12 mA | Std. | 1.55 | 5.65 | 0.26 | 1.66 | 2.14 | 1.10 | 5.65 | 4.91 | 4.55 | 5.25 | 11.44 | 10.69 | ns |
| 100 μA | 16 mA | Std. | 1.55 | 5.36 | 0.26 | 1.66 | 2.14 | 1.10 | 5.36 | 4.76 | 4.61 | 5.41 | 11.14 | 10.55 | ns |
| 100 μA | 24 mA | Std. | 1.55 | 5.20 | 0.26 | 1.66 | 2.14 | 1.10 | 5.20 | 4.78 | 4.69 | 6.00 | 10.99 | 10.56 | ns |

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-45 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

| Drive Strength | Equivalent Software Default Drive Strength Option ¹ | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------------|--|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 100 μA | 4 mA | Std. | 1.55 | 4.65 | 0.26 | 1.66 | 2.14 | 1.10 | 4.65 | 3.64 | 3.80 | 4.00 | 10.44 | 9.43 | ns |
| 100 μA | 8 mA | Std. | 1.55 | 3.85 | 0.26 | 1.66 | 2.14 | 1.10 | 3.85 | 2.99 | 4.25 | 4.91 | 9.64 | 8.77 | ns |
| 100 μA | 12 mA | Std. | 1.55 | 3.40 | 0.26 | 1.66 | 2.14 | 1.10 | 3.40 | 2.68 | 4.55 | 5.49 | 9.19 | 8.46 | ns |
| 100 μA | 16 mA | Std. | 1.55 | 3.33 | 0.26 | 1.66 | 2.14 | 1.10 | 3.33 | 2.62 | 4.62 | 5.65 | 9.11 | 8.41 | ns |
| 100 μA | 24 mA | Std. | 1.55 | 3.36 | 0.26 | 1.66 | 2.14 | 1.10 | 3.36 | 2.54 | 4.71 | 6.24 | 9.15 | 8.32 | ns |

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-46 • Minimum and Maximum DC Input and Output Levels

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|--------------|--------|--------|--------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 4 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 16 | 18 | 10 | 10 |
| 8 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 32 | 37 | 10 | 10 |
| 12 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 65 | 74 | 10 | 10 |
| 16 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 16 | 16 | 83 | 87 | 10 | 10 |
| 24 mA | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 24 | 24 | 169 | 124 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

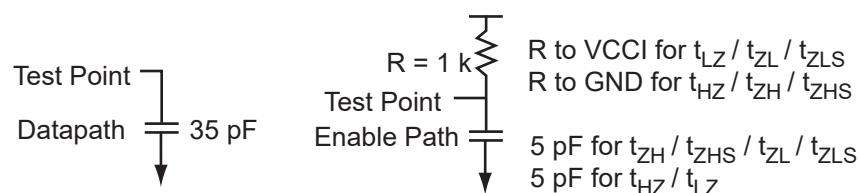


Figure 2-8 • AC Loading

Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 2.5 | 1.2 | – | 5 |

Note: *Measuring point = V_{trip} . See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-48 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Unit |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|------|
| 4 mA | Std. | 0.97 | 5.55 | 0.18 | 1.31 | 1.41 | 0.66 | 5.66 | 4.75 | 2.28 | 1.96 | 9.26 | 8.34 | ns |
| 8 mA | Std. | 0.97 | 4.58 | 0.18 | 1.31 | 1.41 | 0.66 | 4.67 | 4.07 | 2.58 | 2.53 | 8.27 | 7.66 | ns |
| 12 mA | Std. | 0.97 | 3.89 | 0.18 | 1.31 | 1.41 | 0.66 | 3.97 | 3.58 | 2.78 | 2.91 | 7.56 | 7.17 | ns |
| 16 mA | Std. | 0.97 | 3.68 | 0.18 | 1.31 | 1.41 | 0.66 | 3.75 | 3.47 | 2.82 | 3.01 | 7.35 | 7.06 | ns |
| 24 mA | Std. | 0.97 | 3.59 | 0.18 | 1.31 | 1.41 | 0.66 | 3.66 | 3.48 | 2.88 | 3.37 | 7.26 | 7.08 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-49 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Unit |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|------|
| 4 mA | Std. | 0.97 | 2.94 | 0.18 | 1.31 | 1.41 | 0.66 | 3.00 | 2.68 | 2.28 | 2.03 | 6.60 | 6.27 | ns |
| 8 mA | Std. | 0.97 | 2.45 | 0.18 | 1.31 | 1.41 | 0.66 | 2.50 | 2.12 | 2.58 | 2.62 | 6.10 | 5.72 | ns |
| 12 mA | Std. | 0.97 | 2.15 | 0.18 | 1.31 | 1.41 | 0.66 | 2.20 | 1.85 | 2.78 | 2.98 | 5.80 | 5.45 | ns |
| 16 mA | Std. | 0.97 | 2.10 | 0.18 | 1.31 | 1.41 | 0.66 | 2.15 | 1.80 | 2.82 | 3.08 | 5.75 | 5.40 | ns |
| 24 mA | Std. | 0.97 | 2.11 | 0.18 | 1.31 | 1.41 | 0.66 | 2.16 | 1.74 | 2.88 | 3.47 | 5.75 | 5.33 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-50 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 1.55 | 6.25 | 0.26 | 1.55 | 1.77 | 1.10 | 6.36 | 5.34 | 2.81 | 2.63 | 12.14 | 11.13 | ns |
| 8 mA | Std. | 1.55 | 5.18 | 0.26 | 1.55 | 1.77 | 1.10 | 5.26 | 4.61 | 3.13 | 3.32 | 11.05 | 10.39 | ns |
| 12 mA | Std. | 1.55 | 4.42 | 0.26 | 1.55 | 1.77 | 1.10 | 4.49 | 4.08 | 3.36 | 3.76 | 10.28 | 9.86 | ns |
| 16 mA | Std. | 1.55 | 4.19 | 0.26 | 1.55 | 1.77 | 1.10 | 4.25 | 3.96 | 3.40 | 3.89 | 10.04 | 9.75 | ns |
| 24 mA | Std. | 1.55 | 4.09 | 0.26 | 1.55 | 1.76 | 1.10 | 4.15 | 3.97 | 3.47 | 4.32 | 9.94 | 9.76 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 4 mA | Std. | 1.55 | 3.38 | 0.26 | 1.55 | 1.77 | 1.10 | 3.42 | 3.11 | 2.81 | 2.72 | 9.21 | 8.89 | ns |
| 8 mA | Std. | 1.55 | 2.83 | 0.26 | 1.55 | 1.77 | 1.10 | 2.87 | 2.51 | 3.13 | 3.42 | 8.66 | 8.30 | ns |
| 12 mA | Std. | 1.55 | 2.51 | 0.26 | 1.55 | 1.77 | 1.10 | 2.54 | 2.22 | 3.36 | 3.85 | 8.33 | 8.00 | ns |
| 16 mA | Std. | 1.55 | 2.45 | 0.26 | 1.55 | 1.77 | 1.10 | 2.48 | 2.16 | 3.40 | 3.97 | 8.27 | 7.95 | ns |
| 24 mA | Std. | 1.55 | 2.46 | 0.26 | 1.55 | 1.77 | 1.10 | 2.49 | 2.09 | 3.47 | 4.44 | 8.28 | 7.88 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-52 • Minimum and Maximum DC Input and Output Levels

| 1.8 V LVCMOS Drive Strength | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|-----------------------------|--------|-------------|-------------|--------|--------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 2 | 2 | 9 | 11 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 4 | 4 | 17 | 22 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 6 | 6 | 35 | 44 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 8 | 8 | 45 | 51 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 12 | 12 | 91 | 74 | 10 | 10 |
| 16 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI - 0.45 | 16 | 16 | 91 | 74 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

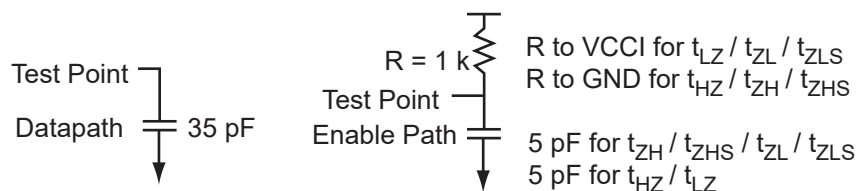


Figure 2-9 • AC Loading

Table 2-53 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 1.8 | 0.9 | - | 5 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-54 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 2 mA | Std. | 0.97 | 7.33 | 0.18 | 1.27 | 1.59 | 0.66 | 7.47 | 6.18 | 2.34 | 1.18 | 11.07 | 9.77 | ns |
| 4 mA | Std. | 0.97 | 6.07 | 0.18 | 1.27 | 1.59 | 0.66 | 6.20 | 5.25 | 2.69 | 2.42 | 9.79 | 8.84 | ns |
| 6 mA | Std. | 0.97 | 5.18 | 0.18 | 1.27 | 1.59 | 0.66 | 5.29 | 4.61 | 2.93 | 2.88 | 8.88 | 8.21 | ns |
| 8 mA | Std. | 0.97 | 4.88 | 0.18 | 1.27 | 1.59 | 0.66 | 4.98 | 4.48 | 2.99 | 3.01 | 8.58 | 8.08 | ns |
| 12 mA | Std. | 0.97 | 4.80 | 0.18 | 1.27 | 1.59 | 0.66 | 4.89 | 4.49 | 3.07 | 3.47 | 8.49 | 8.09 | ns |
| 16 mA | Std. | 0.97 | 4.80 | 0.18 | 1.27 | 1.59 | 0.66 | 4.89 | 4.49 | 3.07 | 3.47 | 8.49 | 8.09 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-55 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 2 mA | Std. | 0.97 | 3.43 | 0.18 | 1.27 | 1.59 | 0.66 | 3.51 | 3.39 | 2.33 | 1.19 | 7.10 | 6.98 | ns |
| 4 mA | Std. | 0.97 | 2.83 | 0.18 | 1.27 | 1.59 | 0.66 | 2.89 | 2.59 | 2.69 | 2.49 | 6.48 | 6.18 | ns |
| 6 mA | Std. | 0.97 | 2.45 | 0.18 | 1.27 | 1.59 | 0.66 | 2.51 | 2.19 | 2.93 | 2.95 | 6.10 | 5.79 | ns |
| 8 mA | Std. | 0.97 | 2.38 | 0.18 | 1.27 | 1.59 | 0.66 | 2.43 | 2.12 | 2.98 | 3.08 | 6.03 | 5.71 | ns |
| 12 mA | Std. | 0.97 | 2.37 | 0.18 | 1.27 | 1.59 | 0.66 | 2.42 | 2.03 | 3.07 | 3.57 | 6.02 | 5.62 | ns |
| 16 mA | Std. | 0.97 | 2.37 | 0.18 | 1.27 | 1.59 | 0.66 | 2.42 | 2.03 | 3.07 | 3.57 | 6.02 | 5.62 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 1.55 | 8.21 | 0.26 | 1.53 | 1.96 | 1.10 | 8.35 | 6.88 | 2.87 | 1.70 | 14.14 | 12.67 | ns |
| 4 mA | Std. | 1.55 | 6.83 | 0.26 | 1.53 | 1.96 | 1.10 | 6.94 | 5.88 | 3.27 | 3.18 | 12.73 | 11.67 | ns |
| 6 mA | Std. | 1.55 | 5.85 | 0.26 | 1.53 | 1.96 | 1.10 | 5.94 | 5.19 | 3.53 | 3.37 | 11.73 | 10.98 | ns |
| 8 mA | Std. | 1.55 | 5.52 | 0.26 | 1.53 | 1.96 | 1.10 | 5.61 | 5.06 | 3.59 | 3.88 | 11.39 | 10.84 | ns |
| 12 mA | Std. | 1.55 | 5.42 | 0.26 | 1.53 | 1.96 | 1.10 | 5.51 | 5.06 | 3.68 | 4.44 | 11.30 | 10.85 | ns |
| 16 mA | Std. | 1.55 | 5.42 | 0.26 | 1.53 | 1.96 | 1.10 | 5.51 | 5.06 | 3.68 | 4.44 | 11.30 | 10.85 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on page 2-6 for derating values.

Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 1.55 | 3.82 | 0.26 | 1.53 | 1.96 | 1.10 | 3.98 | 3.87 | 2.86 | 1.72 | 9.76 | 9.66 | ns |
| 4 mA | Std. | 1.55 | 3.25 | 0.26 | 1.53 | 1.96 | 1.10 | 3.30 | 3.01 | 3.26 | 3.26 | 9.08 | 8.79 | ns |
| 6 mA | Std. | 1.55 | 2.84 | 0.26 | 1.53 | 1.96 | 1.10 | 2.88 | 2.58 | 3.53 | 3.81 | 8.66 | 8.37 | ns |
| 8 mA | Std. | 1.55 | 2.76 | 0.26 | 1.53 | 1.96 | 1.10 | 2.80 | 2.50 | 3.58 | 3.97 | 8.58 | 8.29 | ns |
| 12 mA | Std. | 1.55 | 2.75 | 0.26 | 1.53 | 1.96 | 1.10 | 2.78 | 2.40 | 3.68 | 4.56 | 8.57 | 8.19 | ns |
| 16 mA | Std. | 1.55 | 2.75 | 0.26 | 1.53 | 1.96 | 1.10 | 2.78 | 2.40 | 3.68 | 4.56 | 8.57 | 8.19 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on page 2-6 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-58 • Minimum and Maximum DC Input and Output Levels

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|-----------------|-----------|-------------|-------------|-----------|-------------|-------------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 13 | 16 | 10 | 10 |
| 4 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 25 | 33 | 10 | 10 |
| 6 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 32 | 39 | 10 | 10 |
| 8 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 66 | 55 | 10 | 10 |
| 12 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 66 | 55 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

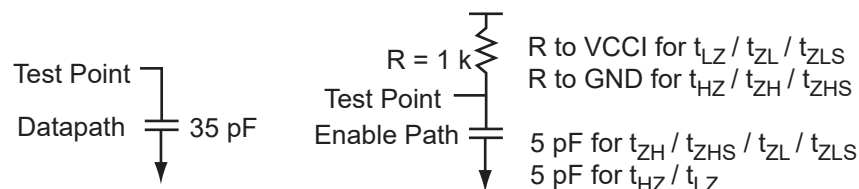


Figure 2-10 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 1.5 | 0.75 | – | 5 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-60 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 2 mA | Std. | 0.97 | 7.61 | 0.18 | 1.47 | 1.77 | 0.66 | 7.76 | 6.33 | 2.81 | 2.34 | 11.36 | 9.92 | ns |
| 4 mA | Std. | 0.97 | 6.54 | 0.18 | 1.47 | 1.77 | 0.66 | 6.67 | 5.56 | 3.09 | 2.88 | 10.26 | 9.16 | ns |
| 6 mA | Std. | 0.97 | 6.15 | 0.18 | 1.47 | 1.77 | 0.66 | 6.27 | 5.42 | 3.15 | 3.02 | 9.87 | 9.02 | ns |
| 8 mA | Std. | 0.97 | 6.07 | 0.18 | 1.47 | 1.77 | 0.66 | 6.20 | 5.42 | 2.64 | 3.56 | 9.79 | 9.02 | ns |
| 12 mA | Std. | 0.97 | 6.07 | 0.18 | 1.47 | 1.77 | 0.66 | 6.20 | 5.42 | 2.64 | 3.56 | 9.79 | 9.02 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-61 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 2 mA | Std. | 0.97 | 3.25 | 0.18 | 1.47 | 1.77 | 0.66 | 3.32 | 3.00 | 2.80 | 2.43 | 6.92 | 6.59 | ns |
| 4 mA | Std. | 0.97 | 2.81 | 0.18 | 1.47 | 1.77 | 0.66 | 2.87 | 2.51 | 3.08 | 2.97 | 6.46 | 6.10 | ns |
| 6 mA | Std. | 0.97 | 2.72 | 0.18 | 1.47 | 1.77 | 0.66 | 2.78 | 2.41 | 3.14 | 3.12 | 6.37 | 6.01 | ns |
| 8 mA | Std. | 0.97 | 2.69 | 0.18 | 1.47 | 1.77 | 0.66 | 2.75 | 2.30 | 3.24 | 3.67 | 6.35 | 5.89 | ns |
| 12 mA | Std. | 0.97 | 2.69 | 0.18 | 1.47 | 1.77 | 0.66 | 2.75 | 2.30 | 3.24 | 3.67 | 6.35 | 5.89 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-62 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 1.55 | 8.53 | 0.26 | 1.72 | 2.16 | 1.10 | 8.67 | 7.05 | 3.39 | 3.09 | 14.46 | 12.83 | ns |
| 4 mA | Std. | 1.55 | 7.34 | 0.26 | 1.72 | 2.16 | 1.10 | 7.46 | 6.22 | 3.70 | 3.73 | 13.25 | 12.01 | ns |
| 6 mA | Std. | 1.55 | 6.91 | 0.26 | 1.72 | 2.16 | 1.10 | 7.03 | 6.07 | 3.77 | 3.90 | 12.82 | 11.85 | ns |
| 8 mA | Std. | 1.55 | 6.83 | 0.26 | 1.72 | 2.16 | 1.10 | 6.94 | 6.07 | 2.91 | 4.54 | 12.73 | 11.86 | ns |
| 12 mA | Std. | 1.55 | 6.83 | 0.26 | 1.72 | 2.16 | 1.10 | 6.94 | 6.07 | 2.91 | 4.54 | 12.73 | 11.86 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-63 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

| Drive Strength | Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|----------------|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA | Std. | 1.55 | 3.72 | 0.26 | 1.72 | 2.16 | 1.10 | 3.78 | 3.45 | 3.38 | 3.19 | 9.56 | 9.24 | ns |
| 4 mA | Std. | 1.55 | 3.23 | 0.26 | 1.72 | 2.16 | 1.10 | 3.27 | 2.92 | 3.69 | 3.83 | 9.06 | 8.71 | ns |
| 6 mA | Std. | 1.55 | 3.13 | 0.26 | 1.72 | 2.16 | 1.10 | 3.18 | 2.82 | 3.76 | 4.01 | 8.96 | 8.61 | ns |
| 8 mA | Std. | 1.55 | 3.10 | 0.26 | 1.72 | 2.16 | 1.10 | 3.15 | 2.70 | 3.86 | 4.68 | 8.93 | 8.49 | ns |
| 12 mA | Std. | 1.55 | 3.10 | 0.26 | 1.72 | 2.16 | 1.10 | 3.15 | 2.70 | 3.86 | 4.68 | 8.93 | 8.49 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-64 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

| 1.2 V LVCMOS ¹ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ² | IIH ³ |
|---------------------------|--------|-------------|-------------|--------|-------------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ⁴ | Max. mA ⁴ | μA ⁵ | μA ⁵ |
| 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 20 | 26 | 10 | 10 |

Notes:

1. Applicable to V2 devices ONLY.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

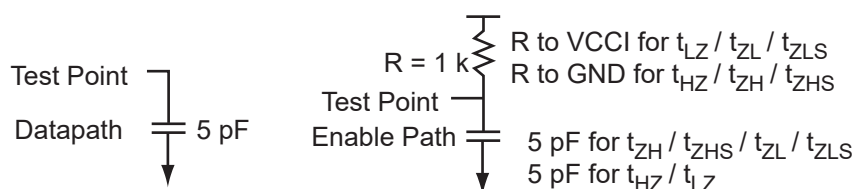


Figure 2-11 • AC Loading

Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0 | 1.2 | 0.6 | - | 5 |

Note: *Measuring point = V_{trip} . See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-66 • 1.2 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 2 mA | Std. | 1.55 | 9.92 | 0.26 | 2.09 | 2.95 | 1.10 | 9.53 | 7.48 | 4.02 | 3.67 | 15.31 | 13.26 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-67 • 1.2 LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

| Drive Strength | Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{PYS} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|----------------|-------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 2 mA | Std. | 1.55 | 4.06 | 0.26 | 2.09 | 2.95 | 1.10 | 3.92 | 3.46 | 4.01 | 3.79 | 9.71 | 9.24 | ns |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

| 1.2 V LVCMOS Wide Range ¹ | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ² | IIH ³ |
|--------------------------------------|--|----------|-------------|-------------|---------|-------------|-------------|-----|-----|------------------------|------------------------|------------------|------------------|
| Drive Strength | Equivalent Software Default Drive Strength Option ⁴ | Min. (V) | Max. (V) | Min. (V) | Max (V) | Max. (V) | Min. (V) | μA | μA | Max. (mA) ⁵ | Max. (mA) ⁵ | μA ⁶ | μA ⁶ |
| 100 μA | 2 mA | -0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 100 | 100 | 20 | 26 | 10 | 10 |

Notes:

1. Applicable to V2 devices ONLY.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is $\pm 100\ \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
5. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
6. Currents are measured at 85°C junction temperature.
7. Software default selection highlighted in gray.

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-48 for worst-case timing.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-69 • Minimum and Maximum DC Input and Output Levels

| 3.3 V PCI/PCI-X | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|-----------------------|----------------|--------|--------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in [Figure 2-12](#).

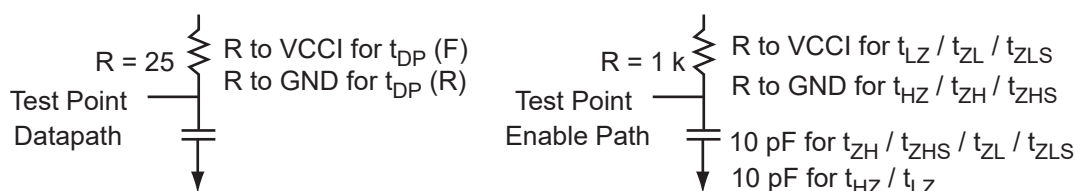


Figure 2-12 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in [Table 2-70](#).

Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|--|-----------------|------------------------|
| 0 | 3.3 | 0.285 * VCCI for t _{DP(R)} 0.615 * VCCI for t _{DP(F)} | – | 10 |

Note: *Measuring point = Vtrip. See [Table 2-23 on page 2-23](#) for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-71 • 3.3 V PCI/PCI-X – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 0.97 | 2.38 | 0.18 | 0.96 | 1.42 | 0.66 | 2.43 | 1.80 | 2.72 | 3.08 | 6.03 | 5.39 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-72 • 3.3 V PCI/PCI-X – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{PYS} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|-----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 1.55 | 2.76 | 0.26 | 1.19 | 1.63 | 1.10 | 2.79 | 2.16 | 3.29 | 3.97 | 8.58 | 7.94 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-73 • Minimum and Maximum DC Input and Output Levels

| 3.3 V GTL Drive Strength | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL ¹ | IIH ² |
|--------------------------------|-----------|-------------|-------------|-----------|----------|-----------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 20 mA ⁵ | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 | 268 | 181 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Output drive strength is below JEDEC specification.

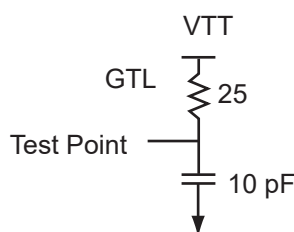


Figure 2-13 • AC Loading

Table 2-74 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.05 | VREF + 0.05 | 0.8 | 0.8 | 1.2 | 10 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-75 • 3.3 V GTL – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 3.0\text{ V}$ $V_{REF} = 0.8\text{ V}$

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 0.98 | 1.83 | 0.19 | 2.41 | 0.67 | 1.84 | 1.83 | | | 5.47 | 5.46 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-76 • 3.3 V GTL – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
 Worst-Case $V_{CCI} = 3.0\text{ V}$ $V_{REF} = 0.8\text{ V}$

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | t_{EOUT} | t_{ZL} | t_{ZH} | t_{LZ} | t_{HZ} | t_{ZLS} | t_{ZHS} | Units |
|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| Std. | 1.55 | 2.09 | 0.26 | 2.75 | 1.10 | 2.10 | 2.09 | | | 7.91 | 7.89 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-77 • Minimum and Maximum DC Input and Output Levels

| 2.5 GTL Drive Strength | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|------------------------------|-----------|-------------|-------------|-----------|-----------|-----------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 20 mA ⁵ | -0.3 | VREF - 0.05 | VREF + 0.05 | 3.6 | 0.4 | - | 20 | 20 | 169 | 124 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Output drive strength is below JEDEC specification.

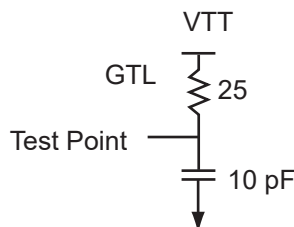


Figure 2-14 • AC Loading

Table 2-78 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.05 | VREF + 0.05 | 0.8 | 0.8 | 1.2 | 10 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-79 • 2.5 V GTL – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 3.0 V VREF = 0.8 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 1.90 | 0.19 | 2.04 | 0.67 | 1.94 | 1.87 | | | 5.57 | 5.50 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-80 • 2.5 V GTL – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
 Worst-Case VCCI = 3.0 V VREF = 0.8 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 2.16 | 0.26 | 2.35 | 1.10 | 2.20 | 2.13 | | | 8.01 | 7.94 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V

Table 2-81 • Minimum and Maximum DC Input and Output Levels

| 3.3 V GTL+ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | III ¹ | IIH ² |
|----------------|--------|------------|------------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 35 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 35 | 35 | 268 | 181 | 10 | 10 |

Notes:

1. III is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

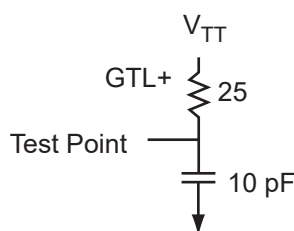


Figure 2-15 • AC Loading

Table 2-82 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 1.0 | 1.0 | 1.5 | 10 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-83 • 3.3 V GTL+ – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 3.0 V VREF = 1.0 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 1.85 | 0.19 | 1.35 | 0.67 | 1.88 | 1.81 | | | 5.51 | 5.44 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-84 • 3.3 V GTL+ – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
 Worst-Case VCCI = 3.0 V VREF = 1.0 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 2.11 | 0.26 | 1.61 | 1.10 | 2.15 | 2.07 | | | 7.95 | 7.88 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-85 • Minimum and Maximum DC Input and Output Levels

| 2.5 V GTL+ | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|----------------|--------|------------|------------|--------|--------|--------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 33 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.6 | - | 33 | 33 | 169 | 124 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

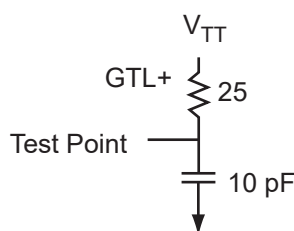


Figure 2-16 • AC Loading

Table 2-86 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 1.0 | 1.0 | 1.5 | 10 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-87 • 2.5 V GTL+ – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 2.3 V VREF = 1.0 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 1.97 | 0.19 | 1.29 | 0.67 | 2.00 | 1.84 | | | 5.63 | 5.47 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-88 • 2.5 V GTL+ – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
 Worst-Case VCCI = 2.3 V VREF = 1.0 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 2.23 | 0.26 | 1.55 | 1.10 | 2.28 | 2.11 | | | 8.08 | 7.91 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-89 • Minimum and Maximum DC Input and Output Levels

| HSTL Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|--------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 8 mA | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 8 | 8 | 32 | 39 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

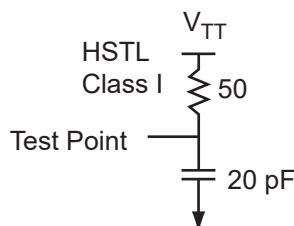


Figure 2-17 • AC Loading

Table 2-90 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-91 • HSTL Class I – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 2.74 | 0.19 | 1.77 | 0.67 | 2.79 | 2.73 | | | 6.42 | 6.36 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-92 • HSTL Class I – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 3.10 | 0.26 | 1.94 | 1.10 | 3.12 | 3.10 | | | 8.93 | 8.91 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGL00e devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-93 • Minimum and Maximum DC Input and Output Levels

| HSTL Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIH ¹ | IIH ² |
|--------------------|--------|------------|------------|--------|--------|------------|-----|-----|----------------------|----------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 15 mA ⁵ | -0.3 | VREF - 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI - 0.4 | 15 | 15 | 66 | 55 | 10 | 10 |

Notes:

1. IIH is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Output drive strength is below JEDEC specification.

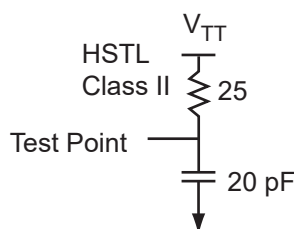


Figure 2-18 • AC Loading

Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-95 • HSTL Class II – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 1.4 V VREF = 0.75 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 2.62 | 0.19 | 1.77 | 0.67 | 2.66 | 2.40 | | | 6.29 | 6.03 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-96 • HSTL Class II – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
 Worst-Case VCCI = 1.4 V VREF = 0.75 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 2.93 | 0.26 | 1.94 | 1.10 | 2.98 | 2.75 | | | 8.79 | 8.55 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-97 • Minimum and Maximum DC Input and Output Levels

| SSTL2 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|------------------|-----------|------------|------------|-----------|-----------|-------------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 15 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI - 0.62 | 15 | 15 | 83 | 87 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

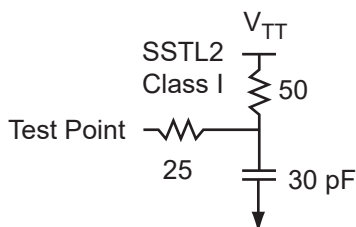


Figure 2-19 • AC Loading

Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-99 • SSTL 2 Class I – Applies to 1.5 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
 Worst-Case VCCI = 2.3 V VREF = 1.25 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 1.91 | 0.19 | 1.15 | 0.67 | 1.94 | 1.72 | | | 5.57 | 5.35 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-100 • SSTL 2 Class I – Applies to 1.2 V DC Core Voltage
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V,
 Worst-Case VCCI = 2.3 V VREF = 1.25 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 2.17 | 0.26 | 1.39 | 1.10 | 2.21 | 2.04 | | | 8.02 | 7.84 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-101 • Minimum and Maximum DC Input and Output Levels

| SSTL2 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|-------------------|-----------|------------|------------|-----------|-----------|-------------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA ³ | Max. mA ³ | μA ⁴ | μA ⁴ |
| 18 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI - 0.43 | 18 | 18 | 169 | 124 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

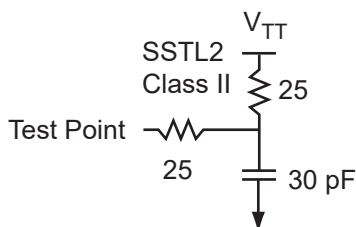


Figure 2-20 • AC Loading

Table 2-102 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input HIGH (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-103 • SSTL 2 Class II – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 1.94 | 0.19 | 1.15 | 0.67 | 1.97 | 1.66 | | | 5.60 | 5.29 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-104 • SSTL 2 Class II – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 2.20 | 0.26 | 1.39 | 1.10 | 2.24 | 1.97 | | | 8.05 | 7.78 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-105 • Minimum and Maximum DC Input and Output Levels

| SSTL3 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|---------------|--------|------------|------------|--------|--------|------------|-----|-----|-----------------|-----------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | mA ³ | mA ³ | μA ⁴ | μA ⁴ |
| 14 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI - 1.1 | 14 | 14 | 51 | 54 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

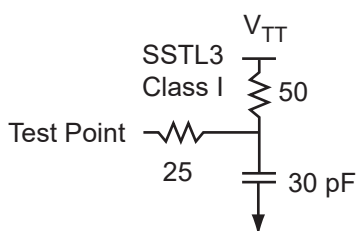


Figure 2-21 • AC Loading

Table 2-106 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-107 • SSTL 3 Class I – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 2.05 | 0.19 | 1.09 | 0.67 | 2.09 | 1.71 | | | 5.72 | 5.34 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-108 • SSTL 3 Class I – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 2.32 | 0.26 | 1.32 | 1.10 | 2.37 | 2.02 | | | 8.17 | 7.83 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-109 • Minimum and Maximum DC Input and Output Levels

| SSTL3 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL ¹ | IIH ² |
|----------------|--------|------------|------------|--------|--------|------------|-----|-----|-----------------|-----------------|------------------|------------------|
| | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | mA ³ | mA ³ | μA ⁴ | μA ⁴ |
| 21 mA | -0.3 | VREF - 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI - 0.9 | 21 | 21 | 103 | 109 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

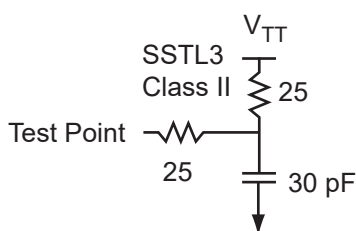


Figure 2-22 • AC Loading

Table 2-110 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C _{LOAD} (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF - 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

Note: Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-111 • SSTL 3 Class II – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 0.98 | 1.86 | 0.19 | 1.09 | 0.67 | 1.89 | 1.58 | | | 5.52 | 5.21 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-112 • SSTL 3 Class II – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 3.0 V VREF = 1.5 V

| Speed Grade | t _{DOUT} | t _{DP} | t _{DIN} | t _{PY} | t _{EOUT} | t _{ZL} | t _{ZH} | t _{LZ} | t _{HZ} | t _{ZLS} | t _{ZHS} | Units |
|-------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std. | 1.55 | 2.12 | 0.26 | 1.32 | 1.10 | 2.16 | 1.89 | | | 7.97 | 7.70 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-23](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, IGLOOe also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

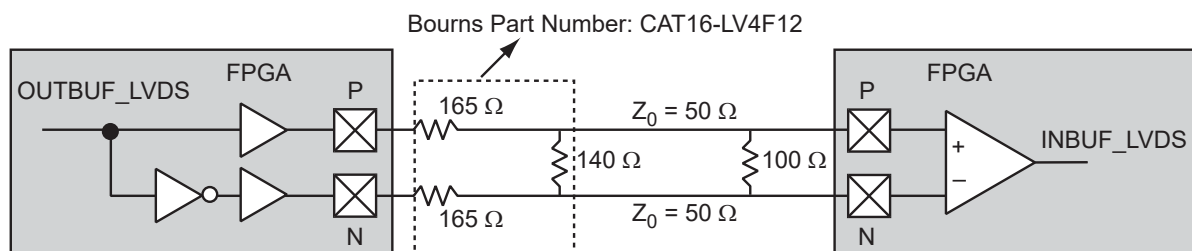


Figure 2-23 • LVDS Circuit Diagram and Board-Level Implementation

Table 2-113 • Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|--------------------|-----------------------------|-------|-------|-------|-------|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Output High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL ¹ | Output Lower Current | 0.65 | 0.91 | 1.16 | mA |
| IOH ¹ | Output High Current | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIH ^{2,3} | Input High Leakage Current | | | 10 | μA |
| IIL ^{2,4} | Input Low Leakage Current | | | 10 | μA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage | 100 | 350 | | mV |

Notes:

1. IOL/IOH is defined by VODIFF/(resistor network).
2. Currents are measured at 85°C junction temperature.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. IIL is the input leakage current per I/O pin over recommended operating conditions where $-0.3 \text{ V} < V_{IN} < V_{IL}$.

Table 2-114 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---------------|----------------|----------------------|-----------------|
| 1.075 | 1.325 | Cross point | – |

Note: *Measuring point = V_{trip} . See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics**1.5 V DC Core Voltage****Table 2-115 • LVDS – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{pY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 0.98 | 1.77 | 0.19 | 1.62 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage**Table 2-116 • LVDS – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{pY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 1.55 | 2.19 | 0.26 | 1.88 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in [Figure 2-24](#). The input and output buffer delays are available in the LVDS section in [Table 2-115 on page 2-63](#) and [Table 2-116 on page 2-63](#).

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60 \Omega$ and $R_T = 70 \Omega$, given $Z_0 = 50 \Omega$ (2") and $Z_{stub} = 50 \Omega$ (~1.5").

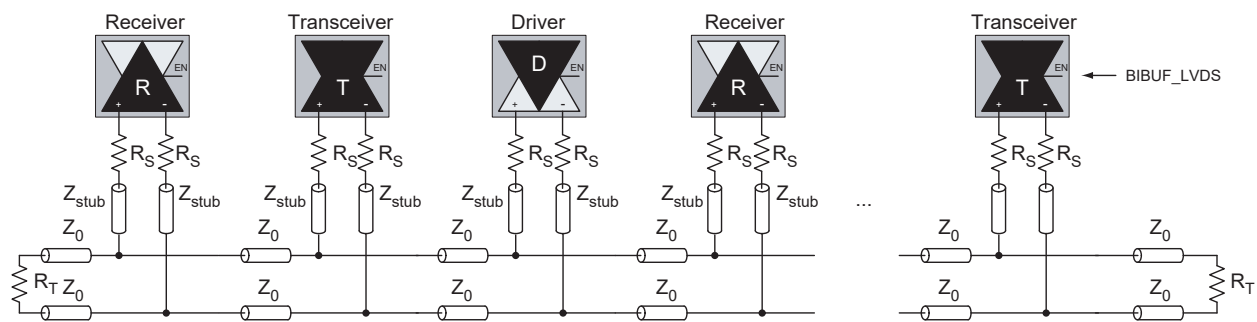


Figure 2-24 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-25](#). The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

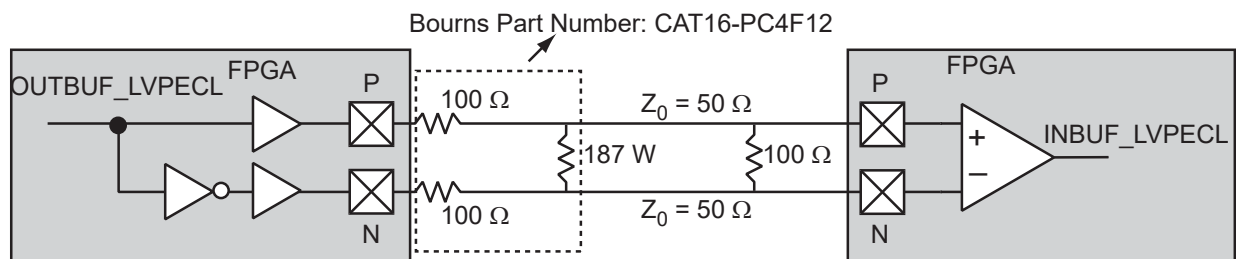


Figure 2-25 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-117 • Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|--------------|--------------------------------|-------|------|-------|------|-------|------|-------|
| VCCI | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | | 300 | | 300 | | mV |

Table 2-118 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input LOW (V) | Input HIGH (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---------------|----------------|----------------------|-----------------|
| 1.64 | 1.94 | Cross point | – |

Note: *Measuring point = V_{trip} . See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-119 • LVPECL – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 0.98 | 1.75 | 0.19 | 1.45 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-120 • LVPECL – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

| Speed Grade | t_{DOUT} | t_{DP} | t_{DIN} | t_{PY} | Units |
|-------------|------------|----------|-----------|----------|-------|
| Std. | 1.55 | 2.16 | 0.26 | 1.70 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

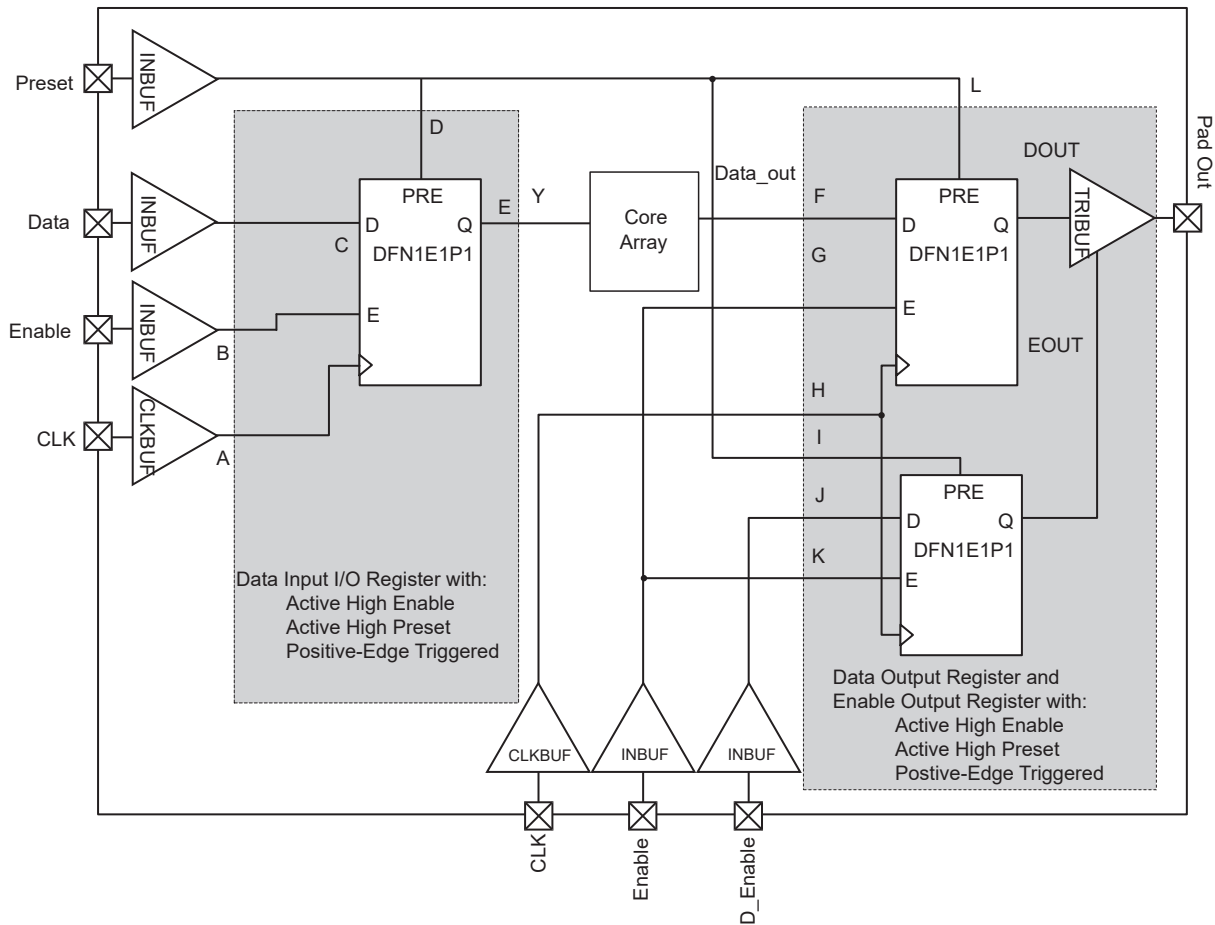


Figure 2-26 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-121 • Parameter Definition and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|----------------|--|-----------------------------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | H, DOUT |
| t_{OSUD} | Data Setup Time for the Output Data Register | F, H |
| t_{OHD} | Data Hold Time for the Output Data Register | F, H |
| t_{OSUE} | Enable Setup Time for the Output Data Register | G, H |
| t_{OHE} | Enable Hold Time for the Output Data Register | G, H |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | H, EOUT |
| t_{OESUD} | Data Setup Time for the Output Enable Register | J, H |
| t_{OEHD} | Data Hold Time for the Output Enable Register | J, H |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | K, H |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | K, H |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |
| t_{iCLKQ} | Clock-to-Q of the Input Data Register | A, E |
| t_{iSUD} | Data Setup Time for the Input Data Register | C, A |
| t_{iHD} | Data Hold Time for the Input Data Register | C, A |
| t_{iSUE} | Enable Setup Time for the Input Data Register | B, A |
| t_{iHE} | Enable Hold Time for the Input Data Register | B, A |
| t_{iPRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| $t_{iREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| $t_{iRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

Note: See Figure 2-26 on page 2-66 for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

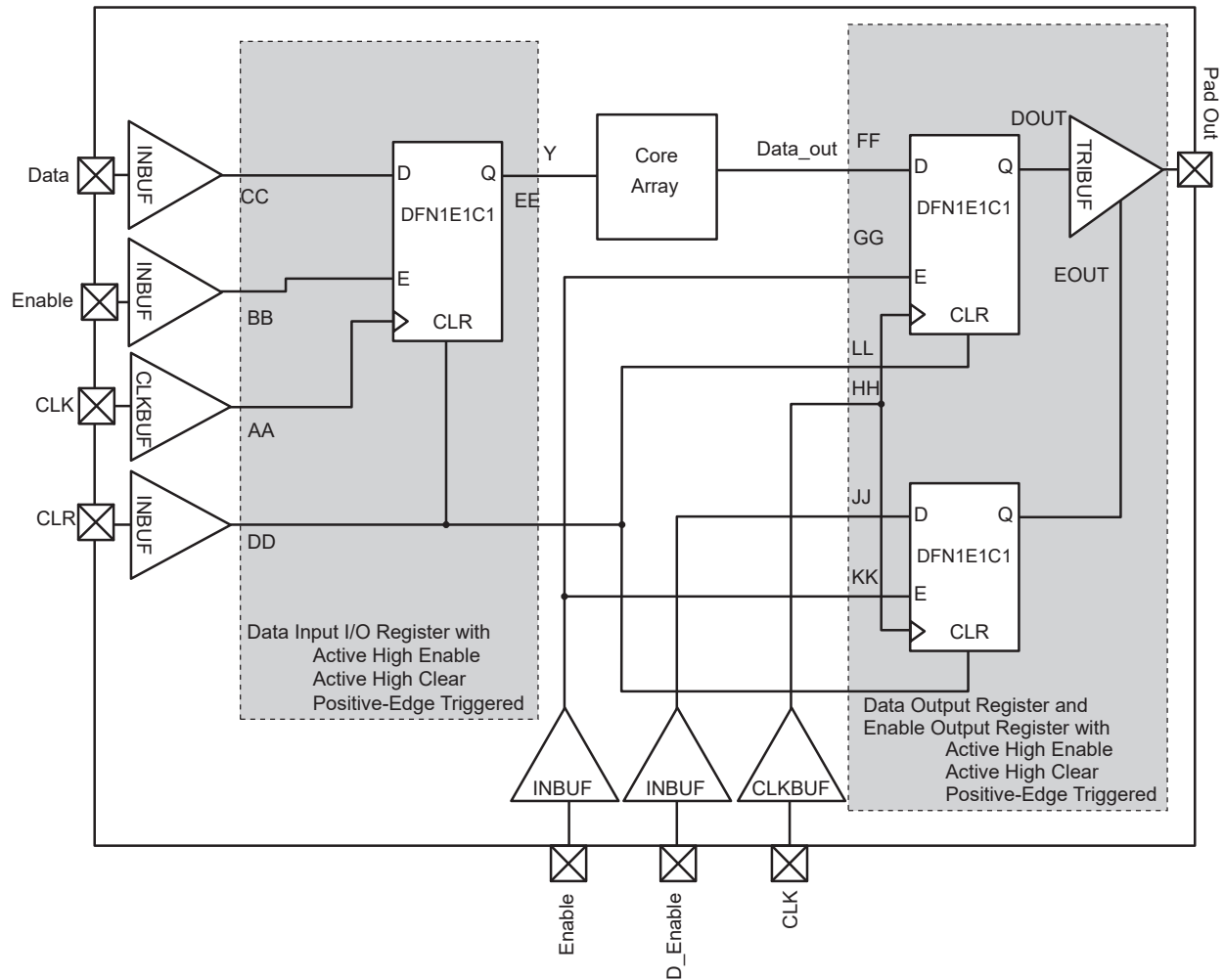


Figure 2-27 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Table 2-122 • Parameter Definition and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|----------------|---|-----------------------------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | HH, DOUT |
| t_{OSUD} | Data Setup Time for the Output Data Register | FF, HH |
| t_{OHD} | Data Hold Time for the Output Data Register | FF, HH |
| t_{OSUE} | Enable Setup Time for the Output Data Register | GG, HH |
| t_{OHE} | Enable Hold Time for the Output Data Register | GG, HH |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OERMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | HH, EOUT |
| t_{OESUD} | Data Setup Time for the Output Enable Register | JJ, HH |
| t_{OEHD} | Data Hold Time for the Output Enable Register | JJ, HH |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | KK, HH |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OERMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERCCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| t_{ICLKQ} | Clock-to-Q of the Input Data Register | AA, EE |
| t_{ISUD} | Data Setup Time for the Input Data Register | CC, AA |
| t_{IHD} | Data Hold Time for the Input Data Register | CC, AA |
| t_{ISUE} | Enable Setup Time for the Input Data Register | BB, AA |
| t_{IHE} | Enable Hold Time for the Input Data Register | BB, AA |
| t_{ICLR2Q} | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IERMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

Note: *See Figure 2-27 on page 2-68 for more information.

1.2 V DC Core Voltage

Table 2-124 • Input Data Register Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | Units |
|---------------------|---|------|-------|
| t_{CLKQ} | Clock-to-Q of the Input Data Register | 0.68 | ns |
| t_{SUD} | Data Setup Time for the Input Data Register | 0.97 | ns |
| t_{IHD} | Data Hold Time for the Input Data Register | 0.00 | ns |
| t_{SUE} | Enable Setup Time for the Input Data Register | 1.02 | ns |
| t_{IHE} | Enable Hold Time for the Input Data Register | 0.00 | ns |
| t_{CLR2Q} | Asynchronous Clear-to-Q of the Input Data Register | 1.19 | ns |
| t_{PRE2Q} | Asynchronous Preset-to-Q of the Input Data Register | 1.19 | ns |
| t_{REMCLR} | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| t_{RECCLR} | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| t_{REMPRE} | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| t_{RECPRE} | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| t_{WCLR} | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| t_{WPRE} | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| t_{CKMPWH} | Clock Minimum Pulse Width HIGH for the Input Data Register | 0.31 | ns |
| t_{CKMPWL} | Clock Minimum Pulse Width LOW for the Input Data Register | 0.28 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Output Register

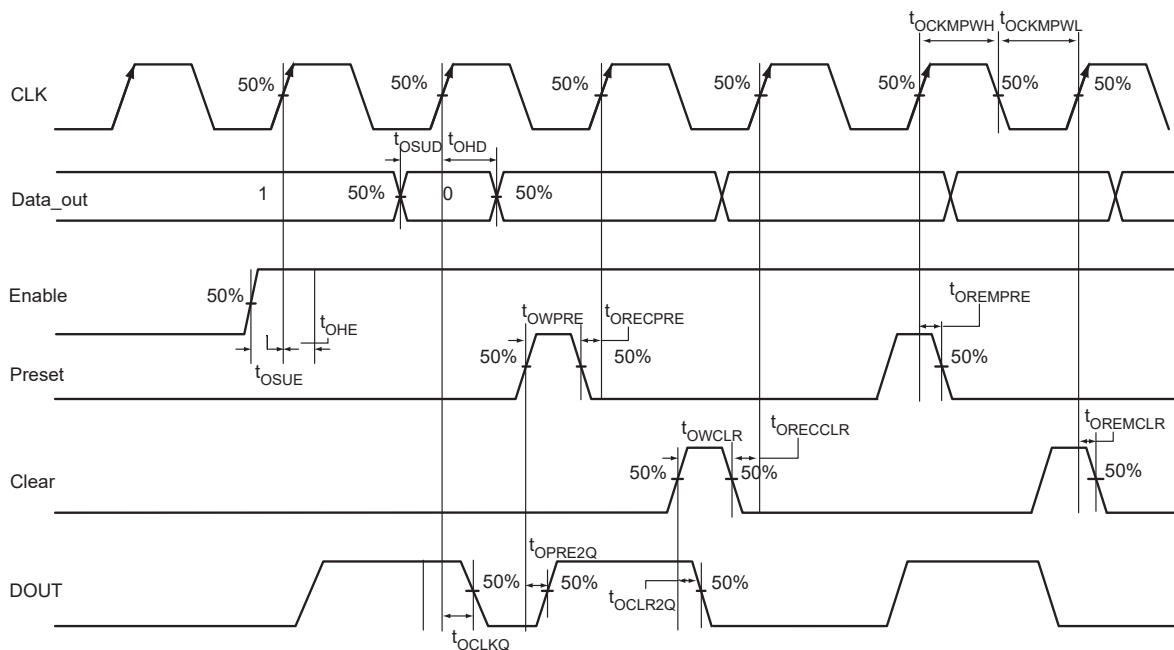


Figure 2-29 • Output Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-125 • Output Data Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | Std. | Units |
|---------------|--|------|-------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | 1.00 | ns |
| t_{OSUD} | Data Setup Time for the Output Data Register | 0.51 | ns |
| t_{OHD} | Data Hold Time for the Output Data Register | 0.00 | ns |
| t_{OSUE} | Enable Setup Time for the Output Data Register | 0.70 | ns |
| t_{OHE} | Enable Hold Time for the Output Data Register | 0.00 | ns |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | 1.34 | ns |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | 1.34 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| t_{OWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| t_{OWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OCLMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Data Register | 0.31 | ns |
| $t_{OCLMPWL}$ | Clock Minimum Pulse Width LOW for the Output Data Register | 0.28 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-126 • Output Data Register Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | Units |
|----------------------|--|------|-------|
| t_{OCLKQ} | Clock-to-Q of the Output Data Register | 1.52 | ns |
| t_{OSUD} | Data Setup Time for the Output Data Register | 1.15 | ns |
| t_{OHD} | Data Hold Time for the Output Data Register | 0.00 | ns |
| t_{OSUE} | Enable Setup Time for the Output Data Register | 1.11 | ns |
| t_{OHE} | Enable Hold Time for the Output Data Register | 0.00 | ns |
| t_{OCLR2Q} | Asynchronous Clear-to-Q of the Output Data Register | 1.96 | ns |
| t_{OPRE2Q} | Asynchronous Preset-to-Q of the Output Data Register | 1.96 | ns |
| t_{OREMCLR} | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| t_{ORECCLR} | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| t_{OREMPRE} | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| t_{ORECPRE} | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| t_{OWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| t_{OWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| t_{OCKMPWH} | Clock Minimum Pulse Width HIGH for the Output Data Register | 0.31 | ns |
| t_{OCKMPWL} | Clock Minimum Pulse Width LOW for the Output Data Register | 0.28 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Output Enable Register

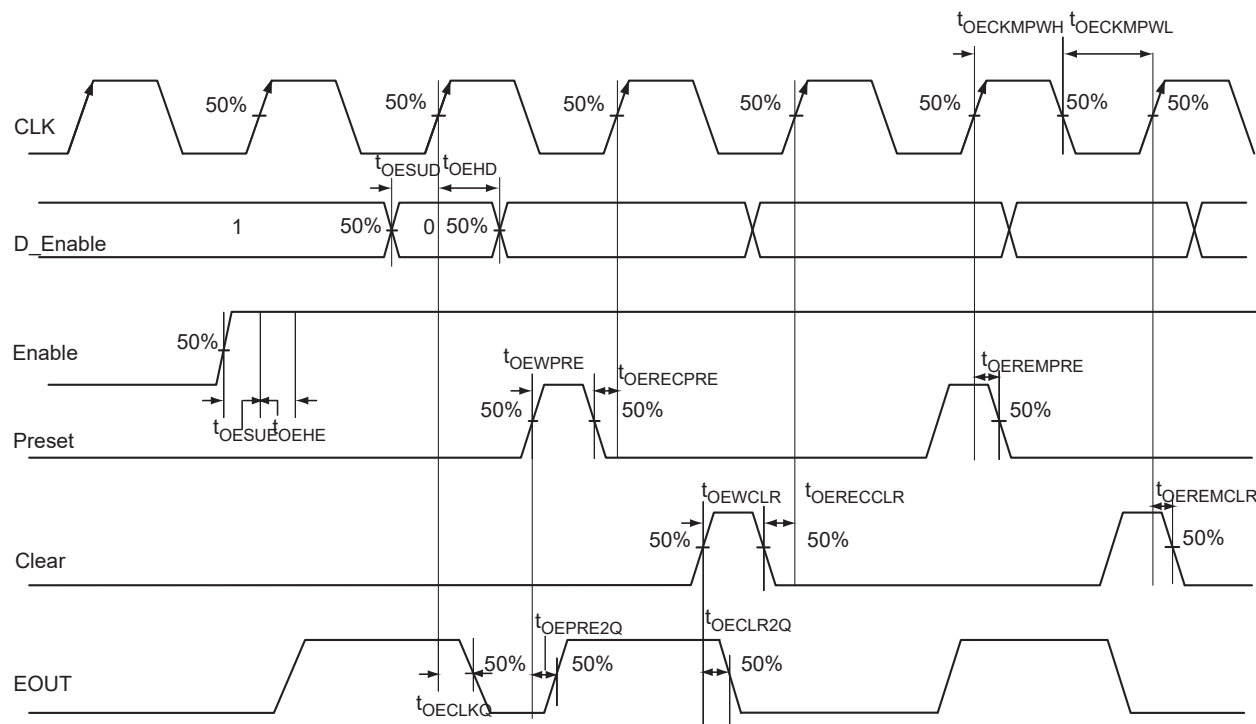


Figure 2-30 • Output Enable Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-127 • Output Enable Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | Std. | Units |
|-----------------|--|------|-------|
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | 0.75 | ns |
| t_{OESUD} | Data Setup Time for the Output Enable Register | 0.51 | ns |
| t_{OEHD} | Data Hold Time for the Output Enable Register | 0.00 | ns |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | 0.73 | ns |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.13 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.13 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRES}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| t_{OEWCLR} | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| t_{OEWPRE} | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Enable Register | 0.28 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-128 • Output Enable Register Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | Units |
|----------------|--|------|-------|
| t_{OECLKQ} | Clock-to-Q of the Output Enable Register | 1.10 | ns |
| t_{OESUD} | Data Setup Time for the Output Enable Register | 1.15 | ns |
| t_{OEHD} | Data Hold Time for the Output Enable Register | 0.00 | ns |
| t_{OESUE} | Enable Setup Time for the Output Enable Register | 1.22 | ns |
| t_{OEHE} | Enable Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRES}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Enable Register | 0.28 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

DDR Module Specifications

Input DDR Module

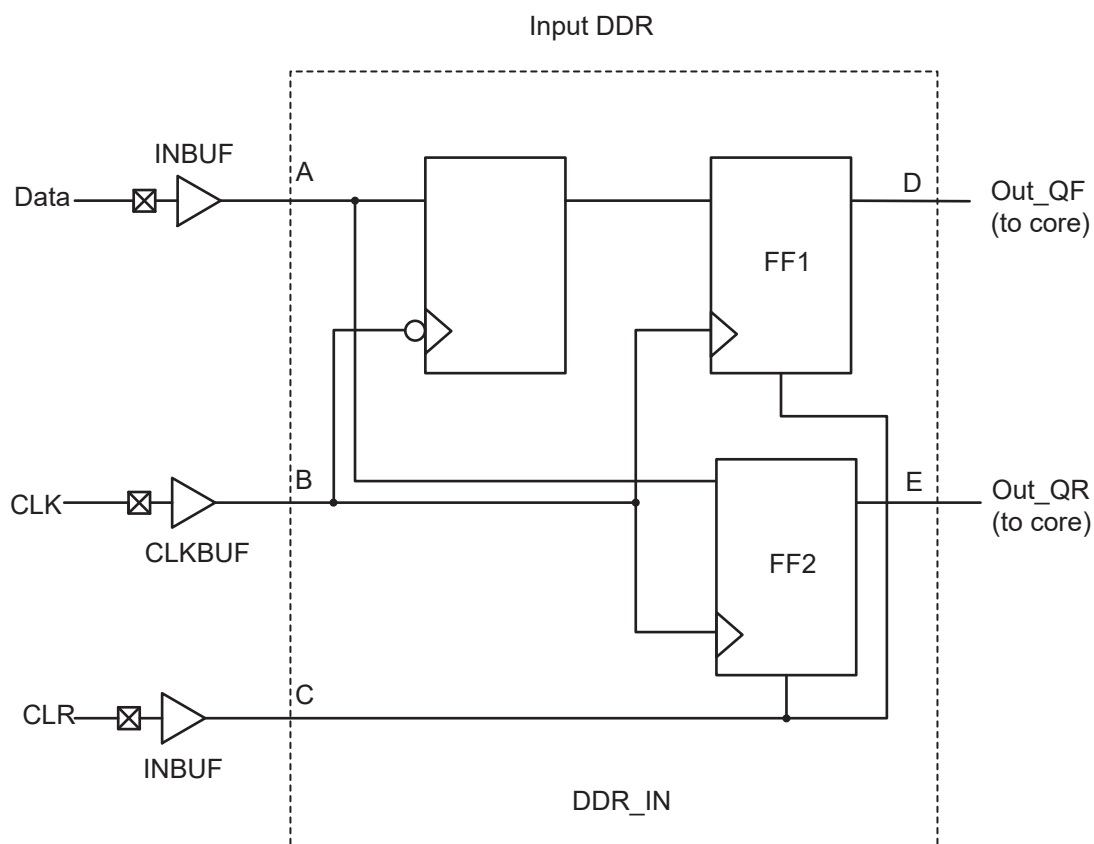


Figure 2-31 • Input DDR Timing Model

Table 2-129 • Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|------------------|------------------------------|----------------------------|
| $t_{DDRICKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| t_{DDRILD} | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

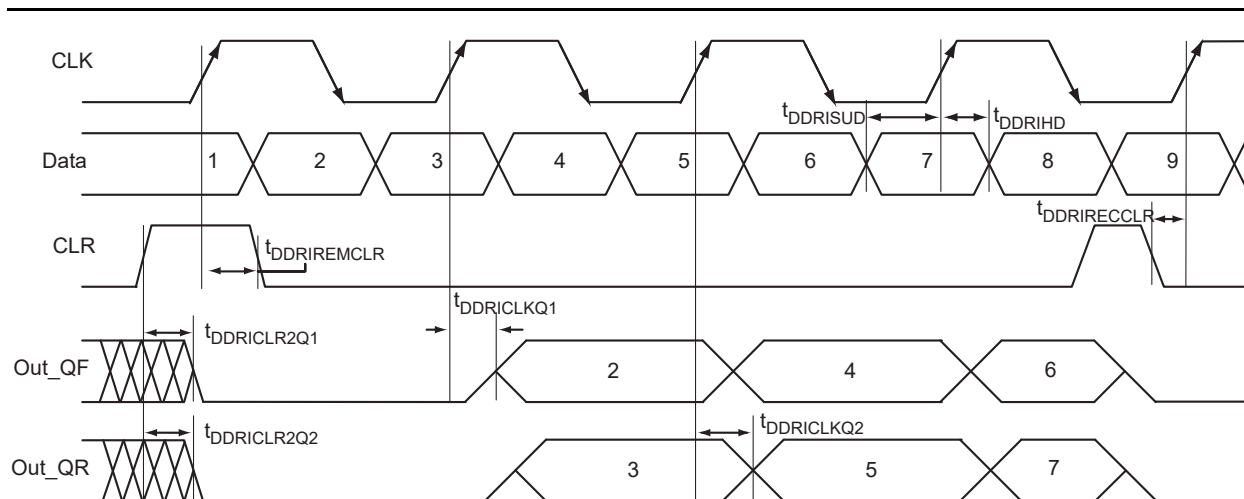


Figure 2-32 • Input DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-130 • Input DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | Std. | Units |
|------------------|--|--------|-------|
| $t_{DDRICKQ1}$ | Clock-to-Out Out_QR for Input DDR | 0.48 | ns |
| $t_{DDRICKQ2}$ | Clock-to-Out Out_QF for Input DDR | 0.65 | ns |
| $t_{DDRISUD1}$ | Data Setup for Input DDR (negedge) | 0.50 | ns |
| $t_{DDRISUD2}$ | Data Setup for Input DDR (posedge) | 0.40 | ns |
| t_{DDRHD1} | Data Hold for Input DDR (negedge) | 0.00 | ns |
| t_{DDRHD2} | Data Hold for Input DDR (posedge) | 0.00 | ns |
| $t_{DDRICLR2Q1}$ | Asynchronous Clear to Out Out_QR for Input DDR | 0.82 | ns |
| $t_{DDRICLR2Q2}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 0.98 | ns |
| $t_{DDRIREMCLR}$ | Asynchronous Clear Removal Time for Input DDR | 0.00 | ns |
| $t_{DDRIRECCLR}$ | Asynchronous Clear Recovery Time for Input DDR | 0.23 | ns |
| $t_{DDRIWCLR}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.19 | ns |
| $t_{DDRICKMPWH}$ | Clock Minimum Pulse Width HIGH for Input DDR | 0.31 | ns |
| $t_{DDRICKMPWL}$ | Clock Minimum Pulse Width LOW for Input DDR | 0.28 | ns |
| $F_{DDRIMAX}$ | Maximum Frequency for Input DDR | 250.00 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-131 • Input DDR Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V

| Parameter | Description | Std. | Units |
|-------------------------|--|--------|-------|
| t_{DDRICKQ1} | Clock-to-Out Out_QR for Input DDR | 0.76 | ns |
| t_{DDRICKQ2} | Clock-to-Out Out_QF for Input DDR | 0.94 | ns |
| t_{DDRISUD1} | Data Setup for Input DDR (negedge) | 0.93 | ns |
| t_{DDRISUD2} | Data Setup for Input DDR (posedge) | 0.84 | ns |
| t_{DDRIHD1} | Data Hold for Input DDR (negedge) | 0.00 | ns |
| t_{DDRIHD2} | Data Hold for Input DDR (posedge) | 0.00 | ns |
| $t_{\text{DDRICLR2Q1}}$ | Asynchronous Clear to Out Out_QR for Input DDR | 1.23 | ns |
| $t_{\text{DDRICLR2Q2}}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 1.42 | ns |
| $t_{\text{DDRIREMCLR}}$ | Asynchronous Clear Removal Time for Input DDR | 0.00 | ns |
| $t_{\text{DDRIRECCLR}}$ | Asynchronous Clear Recovery Time for Input DDR | 0.24 | ns |
| t_{DDRIWCLR} | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.19 | ns |
| $t_{\text{DDRICKMPWH}}$ | Clock Minimum Pulse Width HIGH for Input DDR | 0.31 | ns |
| $t_{\text{DDRICKMPWL}}$ | Clock Minimum Pulse Width LOW for Input DDR | 0.28 | ns |
| F_{DDRIMAX} | Maximum Frequency for Input DDR | 160.00 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Output DDR Module

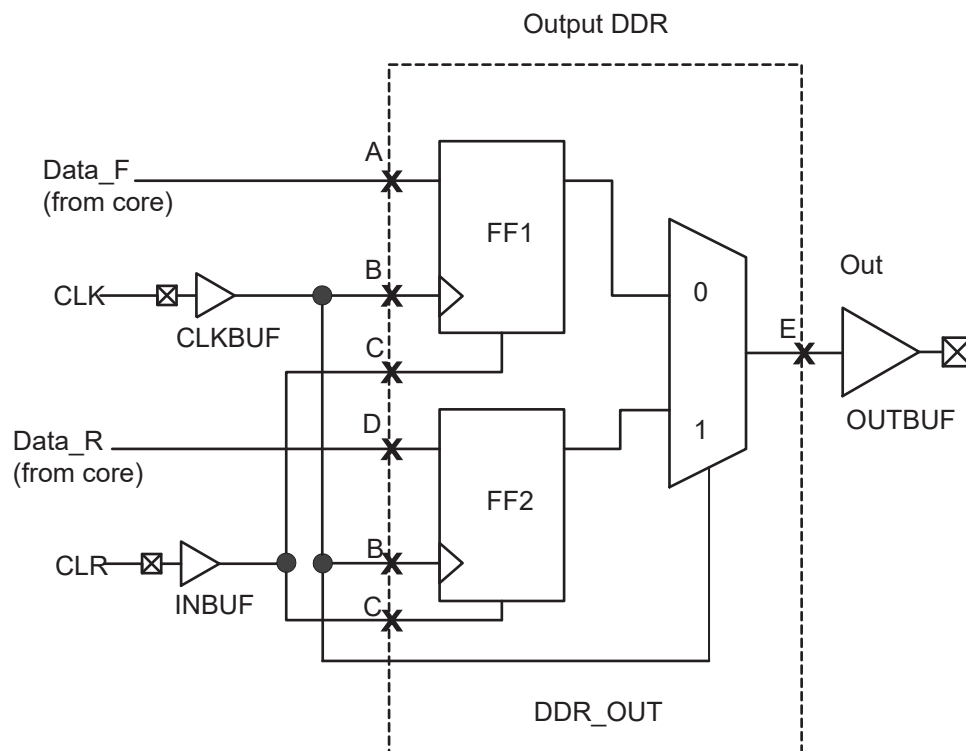


Figure 2-33 • Output DDR Timing Model

Table 2-132 • Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|------------------|---------------------------|----------------------------|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

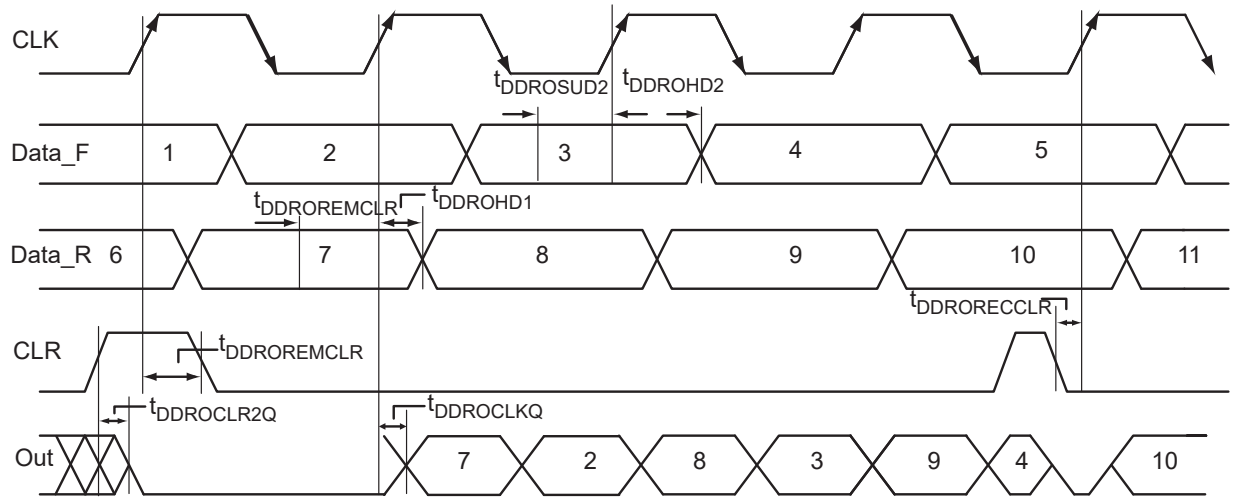


Figure 2-34 • Output DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-133 • Output DDR Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

| Parameter | Description | Std. | Units |
|-------------------------|---|--------|-------|
| t_{DDROCLKQ} | Clock-to-Out of DDR for Output DDR | 1.07 | ns |
| t_{DDROSUD1} | Data_F Data Setup for Output DDR | 0.67 | ns |
| t_{DDROSUD2} | Data_R Data Setup for Output DDR | 0.67 | ns |
| t_{DDROHD1} | Data_F Data Hold for Output DDR | 0.00 | ns |
| t_{DDROHD2} | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{\text{DDROCLR2Q}}$ | Asynchronous Clear-to-Out for Output DDR | 1.38 | ns |
| $t_{\text{DDROREMCLR}}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{\text{DDRORECCLR}}$ | Asynchronous Clear Recovery Time for Output DDR | 0.23 | ns |
| $t_{\text{DDROWCLR1}}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{\text{DDROCKMPWH}}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{\text{DDROCKMPWL}}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| F_{DDOMAX} | Maximum Frequency for the Output DDR | 250.00 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-134 • Output DDR Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V

| Parameter | Description | Std. | Units |
|-------------------------|---|--------|-------|
| t_{DDROCLKQ} | Clock-to-Out of DDR for Output DDR | 1.60 | ns |
| t_{DDROSUD1} | Data_F Data Setup for Output DDR | 1.09 | ns |
| t_{DDROSUD2} | Data_R Data Setup for Output DDR | 1.16 | ns |
| t_{DDROHD1} | Data_F Data Hold for Output DDR | 0.00 | ns |
| t_{DDROHD2} | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{\text{DDROCLR2Q}}$ | Asynchronous Clear-to-Out for Output DDR | 1.99 | ns |
| $t_{\text{DDROREMCLR}}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{\text{DDRORECCLR}}$ | Asynchronous Clear Recovery Time for Output DDR | 0.24 | ns |
| $t_{\text{DDROWCLR1}}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{\text{DDROCKMPWH}}$ | Clock Minimum Pulse Width HIGH for the Output DDR | 0.31 | ns |
| $t_{\text{DDROCKMPWL}}$ | Clock Minimum Pulse Width LOW for the Output DDR | 0.28 | ns |
| F_{DDOMAX} | Maximum Frequency for the Output DDR | 160.00 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOOe library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

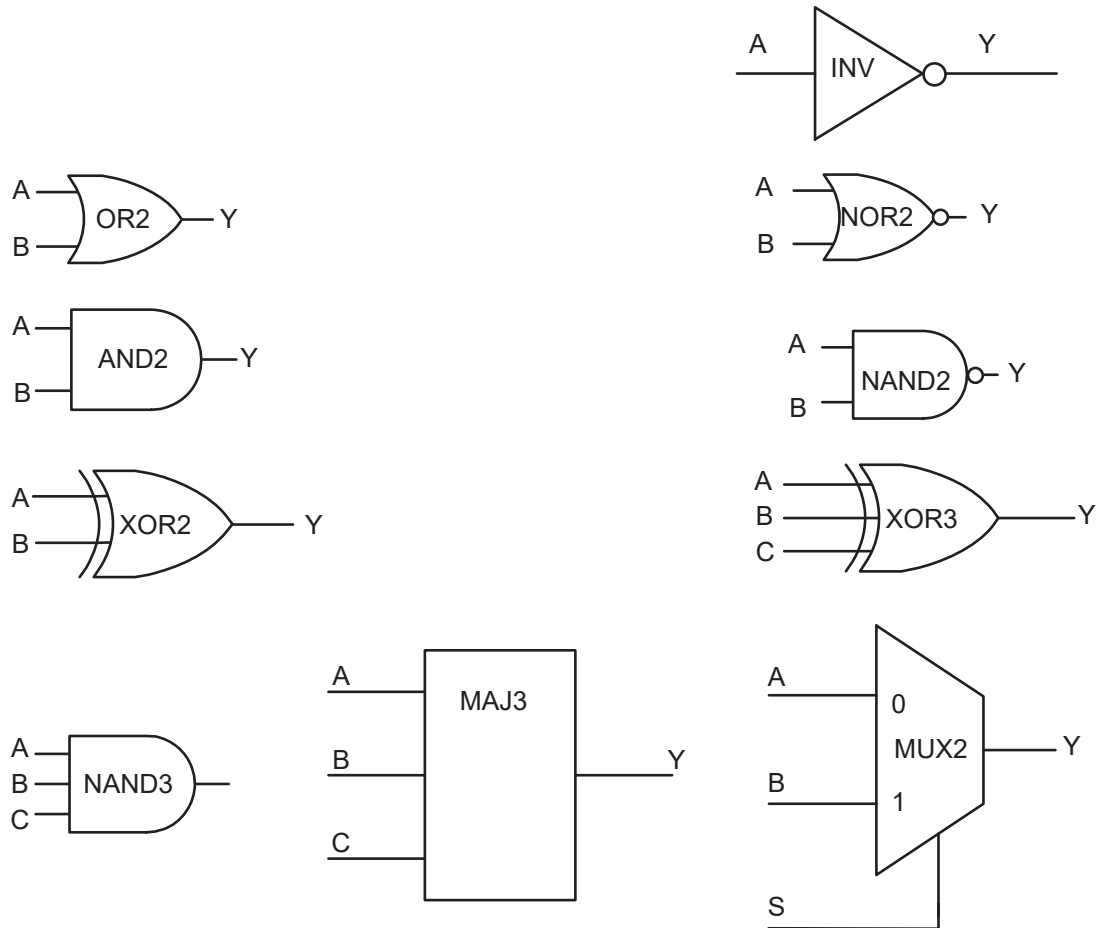


Figure 2-35 • Sample of Combinatorial Cells

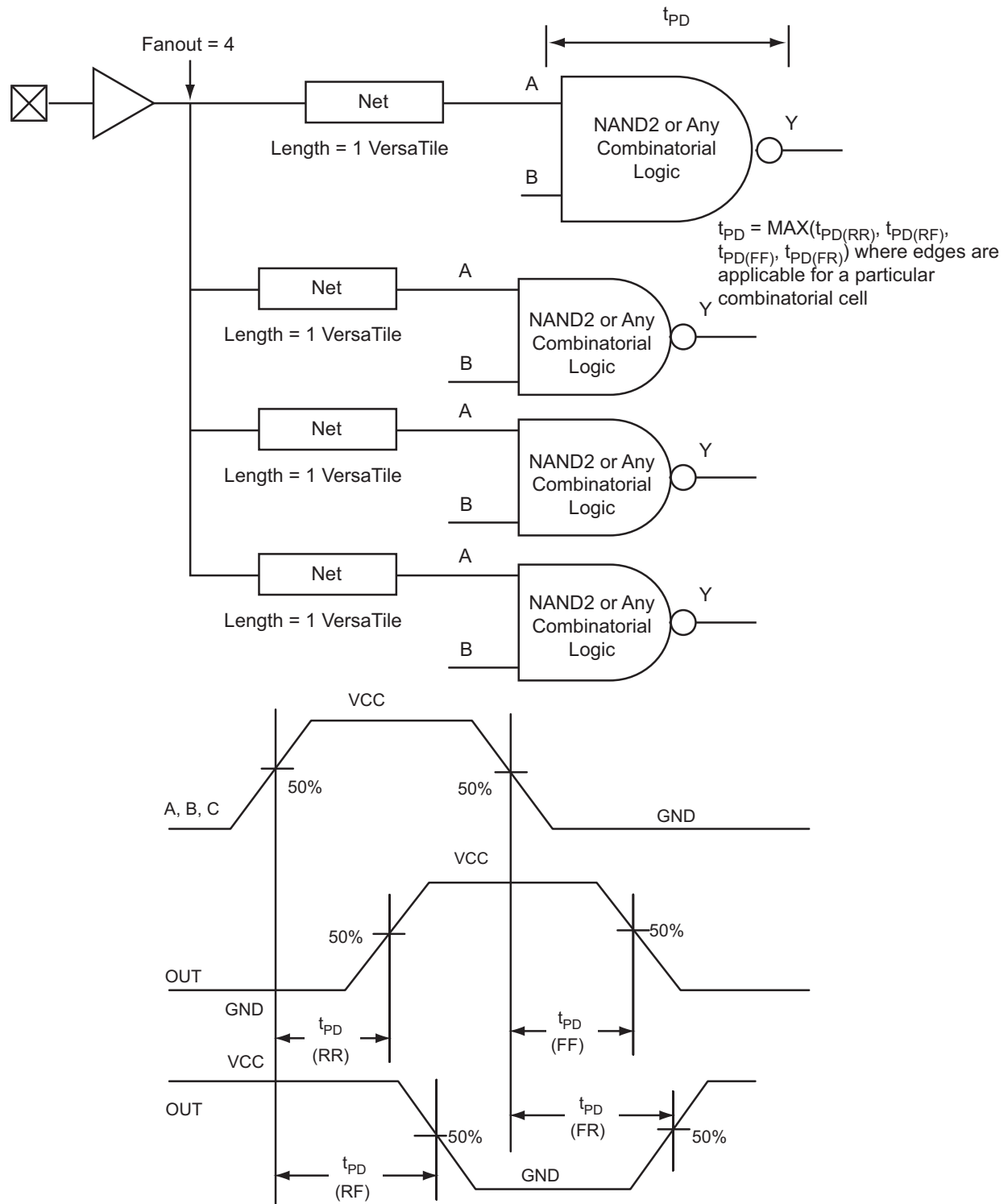


Figure 2-36 • Timing Model and Waveforms

Timing Characteristics

1.5 V DC Core Voltage

Table 2-135 • Combinatorial Cell Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|--------------------|---------------------------|-----------|------|-------|
| INV | $Y = !A$ | t_{PD} | 0.80 | ns |
| AND2 | $Y = A \cdot B$ | t_{PD} | 0.84 | ns |
| NAND2 | $Y = !(A \cdot B)$ | t_{PD} | 0.90 | ns |
| OR2 | $Y = A + B$ | t_{PD} | 1.19 | ns |
| NOR2 | $Y = !(A + B)$ | t_{PD} | 1.10 | ns |
| XOR2 | $Y = A \oplus B$ | t_{PD} | 1.37 | ns |
| MAJ3 | $Y = \text{MAJ}(A, B, C)$ | t_{PD} | 1.33 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | t_{PD} | 1.79 | ns |
| MUX2 | $Y = A !S + B S$ | t_{PD} | 1.48 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | t_{PD} | 1.21 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-136 • Combinatorial Cell Propagation Delays
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|--------------------|---------------------------|-----------|------|-------|
| INV | $Y = !A$ | t_{PD} | 1.35 | ns |
| AND2 | $Y = A \cdot B$ | t_{PD} | 1.42 | ns |
| NAND2 | $Y = !(A \cdot B)$ | t_{PD} | 1.58 | ns |
| OR2 | $Y = A + B$ | t_{PD} | 2.10 | ns |
| NOR2 | $Y = !(A + B)$ | t_{PD} | 1.94 | ns |
| XOR2 | $Y = A \oplus B$ | t_{PD} | 2.33 | ns |
| MAJ3 | $Y = \text{MAJ}(A, B, C)$ | t_{PD} | 2.34 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | t_{PD} | 3.05 | ns |
| MUX2 | $Y = A !S + B S$ | t_{PD} | 2.64 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | t_{PD} | 2.10 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

VersaTile Specifications as a Sequential Module

The IGLOOe library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

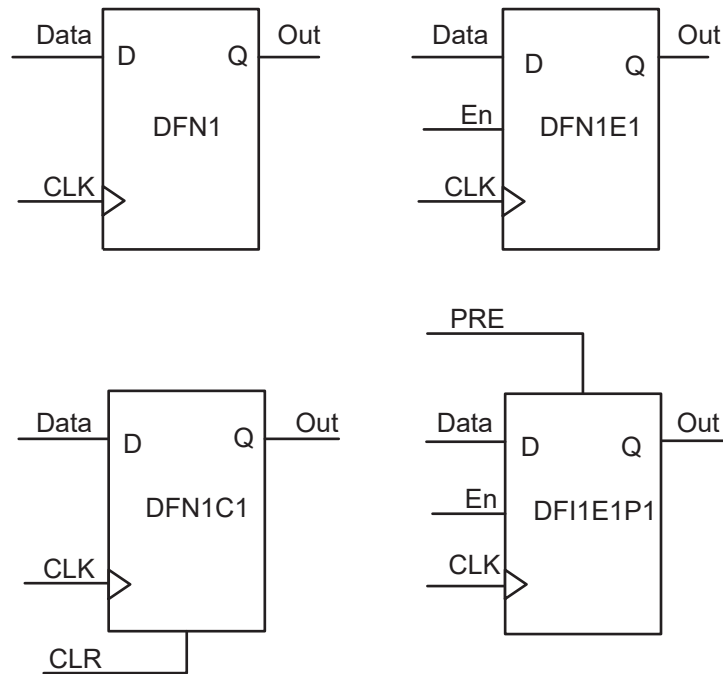


Figure 2-37 • Sample of Sequential Cells

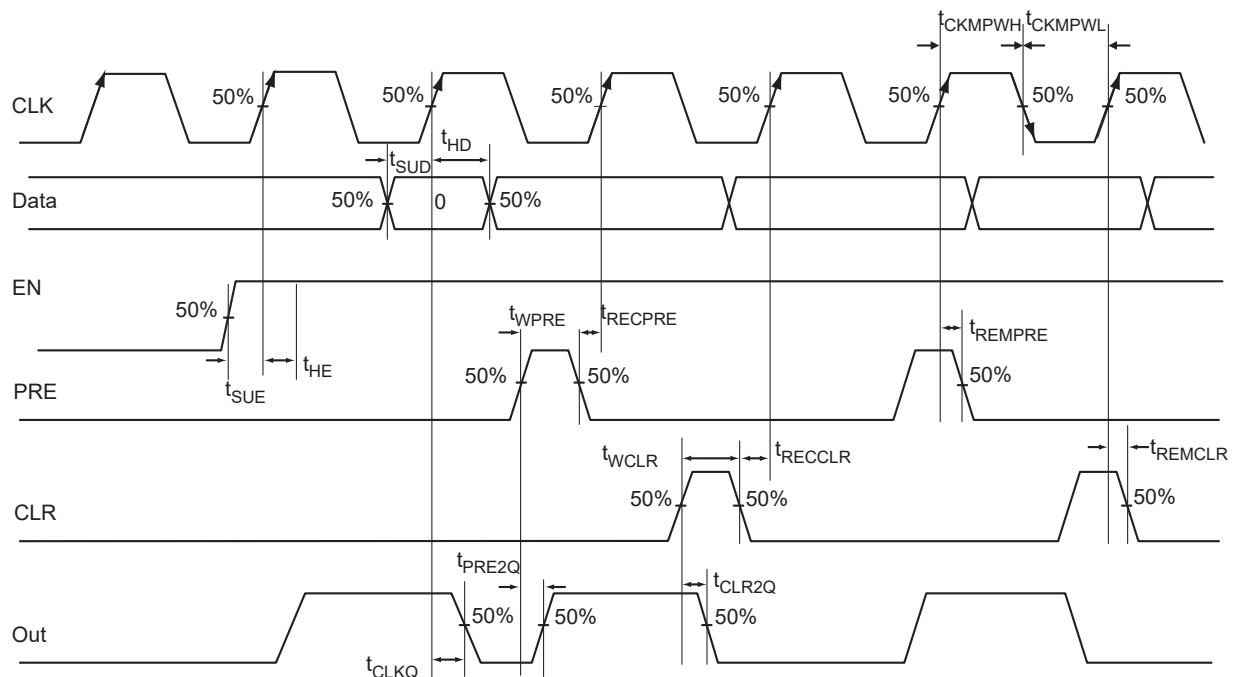


Figure 2-38 • Timing Model and Waveforms

Timing Characteristics

1.5 V DC Core Voltage

Table 2-137 • Register Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

| Parameter | Description | Std. | Units |
|--------------|---|------|-------|
| t_{CLKQ} | Clock-to-Q of the Core Register | 0.89 | ns |
| t_{SUD} | Data Setup Time for the Core Register | 0.81 | ns |
| t_{HD} | Data Hold Time for the Core Register | 0.00 | ns |
| t_{SUE} | Enable Setup Time for the Core Register | 0.73 | ns |
| t_{HE} | Enable Hold Time for the Core Register | 0.00 | ns |
| t_{CLR2Q} | Asynchronous Clear-to-Q of the Core Register | 0.60 | ns |
| t_{PRE2Q} | Asynchronous Preset-to-Q of the Core Register | 0.62 | ns |
| t_{REMCLR} | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| t_{RECCLR} | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| t_{REMPRE} | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| t_{RECPRE} | Asynchronous Preset Recovery Time for the Core Register | 0.23 | ns |
| t_{WCLR} | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.30 | ns |
| t_{WPRE} | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.30 | ns |
| t_{CKMPWH} | Clock Minimum Pulse Width HIGH for the Core Register | 0.56 | ns |
| t_{CKMPWL} | Clock Minimum Pulse Width LOW for the Core Register | 0.56 | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-138 • Register Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | Units |
|---------------------|---|------|-------|
| t_{CLKQ} | Clock-to-Q of the Core Register | 1.61 | ns |
| t_{SUD} | Data Setup Time for the Core Register | 1.17 | ns |
| t_{HD} | Data Hold Time for the Core Register | 0.00 | ns |
| t_{SUE} | Enable Setup Time for the Core Register | 1.29 | ns |
| t_{HE} | Enable Hold Time for the Core Register | 0.00 | ns |
| t_{CLR2Q} | Asynchronous Clear-to-Q of the Core Register | 0.87 | ns |
| t_{PRE2Q} | Asynchronous Preset-to-Q of the Core Register | 0.89 | ns |
| t_{REMCLR} | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| t_{RECLR} | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| t_{REMPRE} | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| t_{RECPRE} | Asynchronous Preset Recovery Time for the Core Register | 0.24 | ns |
| t_{WCLR} | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.46 | ns |
| t_{WPRE} | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.46 | ns |
| t_{CKMPWH} | Clock Minimum Pulse Width HIGH for the Core Register | 0.95 | ns |
| t_{CKMPWL} | Clock Minimum Pulse Width LOW for the Core Register | 0.95 | ns |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Global Resource Characteristics

AGLE600 Clock Tree Topology

Clock delays are device-specific. Figure 2-39 is an example of a global tree used for clock routing. The global tree presented in Figure 2-39 is driven by a CCC located on the west side of the AGL600 device. It is used to drive all D-flip-flops in the device.

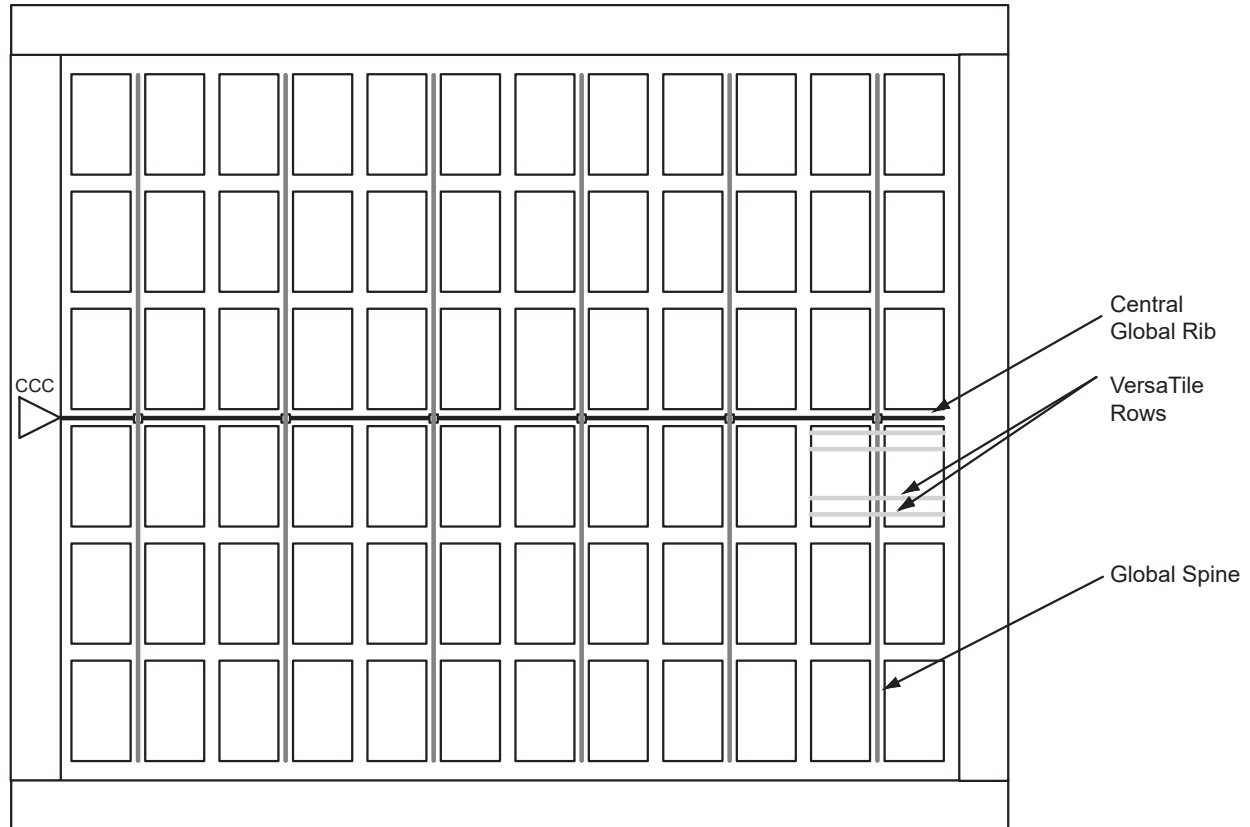


Figure 2-39 • Example of Global Tree Use in an AGL600 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-91. Table 2-139 and Table 2-141 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-139 • AGLE600 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | Std. | | Units |
|---------------|---|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 1.48 | 1.82 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 1.52 | 1.94 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.42 | ns |

Notes:

- Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-140 • AGLE3000 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | Std. | | Units |
|---------------|---|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 2.00 | 2.34 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 2.09 | 2.51 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.42 | ns |

Notes:

- Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-141 • AGLE600 Global Resource
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | | Units |
|---------------|---|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 2.22 | 2.67 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 2.32 | 2.93 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | 1.65 | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.61 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-142 • AGLE3000 Global Resource
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | | Units |
|---------------|---|-------------------|-------------------|-------|
| | | Min. ¹ | Max. ² | |
| t_{RCKL} | Input Low Delay for Global Clock | 2.83 | 3.27 | ns |
| t_{RCKH} | Input High Delay for Global Clock | 3.00 | 3.61 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width HIGH for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width LOW for Global Clock | 1.65 | | ns |
| t_{RCKSW} | Maximum Skew for Global Clock | | 0.61 | ns |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-143 • IGLOOe CCC/PLL Specification
For IGLOOe V2 or V5 Devices, 1.5 V DC Core Supply Voltage

| Parameter | Min. | Typ. | Max. | Units |
|--|--------------------------------|------------------|------------------------|-------|
| Clock Conditioning Circuitry Input Frequency f_{IN_CCC} | 1.5 | | 250 | MHz |
| Clock Conditioning Circuitry Output Frequency f_{OUT_CCC} | 0.75 | | 250 | MHz |
| Serial Clock (SCLK) for Dynamic PLL ¹ | | | 100 | MHz |
| Delay Increments in Programmable Delay Blocks ^{2, 3} | | 360 ⁴ | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | ns |
| Input Cycle-to-Cycle Jitter (peak magnitude) | | | 1 | |
| CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} | Max Peak-to-Peak Period Jitter | | | |
| | 1 Global Network Used | External FB Used | 3 Global Networks Used | |
| 0.75 MHz to 24 MHz | 0.50% | 0.75% | 0.70% | |
| 24 MHz to 100 MHz | 1.00% | 1.50% | 1.20% | |
| 100 MHz to 250 MHz | 2.50% | 3.75% | 2.75% | |
| Acquisition Time | | | | |
| | LockControl = 0 | | 300 | μs |
| | LockControl = 1 | | 6.0 | ms |
| Tracking Jitter ⁵ | | | | |
| | LockControl = 0 | | 2.5 | ns |
| | LockControl = 1 | | 1.5 | ns |
| Output Duty Cycle | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay 1 ^{2, 3, 6} | 1.25 | | 15.65 | ns |
| Delay Range in Block: Programmable Delay 2 ^{2, 3, 6} | 0.469 | | 15.65 | ns |
| Delay Range in Block: Fixed Delay ^{2, 3} | | 3.5 | | ns |

Notes:

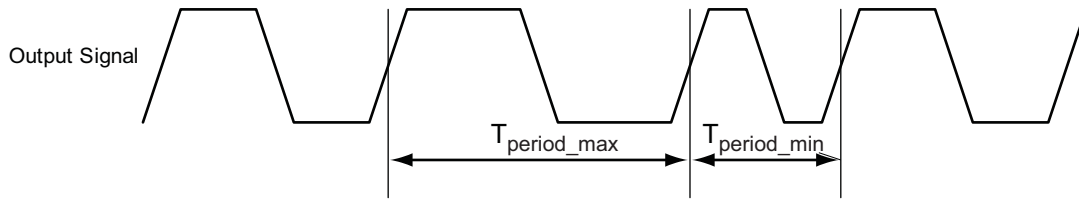
1. Maximum value obtained for a Std. speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
2. This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.
3. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
4. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
6. For definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the IGLOOe FPGA Fabric User's Guide.

Table 2-144 • IGLOOe CCC/PLL Specification
For IGLOOe V2 Devices, 1.2 V DC Core Supply Voltage

| Parameter | Min. | Typ. | Max. | Units |
|---|--------------------------------|------------------|------------------------|-------|
| Clock Conditioning Circuitry Input Frequency f_{IN_CCC} | 1.5 | | 160 | MHz |
| Clock Conditioning Circuitry Output Frequency f_{OUT_CCC} | 0.75 | | 160 | MHz |
| Serial Clock (SCLK) for Dynamic PLL ¹ | | | 60 | MHz |
| Delay Increments in Programmable Delay Blocks ^{2, 3} | | 580 ⁴ | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | |
| Input Cycle-to-Cycle Jitter (peak magnitude) | | | 0.25 | ns |
| CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} ⁵ | Max Peak-to-Peak Period Jitter | | | |
| | 1 Global Network Used | External FB Used | 3 Global Networks Used | |
| 0.75 MHz to 24 MHz | 0.50% | 0.75% | 0.70% | |
| 24 MHz to 100 MHz | 1.00% | 1.50% | 1.20% | |
| 100 MHz to 160 MHz | 2.50% | 3.75% | 2.75% | |
| Acquisition Time | | | | |
| | LockControl = 0 | | 300 | μs |
| LockControl = 1 | | | 6.0 | ms |
| Tracking Jitter ⁶ | | | | |
| | LockControl = 0 | | 4 | ns |
| LockControl = 1 | | | 3 | ns |
| Output Duty Cycle | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay ^{1, 2, 3, 7} | 2.3 | | 20.86 | ns |
| Delay Range in Block: Programmable Delay ^{2, 3, 7} | 0.863 | | 20.86 | ns |
| Delay Range in Block: Fixed Delay ^{2, 3} | | 5.7 | | ns |

Notes:

1. Maximum value obtained for a Std. speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
2. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-6](#) and [Table 2-7 on page 2-6](#) for deratings.
3. $T_j = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
4. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
5. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.
6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.
7. For definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the [IGLOOe FPGA Fabric User's Guide](#).



Note: Peak-to-peak jitter measurements are defined by $T_{\text{peak-to-peak}} = T_{\text{period_max}} - T_{\text{period_min}}$.

Figure 2-40 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics

SRAM

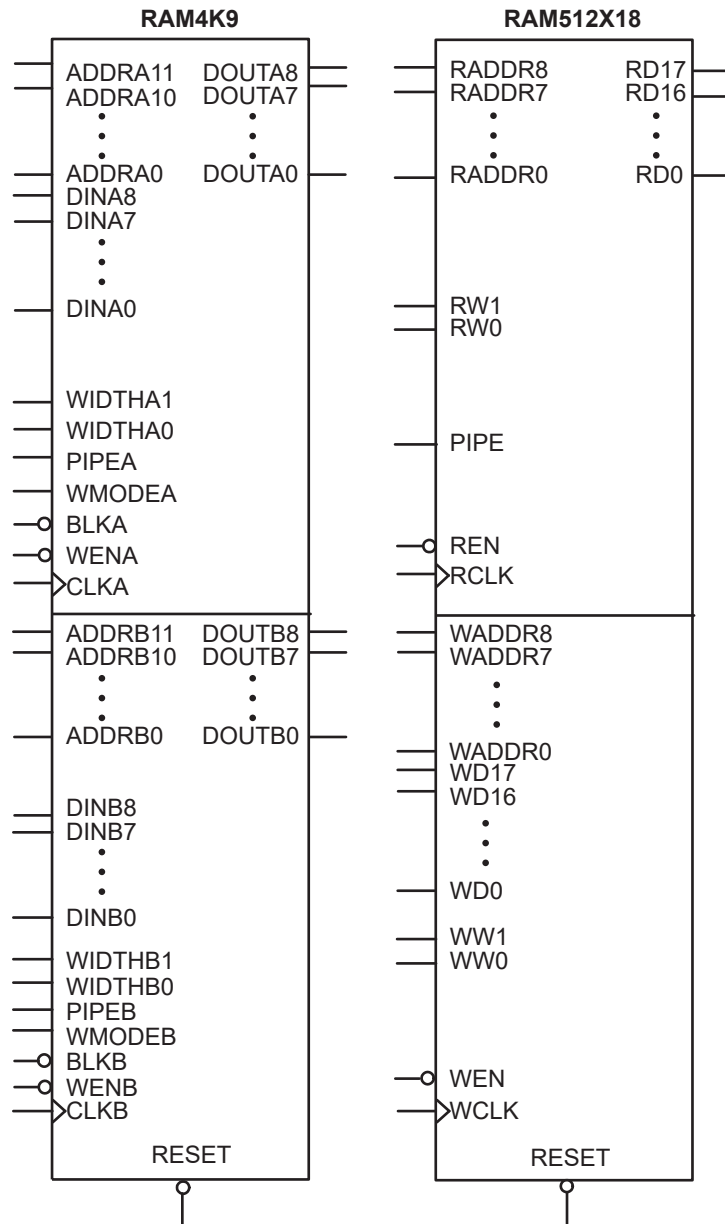


Figure 2-41 • RAM Models

Timing Waveforms

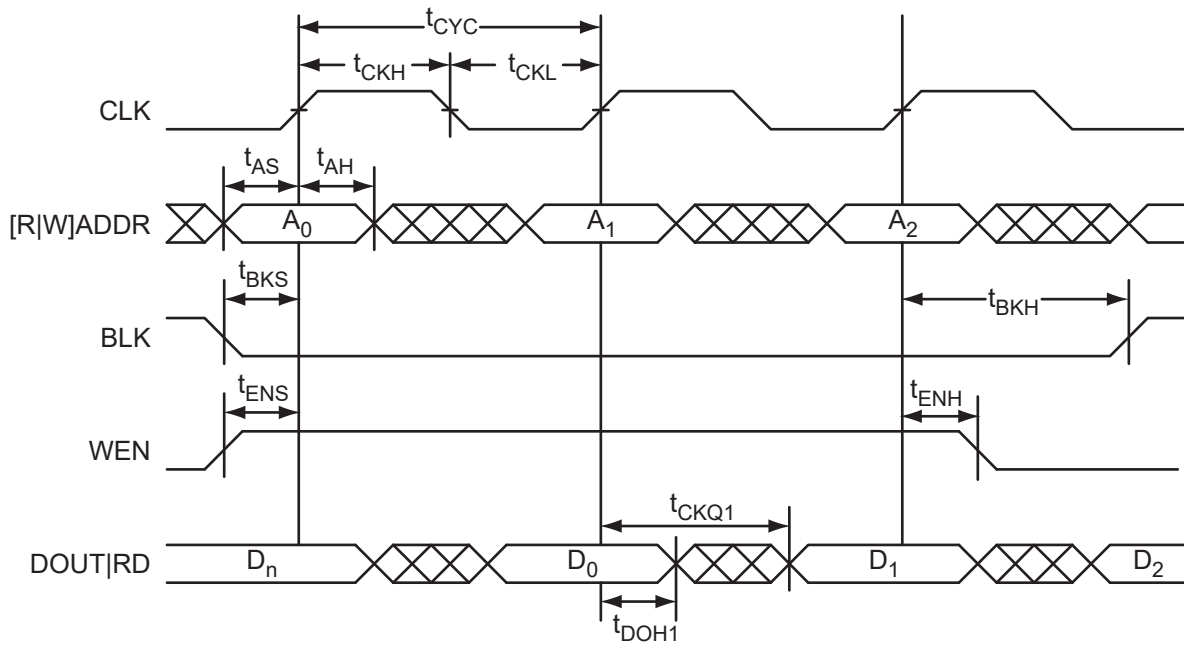


Figure 2-42 • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512X18.

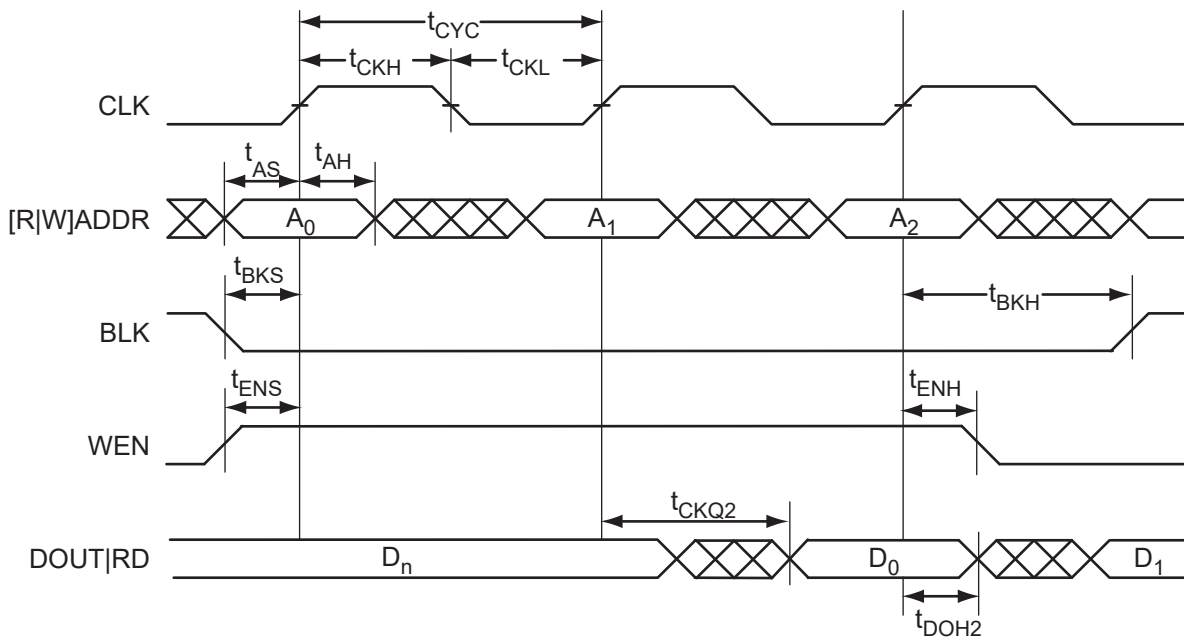


Figure 2-43 • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512X18.

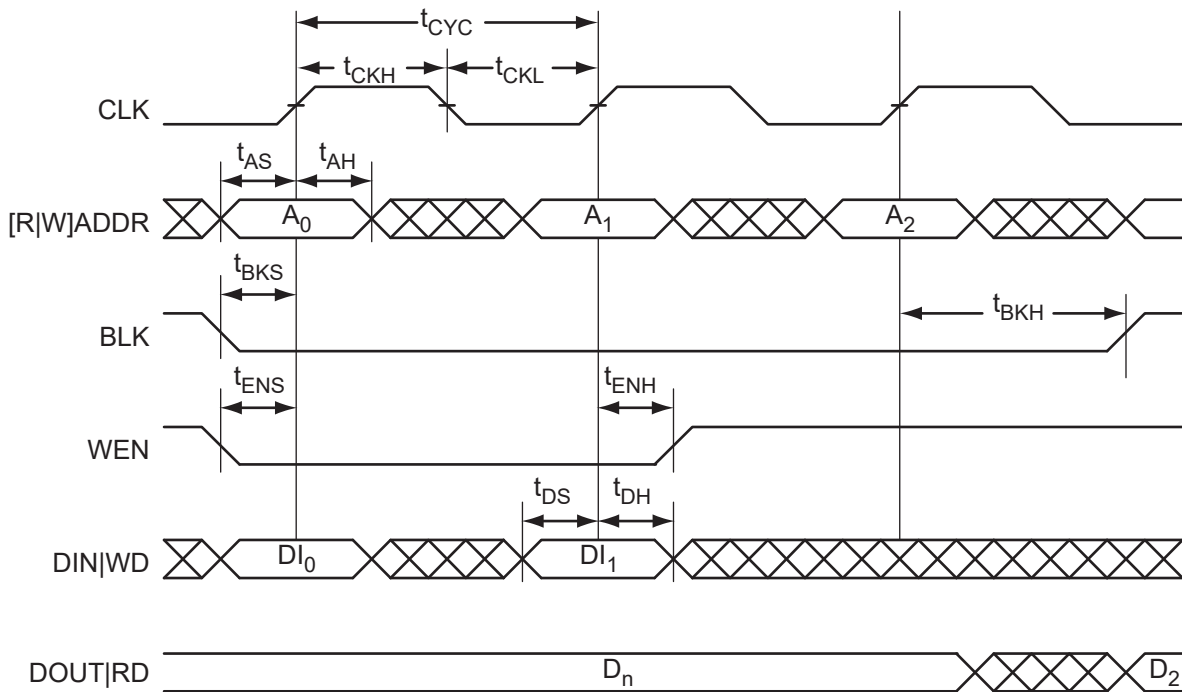


Figure 2-44 • RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512X18.

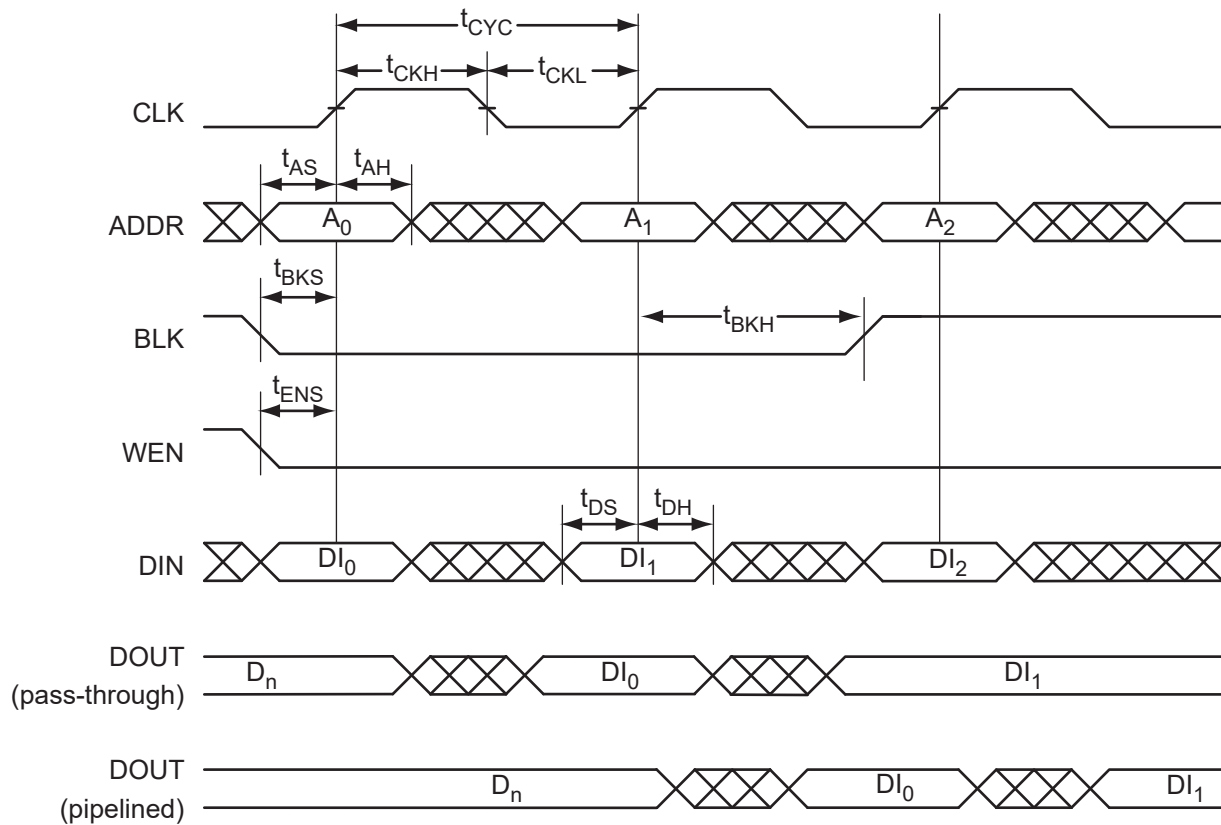


Figure 2-45 • RAM Write, Output as Write Data ($WMODE = 1$). Applicable to RAM4K9 Only.

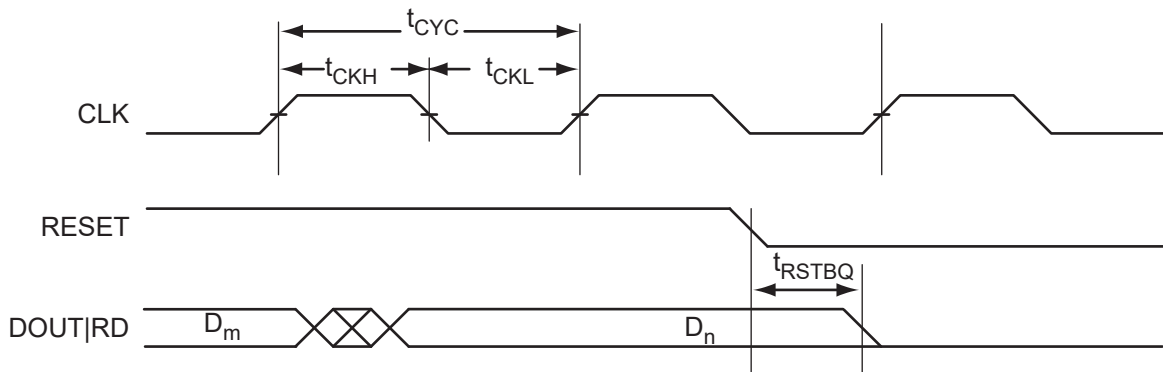


Figure 2-46 • RAM Reset

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-145 • RAM4K9

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

| Parameter | Description | Std. | Units |
|----------------|---|------|-------|
| t_{AS} | Address Setup Time | 0.83 | ns |
| t_{AH} | Address Hold Time | 0.16 | ns |
| t_{ENS} | REN, WEN Setup Time | 0.81 | ns |
| t_{ENH} | REN, WEN Hold Time | 0.16 | ns |
| t_{BKS} | BLK Setup Time | 1.65 | ns |
| t_{BKH} | BLK Hold Time | 0.16 | ns |
| t_{DS} | Input Data (DIN) Setup Time | 0.71 | ns |
| t_{DH} | Input Data (DIN) Hold Time | 0.36 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on DOUT (output retained, WMODE = 0) | 3.53 | ns |
| | Clock HIGH to New Data Valid on DOUT (flow-through, WMODE = 1) | 3.06 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on DOUT (pipelined) | 1.81 | ns |
| t_{C2CWWL}^1 | Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge | 0.23 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.35 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 0.41 | ns |
| | | | |
| t_{RSTBQ} | RESET Low to Data Out Low on DOUT (flow-through) | 2.06 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 2.06 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.68 | ns |
| t_{CYC} | Clock Cycle Time | 6.24 | ns |
| F_{MAX} | Maximum Frequency | 160 | MHz |

Notes:

- For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-146 • RAM512X18**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$**

| Parameter | Description | Std. | Units |
|----------------|---|------|-------|
| t_{AS} | Address Setup Time | 0.83 | ns |
| t_{AH} | Address Hold Time | 0.16 | ns |
| t_{ENS} | REN, WEN Setup Time | 0.73 | ns |
| t_{ENH} | REN, WEN Hold Time | 0.08 | ns |
| t_{DS} | Input Data (WD) Setup Time | 0.71 | ns |
| t_{DH} | Input Data (WD) Hold Time | 0.36 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on RD (output retained, WMODE = 0) | 4.21 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on RD (pipelined) | 1.71 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.35 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 0.42 | ns |
| t_{RSTBQ} | RESET Low to Data Out Low on RD (flow-through) | 2.06 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 2.06 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.68 | ns |
| t_{CYC} | Clock Cycle Time | 6.24 | ns |
| F_{MAX} | Maximum Frequency | 160 | MHz |

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Applies to 1.2 V DC Core Voltage

Table 2-147 • RAM4K9

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | Units |
|----------------|---|-------|-------|
| t_{AS} | Address Setup Time | 1.53 | ns |
| t_{AH} | Address Hold Time | 0.29 | ns |
| t_{ENS} | REN, WEN Setup Time | 1.50 | ns |
| t_{ENH} | REN, WEN Hold Time | 0.29 | ns |
| t_{BKS} | BLK Setup Time | 3.05 | ns |
| t_{BKH} | BLK Hold Time | 0.29 | ns |
| t_{DS} | Input Data (DIN) Setup Time | 1.33 | ns |
| t_{DH} | Input Data (DIN) Hold Time | 0.66 | ns |
| t_{CKQ1} | Clock High to New Data Valid on DOUT (output retained, WMODE = 0) | 6.61 | ns |
| | Clock High to New Data Valid on DOUT (flow-through, WMODE = 1) | 5.72 | ns |
| t_{CKQ2} | Clock High to New Data Valid on DOUT (pipelined) | 3.38 | ns |
| t_{C2CWWL}^1 | Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge | 0.30 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.89 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 1.01 | ns |
| t_{RSTBQ} | RESET Low to Data Out Low on DOUT (pass-through) | 3.86 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 3.86 | ns |
| $t_{REMRSTB}$ | RESET Removal | 1.12 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 5.93 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 1.18 | ns |
| t_{CYC} | Clock Cycle Time | 10.90 | ns |
| F_{MAX} | Maximum Frequency | 92 | MHz |

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-148 • RAM512X18**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$**

| Parameter | Description | Std. | Units |
|----------------|---|-------|-------|
| t_{AS} | Address Setup Time | 1.53 | ns |
| t_{AH} | Address Hold Time | 0.29 | ns |
| t_{ENS} | REN, WEN Setup Time | 1.36 | ns |
| t_{ENH} | REN, WEN Hold Time | 0.15 | ns |
| t_{DS} | Input Data (WD) Setup Time | 1.33 | ns |
| t_{DH} | Input Data (WD) Hold Time | 0.66 | ns |
| t_{CKQ1} | Clock High to New Data Valid on RD (output retained) | 7.88 | ns |
| t_{CKQ2} | Clock High to New Data Valid on RD (pipelined) | 3.20 | ns |
| t_{C2CRWH}^1 | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.87 | ns |
| t_{C2CWRH}^1 | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 1.04 | ns |
| t_{RSTBQ} | RESET Low to Data Out Low on RD (flow-through) | 3.86 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 3.86 | ns |
| $t_{REMRSTB}$ | RESET Removal | 1.12 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 5.93 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 1.18 | ns |
| t_{CYC} | Clock Cycle Time | 10.90 | ns |
| F_{MAX} | Maximum Frequency | 92 | MHz |

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

FIFO

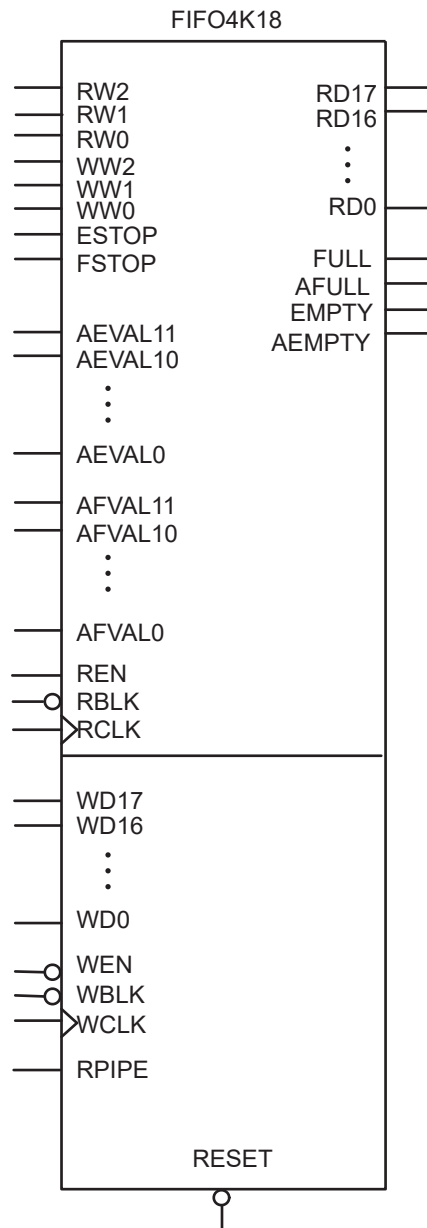


Figure 2-47 • FIFO Model

Timing Waveforms

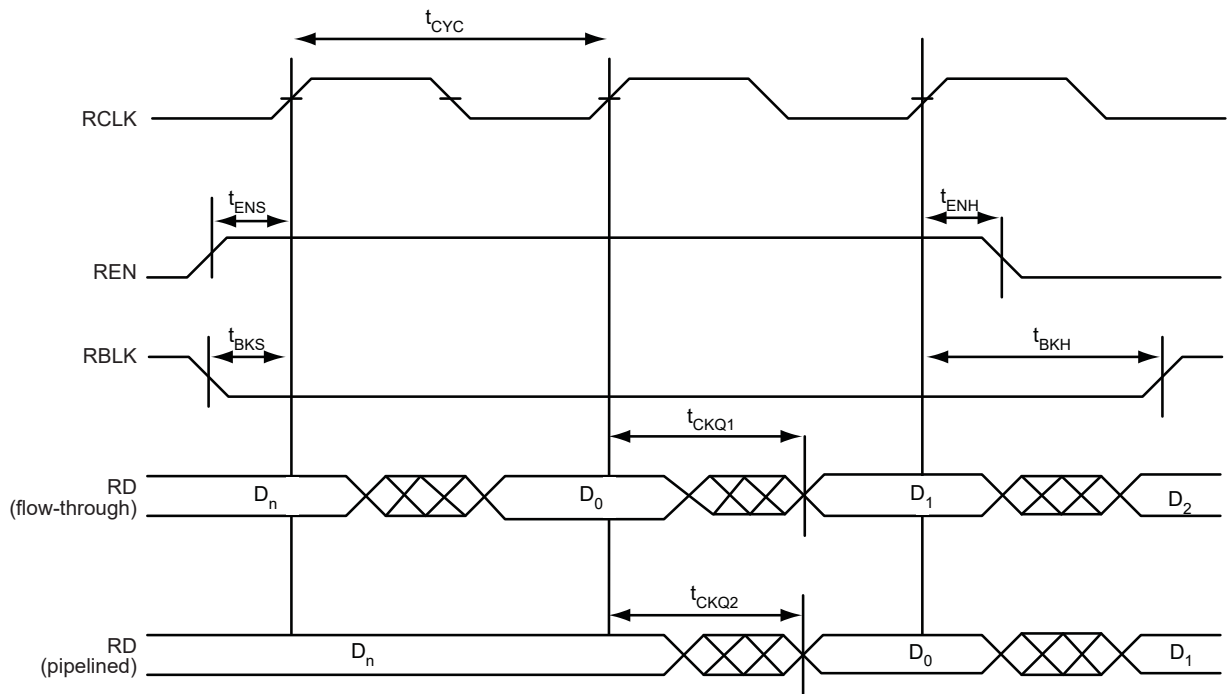


Figure 2-48 • FIFO Read

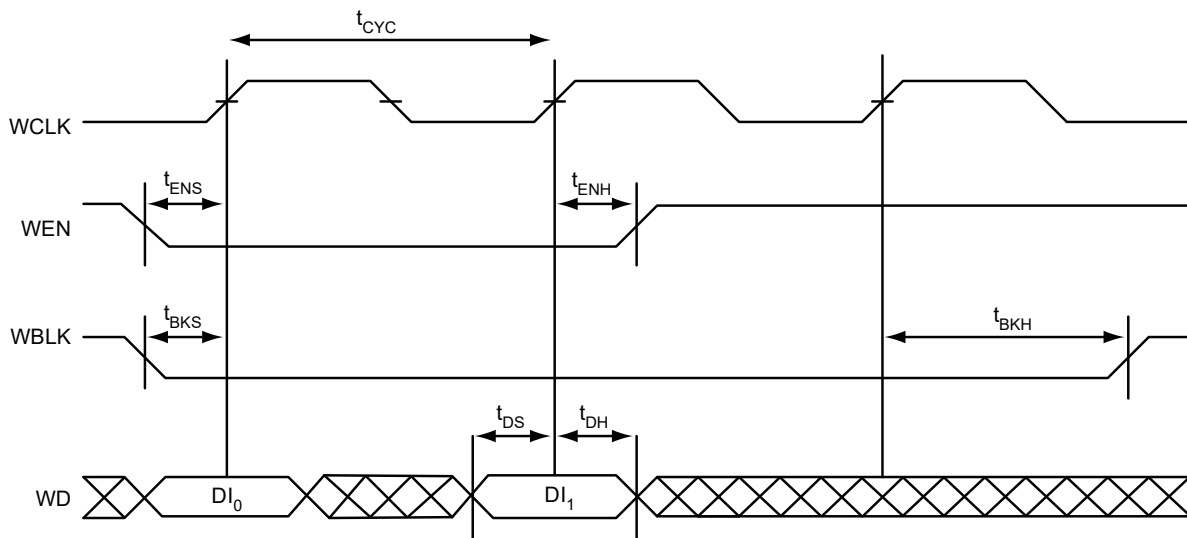


Figure 2-49 • FIFO Write

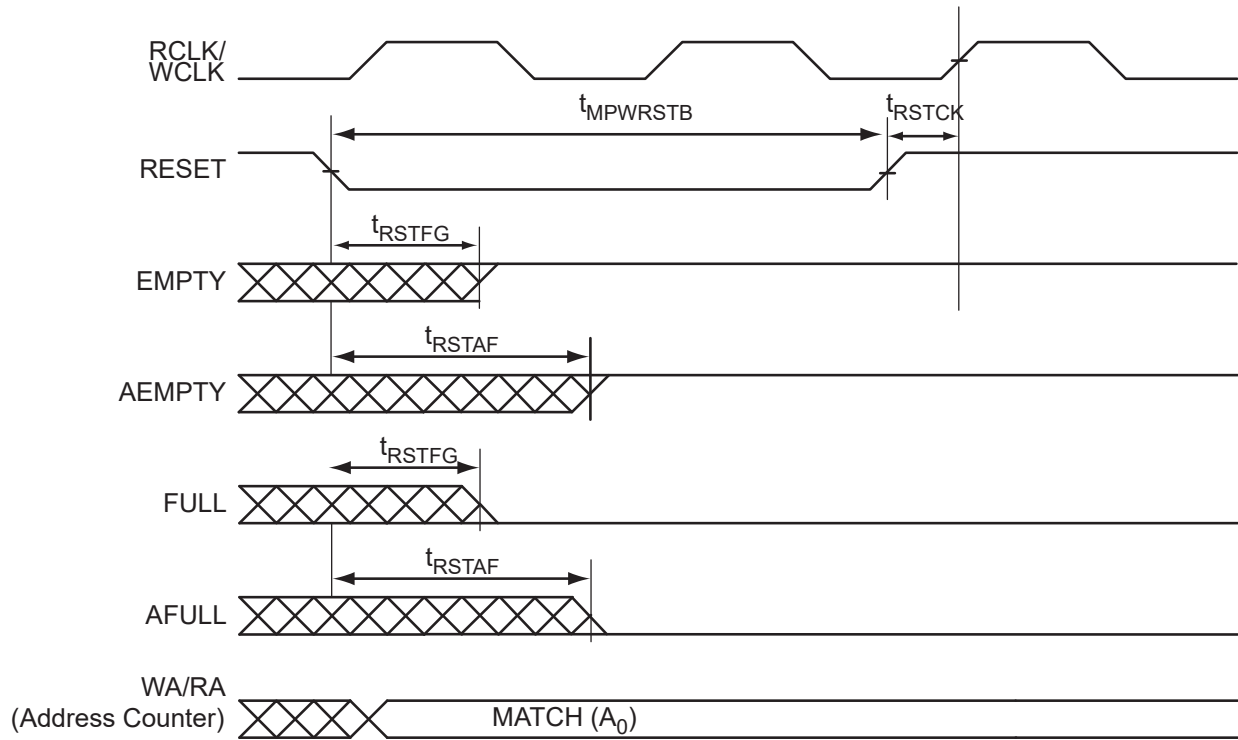


Figure 2-50 • FIFO Reset

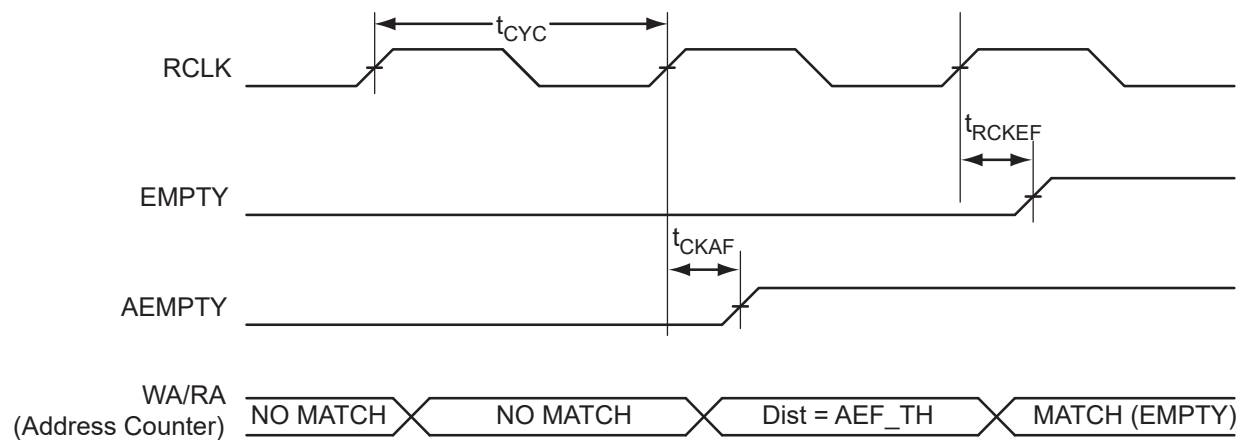


Figure 2-51 • FIFO EMPTY Flag and AEMPTY Flag Assertion

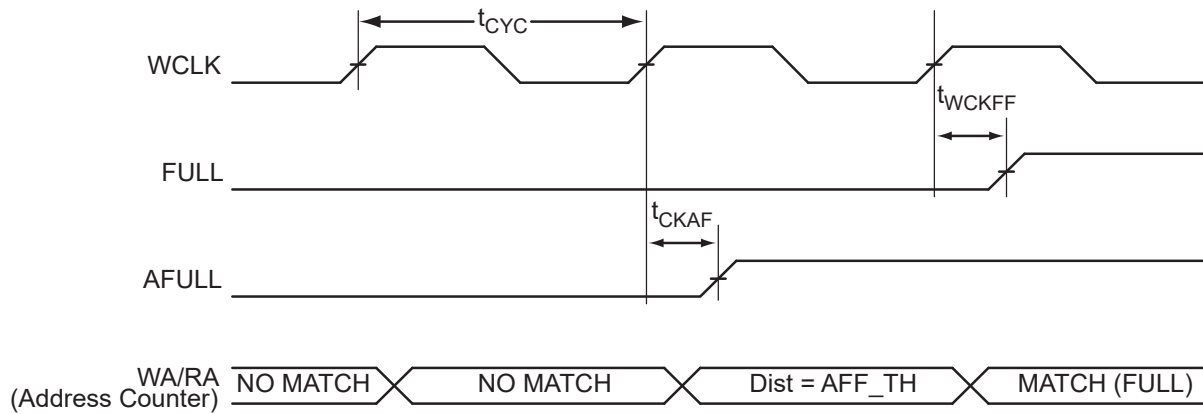


Figure 2-52 • FIFO FULL Flag and AFULL Flag Assertion

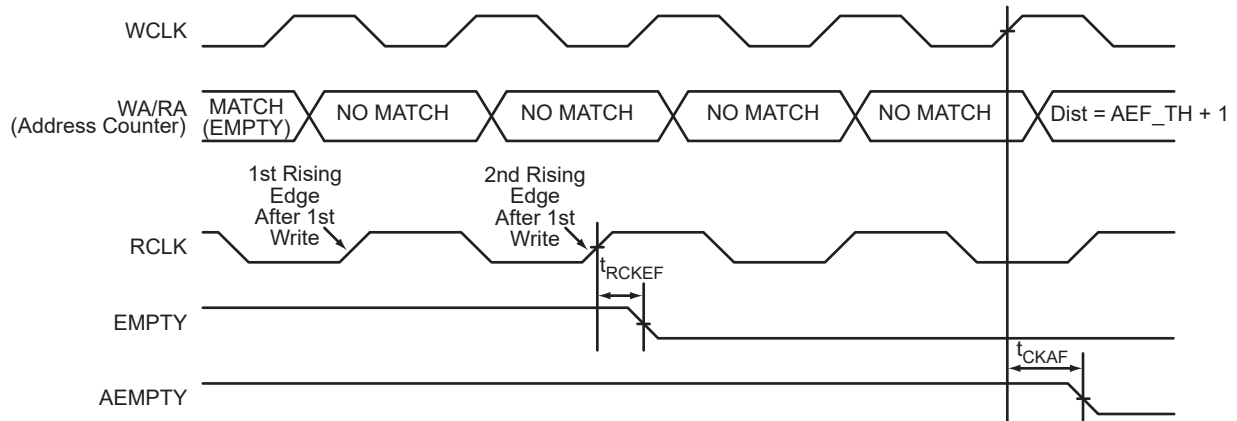


Figure 2-53 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

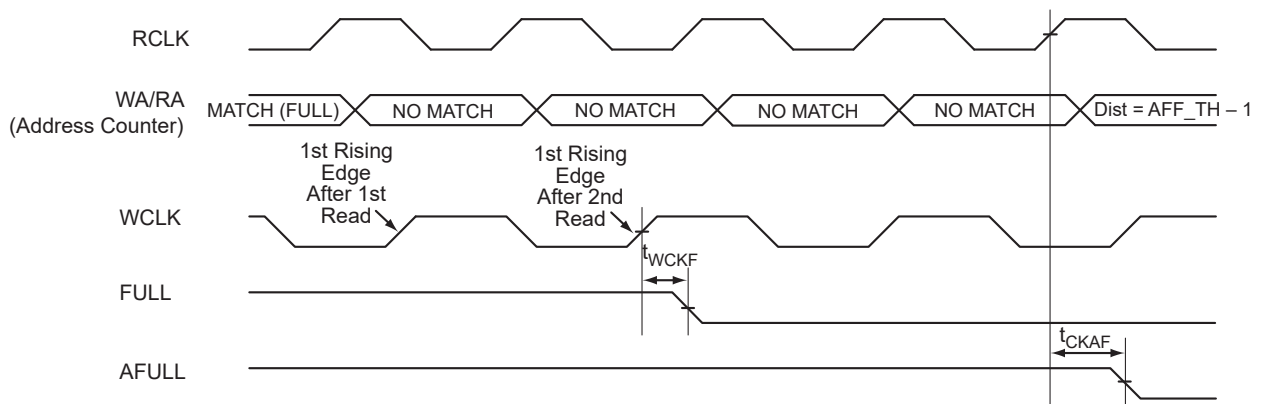


Figure 2-54 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-149 • FIFO

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | Std. | Units |
|---------------|---|-------|-------|
| t_{ENS} | REN, WEN Setup Time | 1.99 | ns |
| t_{ENH} | REN, WEN Hold Time | 0.16 | ns |
| t_{BKS} | BLK Setup Time | 0.30 | ns |
| t_{BKH} | BLK Hold Time | 0.00 | ns |
| t_{DS} | Input Data (WD) Setup Time | 0.76 | ns |
| t_{DH} | Input Data (WD) Hold Time | 0.25 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on RD (pass-through) | 3.33 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on RD (pipelined) | 1.80 | ns |
| t_{RCKEF} | RCLK HIGH to Empty Flag Valid | 3.53 | ns |
| t_{WCKFF} | WCLK HIGH to Full Flag Valid | 3.35 | ns |
| t_{CKAF} | Clock HIGH to Almost Empty/Full Flag Valid | 12.85 | ns |
| t_{RSTFG} | RESET LOW to Empty/Full Flag Valid | 3.48 | ns |
| t_{RSTAF} | RESET LOW to Almost Empty/Full Flag Valid | 12.72 | ns |
| t_{RSTBQ} | RESET LOW to Data Out LOW on RD (pass-through) | 2.02 | ns |
| | RESET LOW to Data Out LOW on RD (pipelined) | 2.02 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.68 | ns |
| t_{CYC} | Clock Cycle Time | 6.24 | ns |
| F_{MAX} | Maximum Frequency | 160 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Applies to 1.2 V DC Core Voltage

Table 2-150 • FIFO

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | Units |
|---------------|---|-------|-------|
| t_{ENS} | REN, WEN Setup Time | 4.13 | ns |
| t_{ENH} | REN, WEN Hold Time | 0.31 | ns |
| t_{BKS} | BLK Setup Time | 0.47 | ns |
| t_{BKH} | BLK Hold Time | 0.00 | ns |
| t_{DS} | Input Data (WD) Setup Time | 1.56 | ns |
| t_{DH} | Input Data (WD) Hold Time | 0.49 | ns |
| t_{CKQ1} | Clock HIGH to New Data Valid on RD (pass-through) | 6.80 | ns |
| t_{CKQ2} | Clock HIGH to New Data Valid on RD (pipelined) | 3.62 | ns |
| t_{RCKEF} | RCLK HIGH to Empty Flag Valid | 7.23 | ns |
| t_{WCKFF} | WCLK HIGH to Full Flag Valid | 6.85 | ns |
| t_{CKAF} | Clock HIGH to Almost Empty/Full Flag Valid | 26.61 | ns |
| t_{RSTFG} | RESET LOW to Empty/Full Flag Valid | 7.12 | ns |
| t_{RSTAF} | RESET LOW to Almost Empty/Full Flag Valid | 26.33 | ns |
| t_{RSTBQ} | RESET LOW to Data Out LOW on RD (pass-through) | 4.09 | ns |
| | RESET LOW to Data Out LOW on RD (pipelined) | 4.09 | ns |
| $t_{REMRSTB}$ | RESET Removal | 1.23 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 6.58 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 1.18 | ns |
| t_{CYC} | Clock Cycle Time | 10.90 | ns |
| F_{MAX} | Maximum Frequency | 92 | MHz |

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Embedded FlashROM Characteristics

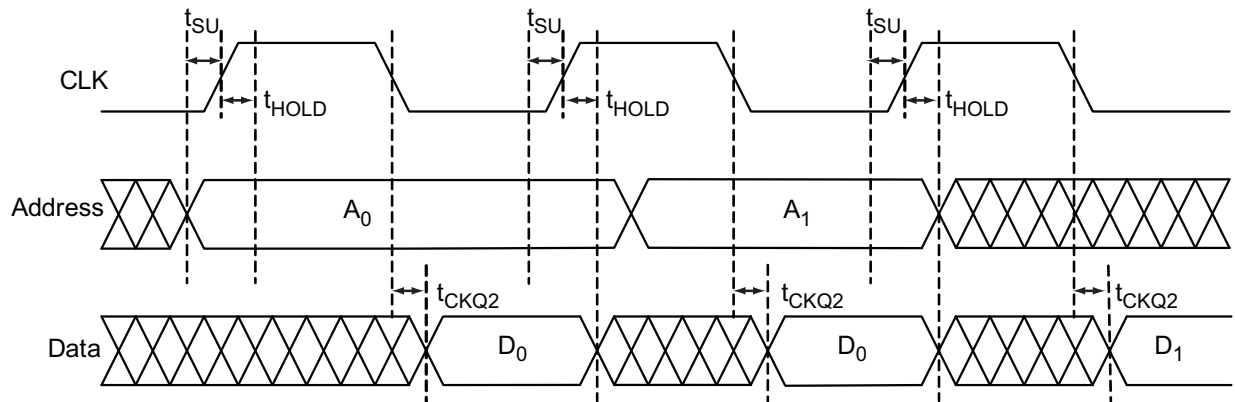


Figure 2-55 • Timing Diagram

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-151 • Embedded FlashROM Access Time

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

| Parameter | Description | Std. | Units |
|-------------------|-------------------------|-------|-------|
| t _{SU} | Address Setup Time | 0.58 | ns |
| t _{HOLD} | Address Hold Time | 0.00 | ns |
| t _{CK2Q} | Clock-to-Out | 34.14 | ns |
| F _{MAX} | Maximum Clock Frequency | 15 | MHz |

Applies to 1.2 V DC Core Voltage

Table 2-152 • Embedded FlashROM Access Time

Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

| Parameter | Description | Std. | Units |
|-------------------|-------------------------|-------|-------|
| t _{SU} | Address Setup Time | 0.59 | ns |
| t _{HOLD} | Address Hold Time | 0.00 | ns |
| t _{CK2Q} | Clock-to-Out | 52.90 | ns |
| F _{MAX} | Maximum Clock Frequency | 10 | MHz |

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-16 for more details.

Timing Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-153 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$

| Parameter | Description | Std. | Units |
|---------------|-----------------------------|-------|-------|
| t_{DISU} | Test Data Input Setup Time | 1.50 | ns |
| t_{DIHD} | Test Data Input Hold Time | 3.00 | ns |
| t_{TMSSU} | Test Mode Select Setup Time | 1.50 | ns |
| t_{TMDHD} | Test Mode Select Hold Time | 3.00 | ns |
| t_{TCK2Q} | Clock to Q (data out) | 11.00 | ns |
| t_{RSTB2Q} | Reset to Q (data out) | 30.00 | ns |
| F_{TCKMAX} | TCK Maximum Frequency | 9.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 1.18 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Applies to 1.5 V DC Core Voltage

Table 2-154 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

| Parameter | Description | Std. | Units |
|---------------|-----------------------------|-------|-------|
| t_{DISU} | Test Data Input Setup Time | 1.00 | ns |
| t_{DIHD} | Test Data Input Hold Time | 2.00 | ns |
| t_{TMSSU} | Test Mode Select Setup Time | 1.00 | ns |
| t_{TMDHD} | Test Mode Select Hold Time | 2.00 | ns |
| t_{TCK2Q} | Clock to Q (data out) | 8.00 | ns |
| t_{RSTB2Q} | Reset to Q (data out) | 25.00 | ns |
| F_{TCKMAX} | TCK Maximum Frequency | 15.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.58 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

3 – Pin Descriptions and Packaging

Supply Pins

GND

Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ

Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC

Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5 V for IGLOOe V5 devices, and 1.2 V or 1.5 V for IGLOOe V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOOe V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx

I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOOe devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx

I/O Supply Voltage (quiet)

Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F

PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V, depending on the device.

- 1.5 V for IGLOOe devices
- 1.2 V or 1.5 V for IGLOOe V2 devices

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section in the "Clock Conditioning Circuits in Low Power Flash FPGAs and Mixed Signal FPGAs" chapter in the *IGLOOe FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on IGLOOe devices.

VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on IGLOOe devices.

VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

IGLOOe devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User-Defined Supply Pins

VREF I/O Voltage Reference

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOOe FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the *IGLOOe FPGA Fabric User's Guide* for an explanation of the naming of global pins.

FF **Flash*Freeze Mode Activation Pin**

Flash*Freeze mode is available on IGLOOe devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O. The FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOOe FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

Table 3-1 • Flash*Freeze Pin Locations for IGLOOe Devices

| Package | Flash*Freeze Pin |
|---------|------------------|
| FG256 | T3 |
| FG484 | W6 |

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK

Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to Table 3-2 for more information.

Table 3-2 • Recommended Tie-Off Values for the TCK and TRST Pins

| VJTAG | Tie-Off Resistance ^{1,2} |
|----------------|-----------------------------------|
| VJTAG at 3.3 V | 200 Ω to 1 k Ω |
| VJTAG at 2.5 V | 200 Ω to 1 k Ω |
| VJTAG at 1.8 V | 500 Ω to 1 k Ω |
| VJTAG at 1.5 V | 500 Ω to 1 k Ω |

Notes:

1. The TCK pin can be pulled-up or pulled-down.
2. The TRST pin is pulled-down.
3. Equivalent parallel resistance if more than one device is on the JTAG chain

Table 3-3 • TRST and TCK Pull-Down Recommendations

| VJTAG | Tie-Off Resistance* |
|----------------|------------------------------|
| VJTAG at 3.3 V | 200 Ω to 1 k Ω |
| VJTAG at 2.5 V | 200 Ω to 1 k Ω |
| VJTAG at 1.8 V | 500 Ω to 1 k Ω |
| VJTAG at 1.5 V | 500 Ω to 1 k Ω |

Note: Equivalent parallel resistance if more than one device is on the JTAG chain

TDI **Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO **Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST **Boundary Scan Reset Pin**

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from [Table 3-2](#) and must satisfy the parallel resistance value requirement. The values in [Table 3-2](#) correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

User's Guides

IGLOOe FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/IGLOOe_UG.pdf

Packaging Documents

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

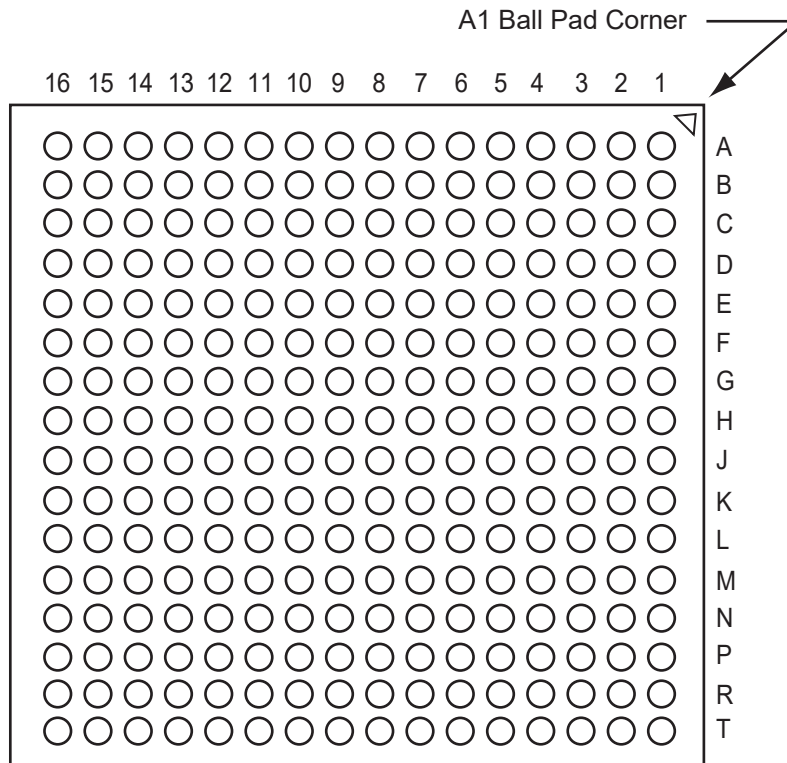
<http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf>

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials: <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

4 – Package Pin Assignments

FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

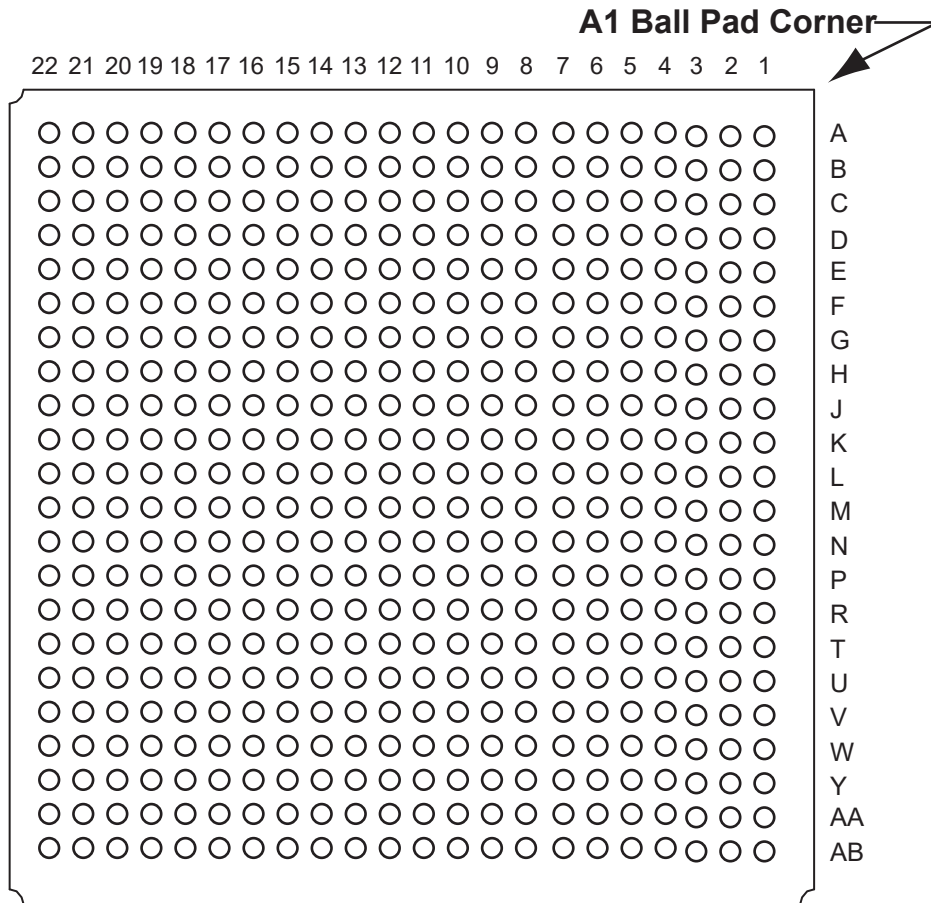
| FG256 | | FG256 | | FG256 | |
|------------|------------------|------------|------------------|------------|------------------|
| Pin Number | AGLE600 Function | Pin Number | AGLE600 Function | Pin Number | AGLE600 Function |
| A1 | GND | C5 | GAC0/IO02NDB0V0 | E9 | IO21NDB1V0 |
| A2 | GAA0/IO00NDB0V0 | C6 | GAC1/IO02PDB0V0 | E10 | VCCIB1 |
| A3 | GAA1/IO00PDB0V0 | C7 | IO15NDB0V2 | E11 | VCCIB1 |
| A4 | GAB0/IO01NDB0V0 | C8 | IO15PDB0V2 | E12 | VMV1 |
| A5 | IO05PDB0V0 | C9 | IO20PDB1V0 | E13 | GBC2/IO38PDB2V0 |
| A6 | IO10PDB0V1 | C10 | IO25NDB1V0 | E14 | IO37NDB2V0 |
| A7 | IO12PDB0V2 | C11 | IO27PDB1V0 | E15 | IO41NDB2V0 |
| A8 | IO16NDB0V2 | C12 | GBC0/IO33NDB1V1 | E16 | IO41PDB2V0 |
| A9 | IO23NDB1V0 | C13 | VCCPLB | F1 | IO124PDB7V0 |
| A10 | IO23PDB1V0 | C14 | VMV2 | F2 | IO125PDB7V0 |
| A11 | IO28NDB1V1 | C15 | IO36NDB2V0 | F3 | IO126PDB7V0 |
| A12 | IO28PDB1V1 | C16 | IO42PDB2V0 | F4 | IO130NDB7V1 |
| A13 | GBB1/IO34PDB1V1 | D1 | IO128PDB7V1 | F5 | VCCIB7 |
| A14 | GBA0/IO35NDB1V1 | D2 | IO129PDB7V1 | F6 | GND |
| A15 | GBA1/IO35PDB1V1 | D3 | GAC2/IO132PDB7V1 | F7 | VCC |
| A16 | GND | D4 | VCOMPLA | F8 | VCC |
| B1 | GAB2/IO133PDB7V1 | D5 | GNDQ | F9 | VCC |
| B2 | GAA2/IO134PDB7V1 | D6 | IO09NDB0V1 | F10 | VCC |
| B3 | GNDQ | D7 | IO09PDB0V1 | F11 | GND |
| B4 | GAB1/IO01PDB0V0 | D8 | IO13PDB0V2 | F12 | VCCIB2 |
| B5 | IO05NDB0V0 | D9 | IO21PDB1V0 | F13 | IO38NDB2V0 |
| B6 | IO10NDB0V1 | D10 | IO25PDB1V0 | F14 | IO40NDB2V0 |
| B7 | IO12NDB0V2 | D11 | IO27NDB1V0 | F15 | IO40PDB2V0 |
| B8 | IO16PDB0V2 | D12 | GNDQ | F16 | IO45PSB2V1 |
| B9 | IO20NDB1V0 | D13 | VCOMPLB | G1 | IO124NDB7V0 |
| B10 | IO24NDB1V0 | D14 | GBB2/IO37PDB2V0 | G2 | IO125NDB7V0 |
| B11 | IO24PDB1V0 | D15 | IO39PDB2V0 | G3 | IO126NDB7V0 |
| B12 | GBC1/IO33PDB1V1 | D16 | IO39NDB2V0 | G4 | GFC1/IO120PPB7V0 |
| B13 | GBB0/IO34NDB1V1 | E1 | IO128NDB7V1 | G5 | VCCIB7 |
| B14 | GNDQ | E2 | IO129NDB7V1 | G6 | VCC |
| B15 | GBA2/IO36PDB2V0 | E3 | IO132NDB7V1 | G7 | GND |
| B16 | IO42NDB2V0 | E4 | IO130PDB7V1 | G8 | GND |
| C1 | IO133NDB7V1 | E5 | VMV0 | G9 | GND |
| C2 | IO134NDB7V1 | E6 | VCCIB0 | G10 | GND |
| C3 | VMV7 | E7 | VCCIB0 | G11 | VCC |
| C4 | VCCPLA | E8 | IO13NDB0V2 | G12 | VCCIB2 |

| FG256 | | FG256 | | FG256 | |
|------------|------------------|------------|------------------|------------|------------------|
| Pin Number | AGLE600 Function | Pin Number | AGLE600 Function | Pin Number | AGLE600 Function |
| G13 | GCC1/IO50PPB2V1 | K1 | GFC2/IO115PSB6V1 | M5 | VMV5 |
| G14 | IO44NDB2V1 | K2 | IO113PPB6V1 | M6 | VCCIB5 |
| G15 | IO44PDB2V1 | K3 | IO112PDB6V1 | M7 | VCCIB5 |
| G16 | IO49NSB2V1 | K4 | IO112NDB6V1 | M8 | IO84NDB5V0 |
| H1 | GFB0/IO119NPB7V0 | K5 | VCCIB6 | M9 | IO84PDB5V0 |
| H2 | GFA0/IO118NDB6V1 | K6 | VCC | M10 | VCCIB4 |
| H3 | GFB1/IO119PPB7V0 | K7 | GND | M11 | VCCIB4 |
| H4 | VCOMPLF | K8 | GND | M12 | VMV3 |
| H5 | GFC0/IO120NPB7V0 | K9 | GND | M13 | VCCPLD |
| H6 | VCC | K10 | GND | M14 | GDB1/IO66PPB3V1 |
| H7 | GND | K11 | VCC | M15 | GDC1/IO65PDB3V1 |
| H8 | GND | K12 | VCCIB3 | M16 | IO61NDB3V1 |
| H9 | GND | K13 | IO54NPB3V0 | N1 | IO105PDB6V0 |
| H10 | GND | K14 | IO57NPB3V0 | N2 | IO105NDB6V0 |
| H11 | VCC | K15 | IO55NPB3V0 | N3 | GEC1/IO104PPB6V0 |
| H12 | GCC0/IO50NPB2V1 | K16 | IO57PPB3V0 | N4 | VCOMPLE |
| H13 | GCB1/IO51PPB2V1 | L1 | IO113NPB6V1 | N5 | GNDQ |
| H14 | GCA0/IO52NPB3V0 | L2 | IO109PPB6V0 | N6 | GEA2/IO101PPB5V2 |
| H15 | VCOMPLC | L3 | IO108PDB6V0 | N7 | IO92NDB5V1 |
| H16 | GCB0/IO51NPB2V1 | L4 | IO108NDB6V0 | N8 | IO90NDB5V1 |
| J1 | GFA2/IO117PSB6V1 | L5 | VCCIB6 | N9 | IO82NDB5V0 |
| J2 | GFA1/IO118PDB6V1 | L6 | GND | N10 | IO74NDB4V1 |
| J3 | VCCPLF | L7 | VCC | N11 | IO74PDB4V1 |
| J4 | IO116NDB6V1 | L8 | VCC | N12 | GNDQ |
| J5 | GFB2/IO116PDB6V1 | L9 | VCC | N13 | VCOMPLD |
| J6 | VCC | L10 | VCC | N14 | VJTAG |
| J7 | GND | L11 | GND | N15 | GDC0/IO65NDB3V1 |
| J8 | GND | L12 | VCCIB3 | N16 | GDA1/IO67PDB3V1 |
| J9 | GND | L13 | GDB0/IO66NPB3V1 | P1 | GEB1/IO103PDB6V0 |
| J10 | GND | L14 | IO60NDB3V1 | P2 | GEB0/IO103NDB6V0 |
| J11 | VCC | L15 | IO60PDB3V1 | P3 | VMV6 |
| J12 | GCB2/IO54PPB3V0 | L16 | IO61PDB3V1 | P4 | VCCPLE |
| J13 | GCA1/IO52PPB3V0 | M1 | IO109NPB6V0 | P5 | IO101NPB5V2 |
| J14 | GCC2/IO55PPB3V0 | M2 | IO106NDB6V0 | P6 | IO95PPB5V1 |
| J15 | VCCPLC | M3 | IO106PDB6V0 | P7 | IO92PDB5V1 |
| J16 | GCA2/IO53PSB3V0 | M4 | GEC0/IO104NPB6V0 | P8 | IO90PDB5V1 |

| FG256 | |
|------------|-------------------------|
| Pin Number | AGLE600 Function |
| P9 | IO82PDB5V0 |
| P10 | IO76NDB4V1 |
| P11 | IO76PDB4V1 |
| P12 | VMV4 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO67NDB3V1 |
| R1 | GEA1/IO102PDB6V0 |
| R2 | GEA0/IO102NDB6V0 |
| R3 | GNDQ |
| R4 | GEC2/IO99PDB5V2 |
| R5 | IO95NPB5V1 |
| R6 | IO91NDB5V1 |
| R7 | IO91PDB5V1 |
| R8 | IO83NDB5V0 |
| R9 | IO83PDB5V0 |
| R10 | IO77NDB4V1 |
| R11 | IO77PDB4V1 |
| R12 | IO69NDB4V0 |
| R13 | GDB2/IO69PDB4V0 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO100NDB5V2 |
| T3 | FF/GEB2/IO100PDB5 V2 |
| T4 | IO99NDB5V2 |
| T5 | IO88NDB5V0 |
| T6 | IO88PDB5V0 |
| T7 | IO89NSB5V0 |
| T8 | IO80NSB4V1 |
| T9 | IO81NDB4V1 |
| T10 | IO81PDB4V1 |
| T11 | IO70NDB4V0 |

| FG256 | |
|------------|------------------|
| Pin Number | AGLE600 Function |
| T12 | GDC2/IO70PDB4V0 |
| T13 | IO68NDB4V0 |
| T14 | GDA2/IO68PDB4V0 |
| T15 | TMS |
| T16 | GND |

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | IO10NDB0V1 |
| A5 | IO10PDB0V1 |
| A6 | IO16NDB0V1 |
| A7 | IO16PDB0V1 |
| A8 | IO18PDB0V2 |
| A9 | IO24PDB0V2 |
| A10 | IO28NDB0V3 |
| A11 | IO28PDB0V3 |
| A12 | IO46PDB1V0 |
| A13 | IO54PDB1V1 |
| A14 | IO56NDB1V1 |
| A15 | IO56PDB1V1 |
| A16 | IO64NDB1V2 |
| A17 | IO64PDB1V2 |
| A18 | IO72NDB1V3 |
| A19 | IO74NDB1V4 |
| A20 | VCCIB1 |
| A21 | GND |
| A22 | GND |
| AA1 | GND |
| AA2 | VCCIB6 |
| AA3 | IO228PDB5V4 |
| AA4 | IO224PDB5V3 |
| AA5 | IO218NDB5V3 |
| AA6 | IO218PDB5V3 |
| AA7 | IO212NDB5V2 |
| AA8 | IO212PDB5V2 |
| AA9 | IO198PDB5V0 |
| AA10 | IO198NDB5V0 |
| AA11 | IO188PPB4V4 |
| AA12 | IO180NDB4V3 |
| AA13 | IO180PDB4V3 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| AA14 | IO170NDB4V2 |
| AA15 | IO170PDB4V2 |
| AA16 | IO166NDB4V1 |
| AA17 | IO166PDB4V1 |
| AA18 | IO160NDB4V0 |
| AA19 | IO160PDB4V0 |
| AA20 | IO158NPB4V0 |
| AA21 | VCCIB3 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB5 |
| AB4 | IO216NDB5V2 |
| AB5 | IO216PDB5V2 |
| AB6 | IO210NDB5V2 |
| AB7 | IO210PDB5V2 |
| AB8 | IO208NDB5V1 |
| AB9 | IO208PDB5V1 |
| AB10 | IO197NDB5V0 |
| AB11 | IO197PDB5V0 |
| AB12 | IO174NDB4V2 |
| AB13 | IO174PDB4V2 |
| AB14 | IO172NDB4V2 |
| AB15 | IO172PDB4V2 |
| AB16 | IO168NDB4V1 |
| AB17 | IO168PDB4V1 |
| AB18 | IO162NDB4V1 |
| AB19 | IO162PDB4V1 |
| AB20 | VCCIB4 |
| AB21 | GND |
| AB22 | GND |
| B1 | GND |
| B2 | VCCIB7 |
| B3 | IO06PPB0V0 |
| B4 | IO08NDB0V0 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| B5 | IO08PDB0V0 |
| B6 | IO14NDB0V1 |
| B7 | IO14PDB0V1 |
| B8 | IO18NDB0V2 |
| B9 | IO24NDB0V2 |
| B10 | IO34PDB0V4 |
| B11 | IO40PDB0V4 |
| B12 | IO46NDB1V0 |
| B13 | IO54NDB1V1 |
| B14 | IO62NDB1V2 |
| B15 | IO62PDB1V2 |
| B16 | IO68NDB1V3 |
| B17 | IO68PDB1V3 |
| B18 | IO72PDB1V3 |
| B19 | IO74PDB1V4 |
| B20 | IO76NPB1V4 |
| B21 | VCCIB2 |
| B22 | GND |
| C1 | VCCIB7 |
| C2 | IO303PDB7V3 |
| C3 | IO305PDB7V3 |
| C4 | IO06NPB0V0 |
| C5 | GND |
| C6 | IO12NDB0V1 |
| C7 | IO12PDB0V1 |
| C8 | VCC |
| C9 | VCC |
| C10 | IO34NDB0V4 |
| C11 | IO40NDB0V4 |
| C12 | IO48NDB1V0 |
| C13 | IO48PDB1V0 |
| C14 | VCC |
| C15 | VCC |
| C16 | IO70NDB1V3 |
| C17 | IO70PDB1V3 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| C18 | GND |
| C19 | IO76PPB1V4 |
| C20 | IO88NDB2V0 |
| C21 | IO94PPB2V1 |
| C22 | VCCIB2 |
| D1 | IO293PDB7V2 |
| D2 | IO303NDB7V3 |
| D3 | IO305NDB7V3 |
| D4 | GND |
| D5 | GAA0/IO00NDB0V0 |
| D6 | GAA1/IO00PDB0V0 |
| D7 | GAB0/IO01NDB0V0 |
| D8 | IO20PDB0V2 |
| D9 | IO22PDB0V2 |
| D10 | IO30PDB0V3 |
| D11 | IO38NDB0V4 |
| D12 | IO52NDB1V1 |
| D13 | IO52PDB1V1 |
| D14 | IO66NDB1V3 |
| D15 | IO66PDB1V3 |
| D16 | GBB1/IO80PDB1V4 |
| D17 | GBA0/IO81NDB1V4 |
| D18 | GBA1/IO81PDB1V4 |
| D19 | GND |
| D20 | IO88PDB2V0 |
| D21 | IO90PDB2V1 |
| D22 | IO94NPB2V1 |
| E1 | IO293NDB7V2 |
| E2 | IO299PPB7V3 |
| E3 | GND |
| E4 | GAB2/IO308PDB7V4 |
| E5 | GAA2/IO309PDB7V4 |
| E6 | GNDQ |
| E7 | GAB1/IO01PDB0V0 |
| E8 | IO20NDB0V2 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| E9 | IO22NDB0V2 |
| E10 | IO30NDB0V3 |
| E11 | IO38PDB0V4 |
| E12 | IO44NDB1V0 |
| E13 | IO58NDB1V2 |
| E14 | IO58PDB1V2 |
| E15 | GBC1/IO79PDB1V4 |
| E16 | GBB0/IO80NDB1V4 |
| E17 | GNDQ |
| E18 | GBA2/IO82PDB2V0 |
| E19 | IO86NDB2V0 |
| E20 | GND |
| E21 | IO90NDB2V1 |
| E22 | IO98PDB2V2 |
| F1 | IO299NPB7V3 |
| F2 | IO301NDB7V3 |
| F3 | IO301PDB7V3 |
| F4 | IO308NDB7V4 |
| F5 | IO309NDB7V4 |
| F6 | VMV7 |
| F7 | VCCPLA |
| F8 | GAC0/IO02NDB0V0 |
| F9 | GAC1/IO02PDB0V0 |
| F10 | IO32NDB0V3 |
| F11 | IO32PDB0V3 |
| F12 | IO44PDB1V0 |
| F13 | IO50NDB1V1 |
| F14 | IO60PDB1V2 |
| F15 | GBC0/IO79NDB1V4 |
| F16 | VCCPLB |
| F17 | VMV2 |
| F18 | IO82NDB2V0 |
| F19 | IO86PDB2V0 |
| F20 | IO96PDB2V1 |
| F21 | IO96NDB2V1 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| F22 | IO98NDB2V2 |
| G1 | IO289NDB7V1 |
| G2 | IO289PDB7V1 |
| G3 | IO291PPB7V2 |
| G4 | IO295PDB7V2 |
| G5 | IO297PDB7V2 |
| G6 | GAC2/IO307PDB7V4 |
| G7 | VCOMPLA |
| G8 | GNDQ |
| G9 | IO26NDB0V3 |
| G10 | IO26PDB0V3 |
| G11 | IO36PDB0V4 |
| G12 | IO42PDB1V0 |
| G13 | IO50PDB1V1 |
| G14 | IO60NDB1V2 |
| G15 | GNDQ |
| G16 | VCOMPLB |
| G17 | GBB2/IO83PDB2V0 |
| G18 | IO92PDB2V1 |
| G19 | IO92NDB2V1 |
| G20 | IO102PDB2V2 |
| G21 | IO102NDB2V2 |
| G22 | IO105NDB2V2 |
| H1 | IO286PSB7V1 |
| H2 | IO291NPB7V2 |
| H3 | VCC |
| H4 | IO295NDB7V2 |
| H5 | IO297NDB7V2 |
| H6 | IO307NDB7V4 |
| H7 | IO287PDB7V1 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO36NDB0V4 |
| H12 | IO42NDB1V0 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| H13 | VCCIB1 |
| H14 | VCCIB1 |
| H15 | VMV1 |
| H16 | GBC2/IO84PDB2V0 |
| H17 | IO83NDB2V0 |
| H18 | IO100NDB2V2 |
| H19 | IO100PDB2V2 |
| H20 | VCC |
| H21 | VMV2 |
| H22 | IO105PDB2V2 |
| J1 | IO285NDB7V1 |
| J2 | IO285PDB7V1 |
| J3 | VMV7 |
| J4 | IO279PDB7V0 |
| J5 | IO283PDB7V1 |
| J6 | IO281PDB7V0 |
| J7 | IO287NDB7V1 |
| J8 | VCCIB7 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB2 |
| J16 | IO84NDB2V0 |
| J17 | IO104NDB2V2 |
| J18 | IO104PDB2V2 |
| J19 | IO106PPB2V3 |
| J20 | GNDQ |
| J21 | IO109PDB2V3 |
| J22 | IO107PDB2V3 |
| K1 | IO277NDB7V0 |
| K2 | IO277PDB7V0 |
| K3 | GNDQ |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| K4 | IO279NDB7V0 |
| K5 | IO283NDB7V1 |
| K6 | IO281NDB7V0 |
| K7 | GFC1/IO275PPB7V0 |
| K8 | VCCIB7 |
| K9 | VCC |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | VCC |
| K15 | VCCIB2 |
| K16 | GCC1/IO112PPB2V3 |
| K17 | IO108NDB2V3 |
| K18 | IO108PDB2V3 |
| K19 | IO110NPB2V3 |
| K20 | IO106NPB2V3 |
| K21 | IO109NDB2V3 |
| K22 | IO107NDB2V3 |
| L1 | IO257PSB6V2 |
| L2 | IO276PDB7V0 |
| L3 | IO276NDB7V0 |
| L4 | GFB0/IO274NPB7V0 |
| L5 | GFA0/IO273NDB6V4 |
| L6 | GFB1/IO274PPB7V0 |
| L7 | VCOMPLF |
| L8 | GFC0/IO275NPB7V0 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | VCC |
| L15 | GCC0/IO112NPB2V3 |
| L16 | GCB1/IO113PPB2V3 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| L17 | GCA0/IO114NPB3V0 |
| L18 | VCOMPLC |
| L19 | GCB0/IO113NPB2V3 |
| L20 | IO110PPB2V3 |
| L21 | IO111NDB2V3 |
| L22 | IO111PDB2V3 |
| M1 | GNDQ |
| M2 | IO255NPB6V2 |
| M3 | IO272NDB6V4 |
| M4 | GFA2/IO272PDB6V4 |
| M5 | GFA1/IO273PDB6V4 |
| M6 | VCCPLF |
| M7 | IO271NDB6V4 |
| M8 | GFB2/IO271PDB6V4 |
| M9 | VCC |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | VCC |
| M15 | GCB2/IO116PPB3V0 |
| M16 | GCA1/IO114PPB3V0 |
| M17 | GCC2/IO117PPB3V0 |
| M18 | VCCPLC |
| M19 | GCA2/IO115PDB3V0 |
| M20 | IO115NDB3V0 |
| M21 | IO126PDB3V1 |
| M22 | IO124PSB3V1 |
| N1 | IO255PPB6V2 |
| N2 | IO253NDB6V2 |
| N3 | VMV6 |
| N4 | GFC2/IO270PPB6V4 |
| N5 | IO261PPB6V3 |
| N6 | IO263PDB6V3 |
| N7 | IO263NDB6V3 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| N8 | VCCIB6 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | VCC |
| N15 | VCCIB3 |
| N16 | IO116NPB3V0 |
| N17 | IO132NPB3V2 |
| N18 | IO117NPB3V0 |
| N19 | IO132PPB3V2 |
| N20 | GNDQ |
| N21 | IO126NDB3V1 |
| N22 | IO128PDB3V1 |
| P1 | IO247PDB6V1 |
| P2 | IO253PDB6V2 |
| P3 | IO270NPB6V4 |
| P4 | IO261NPB6V3 |
| P5 | IO249PPB6V1 |
| P6 | IO259PDB6V3 |
| P7 | IO259NDB6V3 |
| P8 | VCCIB6 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB3 |
| P16 | GDB0/IO152NPB3V4 |
| P17 | IO136NDB3V2 |
| P18 | IO136PDB3V2 |
| P19 | IO138PDB3V3 |
| P20 | VMV3 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| P21 | IO130PDB3V2 |
| P22 | IO128NDB3V1 |
| R1 | IO247NDB6V1 |
| R2 | IO245PDB6V1 |
| R3 | VCC |
| R4 | IO249NPB6V1 |
| R5 | IO251NDB6V2 |
| R6 | IO251PDB6V2 |
| R7 | GEC0/IO236NPB6V0 |
| R8 | VMV5 |
| R9 | VCCIB5 |
| R10 | VCCIB5 |
| R11 | IO196NDB5V0 |
| R12 | IO196PDB5V0 |
| R13 | VCCIB4 |
| R14 | VCCIB4 |
| R15 | VMV3 |
| R16 | VCCPLD |
| R17 | GDB1/IO152PPB3V4 |
| R18 | GDC1/IO151PDB3V4 |
| R19 | IO138NDB3V3 |
| R20 | VCC |
| R21 | IO130NDB3V2 |
| R22 | IO134PDB3V2 |
| T1 | IO243PPB6V1 |
| T2 | IO245NDB6V1 |
| T3 | IO243NPB6V1 |
| T4 | IO241PDB6V0 |
| T5 | IO241NDB6V0 |
| T6 | GEC1/IO236PPB6V0 |
| T7 | VCOMPLE |
| T8 | GNDQ |
| T9 | GEA2/IO233PPB5V4 |
| T10 | IO206NDB5V1 |
| T11 | IO202NDB5V1 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| T12 | IO194NDB5V0 |
| T13 | IO186NDB4V4 |
| T14 | IO186PDB4V4 |
| T15 | GNDQ |
| T16 | VCOMPLD |
| T17 | VJTAG |
| T18 | GDC0/IO151NDB3V4 |
| T19 | GDA1/IO153PDB3V4 |
| T20 | IO144PDB3V3 |
| T21 | IO140PDB3V3 |
| T22 | IO134NDB3V2 |
| U1 | IO240PPB6V0 |
| U2 | IO238PDB6V0 |
| U3 | IO238NDB6V0 |
| U4 | GEB1/IO235PDB6V0 |
| U5 | GEB0/IO235NDB6V0 |
| U6 | VMV6 |
| U7 | VCCPLE |
| U8 | IO233NPB5V4 |
| U9 | IO222PPB5V3 |
| U10 | IO206PDB5V1 |
| U11 | IO202PDB5V1 |
| U12 | IO194PDB5V0 |
| U13 | IO176NDB4V2 |
| U14 | IO176PDB4V2 |
| U15 | VMV4 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO153NDB3V4 |
| U20 | IO144NDB3V3 |
| U21 | IO140NDB3V3 |
| U22 | IO142PDB3V3 |
| V1 | IO239PDB6V0 |
| V2 | IO240NPB6V0 |

| FG484 | |
|------------|-------------------------|
| Pin Number | AGLE3000 Function |
| V3 | GND |
| V4 | GEA1/IO234PDB6V0 |
| V5 | GEA0/IO234NDB6V0 |
| V6 | GNDQ |
| V7 | GEC2/IO231PDB5V4 |
| V8 | IO222NPB5V3 |
| V9 | IO204NDB5V1 |
| V10 | IO204PDB5V1 |
| V11 | IO195NDB5V0 |
| V12 | IO195PDB5V0 |
| V13 | IO178NDB4V3 |
| V14 | IO178PDB4V3 |
| V15 | IO155NDB4V0 |
| V16 | GDB2/IO155PDB4V0 |
| V17 | TDI |
| V18 | GNDQ |
| V19 | TDO |
| V20 | GND |
| V21 | IO146PDB3V4 |
| V22 | IO142NDB3V3 |
| W1 | IO239NDB6V0 |
| W2 | IO237PDB6V0 |
| W3 | IO230PSB5V4 |
| W4 | GND |
| W5 | IO232NDB5V4 |
| W6 | FF/GEB2/IO232PDB5 V4 |
| W7 | IO231NDB5V4 |
| W8 | IO214NDB5V2 |
| W9 | IO214PDB5V2 |
| W10 | IO200NDB5V0 |
| W11 | IO192NDB4V4 |
| W12 | IO184NDB4V3 |
| W13 | IO184PDB4V3 |
| W14 | IO156NDB4V0 |

| FG484 | |
|------------|-------------------|
| Pin Number | AGLE3000 Function |
| W15 | GDC2/IO156PDB4V0 |
| W16 | IO154NDB4V0 |
| W17 | GDA2/IO154PDB4V0 |
| W18 | TMS |
| W19 | GND |
| W20 | IO150NDB3V4 |
| W21 | IO146NDB3V4 |
| W22 | IO148PPB3V4 |
| Y1 | VCCIB6 |
| Y2 | IO237NDB6V0 |
| Y3 | IO228NDB5V4 |
| Y4 | IO224NDB5V3 |
| Y5 | GND |
| Y6 | IO220NDB5V3 |
| Y7 | IO220PDB5V3 |
| Y8 | VCC |
| Y9 | VCC |
| Y10 | IO200PDB5V0 |
| Y11 | IO192PDB4V4 |
| Y12 | IO188NPB4V4 |
| Y13 | IO187PSB4V4 |
| Y14 | VCC |
| Y15 | VCC |
| Y16 | IO164NDB4V1 |
| Y17 | IO164PDB4V1 |
| Y18 | GND |
| Y19 | IO158PPB4V0 |
| Y20 | IO150PDB3V4 |
| Y21 | IO148NPB3V4 |
| Y22 | VCCIB3 |

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOOe datasheet.

| Revision | Changes | Page |
|---------------------------------|--|---------------|
| Revision 14 (October 2019) | All references to FBGA package FG896 have been removed from this document. | |
| | The maximum user I/Os specification in "Features and Benefits" and Table 1 • IGLOOe Product Family were revised to reflect current specifications. | I |
| | The maximum user I/Os specification in "General Description" section was revised to reflect current specifications. | |
| | The "IGLOOe Ordering Information" and "Temperature Grade Offerings" section ambient temperature specifications were revised to reflect junction temperature specifications. | III, IV |
| | Ambient Temperature specifications have been removed from Table 2-2 • Recommended Operating Conditions ¹ . Note 2 was added. | 2-2 |
| Revision 13 (December 2012) | The "IGLOOe Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43176). Also added the missing heading 'Supply Voltage' under V2. | III |
| | The note in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42568). | 2-91, 2-92 |
| | Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 12 (September 2012) | The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data. | 1-2 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40272). | N/A |

| Revision | Changes | Page |
|------------------------------|---|------|
| Revision 11 (August 2012) | <p>The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 37180):</p> <p>Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels, 2-20</p> <p>Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings 2-25</p> <p>Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings 2-26</p> <p>Table 2-28 • I/O Output Buffer Maximum Resistances¹ 2-28</p> <p>Table 2-73 • Minimum and Maximum DC Input and Output Levels 2-51</p> <p>Table 2-77 • Minimum and Maximum DC Input and Output Levels 2-53</p> <p>Also added note stating "Output drive strength is below JEDEC specification." for Tables 2-25, 2-26, and 2-28.</p> <p>Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-21 (SAR 39713).</p> | |
| | <p>In Table 2-117 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37183).</p> | 2-65 |
| | <p>The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38318). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.</p> | 3-1 |

| Revision | Changes | Page |
|-----------------------------|--|------------------------|
| Revision 10 (April 2012) | In Table 2-2 • Recommended Operating Conditions ¹ , VPUMP programming voltage for operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 32256). Values for VCCPLL at 1.2–1.5 V DC core supply voltage were changed from "1.14 to 1.26 V" to "1.14 to 1.575 V" (SAR 34701). | 2-2 |
| | The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD. Table 2-8 • Power Supply State per Mode is new (SARs 34745, 36949). | 2-7 |
| | t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37105). | 2-17 |
| | "TBD" for 3.3 V LVCMOS Wide Range in Table 2-28 • I/O Output Buffer Maximum Resistances ¹ and Table 2-30 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33855). Values were also added for 1.2 V LVCMOS and 1.2 V LVCMOS Wide Range. | 2-28, 2-30 |
| | The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34753). | 2-29 |
| | IOSH and IOSL values were added to 3.3 V LVCMOS Wide Range Table 2-40 • Minimum and Maximum DC Input and Output Levels , 1.2 V LVCMOS Table 2-64 • Minimum and Maximum DC Input and Output Levels , and 1.2 V LVCMOS Wide Range Table 2-68 • Minimum and Maximum DC Input and Output Levels (SAR 33855). | 2-35, 2-47, 2-48 |
| | Figure 2-48 • FIFO Read and Figure 2-49 • FIFO Write have been added (SAR 34844). | 2-103 |
| | Values for $F_{DDRIMAX}$ and F_{DDOMAX} were added to the tables in the Input DDR " Timing Characteristics " section and Output DDR " Timing Characteristics " section (SAR 34802). | 2-77,2- 81 |
| | Minimum pulse width High and Low values were added to the tables in the " Global Tree Timing Characteristics " section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36952). | 2-89 |
| Revision 9 (March 2012) | The " In-System Programming (ISP) and Security " section and " Security " section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34665). | I, 1-2 |
| | The Y security option and Licensed DPA Logo were added to the " IGLOOe Ordering Information " section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34725). | III |
| | The following sentence was removed from the " Advanced Architecture " section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOOe devices via an IEEE 1532 JTAG interface" (SAR 34685). | 1-3 |
| | The " Specifying I/O States During Programming " section is new (SAR 34696). | 1-7 |
| | Values for VCCPLL at 1.5 V DC core supply voltage were changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" in Table 2-2 • Recommended Operating Conditions ¹ (SAR 32292). | 2-2 |
| | The reference to guidelines for global spines and VersaTile rows, given in the " Global Clock Contribution—P_{CLOCK} " section, was corrected to the " Spine Architecture " section of the Global Resources chapter in the <i>IGLOOe FPGA Fabric User's Guide</i> (SAR 34731). | 2-13 |

| Revision | Changes | Page |
|---|--|-----------------------------------|
| Revision 9 (continued) | The example in the paragraph above Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 32287). | 2-31 |
| | The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 34766). | 2-23, 2-35, 2-48 |
| | The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34886). | 2-32 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34793): "It uses a 5 V–tolerant input buffer and push-pull output buffer." | 2-38 |
| | Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34818). | 2-91, 2-92 |
| | The following figures were deleted. Reference was made to a new application note, <i>Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs</i> , which covers these cases in detail (SAR 34869). Figure 2-46 • Write Access after Write onto Same Address Figure 2-47 • Read Access after Write onto Same Address Figure 2-48 • Write Access after Read onto Same Address | 2-95, 2-98, 2-104, 2-106 |
| | The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-50 • FIFO Reset , and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35749). | |
| | The "Pin Descriptions and Packaging" chapter is new (SAR 34768). | 3-1 |
| Package names used in the "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 34768) | 4-1 | |
| July 2010 | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOOe Device Status" table on page II indicates the status for each device in the device family. | N/A |

| Revision | Changes | Page |
|---------------------------------------|---|------|
| Revision 8 (Nov 2009) | The version changed to v2.0 for IGLOOe datasheet chapters, indicating the datasheet contains information based on final characterization. | N/A |
| Product Brief v2.0 | The "Pro (Professional) I/O" section was revised to add "Hot-swappable and cold-sparing I/Os." | I |
| | The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance." | I |
| DC and Switching Characteristics v2.0 | Definitions of hot-swap and cold-sparing were added to the "Pro I/Os with Advanced I/O Standards" section. | 1-7 |
| | 3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data. | N/A |

| Revision | Changes | Page |
|--|---|---------------------|
| | IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables. | N/A |
| | Values for 1.2 V wide range DC core supply voltage were added to Table 2-2 • Recommended Operating Conditions ¹ . Table notes regarding 3.3 V wide range and the core voltage required for programming were added to the table. | 2-2 |
| | The data in Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (1.5 V DC core supply voltage) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (1.2 V DC core supply voltage) was revised. | 2-6 |
| | 3.3 V LVCMOS wide range data was included in Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹ . Table notes were added in connection with this data. | 2-9, 2-10 |
| | The temperature was revised from 110°C to 100°C in Table 2-31 • Duration of Short Circuit Event before Failure and Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability [*] . | 2-31, 2-31 |
| | The tables in the "Overview of I/O Performance" section and "Detailed I/O DC Characteristics" section were revised to include 3.3 V LVCMOS and 1.2 V LVCMOS wide range. | 2-20, 2-28 |
| | Most tables were updated in the following sections, revising existing values and adding information for 3.3 V and 1.2 V wide range: "Single-Ended I/O Characteristics" "Voltage-Referenced I/O Characteristics" "Differential I/O Characteristics" | 2-32, 2-51, 2-62 |
| | The value for "Delay range in block: fixed delay" was revised in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification . | 2-91, 2-92 |
| | The timing characteristics tables for RAM4K9 and RAM512X18 were updated, including renaming of the address collision parameters. | 2-98 – 2-101 |
| Revision 7 (Apr 2009) Product Brief v1.4 DC and Switching Characteristics Advance v0.4 | The –F speed grade is no longer offered for IGLOOe devices and was removed from the documentation. The speed grade column and note regarding –F speed grade were removed from " IGLOOe Ordering Information ". The " Speed Grade and Temperature Grade Matrix " section was removed. | III, IV |

| Revision | Changes | Page |
|---|--|------|
| Revision 6 (Feb 2009) Product Brief v1.3 | The "Pro (Professional) I/O" section was revised to add two bullets regarding wide range power supply voltage support. | I |
| | 3.0 V was added to the list of supported voltages in the "Pro I/Os with Advanced I/O Standards" section. The "Wide Range I/O Support" section is new. | 1-7 |
| Revision 5 (Oct 2008) Product Brief v1.2 | The Quiescent Current values in Table 1 • IGLOOe Product Family table were updated. | I |
| Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3 | As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V. | N/A |
| Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2 | Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. The power data table has been updated to match SmartPower data rather than simulation values. | N/A |
| | Table 2-144 • IGLOOe CCC/PLL Specification was updated to add VMV to the VCCI parameter row and remove the word "output" from the parameter description for VCCI. Table note 3 was added. | 2-92 |
| | Table 2-2 • Recommended Operating Conditions ¹ was updated to include the T _J parameter. Table note 9 is new. | 2-2 |
| | In Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature ¹ , the maximum operating junction temperature was changed from 110° to 100°. | 2-3 |
| | VMV was removed from Table 2-4 • Overshoot and Undershoot Limits 1, 3 . The title of the table was revised to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted. | 2-3 |
| | The "PLL Behavior at Brownout Condition" section is new. | 2-4 |
| | Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels is new. | 2-5 |
| | EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed. | 2-6 |
| | The table notes for Table 2-9 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode* , Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Sleep Mode* , and Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode* were updated to remove VMV and include PDC6 and PDC7. VCCI and VJTAG were removed from the statement about IDD in the table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode* . | 2-7 |
| | Note 2 of Table 2-12 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode ¹ was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7. | 2-8 |
| Table note 3 was added to Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and referenced for 1.2 V LVCMOS. | 2-9 | |

| Revision | Changes | Page | | | | | | | | | | | | | | |
|--|---|-----------------|-------------------|-----|------------|-----|------------|----|-------------|----|-------------|----|------------------|----|-------------|-----|
| Revision 3 (cont'd) | Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹ was updated to change PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI. Table note 4 is new. | 2-10 | | | | | | | | | | | | | | |
| | Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power. | 2-11, 2-12 | | | | | | | | | | | | | | |
| | A table subtitle was added for Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices. | 2-12 | | | | | | | | | | | | | | |
| | The "Total Static Power Consumption—P _{STAT} " section was updated to revise the calculation of P _{STAT} , including PDC6 and PDC7. | 2-13 | | | | | | | | | | | | | | |
| | Footnote 1 was updated to include information about P _{AC13} . The PLL Contribution equation was changed from: P _{PLL} = P _{AC13} + P _{AC14} * F _{CLKOUT} to P _{PLL} = P _{DC4} + P _{AC13} * F _{CLKOUT} . | 2-14 | | | | | | | | | | | | | | |
| | The "Timing Model" was updated to be consistent with the revised timing numbers. | 2-16 | | | | | | | | | | | | | | |
| | In Table 2-22 • Summary of Maximum and Minimum DC Input Levels, T _J was changed to T _A in notes 1 and 2. | 2-22 | | | | | | | | | | | | | | |
| | Table 2-22 • Summary of Maximum and Minimum DC Input Levels was updated to include a hysteresis value for 1.2 V LVCMOS (Schmitt trigger mode). | 2-22 | | | | | | | | | | | | | | |
| | All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF. | N/A | | | | | | | | | | | | | | |
| The "1.2 V LVCMOS (JESD8-12A)" section is new. | 2-47 | | | | | | | | | | | | | | | |
| Revision 2 (Jun 2008) Product Brief v1.0 | The product brief section of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview. | N/A | | | | | | | | | | | | | | |
| Revision 2 (cont'd) Packaging v1.1 | The naming conventions changed for the following pins in the "FG484" for the A3GLE600: <table border="0" style="margin-left: 20px;"> <tr> <td>Pin Number</td> <td>New Function Name</td> </tr> <tr> <td>J19</td> <td>IO45PPB2V1</td> </tr> <tr> <td>K20</td> <td>IO45NPB2V1</td> </tr> <tr> <td>M2</td> <td>IO114NPB6V1</td> </tr> <tr> <td>N1</td> <td>IO114PPB6V1</td> </tr> <tr> <td>N4</td> <td>GFC2/IO115PPB6V1</td> </tr> <tr> <td>P3</td> <td>IO115NPB6V1</td> </tr> </table> | Pin Number | New Function Name | J19 | IO45PPB2V1 | K20 | IO45NPB2V1 | M2 | IO114NPB6V1 | N1 | IO114PPB6V1 | N4 | GFC2/IO115PPB6V1 | P3 | IO115NPB6V1 | N/A |
| Pin Number | New Function Name | | | | | | | | | | | | | | | |
| J19 | IO45PPB2V1 | | | | | | | | | | | | | | | |
| K20 | IO45NPB2V1 | | | | | | | | | | | | | | | |
| M2 | IO114NPB6V1 | | | | | | | | | | | | | | | |
| N1 | IO114PPB6V1 | | | | | | | | | | | | | | | |
| N4 | GFC2/IO115PPB6V1 | | | | | | | | | | | | | | | |
| P3 | IO115NPB6V1 | | | | | | | | | | | | | | | |
| Revision 1 (Mar 2008) Product Brief rev. 1 | The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 25 μW)" was removed from "Low Power Active FPGA Operation." 1.2_V was added to the list of core and I/O voltages in the "Pro (Professional) I/O" and "Pro I/Os with Advanced I/O Standards" section sections. | I I, 1-7 | | | | | | | | | | | | | | |
| Revision 0 (Jan 2008) | This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700096-001-0. | N/A | | | | | | | | | | | | | | |

| Revision | Changes | Page |
|---|--|----------------|
| Advance v0.4 (December 2007) | The Table 1 • IGLOOe Product Family table was updated to change the maximum number of user I/Os for AGLE3000. | I |
| | The " IGLOOe FPGAs Package Sizes Dimensions " table is new. Package dimensions were removed from the " I/Os Per Package¹ " table. The number of I/Os was updated for FG896. | II |
| | A note regarding marking information was added to the " IGLOOe Ordering Information " table. | III |
| | Table 2-4 • IGLOOe CCC/PLL Specification and Table 2-5 • IGLOOe CCC/PLL Specification were updated. | 2-18, 2-19 |
| | The "During Flash*Freeze Mode" section was updated to include information about the output of the I/O to the FPGA core. | 2-60 |
| | Figure 2-38 • Flash*Freeze Mode Type 1 – Timing Diagram was updated to modify the LSICC signal. | 2-56 |
| | Table 2-32 • Flash*Freeze Pin Location in IGLOOe Family Packages (device-independent) was updated for the FG896 package. | 2-64 |
| | Figure 2-40 • Flash*Freeze Mode Type 2 – Timing Diagram was updated to modify the LSICC Signal. | 2-58 |
| | Information regarding calculation of the quiescent supply current was added to the "Quiescent Supply Current" section. | 3-6 |
| | Table 3-8 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode† was updated. | 3-6 |
| | Table 3-9 • Quiescent Supply Current (IDD), IGLOOe Sleep Mode (VCC = 0 V)† was updated. | 3-6 |
| | Table 3-11 • Quiescent Supply Current, No IGLOOe Flash*Freeze Mode ¹ was updated. | 3-6 |
| | Table 3-99 • Minimum and Maximum DC Input and Output Levels was updated. | 3-51 |
| | Table 3-136 • JTAG 1532 and Table 3-135 • JTAG 1532 were updated. | 3-95 |
| | The "484-Pin FBGA" table for AGLE3000 is new. | 4-11 |
| The "896-Pin FBGA" package and table for AGLE3000 is new. | 4-16 | |
| Advance v0.3 (September 2007) | Cortex-M1 device information was added to the Table 1 • IGLOOe Product Family table, the " I/Os Per Package¹ " table, " IGLOOe Ordering Information ", and " Temperature Grade Offerings ". | I, II, III, IV |
| Advance v0.2 | The words "ambient temperature" were added to the temperature range in the " IGLOOe Ordering Information ", " Temperature Grade Offerings ", and " Speed Grade and Temperature Grade Matrix " sections. | III, IV |
| | The T _J parameter in Table 3-2 • Recommended Operating Conditions was changed to T _A , ambient temperature, and table notes 6–8 were added. | 3-2 |

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOOe Device Status" table, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.

