PRECISION P-CHANNEL EPAD® MOSFET ARRAY

QUAD ENHANCED MODE MATCHED PAIR

VGS(th)= -0.80V

GENERAL DESCRIPTION

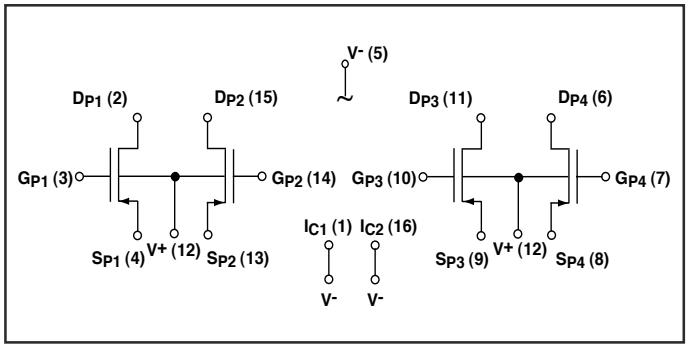
ALD310708A/ALD310708 high precision monolithic quad P-Channel MOSFET arrays are matched at the factory using ALD's proven EPAD® CMOS technology. This device is available in a quad version and is a member of the EPAD® Matched Pair MOSFET Family. The ALD310708A/ALD310708 is a P-channel version of the popular ALD110808A/ALD110808 Precision Threshold device. Together, these two MOSFET series enable complementary precision N-Channel and P-Channel MOSFET array based circuits.

Intended for low voltage and low power small signal applications, the ALD310708A/ALD310708 features precision -0.80V Gate Threshold Voltage, which enables circuit designs with very low operating voltages such as 2V power supplies where the circuits operate below the threshold voltage of the ALD310708A/ALD310708. This feature also enhances input/output signal operating ranges, especially in very low operating voltage environments. With these low threshold precision devices, a circuit with multiple cascading stages can be constructed to operate at extremely low supply or bias voltage levels. ALD310708A/ALD310708 also features high input impedance ($2.5 \times 10^{10}\Omega$) and high DC current gain ($>10^8$).

ALD310708A/ALD310708 MOSFETs are designed for exceptional matching of device electrical characteristics. The Gate Threshold Voltage $V_{GS(th)}$ is set precisely at -0.80V +/-0.02V, featuring a typical offset voltage of only +/-0.001V (1mV). As these devices are on the same monolithic chip, they also exhibit excellent temperature tracking characteristics. They are versatile design components for a broad range of precision analog applications such as basic building blocks for current mirrors, matching circuits, current sources, differential amplifier input stages, transmission gates, and multiplexers. These devices also excel in limited operating voltage applications such as very low level precision voltage-clamps. In addition to matched pair electrical characteristics, each individual MOSFET exhibits individual well controlled manufacturing characteristics, enabling the user to depend on tight design limits from different production batches.

(Continued on next page)

BLOCK DIAGRAM



ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range * 0°C to +70°C	
16-Pin SOIC Package	16-Pin Plastic Dip Package
ALD310708ASCL ALD310708SCL	ALD310708APCL ALD310708PCL

*Contact factory for industrial temp. range or user-specified threshold voltage values.

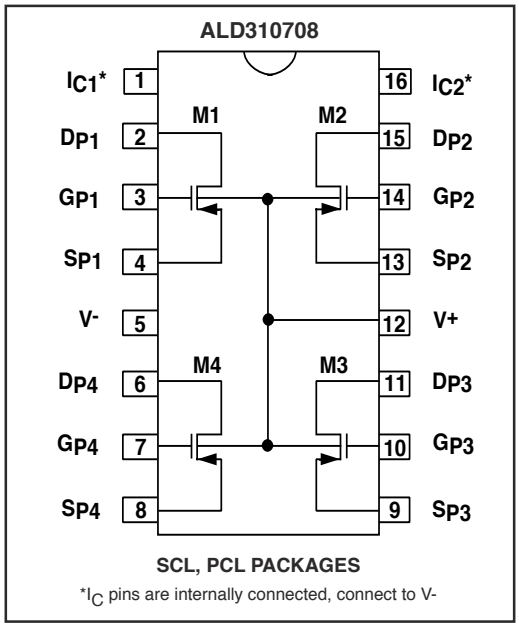
APPLICATIONS

- 0.5% precision current mirrors and current sources
- Low Tempco (<= 50ppm/°C) current mirrors/sources
- Energy harvesting circuits
- Very low voltage analog and digital circuits
- Backup battery circuits & power failure detectors
- Precision low level voltage-clamps
- Low level zero-crossing detector
- Source followers and buffers
- Precision capacitive probes and sensor interfaces
- Precision charge detectors and charge integrators
- Discrete differential amplifier input stage
- Peak-detectors and level-shifters
- High-side switches and Sample-and-Hold switches
- Precision current multipliers
- Discrete analog switches / multiplexers
- Discrete voltage comparators

FEATURES & BENEFITS

- Precision matched Gate Threshold Voltages
- Precision offset voltages (V_{OS}):
  - ALD310708A: 1mV typical
  - ALD310708: 2mV typical
- Sub-threshold voltage operation
- Low min. operating voltage of less than 0.8V
- Ultra low min. operating current of less than 1nA
- Nano-power operation
- Wide dynamic operating current ranges
- Exponential operating current ranges
- Matched transconductance and output conductance
- Matched and tracked temperature characteristics
- Tight lot-to-lot parametric control
- Positive, zero, and negative $V_{GS(th)}$ tempco bias currents
- Low input capacitance
- Low input/output leakage currents

PIN CONFIGURATION



SCL, PCL PACKAGES

*I_C pins are internally connected, connect to V-

GENERAL DESCRIPTION (cont.)

These devices are built to offer minimum offset voltage and differential thermal response, and they can also be used for switching and amplifying applications in -0.80V to -8.0V (+/-0.40V to +/-4.0V) powered systems where low input bias current, low input capacitance, and fast switching speed are desired. These devices, exhibiting well controlled turn-off and sub-threshold characteristics, operate the same as standard enhancement mode P-Channel MOSFETs. However, the precision of the Gate Threshold Voltage enable two key additional characteristics, or operating features. First, the operating current level varies exponentially with gate bias voltage at or below the Gate Threshold Voltage (subthreshold region). Second, the circuit can be biased and operated in the subthreshold region with nA of bias current and nW of power dissipation.

For most general applications, connect the V+ pin to the most positive voltage and the V- and IC (internally-connected) pins to the most negative voltage in the system. All other pins must have voltages within these voltage limits at all times. Standard ESD protection facilities and procedures for static sensitive devices are required when handling these devices.

ABSOLUTE MAXIMUM RATINGS

Drain-Source voltage, V_{DS} ——— -8.0V
Gate-Source voltage, V_{GS} ——— -8.0V
Operating Current ——— 80mA
Power dissipation ——— 500mW
Operating temperature range SCL, PCL ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

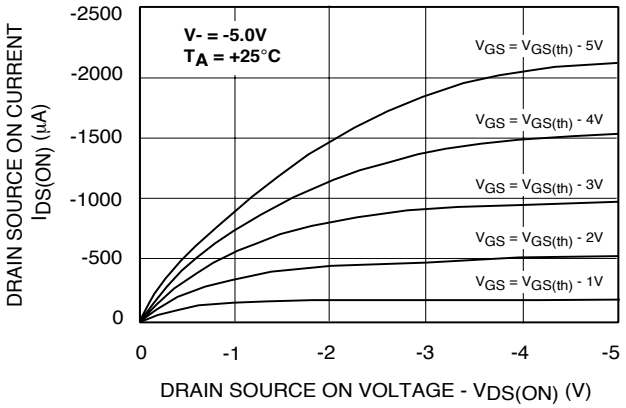
V+ = +5V V- = GND T_A = 25°C unless otherwise specified

Parameter	Symbol	ALD310708A			ALD310708			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Gate Threshold Voltage	$V_{GS(th)}$	-0.82	-0.80	-0.78	-0.82	-0.80	-0.78	V	I_{DS} = -1μA, V_{DS} = -0.1V
Offset Voltage	V_{OS}		1	5		2	20	mV	$V_{GS(th)M1}$ - $V_{GS(th)M2}$ or $V_{GS(th)M3}$ - $V_{GS(th)M4}$
Gate Threshold Temperature	$TC_{VGS(th)}$		-2			-2		mV/°C	
Drain Source On Current	$I_{DS(ON)}$		-1.65			-1.65		mA	V_{GS} = V_{DS} = -5.0V
Transconductance Current[2]	G_{FS}		570			570		μA/V	V_{GS} = V_{DS} = -5.0V
Transconductance Mismatch	ΔG_{FS}		1			1		%	V_{GS} = V_{DS} = -5.0V
Output Conductance[2]	G_{OS}		48			48		μA/V	$V_{GS(th)}$ = -4.0V, V_{DS} = -5.0V
Drain Source On Resistance	$R_{DS(ON)}$		1.25			1.25		KΩ	V_{GS} = -5.0V, V_{DS} = -0.1V
Drain Source On Resistance Mismatch	$\Delta R_{DS(ON)}$		1			1		%	
Drain Source Breakdown	BV_{DSX}	-8.0			-8.0			V	
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$			400			400	pA	
Gate Leakage Current	I_{GSS}			200			200	pA	
Input Capacitance[2]	C_{ISS}		2.5			2.5		pF	

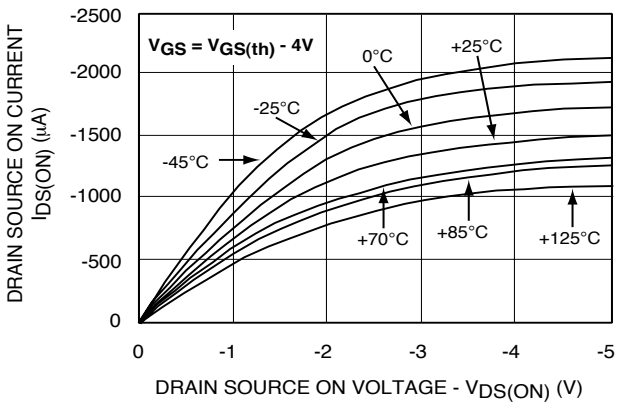
Notes: [1] Consists of junction leakage currents
[2] Sample tested parameters

TYPICAL PERFORMANCE CHARACTERISTICS

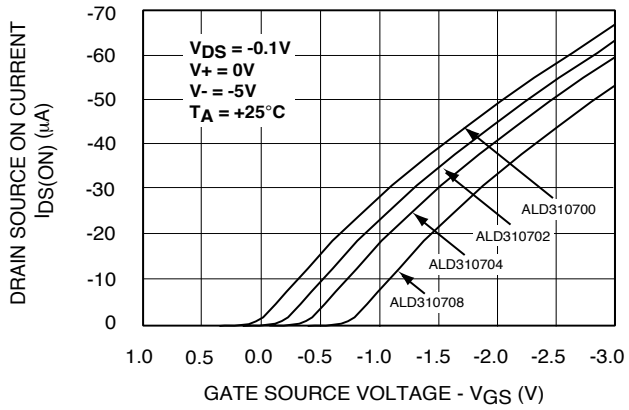
OUTPUT CHARACTERISTICS



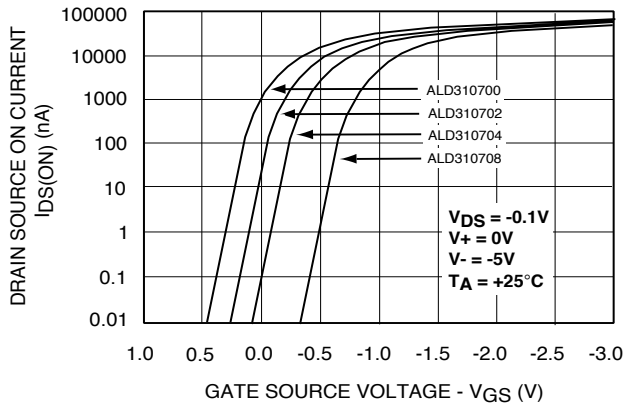
OUTPUT CHARACTERISTICS



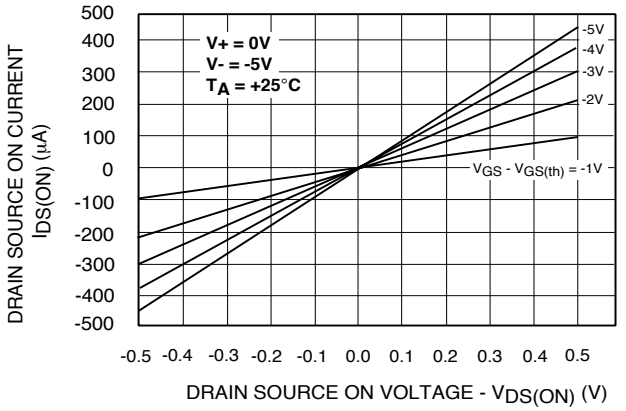
FORWARD TRANSFER CHARACTERISTICS



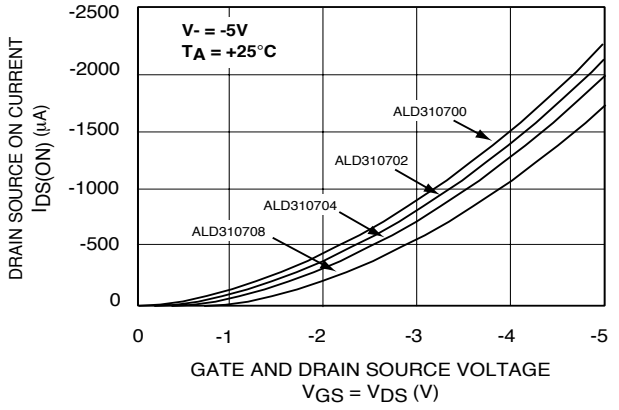
FORWARD TRANSFER CHARACTERISTICS (SUBTHRESHOLD)



LOW VOLTAGE OUTPUT CHARACTERISTICS

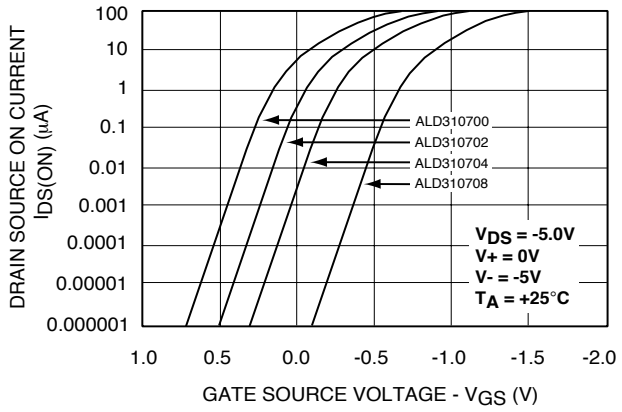


DRAIN SOURCE ON CURRENT vs. GATE AND DRAIN SOURCE VOLTAGE

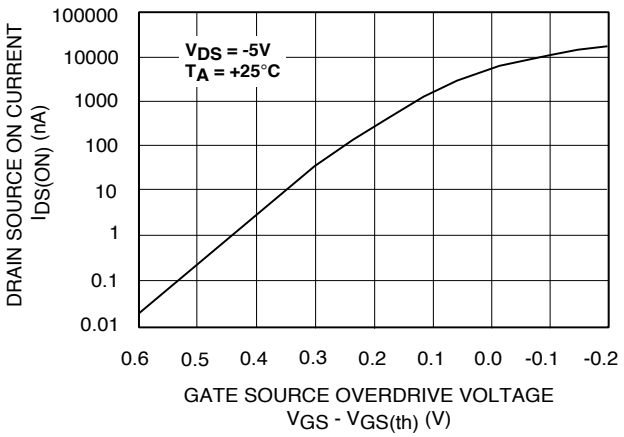


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

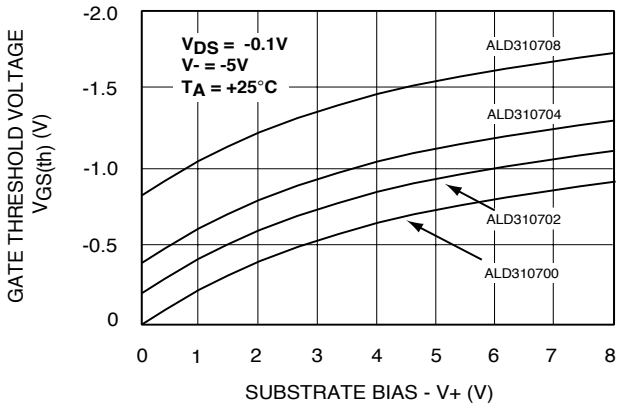
FORWARD TRANSFER CHARACTERISTICS EXPANDED (SUBTHRESHOLD)



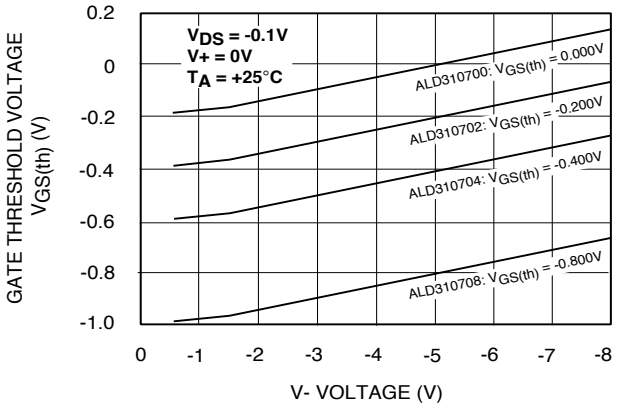
FORWARD TRANSFER CHARACTERISTICS FURTHER EXPANDED (SUBTHRESHOLD)



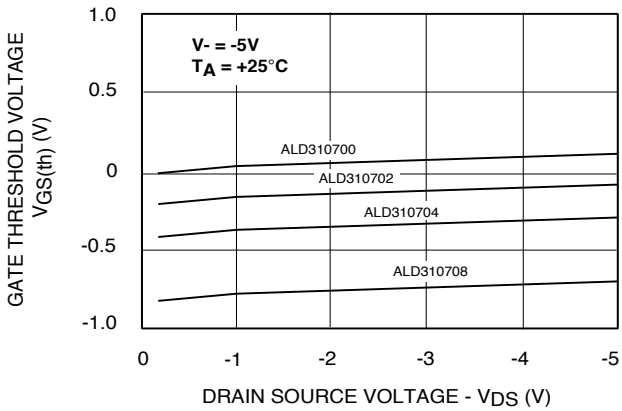
GATE THRESHOLD VOLTAGE vs. SUBSTRATE BIAS



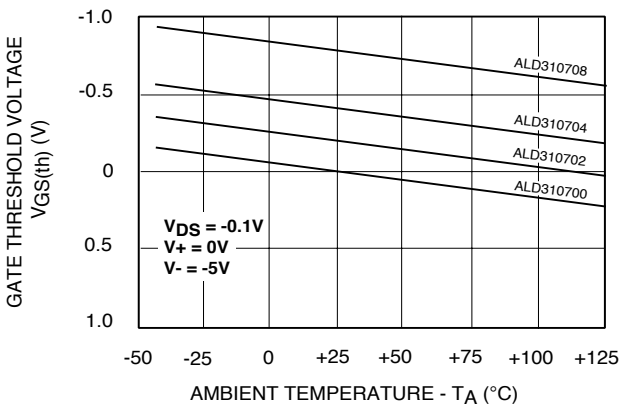
GATE THRESHOLD VOLTAGE vs. V- VOLTAGE



GATE THRESHOLD VOLTAGE vs. DRAIN SOURCE VOLTAGE

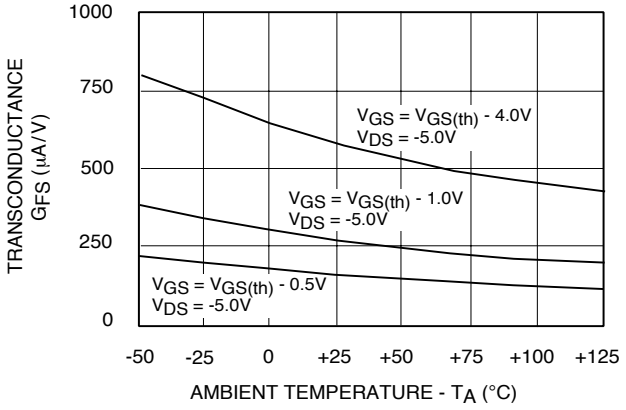


GATE THRESHOLD VOLTAGE vs. AMBIENT TEMPERATURE

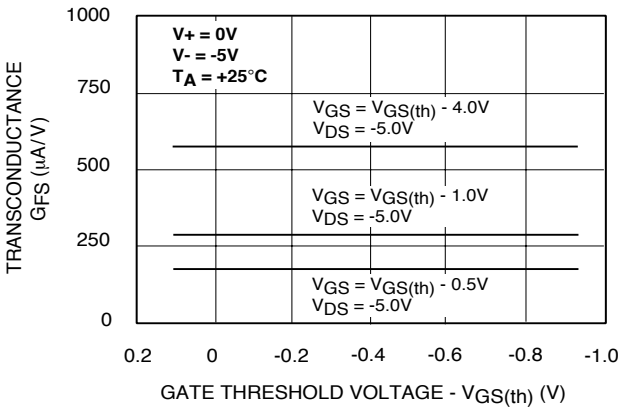


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

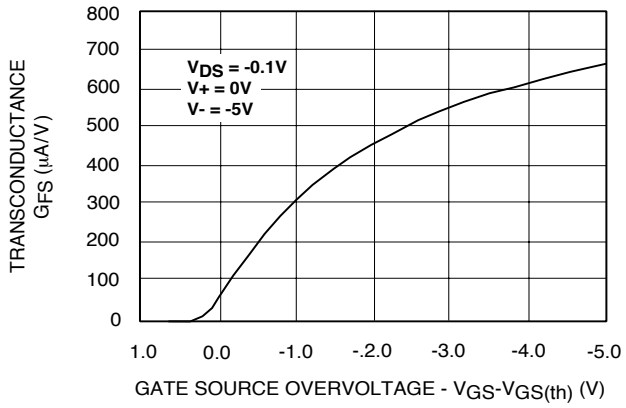
TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE



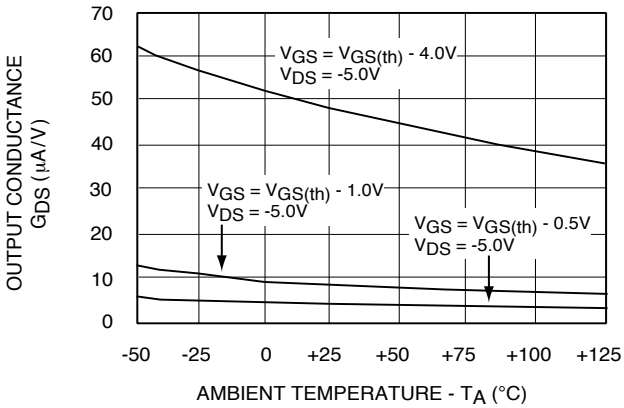
TRANSCONDUCTANCE vs. GATE THRESHOLD VOLTAGE



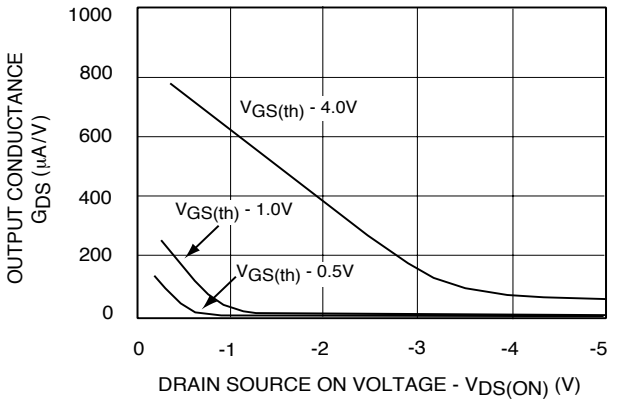
TRANSCONDUCTANCE vs. GATE SOURCE OVERVOLTAGE



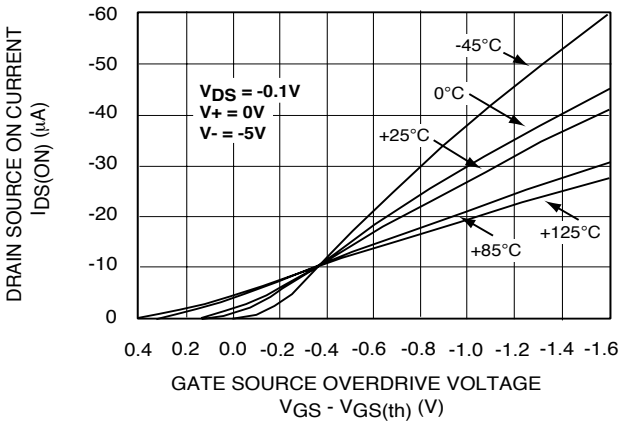
OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE



OUTPUT CONDUCTANCE vs. DRAIN SOURCE ON VOLTAGE

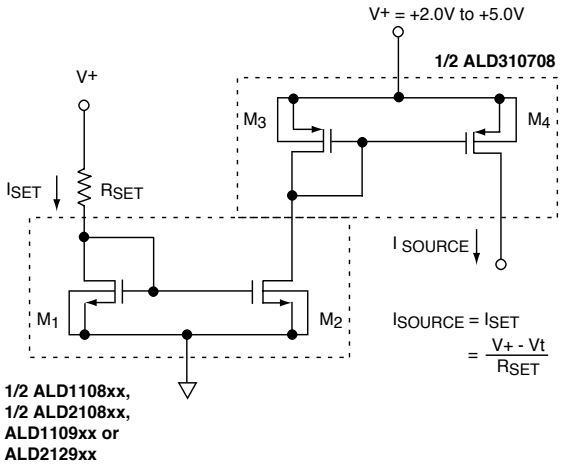


ZERO TEMPERATURE COEFFICIENT (ZTC)



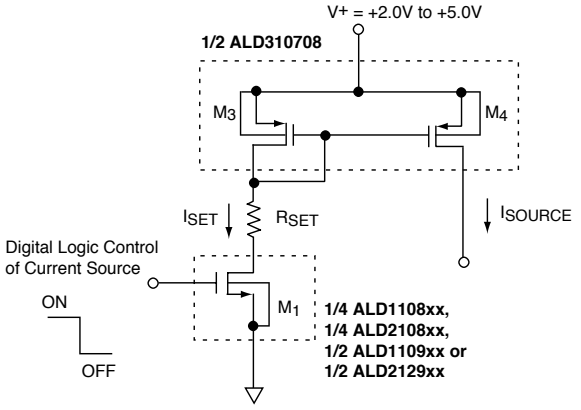
TYPICAL APPLICATIONS

LOW VOLTAGE CURRENT SOURCE MIRROR



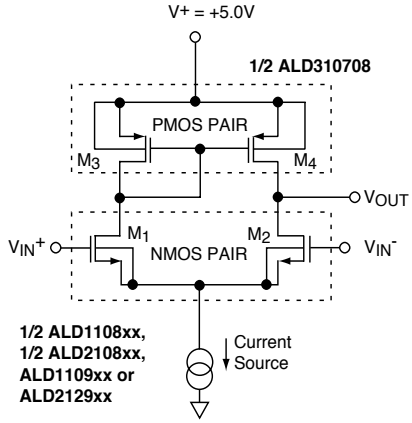
M_1, M_2: N-Channel MOSFET
M_3, M_4: P-Channel MOSFET

LOW VOLTAGE CURRENT SOURCE W/ GATE CONTROL



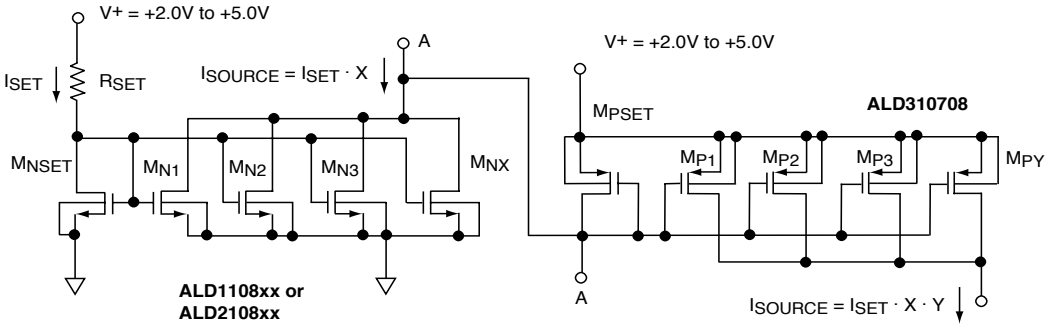
M_1 : N-Channel MOSFET
M_3, M_4: P-Channel MOSFET

LOW VOLTAGE DIFFERENTIAL AMPLIFIER



M_1, M_2: N-Channel MOSFET
M_3, M_4: P-Channel MOSFET

0.5% PRECISION LOW VOLTAGE CURRENT SOURCE MULTIPLICATION

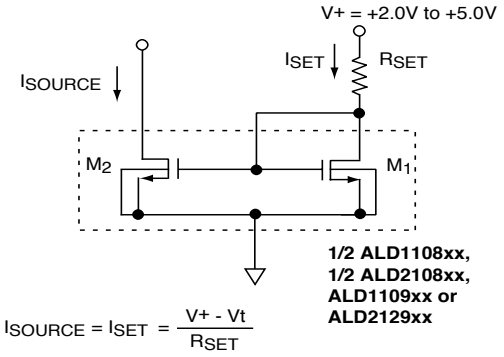


M_{NSET}: M_{N1}, M_{N2}..M_{NX}: N-Channel MOSFET

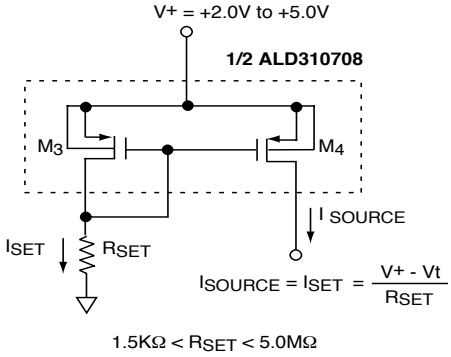
M_{PSET}: M_{P1}, M_{P2}..M_{PY}: P-Channel MOSFET

TYPICAL APPLICATIONS (cont.)

0.5% LOW VOLTAGE PRECISION CURRENT MIRRORS

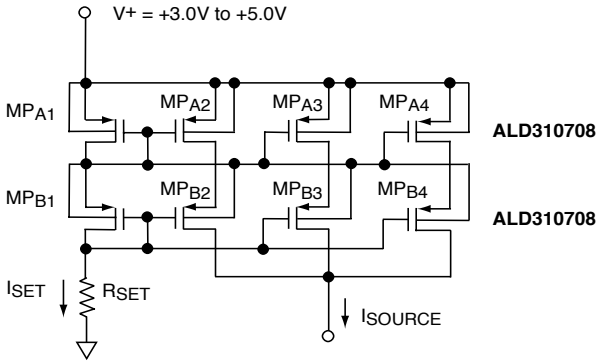


M_1, M_2: N-Channel MOSFET



M_3, M_4: P-Channel MOSFET

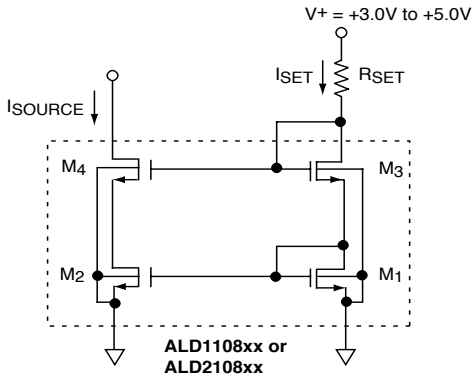
0.5% PRECISION LOW VOLTAGE CASCODE CURRENT SOURCES



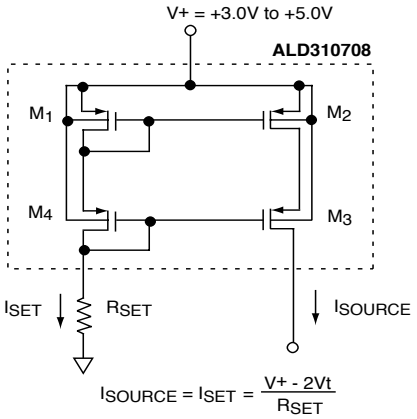
$I_{SOURCE} = 3 \cdot I_{SET} = 3\left(\frac{V+ - 2Vt}{R_{SET}}\right)$

MP_{A1}...MP_{A4}: ALD310708 P-Channel MOSFET (1st individual pkg)
MP_{B1}...MP_{B4}: ALD310708 P-Channel MOSFET (2nd individual pkg)

0.5% PRECISION LOW TEMPCO CASCODE CURRENT SOURCES



M_1, M_2, M_3, M_4: N-Channel MOSFET

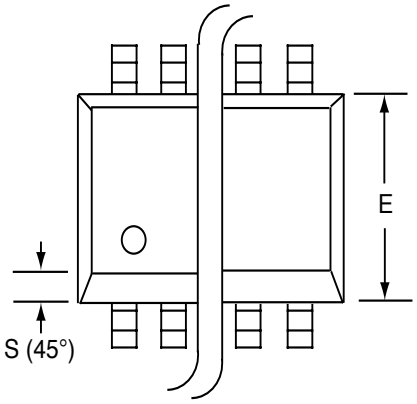


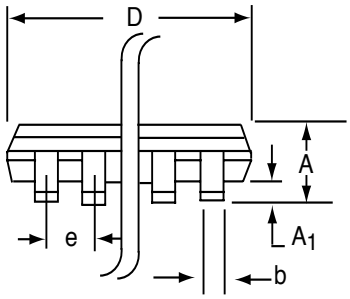
Temperature stable <= 50ppm/°C when I_{SET} = 57μA.

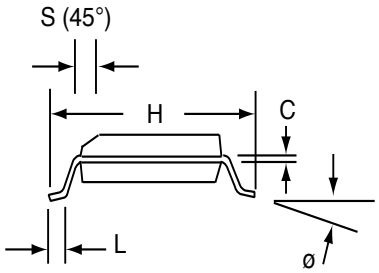
M_1, M_2, M_3, M_4: P-Channel MOSFET

SOIC-16 PACKAGE DRAWING

16 Pin Plastic SOIC Package







Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-16	9.80	10.00	0.385	0.394
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020