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AMIS-492x0

AMIS-492x0 Fieldbus MAU

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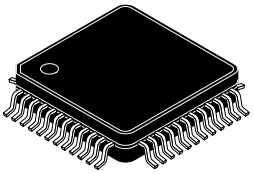
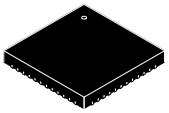


LQFP−44, 10x10
CASE 561AA



NQFP 44, 7x7
CASE 560BD

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

Overview

AMIS−492x0 Fieldbus MAU (Media Access Unit) is a transceiver chip for low speed FOUNDATION® Fieldbus and Profibus PA devices. The AMIS−49200 was originally designed to be a near pin-for-pin replacement of the Yokogawa μSAA22Q MAU. “Near pin-for-pin” means that associated component values may change, but no board changes are required. A micro-leadframe package option (NQFP) is also available, the AMIS−49250.

Features

AMIS−492x0 Fieldbus MAU is a transceiver IC for low speed FOUNDATION Fieldbus and Profibus PA devices. It incorporates the following features:

- All Node Power can be Supplied by the Bus, via the AMIS-492x0
- Current Consumption 500 μA (Typ)
- VCC Voltage: 6.2 V to 4.75 V
- VDD Voltage: 5.5 V to 2.7 V
- Compatible to IEC 1158−2 and ISA 50.02
- Shunt Regulator
- Voltage Reference (Internal Only)
- Series Regulator
- Band-pass Filter
- Slew Rate Control
- Segment Current Control
- Low Voltage Detection
- Carrier Detect
- Data Rate: 31.25 kbps Voltage Mode
- Dual Voltage Supply 3−6.2 V
- 44-pin LQFP/NQFP Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Process Automation
- Pressure and Temperature Monitoring

Definitions, Acronyms and Abbreviations

IC	− Integrated Circuit
ESD	− Electrostatic Discharge
FF	− FOUNDATION Fieldbus
LQFP	− Low Profile Quad Flat Pack
Manchester	− Communications Encoding Scheme Implemented in FOUNDATION Fieldbus
MAU	− Medium Attachment Unit
MDS	− Medium Dependent Sub-layer
NQFP	− “Near Chip-scale” Quad Flat Pack
μSAA22Q	− Name of Yokogawa’s MAU IC

Block Diagram

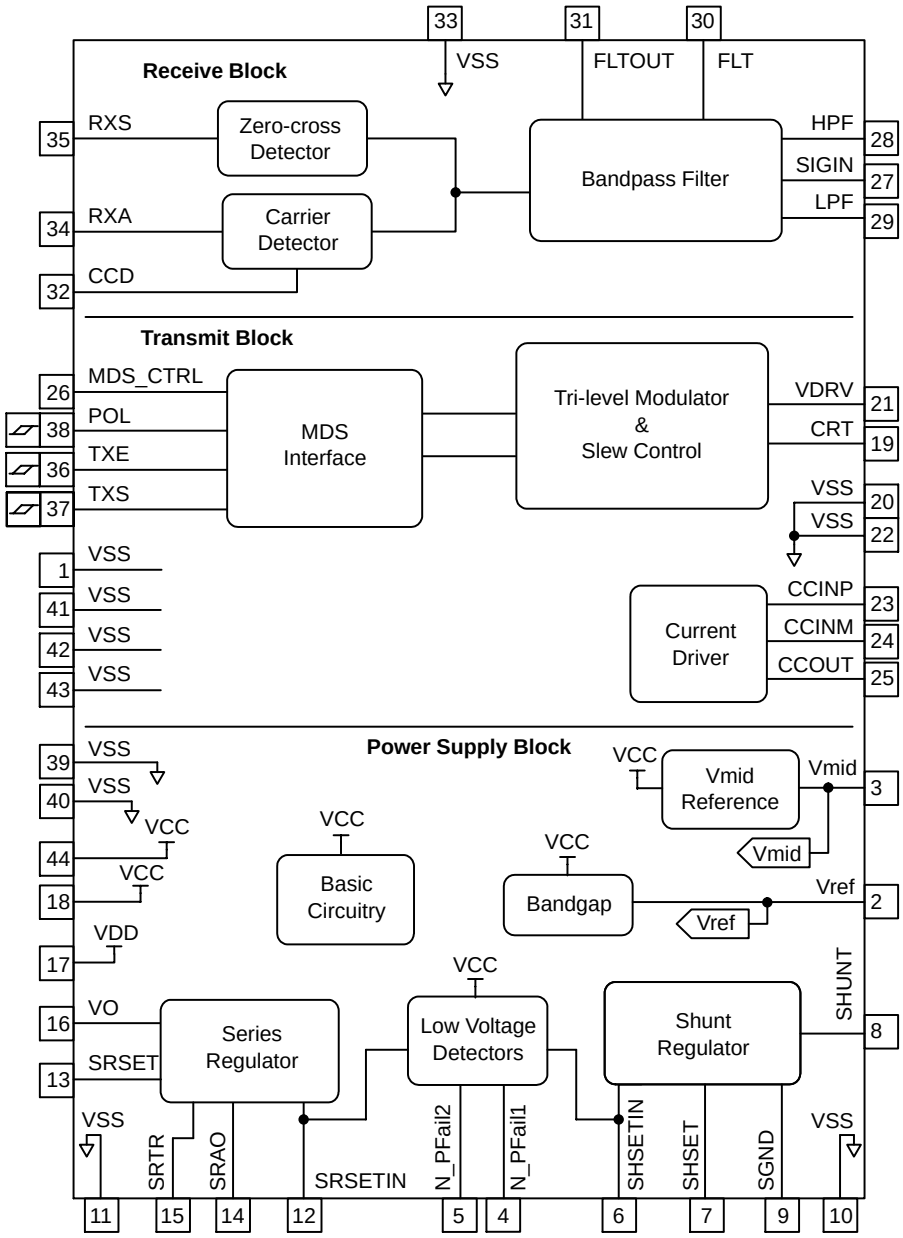


Figure 1. AMIS−492x0 Fieldbus MAU Block Diagram

Table 1. PIN NUMBERS AND SIGNAL DESCRIPTION

Signal Name	Pin No.	I/O (Note 1)	Description
VSS	1	Ground	Connect to Ground.
VREF	2	AO	Internal bandgap voltage (1.18 V).
VMID	3	AO	2 V bias voltage for AC signals.
N_PFAIL1	4	AI/O	Power fail alarm at VCC input. This pin is an open-drain output of negative logic.
N_PFAIL2	5	AI/O	Power fail alarm at VDD input. This pin is an open-drain output of negative logic.
SHSETIN	6	AI	Feedback (non-inverting) input for the shunt regulator.
SHSET	7	AO	Divided voltage of VCC input. Feeding this voltage to SHSETIN pin results in 5 V voltage at VCC.

1. AI = Analog Input, AO = Analog Output, AI/O = Analog Input/Output, DIS = CMOS Digital Input (Schmitt Trigger), DO = CMOS Digital Output.

Table 1. PIN NUMBERS AND SIGNAL DESCRIPTION (continued)

Signal Name	Pin No.	I/O (Note 1)	Description
SHUNT	8	AI	Control pin of the shunt regulator. Its sink current (25 mA max) is controlled so that the voltage at SHSETIN is equal to V_{REF} (1.18 V).
VSS/SGND	9	Ground	The Current absorbed by SHUNT pin (25 mA max) is fed to this pin, which must be connected to the ground level.
VSS	10	Ground	Ground
VSS	11	Ground	Ground
SRSETIN	12	AI	Feedback (inverting) input for the series regulator. The series regulator controls its output (SRAO) to make this input voltage is equal to V_{REF} (1.18 V).
SRSET	13	AO	Divided voltage of VO output. Feeding this voltage into SRSETIN pin results in 3 V at VO pin.
SRAO	14	AO	Output pin of an operational amplifier for the series regulator.
SRTR	15	AI	Gate of a PMOS transistor for the series regulator.
VO	16	AO	Output pin of the series regulator (20 mA max).
VDD	17	Digital Supply	Supply voltage input for digital block.
VCC	18	Analog Supply	Analog supply voltage.
CRT	19	AI/O	Current integration to limit output slew rate.
VSS	20	Ground	Ground
VDRV	21	AO	Output of an operational amplifier for slew rate control. This signal can be fed to current driver.
VSS	22	Ground	Ground
CCINP	23	AI	Non-inverting input of an operational amplifier for transmission current driver.
CCINM	24	AI	Inverting input of an operational amplifier for transmission current driver.
CCOUT	25	AO	Output of an operational amplifier for transmission current driver.
MDS_CTRL	26	AI	For POL = VDD MDS_CTRL should = VSS For POL = VSS MDS_CTRL can be tied to VDD or used as a not reset to control when transmit communications will be enabled.
SIGIN	27	AI	Input pin of the band-pass filter. This pin si connected to VMID bias level with 270 kΩ resistor.
HPF	28	AI	Feedback signal of high-pass filter. This pin si connected to the output of an op-amp for high pass filter with 75 kΩ resistor.
LPF	29	AI	Non-inverting input of an operational amplifier for the low-pass filter.
FLT	30	AI	Input pin of low-pass filter for feedback. This pin is connected to the output of the high-pass filter through 20 kΩ and the non-inverting input of the low-pass filter through 54 kΩ resisters.
FLTOUT	31	AO	Output of the operational amplifier for the low-pass filter. This signal is internally connected to non-inverting input to form a voltage-follower.
CCD	32	AO	Current integration (for carrier detect circuit).
VSS	33	Ground	Ground
RXA	34	DO	MDS−MAU interface signal for received signal activity. This pin is a push-pull output.
RXS	35	DO	MDS−MAU interface signal for received signal. This pin is a push-pull output.
TXE	36	DIS	MDS−MAU interface signal for enable signal transmission (Schmitt Trigger input).
TXS	37	DIS	MDS−MAU interface signal for signal to be transmitted (Schmitt Trigger input).
POL	38	DIS	Selects polarity of TxE input. When this pin is connected to GND, TxE is active high. When this pin is connected to VDD, TxE is active low.
VSS	39	Ground	Ground
VSS	40	Ground	Ground
VSS	41	Ground	Connect to ground.
VSS	42	Ground	Connect to ground.
VSS	43	Ground	Connect to ground.
VCC	44	Analog Supply	Analog supply voltage.

1. AI = Analog Input, AO = Analog Output, AI/O = Analog Input/Output, DIS = CMOS Digital Input (Schmitt Trigger), DO = CMOS Digital Output.

ELECTRICAL CHARACTERISTICS

Operating Conditions

Unless otherwise noted, all block and sub-block specifications apply over the operating temperature (−40 to +85°C).

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Analog Block Supply Voltage	V_{CC}		−0.3	6.5	V
Digital Block Supply Voltage	V_{DD}		−0.3	6.0	V
Digital Input Pin Voltage	V_{IN}	(TxS, TxE and POL Pins)	−0.3	V_{DD} + 0.3	V
Digital Output Pin Voltage	V_{OUT}	(RxS and RxA Pins)	−0.3	V_{DD} + 0.3	V
Input Pin Current	I_{IN}	Not for Shunt Pin	−	±5	mA
Output Pin Current	I_{OUT}	For Shunt, SGND and VO	−	30	mA
ESD, Human Body Model			−	2,250	V
ESD, Machine Model			−	250	V
ESD, Charged Device Model			−	1,000	V
Storage Temperature	$T_{Storage}$		−55	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. NORMAL OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Analog Supply Voltage	VCC	Supply voltages are configurable, or can be supplied from off-chip.	4.75	5	6.2	V
Digital Supply Voltage	VDD		2.7	3	VCC − 1.1	V
Storage Temperature	$T_{Operating}$		−40	−	85	°C
Current Consumption	ICC	25°C, SHUNT current = 1 mA, no current from series regulator.	−	500	800	μA

Table 4. CMOS INPUT SPECIFICATIONS

Parameter	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	$0.7 \times V_{DD}$	V_{DD}	V
Input Low Voltage	V_{IL}	0	$0.3 \times V_{DD}$	V
Input High Current	I_{IH}	−	1	μA
Input Low Current	I_{IL}	−	−1	μA
Schmitt Negative Threshold	V_{t-}	$0.2 \times V_{DD}$	−	V
Schmitt Positive Threshold	V_{t+}	−	$0.8 \times V_{DD}$	V
Schmitt Hysteresis	V_h	1	−	V

Power Supply Blocks

Table 5. REGULATOR SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Shunt Regulator						
Output Voltage	V_{CC}	Preset, I_{SH} = 1 to 5 mA	4.85	5.0	5.15	V
		External Setting	4.75	−	6.2	V
Sink Current	I_{SH}	Internal Pass Transistor N-ch and Pad	0.001	−	25	mA
Load Capacitance	C_{SH}		5	−	−	μF
Load Regulation		I_{SH} = 1 to 25 mA	0	1.6	4	%
Temperature Coefficient	TC_{Vcc}	No Load Capacitance	−	−	±200	ppm/°C
Series Regulator						
Input Voltage	V_{CC}	Internally Tied to V_{CC} Pin	4.75	−	6.2	V
Output Voltage	V_O	Preset, I_{SR} = 0	2.91	3.0	3.09	V
		External Setting and N-JFET	2.85	−	3.5	V
Output Current	I_{SR}	Internal Pass Transistor P-ch and Pad	−	−	20	mA
Load Capacitance	C_{SR}	For Stability use CAP w/ESR	5	−	−	μF
Load Regulation		I_{SR} = 0 to 20 mA	0	2	4	%
Temperature Coefficient	TC_{Vo}		−	±200	−	ppm/°C
Low Voltage Detectors (Applies to N_PFail1 and PFail2)						
Threshold	V_{TH9}	SxSETIN > V_{TH9} (Output: L → H)	85	90	95	% Vref
Hysteresis	V_{HYS5}	SxSETIN < (V_{TH9} − V_{HYS5}) (Output: H → L)	0.012	0.025	0.038	V
Output Sink Current	I_{OL}	V_{OL} = 0.4 V (Open Drain)	30	−	135	μA
Output Leakage Current	I_L	V_{OH} = 5 V	−	−	1	μA

Table 6. VOLTAGE REFERENCE SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bandgap Voltage Reference						
Output Voltage Tolerance	V_{REF}	Equates to: ±2%	1.157	1.185	1.205	V
Temperature Drift			−	50	−	ppm/°C
Hysteresis	V_{REFHYS}	(Note 2)	−	100	−	μV
Supply Voltage	V_{CCREF}		4.75	5	6.2	V
Load Current	I_{REFOUT}	No Load During Operation	−	−	0	μA
V_{MID} Voltage Reference						
Output Voltage	V_{MID}		1.95	2.0	2.05	V
Output Current	I_{MID}		−30	−	100	μA
Load Capacitance	C_{MID}	DVC6000F Uses 1 μF	0.01	0.1	1	μF
Temperature Coefficient	TC_{MID}		−	−	±200	ppm/°C

2. Hysteresis is defined as the change in the 25°C reading after 85°C to 25°C cycle and –40°C to 25°C cycle.

Transmitter Blocks

Table 7. MDS−MAU INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
POL Input Pin	POL	See Schmitt Trigger Input Specs			V
TxE Input Pin	TxE	See Schmitt Trigger Input Specs			V
TxS input Pin	TxS	See Schmitt Trigger Input Specs			V

NOTE: The associated MDS chip must handle the jabber detect function.

Table 8. TRI-LEVEL MODULATOR

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Tri-level Modulator and Slew Control (Output is at VDRV)						
Output Voltage	V_O		V_{MID}	−	3.02	V
Load Current	I_O	$\|\Delta V\|$ 10 mV	−35	−	+120	μA
Output for Silence (Note 3)	V_S	TXE Disabled	V_{MID} + 0.485	V_{MID} + 0.500	V_{MID} + 0.515	V
Output for High Level (Note 3)	V_H	TXE Active	V_S + 0.380	V_S + 0.400	V_S + 0.420	V
Output for Low Level (Note 3)	V_L	TXE Active	V_S − 0.420	V_S − 0.400	V_S − 0.380	V
Asymmetry of V_H and V_L	ΔV_{HL}		−0.02	−	0.02	V
Rise and Fall Times (Note 4)	tf, tr	C_{RT} = 22 pF (Note 4)	−	4.7	−	μsec

3. Nominal values are: V_S = 2.5 V, V_H = 2.9 V and V_L = 2.1 V.
4. By adding an external capacitor between the CRT pin and ground, slew rate at VDRV output can be controlled. The controlling equation is tf or tr = 2 μs + (0.123 μs/pF * C_{RT}). C_{RT} is nominally 22 pF, yielding tf = tr = 4.7 μs. The constant comes from an internal capacitor. The hot side of the capacitor and the CRT pin should have a guard pattern around them to avoid unnecessary interference.

Table 9. CURRENT CONTROL AMPLIFIER

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Common Mode Voltage Range	V_{CM}		0	−	V_{CC} − 1	V
Output Voltage Swing	V_O		1	−	V_{CC} − 0.5	V
Load Current	I_O		−2,300	−	100	μA
Input Offset Voltage	V_{OS}		−3	−	+3	mV
Slew Rate	SR	C_L = 10 pF R_L = 200 kΩ	−	0.54	−	V/μs
Gain Bandwidth Product	GBW		−	1.15	−	MHz
Phase Margin	PM		−	66	−	Deg

Receiver Block

Table 10. RECEIVER SUB-BLOCKS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Band Pass Filter						
Input Voltage	V_{BP}	SIGIN Pint to GND	1	−	4	V
Output Voltage Swing	FLTOUT		1	−	4	V
Output Slew Rate	SR		−	0.6	−	V/μs
Input Offset Voltage	V_{OS}		−	−	±5	mV
Filter Resistors (Note 5)	RF1		60	75	90	kΩ
	RF2		216	270	324	kΩ
	RF3		16	20	24	kΩ
	RF4		43	54	65	kΩ
Carrier Detector						
Threshold Voltage	V_{TH+}	Relative to V_{MID}	40	50	60	mV
	$V_{TH−}$		−60	−50	−40	mV
Output High Voltage	V_{OH}	I_{OH} = 0 mA	V_{DD} − 0.6	−	−	V
Output Low Voltage	V_{OL}	I_{OL} = 0 mA	−	−	0.3	V
Output High Current	I_{OH}	$V_{DD} - V_O \le 0.6$ V	50	−	−	μA
Output Low Current	I_{OL}	$V_O \le 0.6$ V	50	−	−	μA
Output Rising Time	t_R	C_L = 10 pF	−	0.3	−	μs
Output Leak Current	t_F	C_L = 10 pF	−	0.3	−	μs
Zero-cross Detector						
Threshold Voltage	V_{TH+}	No Carrier	V_{MID} + 0.025	V_{MID} + 0.040	V_{MID} + 0.058	V
	$V_{TH−}$	Carrier Active	V_{MID}	V_{MID}	V_{MID}	V
Output High Voltage	V_{OH}	I_{OH} = 0 mA	V_{DD} − 0.6	−	−	V
Output Low Voltage	V_{OL}	I_{OL} = 0 mA	−	−	0.3	V
Output High Current	I_{OH}	$V_{DD} - V_O \le 0.6$ V	50	−	−	μA
Output Low Current	I_{OL}	$V_O \le 0.6$ V	50	−	−	μA
Output Rising Time	t_R	C_L = 10 pF	−	0.3	−	μs
Output Leak Current	t_F	C_L = 10 pF	−	0.3	−	μs

5. The band pass filter is made up of a two pole high pass filter in series with a two pole low pass filter. The filter consists of four resistors internal to AMIS−492x0, and four external capacitors. The active part of each filter is an amplifier connected in a follower configuration.

THEORY OF OPERATION

Overview

The AMIS−492x0 incorporates two different power supply circuits. Both derive their power from the bus. Using the internal configuration, the shunt regulator is set for 5 V and the series regulator is set for 3 V. Users can modify either power supply by adding external components. The AMIS−492x0 Fieldbus can also monitor these power supply voltages and generate power-fail signals if they fall below a specified value. Please refer to the AMIS−492x0 Fieldbus MAU Reference Design Application Note for ways to adjust the shunt and series voltage regulators.

The AMIS−492x0 Fieldbus MAU transmits a Manchester-encoded signal provided from a standard MDS−MAU interface. The output driver makes it possible to design various signal circuits, which depend on the power requirements of your device. The slew rate of the signal can be controlled to minimize unnecessary radiation as specified in IEC/ISA standards.

The AMIS−492x0 Fieldbus MAU has a built-in band pass filter which makes it easy to design your own receiver. The receive block operates on a Manchester-encoded signal. It decodes the signal and verifies proper amplitude with a zero-cross and carrier detect circuit, respectively. Detected signals are then passed on to a controller with the standard MDS−MAU interface.

Power Supply Block

The power supply block contains four sub-blocks:

1. *A Shunt Regulator* − for establishing a supply voltage of V_{CC} (typ. = 5 V) used by the analog circuitry.
2. *A Series Regulator* − for establishing a supply voltage of V_{DD} (typ. = 3 V) used for digital circuitry.
3. *Two Low Voltage Detectors* − for monitoring the two supply voltages.
4. *A Bandgap Voltage Reference* − which is used internally for generating a bias level for AC signals.

Shunt Regulator

The shunt regulator controls its sink current to the SHUNT pin so that the voltage applied to the SHSETIN pin is equal to V_{REF}. The V_{CC} input is divided by an internal network to provide a voltage equal to Vref at the SHSET pin. If SHSET and SHSETIN pins are tied together, and V_{CC} and SHUNT pins are connected to a power source of high impedance (e.g., current mirror circuit of signal driver), the shunt regulator provides 5 V power to itself and external circuits. A capacitor of 5 μF or larger capacity is necessary to stabilize this regulator. Figure 11 shows C10 (22 μF) connected to Pin 8 to accomplish stabilization.

It is possible to increase the V_{CC} voltage up to 6.2 V by dividing V_{CC} with an external network to supply the appropriate voltage to SHSETIN pin. In this case, SHSET pin must be kept open. The output voltage is determined by the following equation:

$$V_{CC} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \qquad \text{(eq. 1)}$$

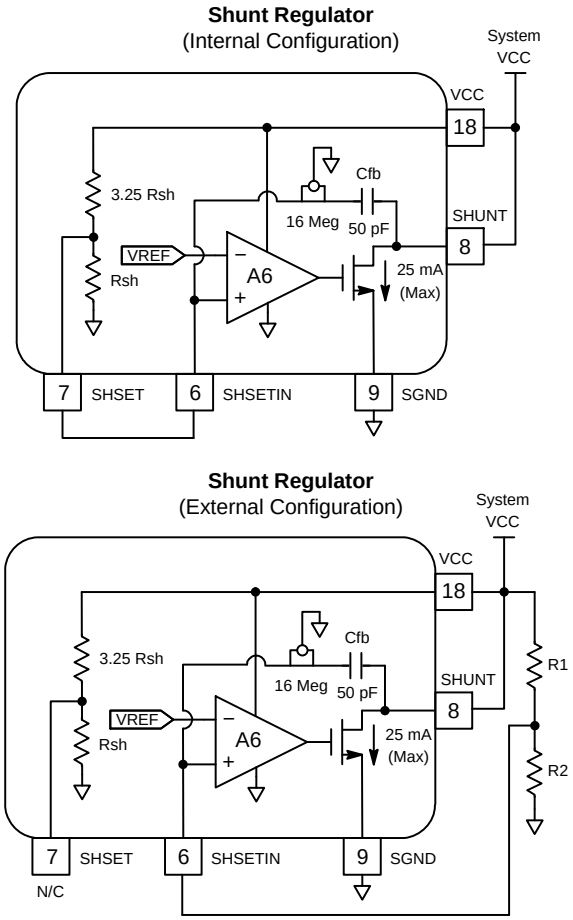


Figure 2. Shunt Regulator

The SHUNT pin is normally connected to V_{CC}. It is possible to insert a resister between V_{CC} and SHUNT to measure the shunt current. Its value should be small enough to keep V_{DS} (voltage between SHUNT pin and SGND pin) larger than 2.5 V (i.e., resistor must be less than 100 Ω).

Since the internal transistor can sink as much as 25 mA, no additional circuit is necessary in most cases. Note that the drain current must not exceed 25 mA because no protection is implemented for the internal transistor. If you do not need the shunt regulator, you should connect SHUNT and SHSETIN pins to GND and open SHSET pin. Then V_{CC} must be supplied from another source.

Series Regulator

The series regulator produces a regulated voltage at the V_O pin from V_{CC}. If you connect SRAO and SRTR pins together, the internal amplifier will regulate the input voltage at SRSETIN pin to equal V_{REF}. An internal feedback signal is generated to produce a voltage equal to V_{REF} at pin SRSET. If you connect SRSET and SRSETIN pins, the series regulator supplies 3 V at pin V_O. A capacitor (C_D in Figure 3) of 5 μF or larger capacity is necessary to stabilize this regulator. The capacitor is expected to have an ESR resistor for the circuit to be stable. If the capacitor is low, a series resistor with the cap load will help stabilize the circuit).

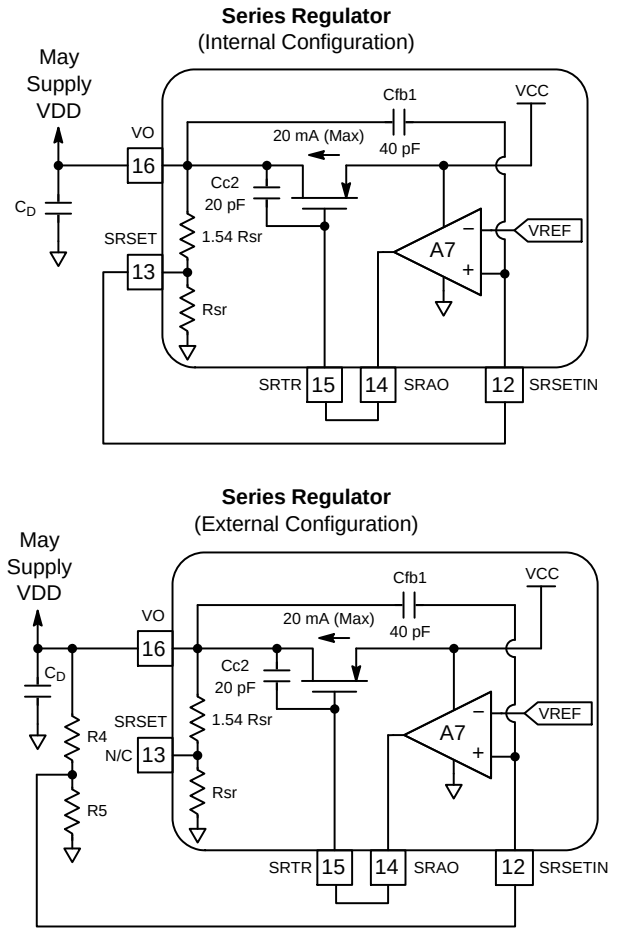


Figure 3. Series Regulator

The supply current must not exceed 20 mA because no current limiting is applied to the internal transistor. You can increase V_O voltage up to 3.5 V by dividing V_O with an external network to supply the appropriate voltage to pin SRSETIN. In this case, pin SRSET must be kept open. The drain-source voltage of the internal transistor must be larger or equal to 2 V. If this condition is not satisfied, you may need an external P-channel JFET to create the desired low voltage-drop regulator. The output voltage is determined by the following equation:

$$V_O = V_{REF} \times \left(1 + \frac{R_4}{R_5}\right) \quad \text{(eq. 2)}$$

Low Voltage Detectors

Low voltage detectors are included to monitor supply voltages and generate “power fail” signals. The low voltage alarms are detected by sensing the voltage on pins SHSETIN and SRSETIN. These pins also provide feedback for the shunt and series regulators. If the voltage on the SHSETIN pin is lower than the threshold, VTH9 (90 percent VREF), N_PFAIL1 goes low. Typically SHSETIN monitors the analog rail voltage VCC. If the voltage on the SRSETIN pin is lower than the threshold, VTH9, N_PFAIL2 goes low. Typically SRSETIN monitors the digital rail voltage VDD.

Both outputs are open drain, so a resistor will be required. If you do not use one of these pins, it should be connected to GND. You can also add capacitors to delay these signals. In this case, sink current must not exceed the maximum value.

If you do not wish to use one of the low voltage detectors its corresponding output pin should be connected to GND.

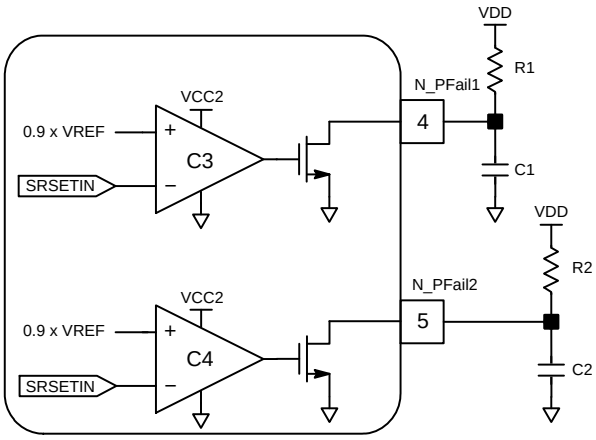


Figure 4. Low Voltage Detectors

If you do not use one of the regulators, the corresponding alarm signal can potentially be used to monitor another signal. For example, if the series regulator is not used, SRAO should be left open, SRTR tied to VCC, VO grounded and SRSET left open. Then SRSETIN can be the input for monitoring another voltage signal with N_PFAIL2.

Voltage Reference

The voltage reference circuitry generates two voltage signals, VREF and VMID. VREF comes from a bandgap circuit and is used as the reference voltage for all circuits in the AMIS−492x0 Fieldbus MAU. The typical value for VREF is 1.185 V. See Figure 5.

An operational amplifier is regulating VMID to provide a bias (common) level for the AC signals. Its typical voltage is 2 V. A capacitor larger than 0.01 μF is necessary on VMID to remove high-frequency ripple.

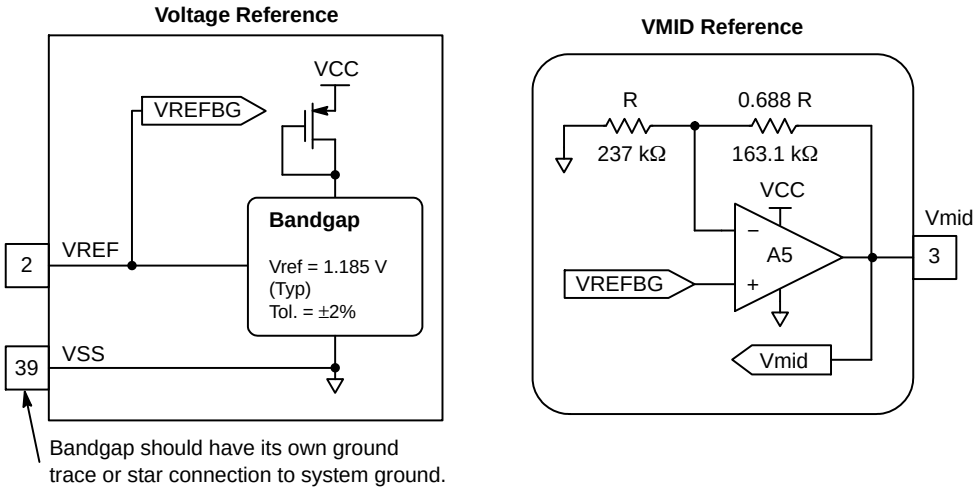


Figure 5. Bandgap and VMID Voltage Reference

Transmit Block

The transmit block contains four sub-blocks:

1. *MDS-interface* – decodes input signals to generate internal control signals.
2. *Tri-level Modulator* – generates current signals used as inputs to the slew-rate controller.
3. *Slew Rate Controller* – converts current to three distinct VDRV voltage levels (V_S, V_H, V_L).
4. *Current Drive Amplifier* – op amp designed to drive current drivers for 31.25 kbps voltage-mode medium.

MDS-interface

The MDS-interface decodes input signals to generate internal control signals. The POL pin is used to select the polarity of TxE (transmit enable). The TxE and TxS (transmit signal) are the MDS−MAU interface signals. TxS represents the manchester encoded output of the Link Layer controller, and is the input signal of the AMIS−492x0. These three signals are CMOS logic signals powered by the V_{DD} supply voltage. When POL is connected to GND, TxE is assumed to be active high (positive logic). Likewise, if POL is connected to V_{DD}, TxE is assumed to be active low (negative logic). See Table 1 on page 2, Table 11, and Figure 6 to see how MDS_CTRL Pin 26 can be used to control MDS interface operation. Table 11 shows the resulting VDRV output for the various combinations of interface signals.

Table 11. MDS-INTERFACE LOGIC

POL	TxE	TxS	VDRV
Low	Low	Low	V_S
		High	
	High	Low	V_H
		High	V_L
High	Low	Low	V_H
		High	V_L
	High	Low	V_S
		High	

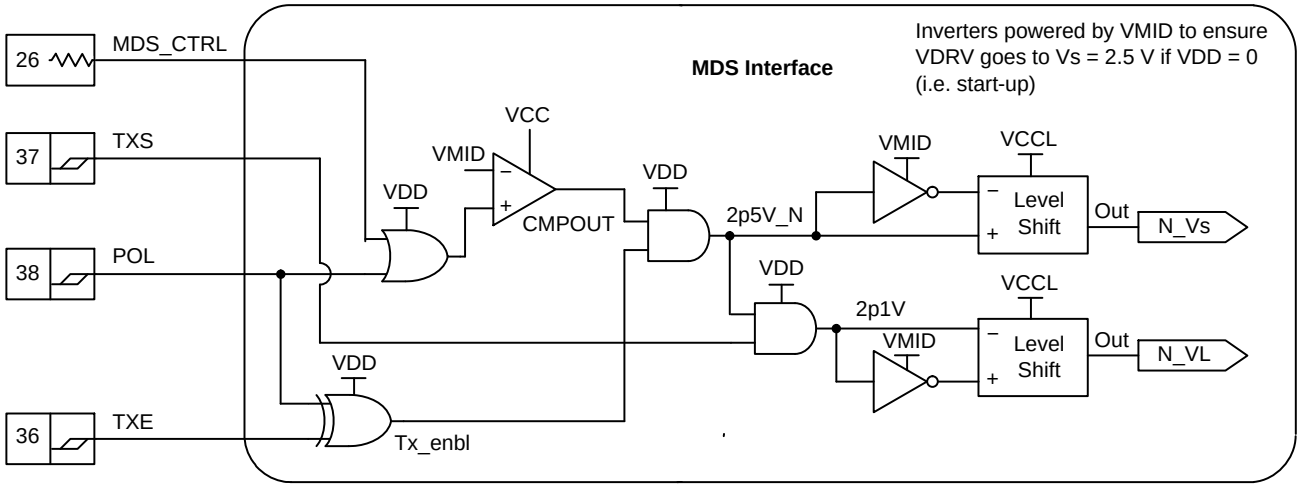


Figure 6. MDS Interface

Tri-level Modulator

The tri-level modulator switches current signals into a summing node. The slew rate controller converts the current to a voltage signal, VDRV. The DC level of silence (V_S) is nominally 2.5 V. Transmission high (V_H) is nominally 2.9 V and transmission low (V_L) is nominally 2.1 V, yielding an amplitude of 0.8 V.

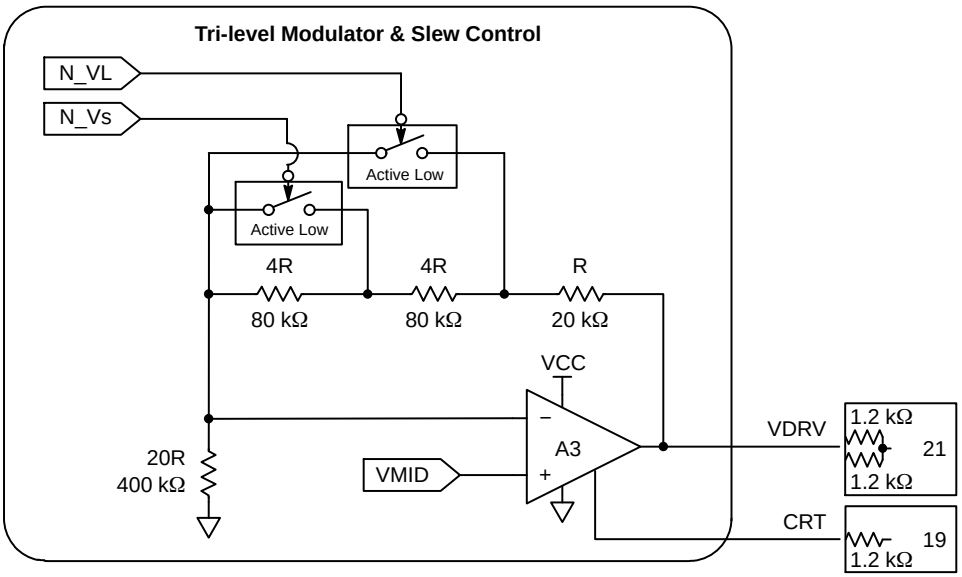


Figure 7. Tri-level Modulator

Slew Rate Controller

Amplifier (A3), shown in the above figure, controls the slew rate. The amplifier converts the current signals from the tri-level modulator to a voltage signal, VDRV. It controls its slew rate with a capacitor (C_{RT}) connected to the CRT pin. The waveform at the VDRV pin is symmetric and the fall/rise times are determined by the following equation:

$$t_F,\ t_R = 2.0[\mu s] + 0.12[\mu s/pF] \times C_{RT} \qquad \text{(eq. 3)}$$

The constant part comes from the internal capacitor (not shown). It is recommended to make a guard pattern on your circuit board around the CRT pin and the hot side of C_{RT} to avoid unnecessary interference.

Current Drive Amplifier

The drive amplifier is an operational amplifier optimized to drive current drivers for 31.25 kbps voltage-mode medium. Its input and output signals are exposed to allow flexible design of the external driver. Note that this amplifier cannot directly sink the necessary current from the medium. In the following drive circuit the current (I_{BUS}) through the current-detect resister (R_F) is determined by the following equation.

$$I_{bus} = \frac{\left[R_3 V_{mid}\left(R_{12} + R_{11}\right)\right] - \left[V_{DRV}\left(R_2 R_{11} + R_3 R_{11}\right)\right]}{-\left[R_F\left(R_2 R_{12} + R_3 R_{12}\right)\right]} \qquad \text{(eq. 4)}$$

A diode and/or a resistor connected to the emitter are necessary to shift the DC level of CCOUT and to suppress the loop gain. The resistance value depends on your design (overall gain and emitter current).

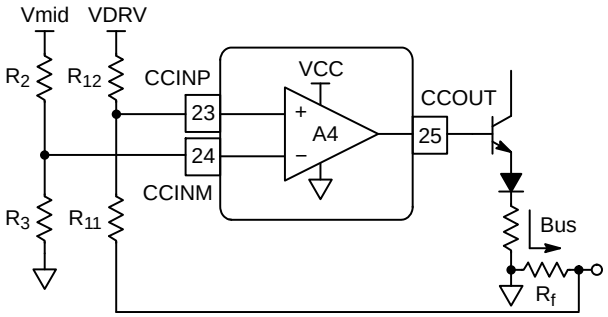


Figure 8. Current Control Circuit

Receive Block

The receive block contains three sub-blocks, which are internally connected:

1. *A Band Pass Filter* – to filter the desired incoming communication signal.
2. *Carrier Detector* – generates the RxA signal by detecting the signal amplitude.
3. *Zero-cross Detector* generates the RxS signal by detecting the high/low transitions of the Manchester code.

Band Pass Filter

The band pass filter is a series connection of a high-pass and a low-pass filters each having two poles. Each filter is comprised of a voltage follower and on chip resisters, so only four external capacitors are necessary. The following figure shows an internal circuit and the connection of external capacitors. Cut-off frequency, f_L, of the high-pass

filter is determined by C_1 and C_2 while cut-off frequency, f_H, of the low-pass filter is determined by C_3 and C_4.

$$f_L = \frac{1}{2\pi}\sqrt{\frac{1}{R_{F1} \times R_{F2} \times C_1 \times C_2}}$$

$$Q_L = \frac{1}{2}\sqrt{\frac{R_{F2}}{R_{F1}}} = 0.95 \quad \text{(eq. 5)}$$

$$f_H = \frac{1}{2\pi}\sqrt{\frac{1}{R_{F3} \times R_{F4} \times C_3 \times C_4}}$$

$$Q_L = 0.44 \times \sqrt{\frac{C_3}{C_4}} = 0.95 \quad \text{(eq. 6)}$$

The possible ranges of f_L and f_H are 1 kHz ~ 10 kHz and 10 kHz ~ 100 kHz, respectively. The values in the following figure are recommended to obtain 1 kHz and 47.6 kHz cut-off frequencies.

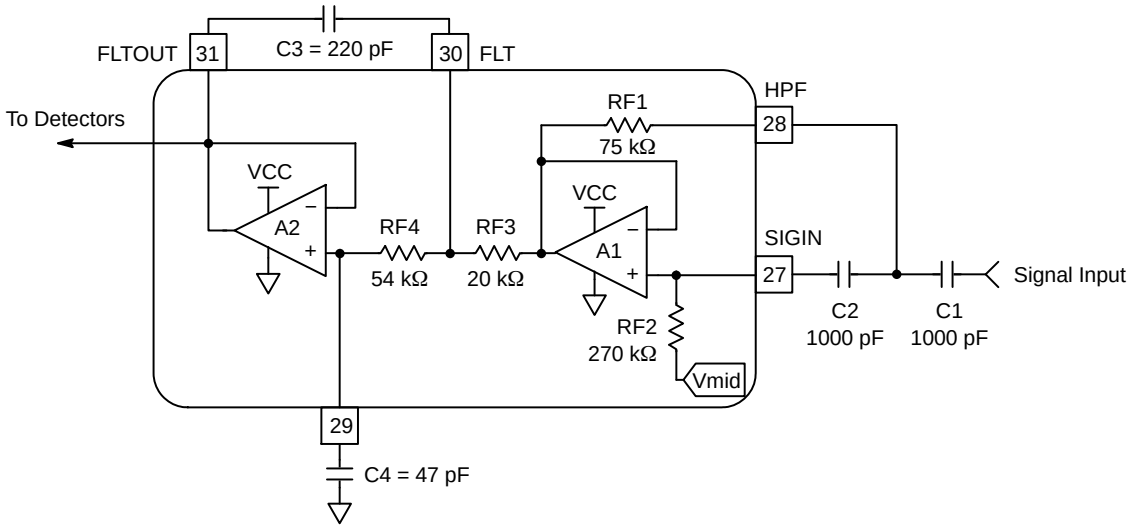


Figure 9. Band Pass Filter

Receive Signal Detection

The carrier detector generates the receive activity (RxA) signal by detecting the input signal amplitude. Minimum amplitude is 100 mVp-p (TYP). A delay, determined by the capacitor connected between the CCD pin and GND, is added to avoid detection of transient noise. The recommended value of C_{CD} is 120 pF. The output can drive a CMOS input of V_{DD} supply voltage.

The zero-cross detector generates the receive signal (RxS) with minimum phase error (jitter) by detecting the transition between high and low levels of the incoming Manchester code. Hysteresis of +40 mV (TYP) is applied to avoid unnecessary switching by noise. Once the carrier-detect goes active the hysteresis is removed and the switching point threshold is set to Vmid. The output can drive a CMOS input of V_{DD} supply voltage. RxS represents the received output of the AMIS−492x0, and is the input signal for the Link Layer controller, which will decode the manchester encoded signal.

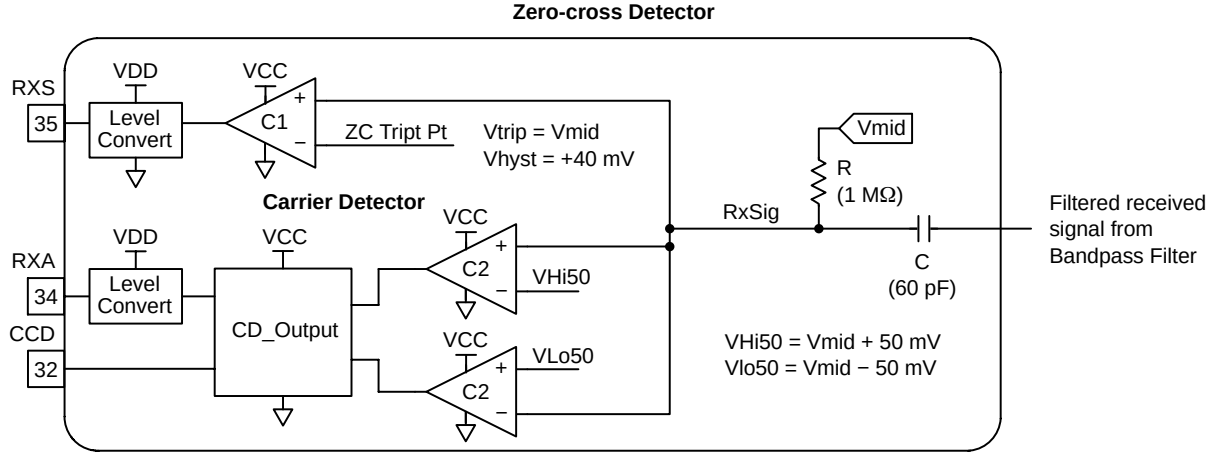


Figure 10. Receive Signal Detectors

AMIS−49200 AS REPLACEMENT FOR YOKOGAWA μSAA22Q

The AMIS−49200 is a near pin-for-pin compatible replacement for the Yokogawa μSAA22Q Fieldbus MAU. There are some differences between the two chips both in the internal operation, the required external connections and the value (or existence) of some of the external components. These differences are small and those who used the μSAA22Q would most likely be able to use the AMIS−49200 in designs with only some component value changes.

Functional Differences between the μSAA22Q and the AMIS−492x0

Jabber Inhibit

The AMIS−492x0 does not implement the Jabber Inhibit function in the μSAA22Q. Typically the AMIS−492x0 will be connected with a link controller chip such as the UFC100−F1 from Aniotek/Softing. This link controller has a Jabber Inhibit function so the absence of this function in the AMIS−492x0 should not be a problem.

As can be seen in Table 12, MDS_CTRL is only connected to ground if POL is connected to VDD. See Table 1 for a detailed description of the interaction between MDS_CTRL and POL.

In Table 12, the μSAA22Q recommends that the JAB/ signal (Pin 39) be connected to ground if the signal is not used. On AMIS−492x0, Pin 39 must be connected to ground.

Low Power Mode

The low power mode on the μSAA22Q allows the user to have a quiescent current draw of less than 10 mA yet still communicate at the proper IEC 61158−2 signal levels. Very few, if any, Fieldbus devices are capable of operating at such a low current level so this capability was not included in the AMIS−492x0.

The pins affected by this are 41, 42 and 43. If the low power mode is not being used on the μSAA22Q, these three pins are grounded. On the AMIS−492x0 it is required that these pins be grounded.

Pin Differences between the μSAA22Q and the AMIS−492x0

Pin differences are shown in Table 12.

Table 12. PIN CONNECTION DIFFERENCES BETWEEN THE μSAA22Q AND THE AMIS−492x0

	μSAA22Q		AMIS−492x0	
Pin No.	Signal Name	Recommended Connection	Signal Name	Required Connection
1	NC	Ground	VSS	Ground
11	NC	Ground	VSS	Ground
22	NC	Ground	VSS	Ground
26	NC	Ground	MDS_CTRL	Ground*
33	NC	Ground	VSS	Ground
39	JAB/	Ground if Not Used	VSS	Ground
41	CJB	1 μF cap	VSS	Ground
42	VTX	Ground	VSS	Ground
43	VSL	Ground	VSS	Ground

*MDS_CTRL is only connected to ground if POL is connected to VDD. See Table 1 for a detailed description of the interaction between MDS_CTRL and POL.

External Circuitry

Figure 11 shows the external circuitry required to connect the AMIS−492x0 to an IEC 61158−2 conformant network. This schematic is the circuit that was used to pass the FOUNDATION Fieldbus Physical Layer Conformance test as specified in FOUNDATION Fieldbus specification FF830, Rev 1.5. This circuit is similar but not identical to the circuit recommended by Yokogawa for the μSAA22Q.

Table 13 lists the four external component values that need to be changed with using the AMIS−492x0 in a circuit that previously used the μSAA22Q.

Table 13. PASSIVE EXTERNAL COMPONENT VALUE DIFFERENCES BETWEEN THE μSAA22Q AND THE AMIS−492x0

Component	μSAA22Q Value	AMIS−492x0 Value
C1	100 pF	150 pF
C3	100 pF	47 pF
C4	470 pF	220 pF
C8	10 nF	1 μF

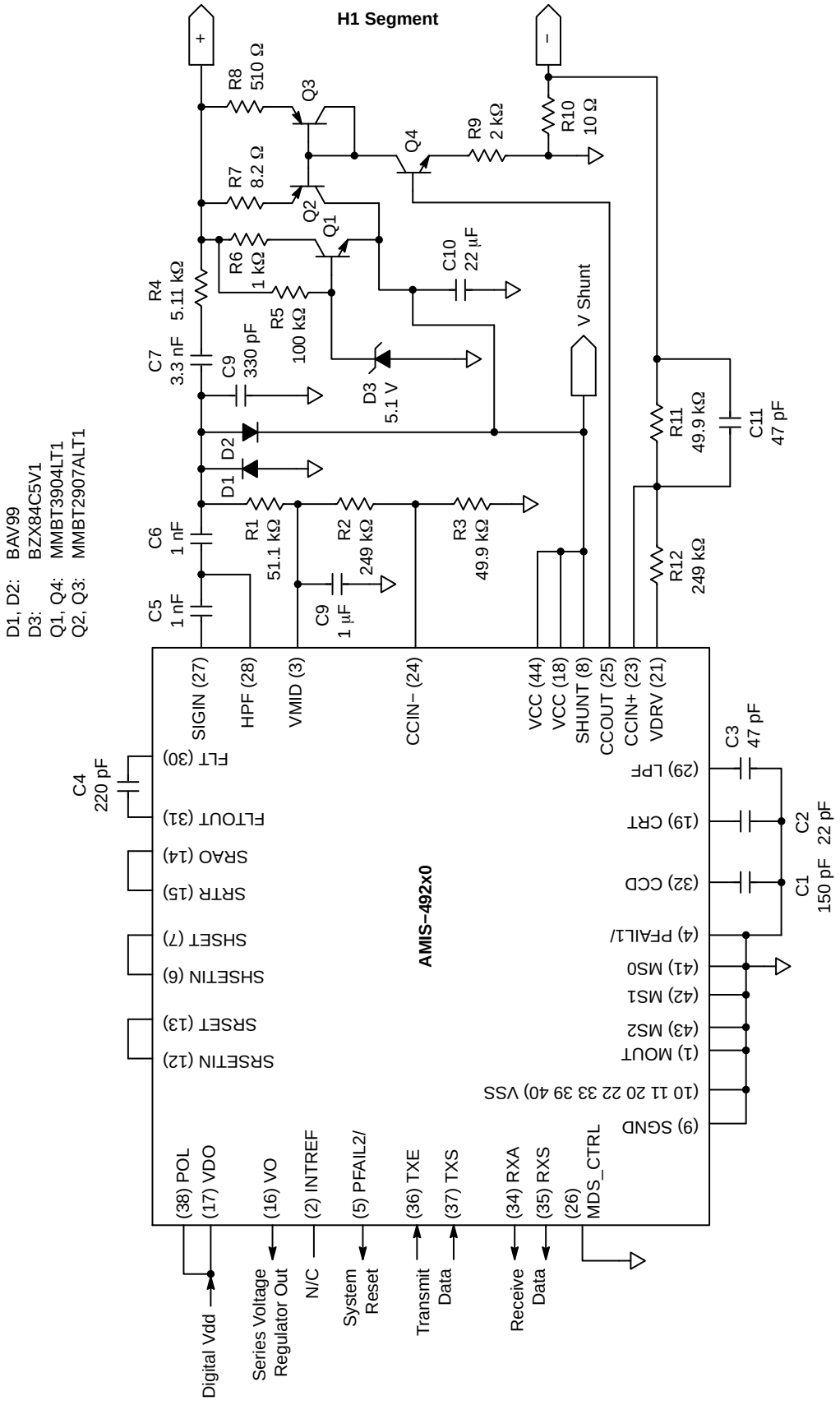


Figure 11. AMIS−492x0 Reference Circuit Implementation

C1 connects to signal CCD (Pin 32) and controls the carrier detect assert and drop-out timing. Particular implementations may require that the value of C1 be changed to accommodate received signal level changes introduced by the addition of intrinsic safety components added to the external circuitry. C3 and C4 are part of the receive filter and determine the band pass characteristics of the receive filter. It is unlikely that these would need to be changed. C8 is a noise filter for VMID. It is important that VMID have as little noise as possible as it is used as a reference for many sub-circuits in the AMIS−492x0. C8 must be a large capacitor with maximum of 100 nF. C8 recommended value is 1 μF.

There is one other minor difference in the recommended external circuitry between the μSAA22Q and the AMIS−492x0. Figure 12 shows the start-up circuits recommended for the μSAA22Q and the AMIS−492x0. The circuit shown for the AMIS−492x0 is different from that shown for the μSAA22Q but either one will work. Both are current sources that turn on when power is applied to the H1 segment terminals so that the AMIS−492x0 can turn on without any turn-on transients on the network.

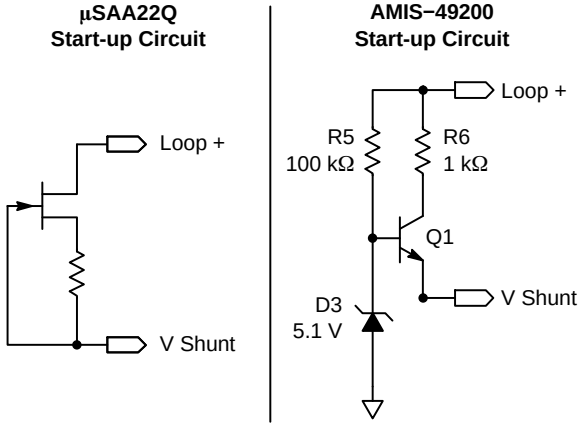


Figure 12. Recommended Start-up Circuits

Active Components

Transistors Q1–Q4 are ordinary small signal transistors. Diodes D1 and D2 are similarly ordinary small signal diodes. Users desiring to replace a μSAA22Q with the AMIS−49200 in an existing design should be able to use whatever transistors and diodes were used with the μSAA22Q. For new designs, the specified transistors can be used or other devices may be chosen.

Alternative Designs

Some users of the Yokogawa μSAA22Q did not use the exact recommended external circuit for the media interface circuit (see Figure 11). Using the AMIS−492x0 without the Yokogawa recommended external circuit may result in some compatibility problems. There are many alternative designs and it is beyond the scope of this document to identify all possible configurations and their associated design implications. Please refer to the AMIS−492x0 Fieldbus MAU Reference Design Application Note for a recommended, FOUNDATION Fieldbus certifiable board design.

Verification

All designs using the AMIS−492x0 should re-run the entire physical layer conformance test as defined in FOUNDATION Fieldbus document FF−830, FOUNDATION® Specification 31.25 kbit/s Physical Layer Conformance Test. Board layout can alter the behavior of all circuit implementations, even designs that follow the recommended implementation.

Table 14. ORDERING INFORMATION

Part Number	Package	Temperature Range	Shipping†
AMIS−49200−XTD	44 LQFP 10 × 10 mm (Pb−Free/RoHS Compliant)	−40°C to 85°C	160 / Tray
AMIS−49200−XTP	44 LQFP 10 × 10 mm (Pb−Free/RoHS Compliant)	−40°C to 85°C	1,500 / Tape & Reel
AMIS−49250−XTD	44 NQFP 7 × 7 mm (Pb−Free/RoHS Compliant)	−40°C to 85°C	160 / Tray
AMIS−49250−XTP	44 NQFP 7 × 7 mm (Pb−Free/RoHS Compliant)	−40°C to 85°C	1,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

APPENDIX − MANCHESTER ENCODING

All Fieldbus devices transmit the data onto the media as a Manchester-encoded baseband signal. With Manchester encoding, zeros and ones are represented by transitions that occur in the middle of the bit period (see below). For FOUNDATION Fieldbus H1 and Profibus PA, the nominal bit time is 32 μsec, with the transition occurring at 16 μsec. The Manchester encoding rules have been extended to include two additional symbols, non-data plus (N+) and non-data minus (N−). The symbol encoding rules are shown in Figure 13.

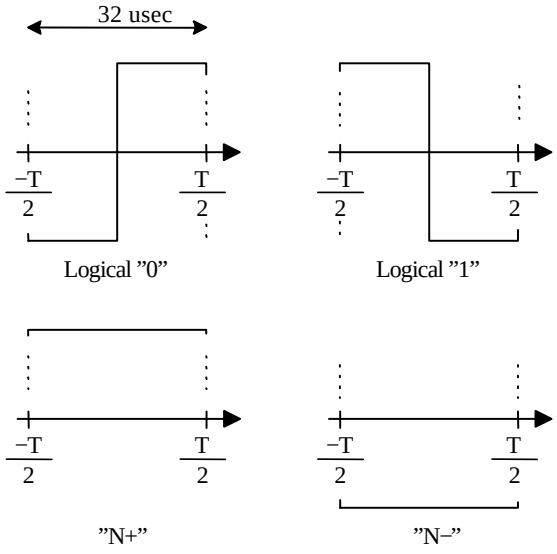
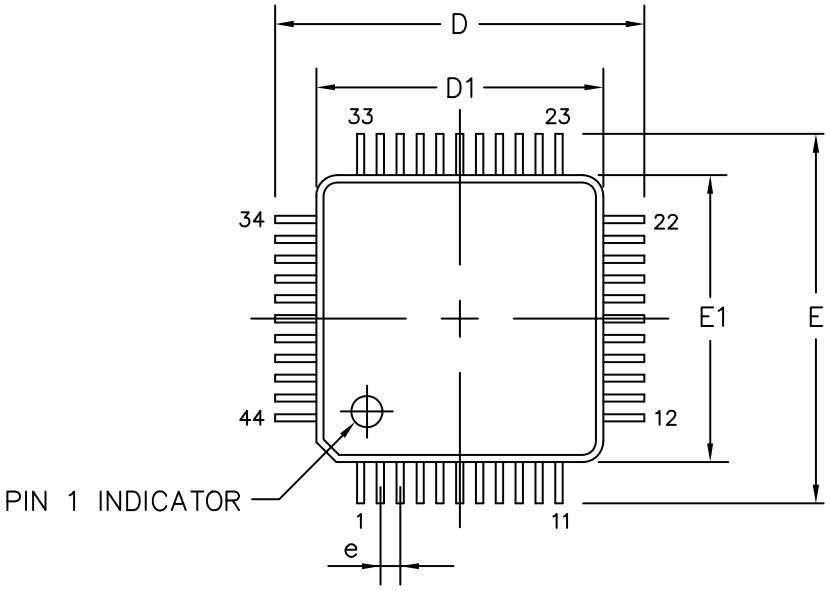


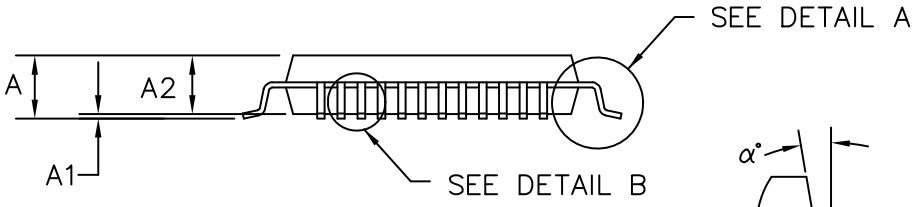
Figure 13. Manchester Encoding

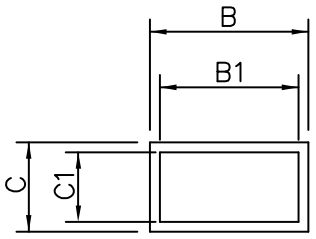
PACKAGE DIMENSIONS

LQFP−44, 10x10
CASE 561AA
ISSUE O

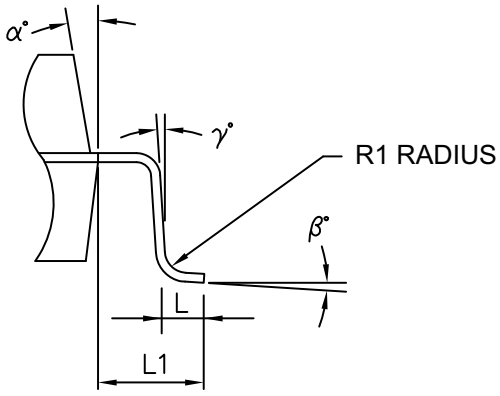


SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–





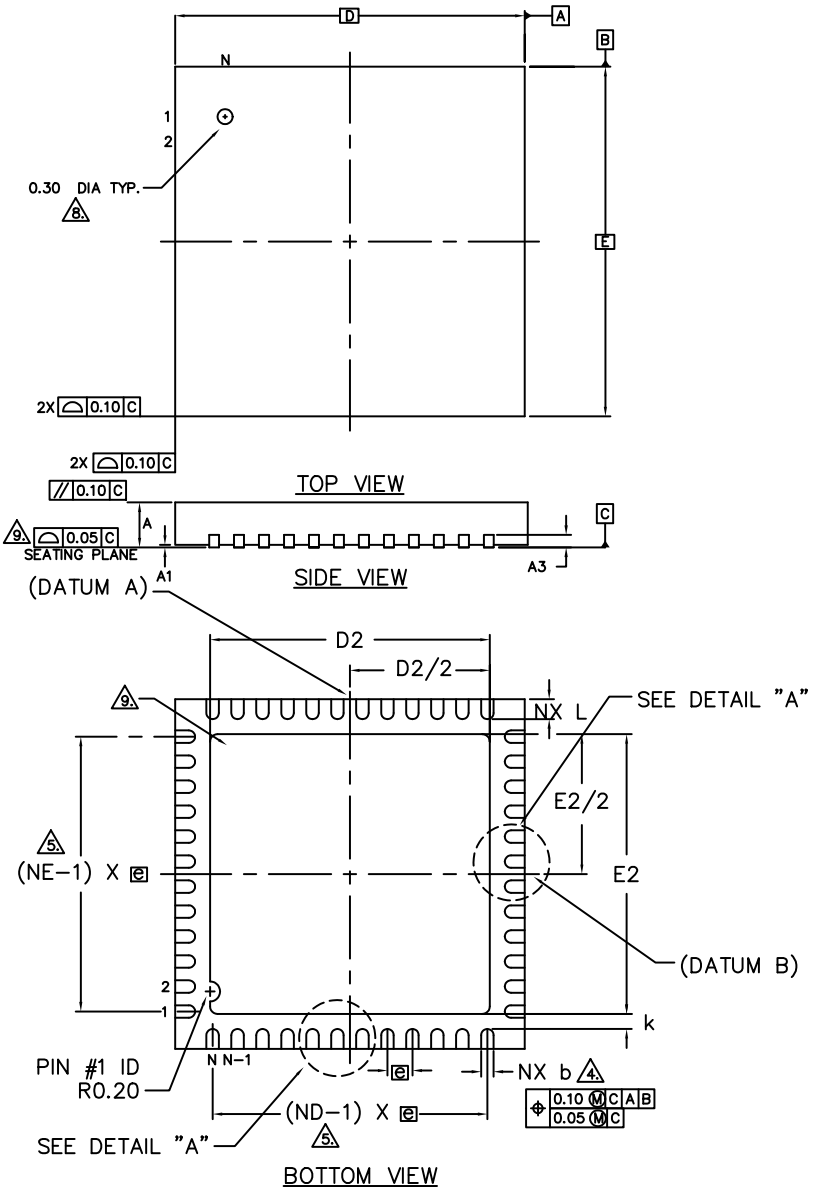
DETAIL B



DETAIL A

PACKAGE DIMENSIONS

NQFP 44, 7x7
CASE 560BD
ISSUE A
(1/2)



NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. − 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, O IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO−220
11. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L1) MAYBE PRESENT
12. PULLBACK DESIGN OPTIONS IS FOR 0.50mm NOMINAL LANDLENGTH ONLY

PACKAGE DIMENSIONS

NQFP 44, 7x7
CASE 560BD
ISSUE A
(2/2)

SYMBOL	0.80mm LEAD PITCH VARIATION A* MIN.	NOM.	MAX.	NOTE
e	0.80 BSC.			
N	28			3
ND	7			5
NE	7			5
L	0.55	0.60	0.65	4
b	0.25	0.30	0.35	4
D2	5.00	5.10	5.20	
E2	5.00	5.10	5.20	

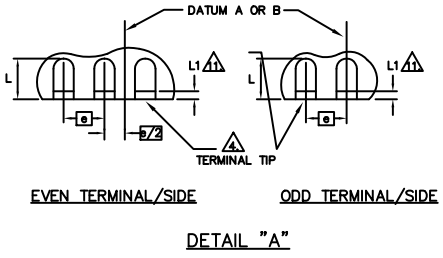
SYMBOL	0.65mm LEAD PITCH VARIATION A MIN.	NOM.	MAX.	NOTE
e	0.65 BSC.			
N	32			3
ND	8			5
NE	8			5
L	0.45	0.50	0.55	4
b	0.25	0.30	0.35	4
D2	5.00	5.10	5.20	
E2	5.00	5.10	5.20	

SYMBOL	0.50mm LEAD PITCH VARIATION A MIN.	NOM.	MAX.	VARIATION B MIN.	NOM.	MAX.	VARIATION C MIN.	NOM.	MAX.	VARIATION D MIN.	NOM.	MAX.	NOTE
e	0.50 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			
N	44			44			44			44			3
ND	11			11			11			11			5
NE	11			11			11			11			5
L	0.45	0.50	0.55	0.55	0.60	0.65	0.55	0.60	0.65	0.55	0.60	0.65	4
b	0.18	0.25	0.30	0.18	0.25	0.30	0.18	0.25	0.30	0.18	0.25	0.30	4
D2	4.60	4.70	4.80	3.20	3.30	3.40	4.60	4.70	4.80	5.00	5.10	5.20	
E2	4.60	4.70	4.80	3.20	3.30	3.40	4.60	4.70	4.80	5.00	5.10	5.20	

SYMBOL	0.50mm LEAD PITCH VARIATION E MIN.	NOM.	MAX.	VARIATION F MIN.	NOM.	MAX.	VARIATION G MIN.	NOM.	MAX.	VARIATION H MIN.	NOM.	MAX.	NOTE
e	0.50 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			
N	48			48			48			48			3
ND	12			12			12			12			5
NE	12			12			12			12			5
L	0.35	0.40	0.45	0.35	0.40	0.45	0.45	0.50	0.55	0.45	0.50	0.55	4
b	0.18	0.25	0.30	0.18	0.25	0.30	0.18	0.25	0.30	0.18	0.25	0.30	4
D2	5.50	5.60	5.70	5.00	5.10	5.20	5.30	5.40	5.50	5.00	5.10	5.20	
E2	5.50	5.60	5.70	5.00	5.10	5.20	5.30	5.40	5.50	5.00	5.10	5.20	

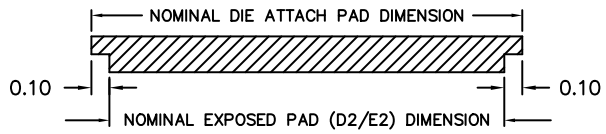
SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3	0.20 REF.			
θ	0	—	12	2
K	0.20 MIN.			
D	7.0 BSC			
E	7.0 BSC			
L1	0.15 mm MAX			1

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A3	0.20 REF.			
θ	0	—	12	2
K	0.20 MIN.			
D	7.0 BSC			
E	7.0 BSC			
L1	0.15 mm MAX			1



DETAIL "A"

GENERAL ; NOMINAL EXPOSED PAD DIMENSION = NOMINAL DIE ATTACH PAD DIMENSION−0.20



<DIE ATTACH PAD X−SECTION VIEW>

1. ALL DIMENSIONS ARE IN MILLIMETERS.