

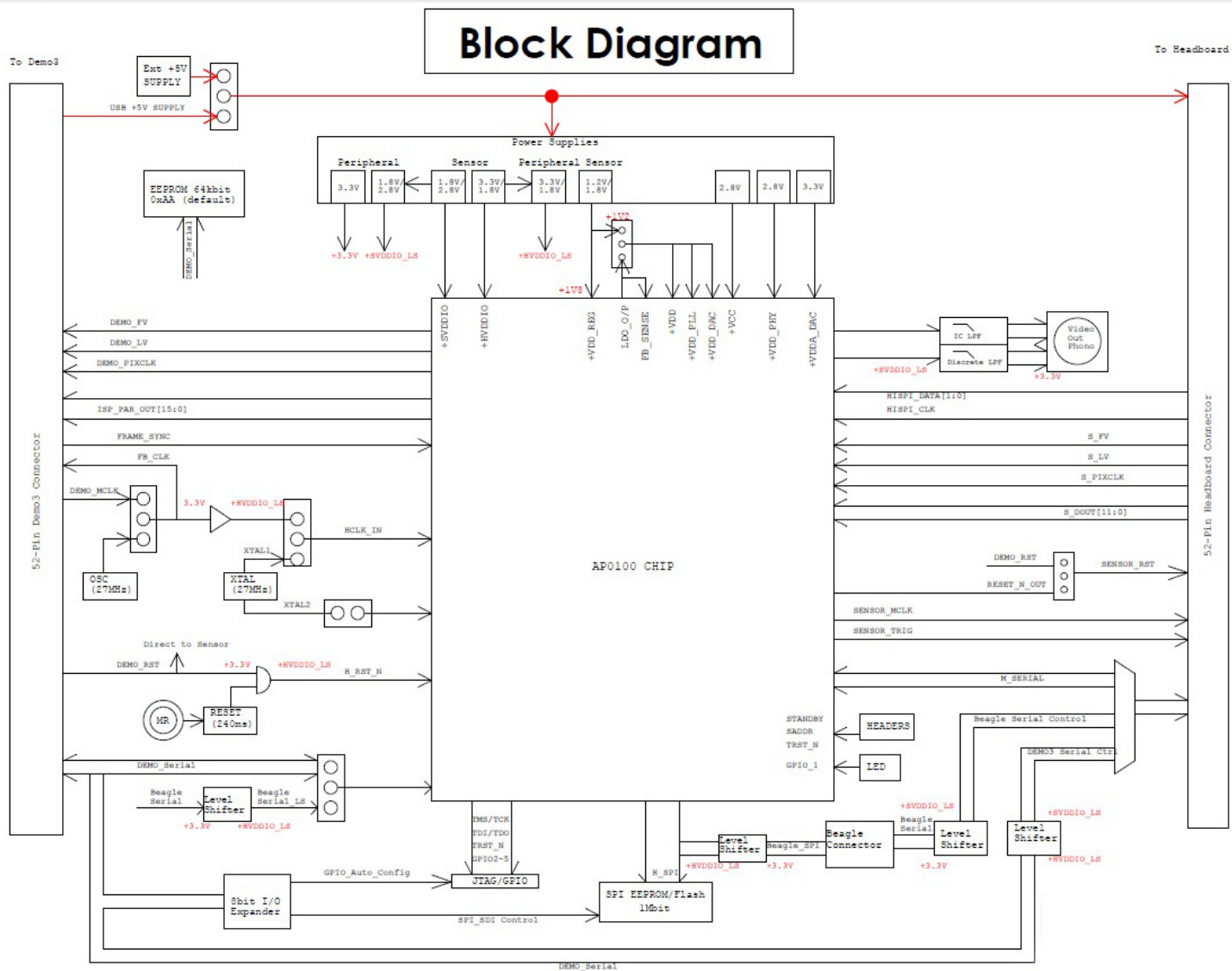


## Schematic for the AP0100AT2L00XUGAH3-GEVB Evaluation Board

# AP0100 100BGA HB DEMO3 Card

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| Rev     | Who    | Date                     | Description   |
|---------|--------|--------------------------|---|
| Rev 0.0 | aralex | 05/29/2014               | Base Schematic for Custom Design  |
| Rev 0.1 | aralex | 06/23/2014               | implemented review comments after online review<br>changed the reference designators in this schematic to align with those of the AP0101 board for ease of layout |
|         | aralex | 08/12/2014               | deleted P4, P39 headers in order to use 1.2V internal regulator of ISP<br>schematic cleanup   |
| Rev 0.2 | aralex | 08/21/2014<br>08/24/2014 | changed R44, R45, R46, R47, R53, R54, R60, R61, R62, R63, R69, R70 pkg from 0803 to 0402<br>Added R98, R67, R95, TP18, TP19                                       |
| Rev 0.3 | aralex | 08/25/2014               | Deleted R92 being redundant. modified connectivity of R91   |
| Rev 0.4 | aralex | 08/26/2014               | Changed TP13-15, TP18-19 from thru hole to SMT<br>Deleted headers P39, P41, P5 and P8 to consolidate the 4 nets to one new 4 X 2 header, P52                      |

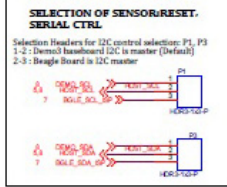
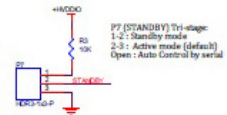
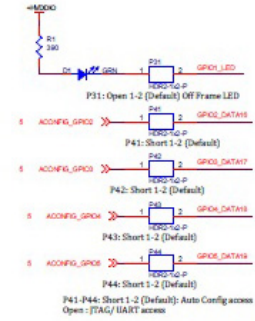
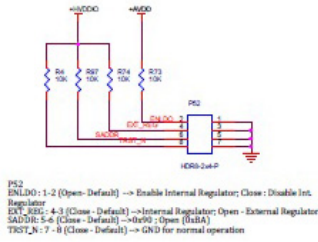




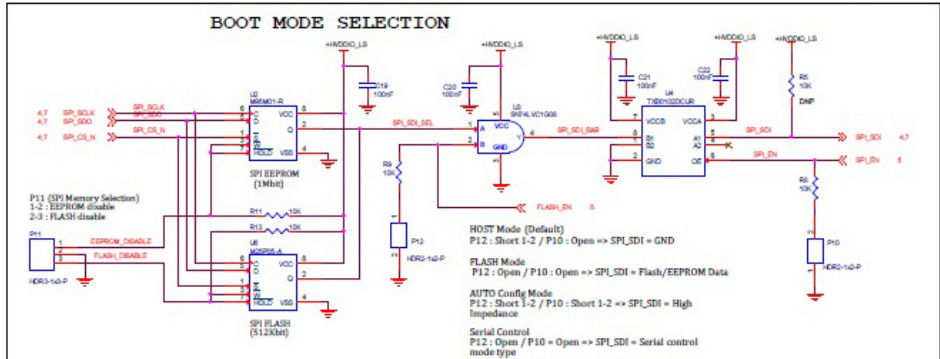
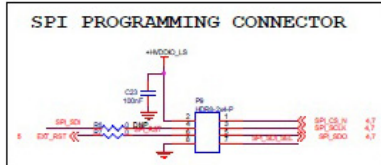
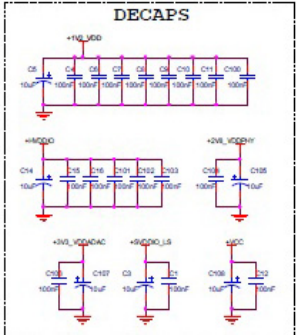
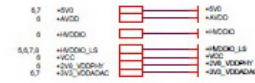
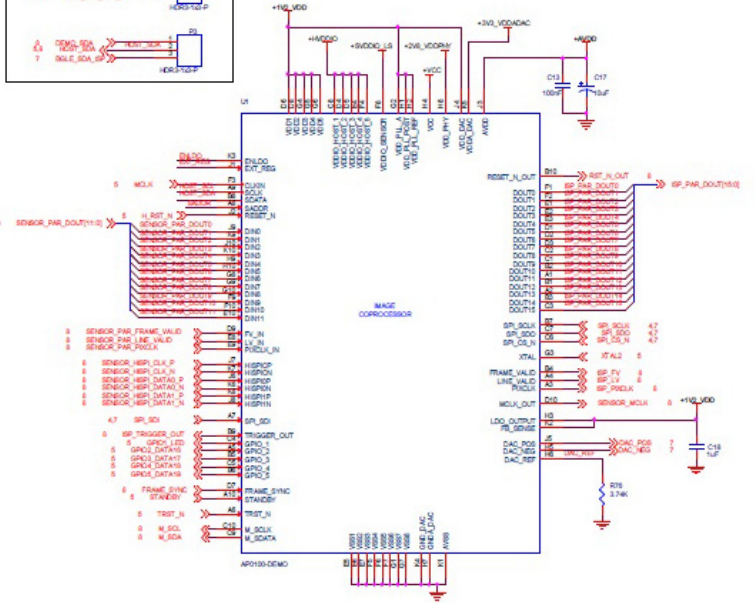
# PINOUT

|   | 1          | 2          | 3          | 4          | 5          | 6          | 7          | 8           | 9       | 10          |
|---|------------|------------|------------|------------|------------|------------|------------|-------------|---------|-------------|
| A | 00U11      | 00U13      | 00U14      | LAC_HOLD   | 0P0_2      | TRST_A     | ST_SEI     | USDR        | SCN     | ST400FF     |
| B | 00U75      | 00U76      | 00U74      | FRAME_HOLD | 0P0_3      | 0P0_5      | 0P_LCLK    | 00ATA       | 0P0_0   | RESET_A_OUT |
| C | 00U78      | 00U79      | 00U75      | 0P0_1      | 0P0_4      | 0P_LCLKA   | 0P_SE0     | 000L_RESET  | 00ATA   | 000L        |
| D | 00U75      | 00U78      | 00U77      | 000L_RESET | 000L_RESET | VS0        | FRAMC_SYNC | VS0         | TV_IN   | 000L_OUT    |
| E | 00U75      | 00U73      | 00U74      | 000L_RESET | VS0        | VS0        | VS0        | LV_IN       | 000L_IN | 00U11       |
| F | 00U75      | 00U77      | 00U78      | 000L_RESET | VS0        | VS0        | VS0        | 000L_SENSOR | 00U75   | 00U76       |
| G | VS0        | 000L_RESET | 00U74      | VS0        | VS0        | VS0        | VS0        | 00U75       | 00U77   | 00U76       |
| H | 000L_RESET | 000L_RESET | 000L_RESET | VS0        | 000L_RESET | 000L_RESET | 000L_RESET | 000L_RESET  | 00U74   | 00U75       |
| J | 000L_RESET | 000L_RESET | 000L_RESET | VS0        | 000L_RESET | 000L_RESET | 000L_RESET | 000L_RESET  | 00U75   | 00U76       |
| K | 000L_RESET | 000L_RESET | 000L_RESET | VS0        | 000L_RESET | 000L_RESET | 000L_RESET | 000L_RESET  | 00U75   | 00U76       |

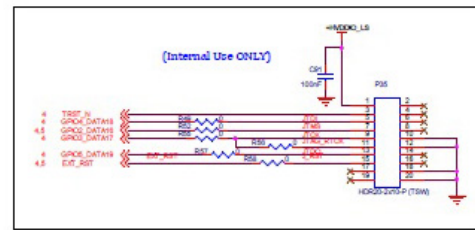
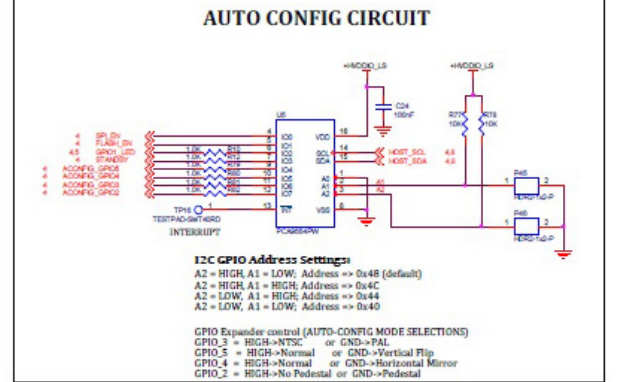
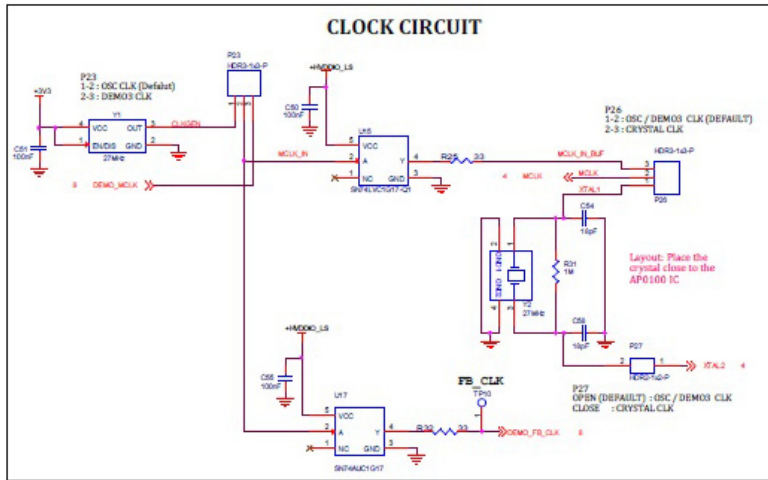
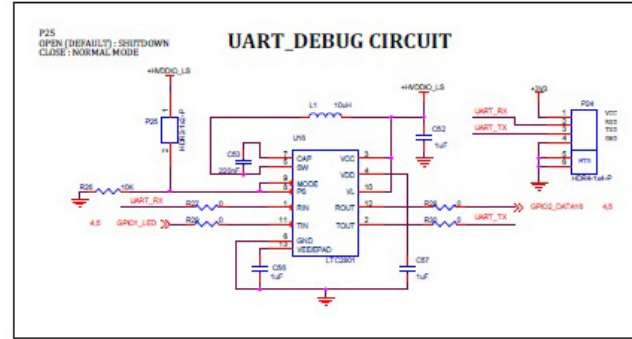
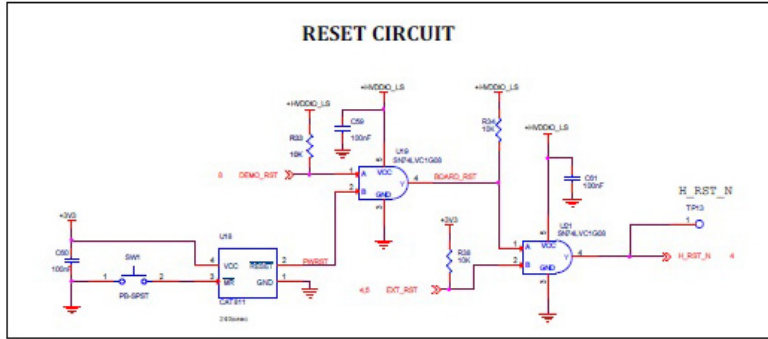
Layout Note: Place all headers on the board edges



**AP0100 IC**


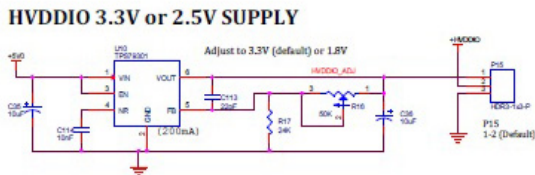
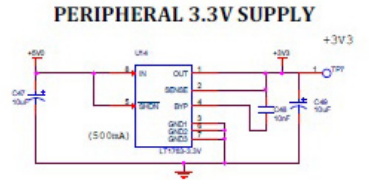
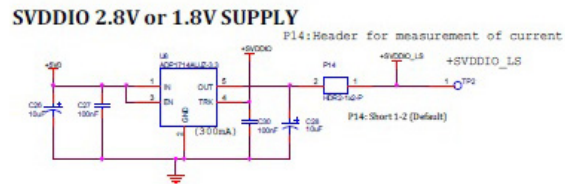
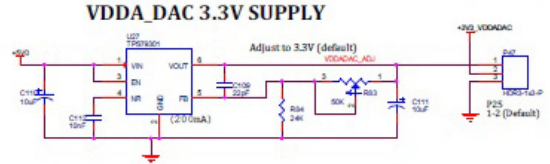
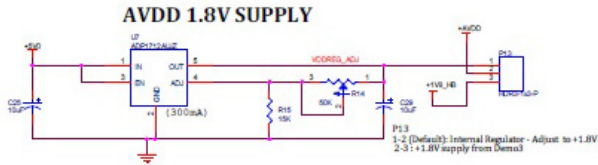


### Clock\_Reset\_UART\_Auto config

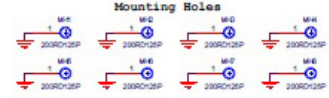
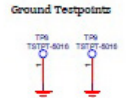
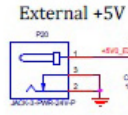
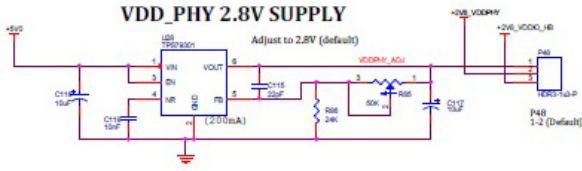
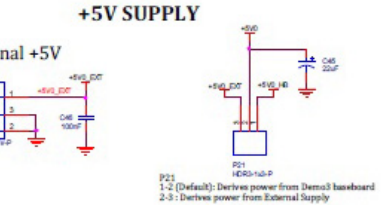
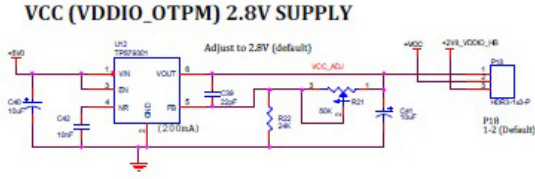
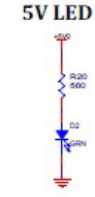


# Power

|         |               |
|---------|---------------|
| 7       | +5V           |
| 4       | +AVDD         |
| 8       | +AVDDIO       |
| 4       | +AVDDIO       |
| 8       | +AVDDIO       |
| 5.7     | +5V           |
| 4.7.3   | +AVDDIO_LS    |
| 4.5.7.1 | +AVDDIO_LS    |
| 4       | +VCC          |
| 4       | +2V1_VDDIO_HB |
| 4.7     | +3V1_VDDIOAC  |

Layout: Mount LED on bottom side of PCB



# BEAGLE Interface / Video Out

