**DIODES INCORPORATED**

**Lead-free Green**

**AP3981B**

## PRIMARY SIDE REGULATED POWER SWITCHER

## Description

The AP3981B is a high performance power switcher integrated with a primary side regulation controller and an N-channel power MOSFET. It can be used for battery charger and adaptor applications, accurate Constant Voltage (CV) and Constant Current (CC) can be achieved without an opto-coupler and secondary control circuitry.

The AP3981B operates in Pulse Frequency Modulation (PFM) mode and peak current Amplitude Modulation (AM) mode to form a fine tune frequency curve within the whole power range. Therefore, the AP3981B can achieve high average efficiency and improve audible noise.

The AP3981B provides comprehensive protections without additional circuitry. It contains $V_{CC}$ over voltage protection, output over voltage protection, output under voltage protection, output short circuit protection, cycle-by-cycle current limit, open loop protection, and internal OTP, etc.
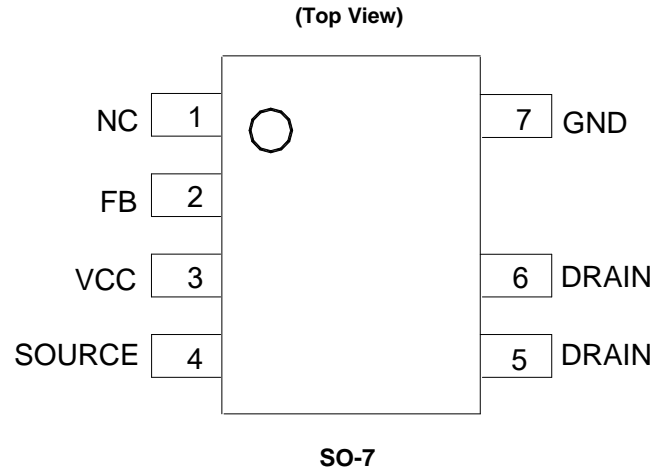
The AP3981B is available in SO-7 package.

## Pin Assignments

**(Top View)**

| | | |
|---|---|---|
| NC | 1 | 7 GND |
| FB | 2 | |
| VCC | 3 | 6 DRAIN |
| SOURCE | 4 | 5 DRAIN |

**SO-7**

## Features

- Primary-Side Control for Eliminating Opto-Coupler
- Built-In 650V Power MOSFET
- 75mW No-Load Input Power
- Flyback Topology in DCM Operation
- External Adjustable Line Compensation for CC
- Fixed Internal Cable Compensation
- Multiple Segment AM/PFM Control Mode to Improve Audio Noise and Efficiency
- Frequency Jitter to Improve System EMI
- Capacitive Load Start-Up Capability
- Valley-On for the Higher Efficiency and Better EMI Behavior
- Multiple Protections:
  - Secondary-Side Over Voltage Protection (SOVP)
  - Secondary-Side Under Voltage Protection (SUVP)
  - Output Short Circuit Protection (SCP)
  - Transformer Saturation Protection (TSP) via Primary Peak Current Limitation
  - Internal Over Temperature Protection (OTP)
- SO-7 Package
- The Recommended Output Power is up to 7.5W
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

## Applications

- Routers
- Set-Top Box (STB) Power Supply
- Network Adaptors

Notes: 
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
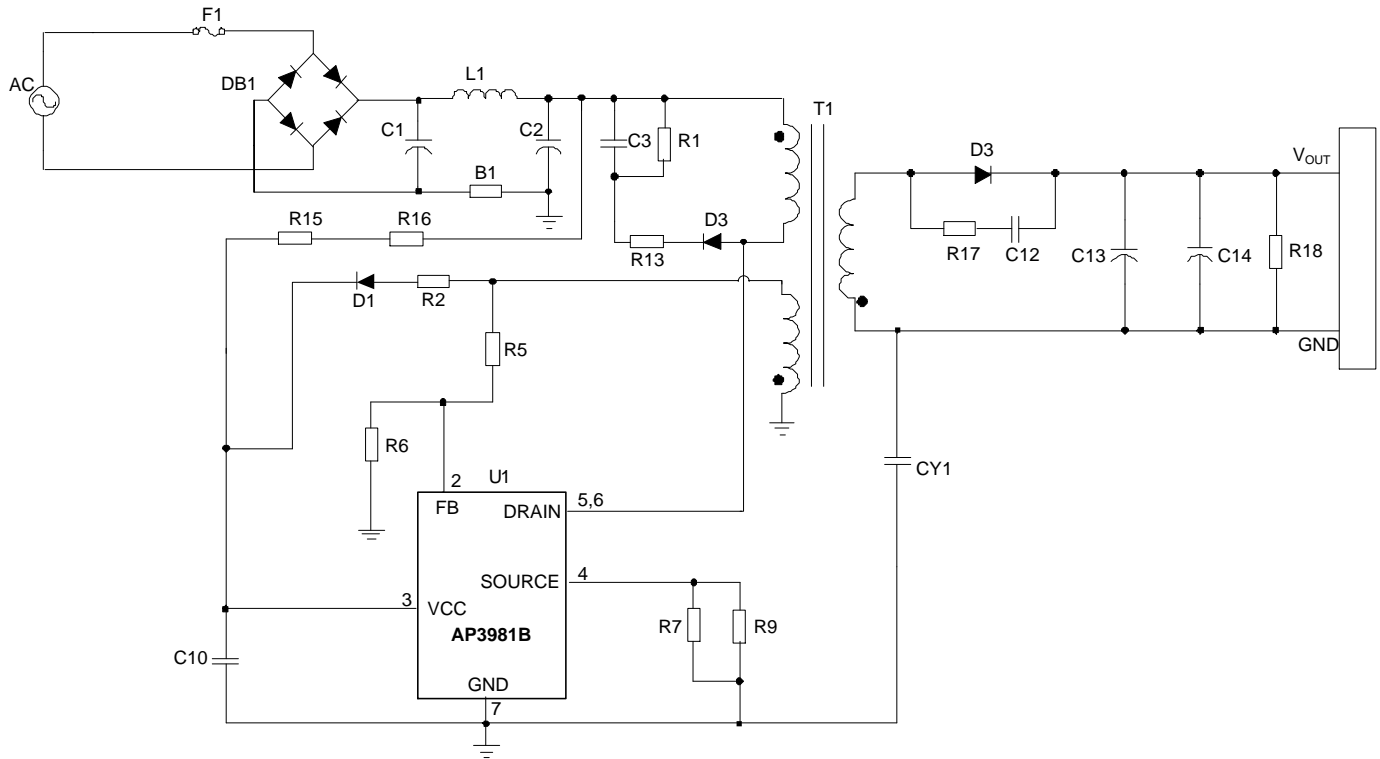
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## Typical Applications Circuit



## Pin Descriptions

| Pin Number | Pin Name | Function |
|---|---|---|
| 1 | NC | No Connection |
| 2 | FB | Connect to the auxiliary winding through a divider network, used as a multi-function pin to realize output voltage sample for CV control, $t_{ONS}$ detection for CC control, line voltage sense for line compensation, and FB-negative-protection detection as well. |
| 3 | VCC | The power supply of the IC |
| 4 | SOURCE | SOURCE terminal of the integrated MOSFET |
| 5, 6 | DRAIN | DRAIN terminal of the integrated MOSFET |
| 7 | GND | The ground of the IC |

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## Functional Block Diagram

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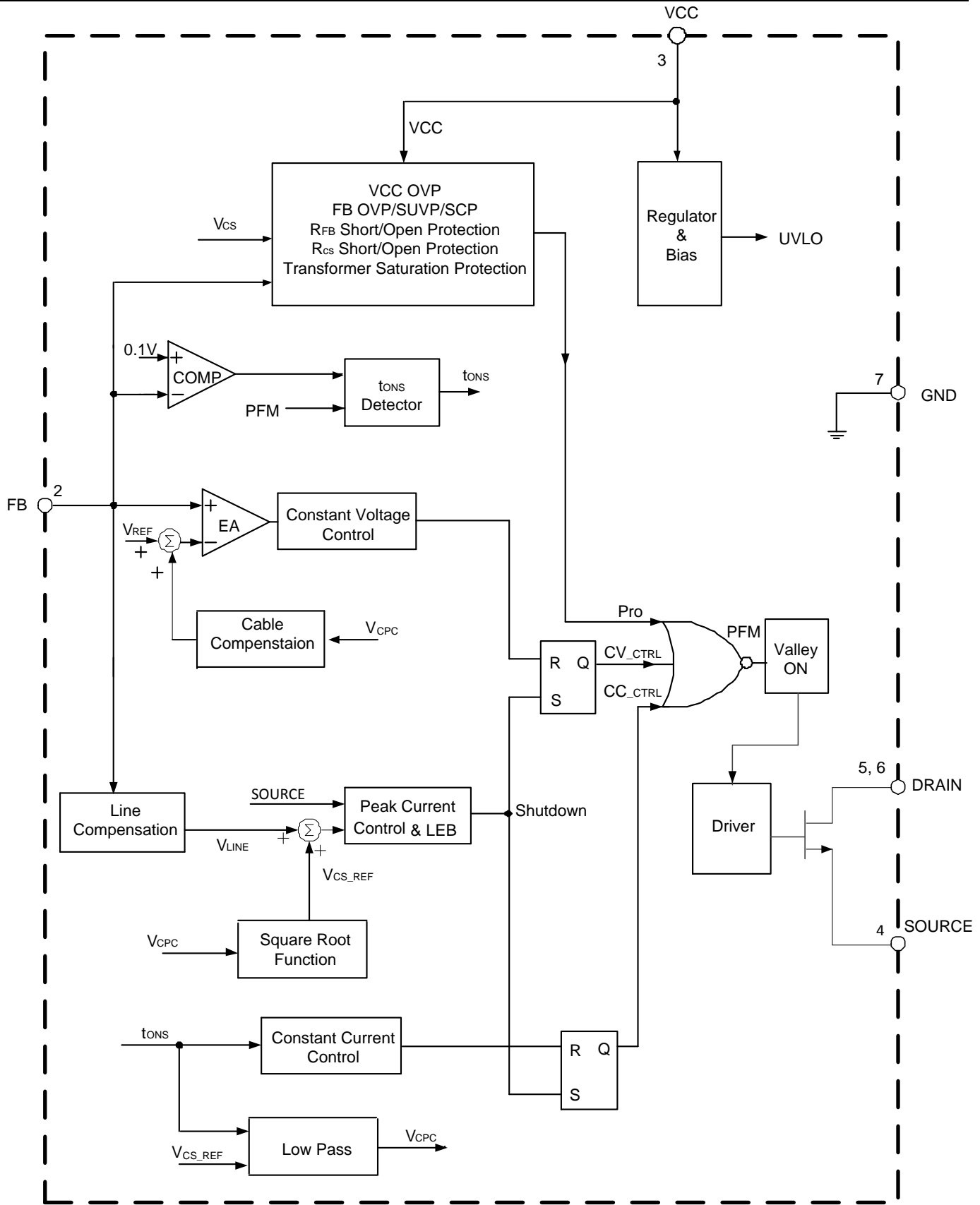
## Absolute Maximum Ratings (Note 4)

| Symbol | Parameter | Rating | Unit |
|:---:|:---|:---:|:---:|
| $V_{CC}$ | Supply Voltage | -0.3 to 35 | V |
| $V_{SOURCE}$ | SOURCE Input Voltage | -0.3 to 8 | V |
| $V_{FB}$ | FB Input Voltage | -0.3 to 8 | V |
| $V_{DS}$ | Drain-Source Voltage ($T_J$ = +25°C) | 650 | V |
| $T_J$ | Operating Junction Temperature | -40 to +150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_{LEAD}$ | Lead Temperature (Soldering, 10s) | +300 | °C |
| $\theta_{JC}$ | Thermal Resistance (Junction to Case) ( Note 5) | 3 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction to Ambient) ( Note 5) | 77 | °C/W |
| — | ESD (Human Body Model) | 2000 | V |
| — | ESD (Charged Device Model) | 1000 | V |

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch$^2$ cooling area.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Unit |
|:---:|:---|:---:|:---:|:---:|
| $V_{CC}$ | Supply Voltage | 10 | 28 | V |
| $T_A$ | Ambient Temperature | -40 | +85 | °C |

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## Electrical Characteristics (@T$_A$ =+25°C, V$_{CC}$ = 15V, unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **STARTUP AND UVLO SECTION** | | | | | | |
| V$_{TH\_ST}$ | Startup Threshold | — | 14.5 | 16 | 17.5 | V |
| V$_{OPR(MIN)}$ | Minimum Operating Voltage | — | 6.1 | 6.8 | 7.5 | V |
| **STANDBY CURRENT SECTION** | | | | | | |
| I$_{ST}$ | Startup Current | V$_{CC}$=V$_{TH\_ST}$-1V before Startup | — | 1 | 3 | μA |
| I$_{CC\_OPR}$ | Minimum Operating Current | Static Current | 450 | 550 | 650 | μA |
| **CURRENT SENSE SECTION** | | | | | | |
| V$_{CS\_H}$ | Peak Current Sense Threshold Voltage | 40% to 100% CC Load | 560 | 630 | 700 | mV |
| V$_{CS\_L}$ | | No Load to 2% CC Load | 160 | 180 | 200 | mV |
| R$_{LINE}$ | Built-In Line Compensation Resistor | — | 45 | 55 | 65 | Ω |
| t$_{LEB}$ | Leading Edge Blanking | — | 330 | 420 | 510 | ns |
| **CONSTANT VOLTAGE SECTION** | | | | | | |
| V$_{FB}$ | Feedback Threshold Voltage | Closed Loop Test of V$_{OUT}$ | 2.35 | 2.4 | 2.45 | V |
| Ratio$_{SAMPLE\_L}$ | Sample Ratio | No Load to 2% CC Load | 45 | 50 | 55 | % |
| Ratio$_{SAMPLE\_H}$ | Sample Ratio | 40% to 100% CC Load | 75 | 80 | 85 | % |
| **CONSTANT CURRENT SECTION** | | | | | | |
| t$_{ONS}$/t$_{SW}$ | Below SUVP | Tested @ V$_{FB}$=1V | — | 0.75 | — | — |
| | Above SUVP | Tested @ V$_{FB}$=2V | — | 0.5 | — | — |
| **FREQUENCY JITTER** | | | | | | |
| ΔV$_{CS}$/V$_{CS}$ | V$_{CS}$ Modulation | 10% Load to Full Load | 1.5 | 2 | 2.5 | % |
| **CABLE COMPENSATION** | | | | | | |
| V$_{CABLE}$/ V$_{OUT}$ | Fixed Cable Compensation Ratio | — | — | 4 | — | % |
| **VALLEY-ON SECTION** | | | | | | |
| t$_{VAL-ON}$ | Valid Off Time of Valley-On | From the End of t$_{ONS}$ | 26 | 32 | 38 | μs |
| **DYNAMIC SECTION** | | | | | | |
| t$_{OFF(MAX)}$ | Maximum Off Time | — | 1.35 | 1.5 | 1.65 | ms |
| **PROTECTION FUNCTION SECTION** | | | | | | |
| V$_{FB(SOVP)}$ | Over Voltage Protection at FB Pin | — | 3.3 | 3.6 | 3.9 | V |
| V$_{FB(SUVP)}$ | Under Voltage Protection at FB Pin | — | 1.22 | 1.35 | 1.48 | V |
| t$_{DELAY(SUVP)}$ | Delay Time of SUVP | — | 116 | 128 | 140 | ms |
| V$_{FB(SCP)}$ | Output Short Protection at FB Pin | — | 680 | 750 | 820 | mV |
| t$_{DELAY(SCP)}$ | Delay Time of SCP | — | 58 | 64 | 70 | ms |
| V$_{CC(OVP)}$ | Over Voltage Protection at VCC Pin | — | 29.5 | 32 | 34.5 | V |
| t$_{ONP(MAX)}$ | Maximum Turn-on Time | — | 12 | 16 | 20 | μs |
| V$_{CS(MIN)}$ | Minimum Peak Current Sense Voltage at t$_{ONP}$ = 4μs | — | 120 | 150 | 180 | mV |
| V$_{CS(MAX)}$ | Maximum CS Voltage | — | 720 | 800 | 880 | mV |

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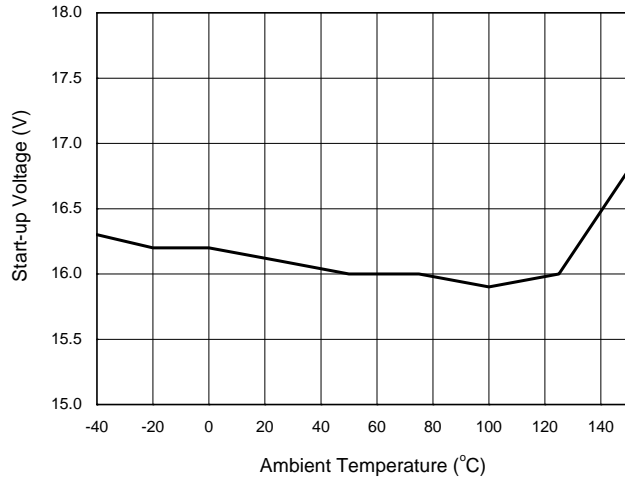
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**Electrical Characteristics** (continued) (@T$_A$ =+25°C, V$_{CC}$ = 15V, unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PROTECTION FUNCTION SECTION** | | | | | | |
| V$_{FB\_NEG\_L}$ | Low Threshold for FB Negative Voltage Protection | — | 11 | 14 | 17 | mV |
| V$_{FB\_NEG\_H}$ | High Threshold for FB Negative Voltage Protection | — | 27 | 36 | 45 | mV |
| T$_{OTP}$ | Shutdown Temperature | — | +125 | +140 | +155 | °C |
| T$_{HYS}$ | Temperature Hysteresis | — | +27 | +30 | +33 | °C |
| **POWER MOSFET SECTION** | | | | | | |
| BV$_{DSS}$ | Integrated MOSFET Drain-Source Break-Down Voltage (Note 6) | — | 650 | — | — | V |
| R$_{DS(ON)}$ | Static Drain-Source On-Resistance | — | — | 7.8 | 9.3 | Ω |
| I$_D$ | Continuous Drain Current | — | — | — | 1.5 | A |

Note： 6. The aging condition of drain-source voltage is 80% of BV$_{DSS}$.

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## Performance Characteristics

### Start-Up Voltage vs. Ambient Temperature



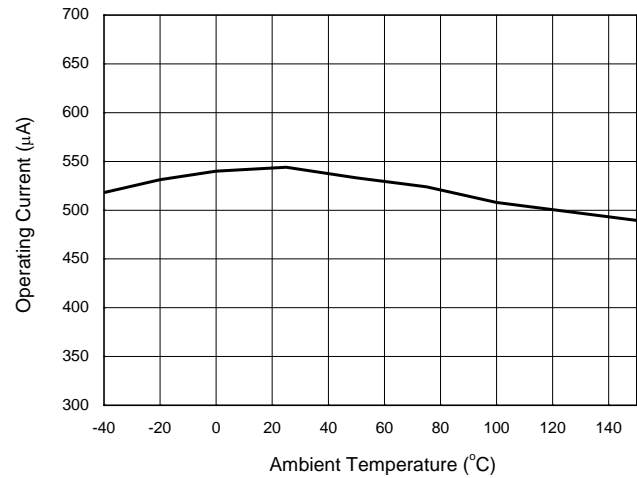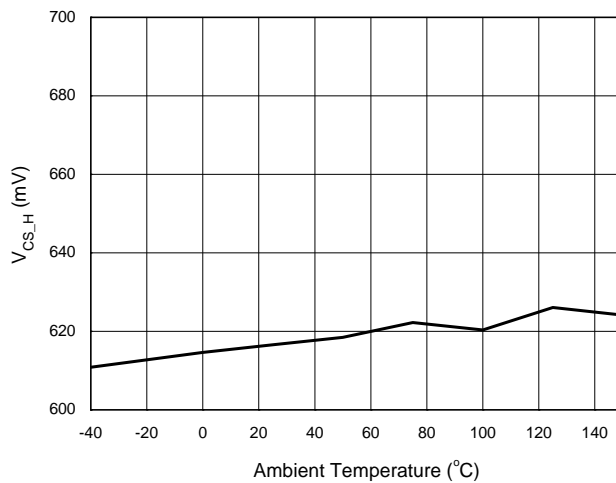### Start-Up Current vs. Ambient Temperature
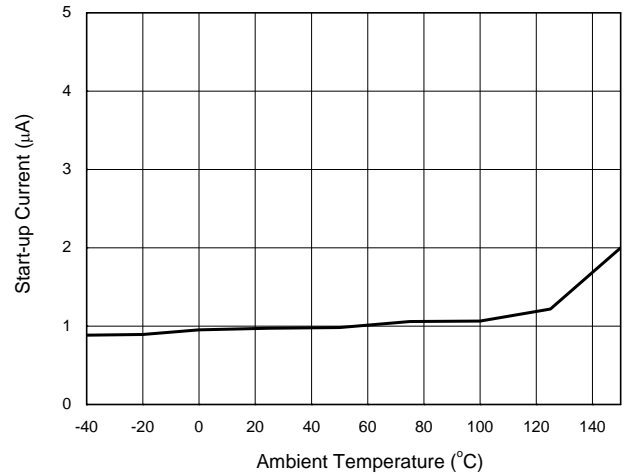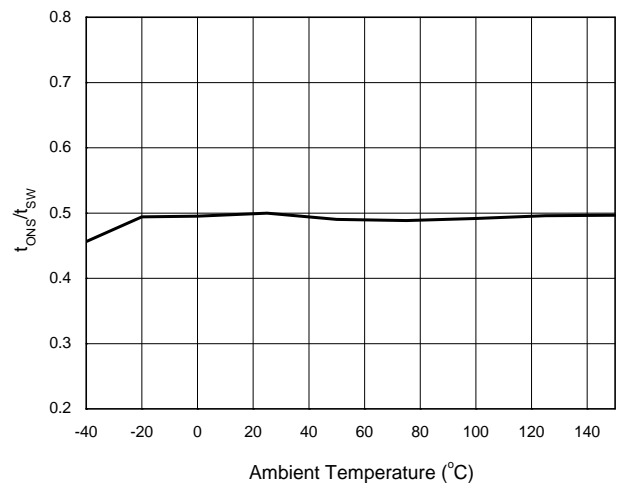


### Minimal Operating Voltage vs. Ambient Temperature
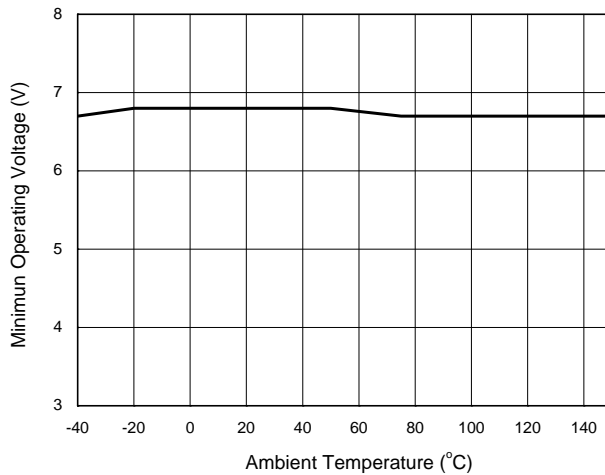


### Operating Current vs. Ambient Temperature
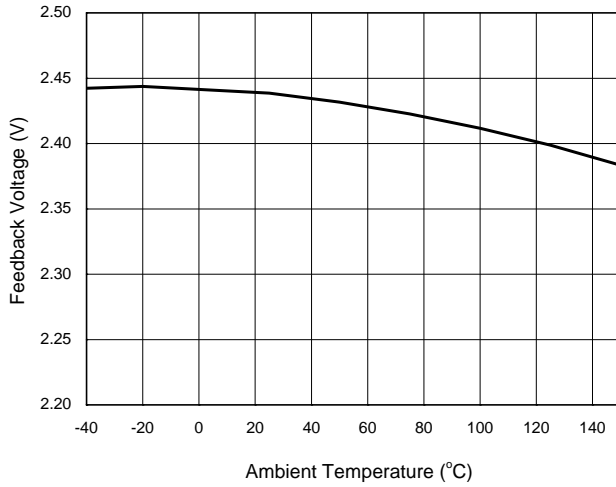


### $V_{CS\_H}$ vs. Ambient Temperature



### $t_{ONS}/t_{SW}$ Above SUVP vs. Ambient Temperature

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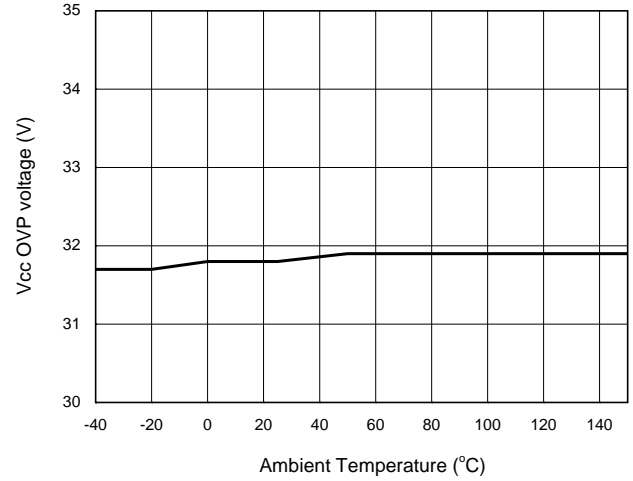**www.diodes.com**

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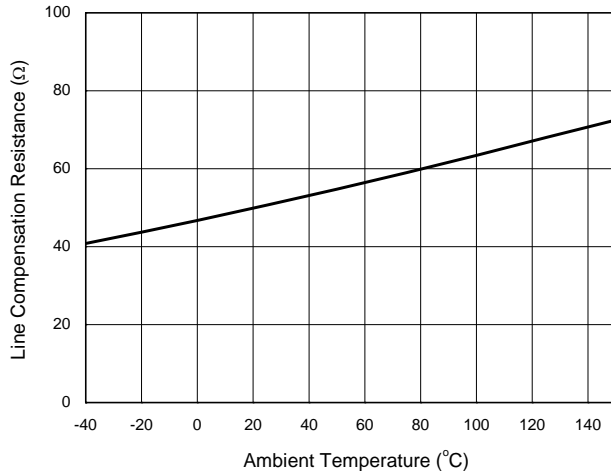**Performance Characteristics** (continued)

**Feedback Voltage vs. Ambient Temperature**
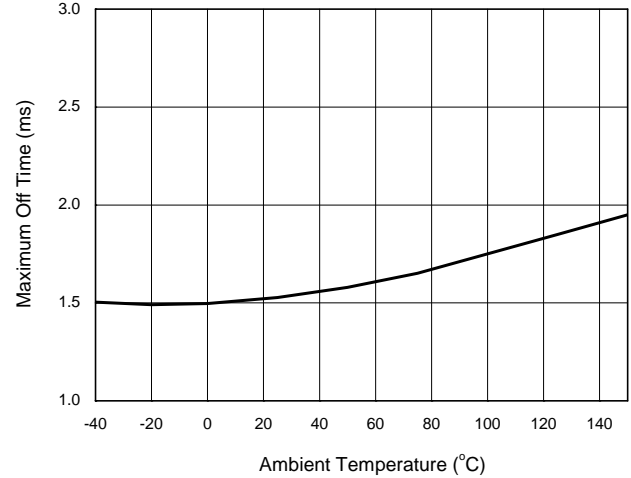


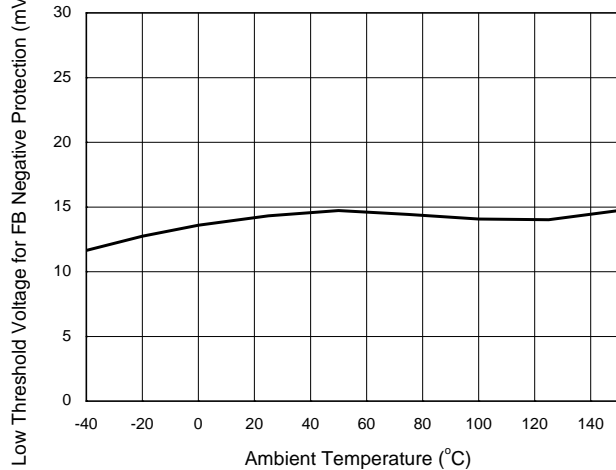**V$_{CC}$ OVP Voltage vs. Ambient Temperature**



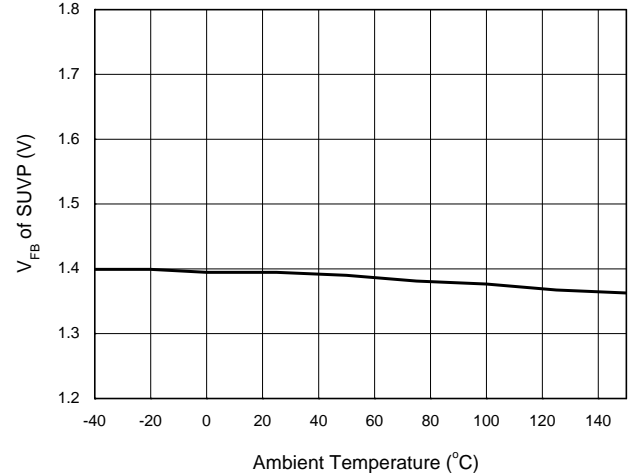**Line Compensation Resistance vs. Ambient Temperature**



**Maximum Off Time vs. Ambient Temperature**



**Low Threshold Voltage for FB Negative Protection vs. Ambient Temperature**



**Feedback Voltage of SUVP vs. Ambient Temperature**



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## Operation Principle Description

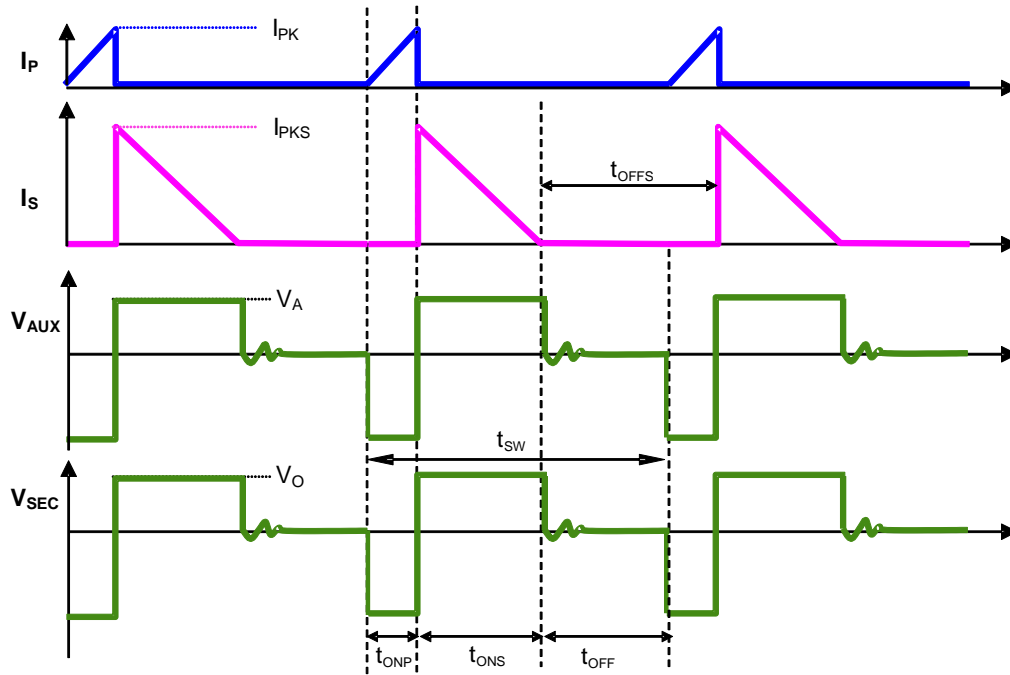### 1. The Conventional PSR Operating Waveforms



Figure 1. The Operation Waveform of Flyback PSR System

Figure 1 shows the typical waveforms which demonstrate the basic operating principle of AP3981B application. And the parameters are defined as following:

$I_P$---The primary-side current

$I_S$ ---The secondary-side current

$I_{PK}$---Peak value of primary-side current

$I_{PKS}$---Peak value of secondary-side current

$V_{SEC}$---The transient voltage at secondary winding

$V_O$---The output voltage

$V_{AUX}$---The transient voltage at auxiliary winding

$V_A$--- The stable voltage at auxiliary winding when rectification diode is in conducting status, which equals the sum of voltage $V_{CC}$ and the forward voltage drop of auxiliary diode

$t_{SW}$ ---The period of switching frequency

$t_{ONP}$ ---The conduction time when primary-side switch is "ON"

$t_{ONS}$ ---The conduction time when secondary-side diode is "ON"

$t_{OFF}$ ---The dead time when neither primary-side switch nor secondary-side diode is "ON"

$t_{OFFS}$ --- The time when secondary-side diode is "OFF"

For primary-side regulation, the primary current ip(t) is sensed by a current sense resistor $R_{CS}$ connected to SOURCE pin. The current rises up linearly at a rate of:

$$\frac{dip(t)}{dt} = \frac{V_{IN}(t)}{L_M} \qquad (1)$$

As illustrated in Figure 1, when the current ip(t) rises up to $I_{PK}$, the primary MOSFET will turn off. The constant peak current is given by:

$$I_{PK} = \frac{V_{CS}}{R_{CS}} \qquad (2)$$

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## Operation Principle Description (continued)

The energy stored in the magnetizing inductance $L_M$ each cycle is therefore:

$$Eg = \frac{1}{2} \times L_M \cdot I_{PK}{}^2 \qquad (3)$$

So the power transferring from the input to the output is given by:

$$P = \frac{1}{2} \times L_M \times I_{PK}{}^2 \times f_{SW} \qquad (4)$$

Where, the $f_{SW}$ is the switching frequency. When the peak current $I_{PK}$ is constant, the output power will depend on the switching frequency $f_{SW}$.

### 2. Constant Voltage Operation

The output voltage is proportional to the auxiliary winding voltage during $t_{ONS}$ period indicated by Formula 5, this auxiliary winding voltage is divided by resistors $R_{FB1}$ and $R_{FB2}$ (refer to Figure 5) before inputting to the FB pin. As Figure 2 illustrated, the AP3981B detects the FB voltage at the end of $t_{SAMPLE}$ during $t_{ONS}$ period, and the detected voltage which reflects the output voltage is regulated to $V_{FB}$ of 2.4V with the help of the constant voltage control block in AP3981B. For system design, adjusting the ratio of $R_{FB1}$ and $R_{FB2}$ can get the target output voltage value.

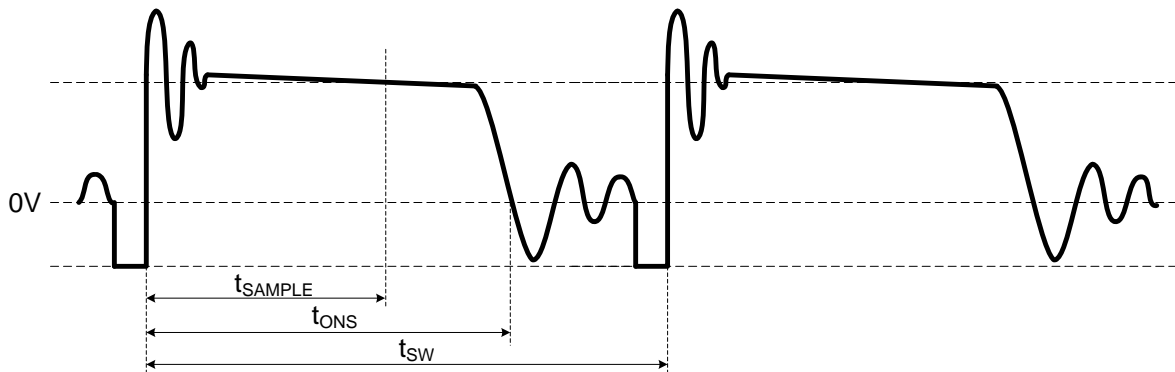$$V_{AUX} = \frac{N_{AUX}}{N_S} \times (Vo + Vd) \qquad (5)$$



Figure 2. Auxiliary Voltage Waveform

### 3. Constant Current Control

In the AP3981B, Formula 6 shows the related parameters that determine the output current. To get a constant output current, the $V_{CS}$ and $t_{ONS}/t_{SW}$ is fixed in AP3981B during CC mode. Meanwhile, a reliable control logic is integrated within AP3981B to ensure the system swift smoothly between CC mode and CV mode.

$$I_{OUT} = \frac{1}{2} * \frac{Np}{Ns} * Ipk * \frac{t_{ONS}}{t_{SW}} = \frac{1}{2} * \frac{Np}{Ns} * \frac{Vcs}{Rcs} * \frac{t_{ONS}}{t_{SW}} \qquad (6)$$

### 4. Multiple Segment Peak Current

In the original PFM PSR system, the switching frequency decreases with the decreasing output current, which will encounter audible noise issue when switching frequency decreases below 20kHz.

In order to avoid audible noise issue and a big drop in efficiency at light load, the AP3981B uses a 3-segment primary peak current control method at CV mode, the current sense threshold voltage is piecewise defined. As shown in Figure 3, the low threshold $V_{CS\_L}$ is set under 2% CC load, while the high threshold $V_{CS\_H}$ is set above 40% CC load. Within the range from 2% to 40%, the threshold $V_{CS\_M}$ increases based on the load condition, the $V_{CS\_M}$ is carefully calculated inside AP3981B to make the system operate at a reasonable switching frequency which rises above 20kHz at a varying slope.

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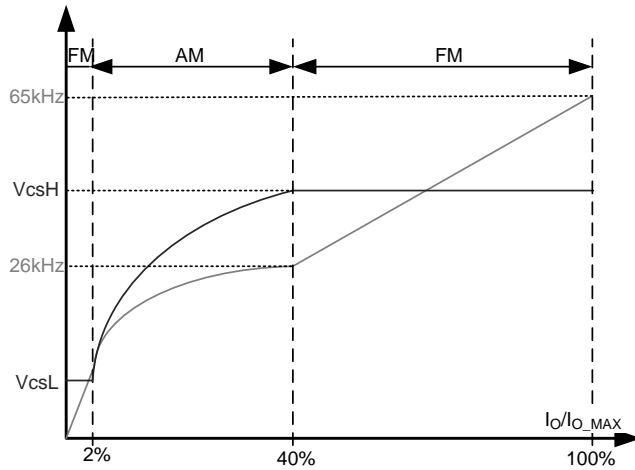
## Operation Principle Description (continued)

Figure 3. Segment Peak Current and Operating Frequency at CV Mode

### 5. Sample Time

As shown in Equation 5 and Figure 2, the detected auxiliary voltage reflects the output voltage. To be compatible with different system designs and avoid the turn-off ringing voltage influence on CV sampling, the $t_{SAMPLE}$ is designed to be proportional of $t_{ONS}$. On the other hand, to alleviate the Vd effect on the accuracy of $V_{OUT}$, the sample ratio of $t_{SAMPLE}$ to $t_{ONS}$ varies according to load condition. The $t_{SAMPLE}$ is usually 50% of $t_{ONS}$ for the below 2% CC load conditions, and 80% of $t_{ONS}$ for the above 40% CC load conditions. Within the range from 2% to 40% loading, the sample ratio rises linearly from 50% to 80%.

### 6. Capacitive Load Start-Up Capability

In order to achieve fast start-up for capacitive load startup applications, the AP3981B induces a two-level CC point design during startup time. The output voltage rises after power on, when the detected output voltage is lower than SUVP point, the $t_{ONS}/t_{SW}$ is set to be 0.75, which means output constant current is 1.5 times of normal output constant current. When the output voltage rises above SUVP point, the $t_{ONS}/t_{SW}$ is switched to the normal value of 0.5.

### 7. Leading Edge Blanking

When the power switch is turned on, a turn-on spike voltage will occur on the $V_{CS}$ sense resistor. To avoid false-termination of the switching pulse, a fixed 420ns leading-edge blanking time is built in. During this blanking period, the current sense comparator is disabled and the primary MOSFET cannot be turned off.

### 8. Valley Turn-On

When the off time ($t_{OFF}$) is shorter than $t_{VAL-ON}$, the AP3981B power system can work with valley turn-on. It can reduce the switch-on power losses and achieve high overall efficiency. At the same time, because of valley turn-on, the switching frequency has the random jitter feature, which will be of benefit to conductive EMI performance. The valley turn-on can also reduce the power switch turn-on spike current and then achieve the better radiative EMI performance.

### 9. $V_{CS}$ Jitter

Even though the valley turn-on function produces the random frequency jitter feature, an active frequency jitter function is added in the AP3981B. The active frequency dithering is realized by applying variation on $V_{CS}$ reference ($V_{CS\_REF}$). The $V_{CS\_REF}$ is changed every 2 cycles and the period of variation is 12 cycles, which is shown as Figure 4. The variation between $V_{CS4}$ and $V_{CS1}$ is +/-2% using the mean level as a reference.

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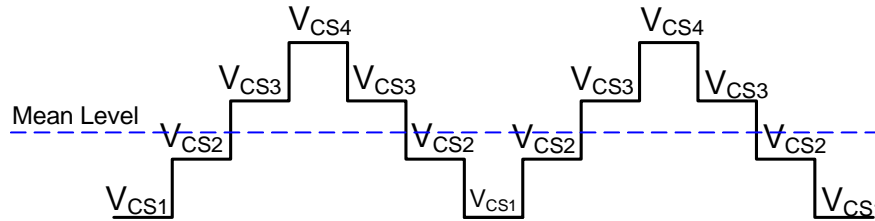## Operation Principle Description (continued)



Figure 4. $V_{CS}$ Jitter

### 10. Adjustable Line Compensation

In real system, there exists a delay time, from the $V_{SOURCE}$ reach the inner $V_{CS}$ threshold to the actual switch turn-off point. The delay time contains the propagation time of the inner comparator and the driver delay, and it does not change with line voltage. The delay time leads to different primary peak current under different line voltage, which results in different output current in CC mode.
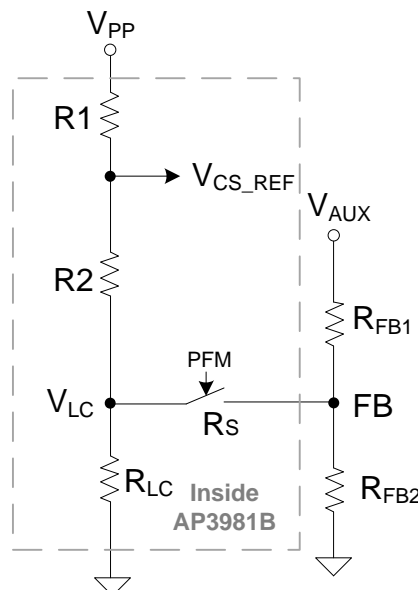


Figure 5.  Line Compensation Control Circuit

In order to alleviate the difference under the universal input voltage, the AP3981B integrates the line compensation control circuit shown as Figure 5. During the primary on stage, an inner switcher $R_S$ switches on, and the $R_{LC}$ is much smaller compared with $R_{FB2}$, so the $R_{FB2}$'s effect on line compensation can be neglected, the proportional line voltage is detected through $R_{FB1}$ and $R_{LC}$, and is added to the $V_{CS}$ threshold ($V_{CS\_REF}$). The $V_{LC}$ can be derived from the Formula 7:

$$V_{LC} = \frac{\dfrac{R_{FB1}}{3*R2}*V_{PP} - V_{AUX}}{1 + \dfrac{R_{FB1}}{3*R2} + \dfrac{R_{FB1}}{R_{LC}}} \qquad (7)$$

The final compensated $V_{CS}$ is:

$$V_{CS\_REF} = \frac{1}{3}*V_{PP} + \frac{2}{3}*V_{LC} \qquad (8)$$

In the above formulas, $V_{PP}$ is 1.8V at CC mode, $R_{LC}$ is 55$\Omega$, R2 is 60k$\Omega$, R1 is two times of R2, $V_{AUX}$ is the value of auxiliary winding voltage during primary-on period and it is proportional to bus voltage. Based on the formula, we can make a conclusion that a smaller $R_{FB1}$ results in deeper line compensation. If we know the delay time, $t_{DELAY}$, typically 150ns in AP3981B, we can calculate the $R_{FB1}$ as a reference for the system design.

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## Operation Principle Description (continued)

### 11. Protection

The AP3981B provides versatile protections to prevent the system from damage under various fault conditions. Most protections will trigger auto-recovery mode in which the system will restart as soon as the $V_{CC}$ drops to $V_{OPR(MIN)}$, when the fault conditions are removed, the system will recover to normal operation automatically.

### $V_{CC}$ OVP

A $V_{CC}$ OVP threshold is set to protect the IC from damage. When the $V_{CC}$ OVP protection is triggered, the IC will stop outputting drive signal immediately and the system will enter auto-recovery mode.

### Secondary-Side Over Voltage Protection (SOVP)

As it described above that the FB pin voltage during $t_{ONS}$ reflects the output voltage proportionally, this voltage can be used to realize SOVP. The AP3981B set a higher threshold, $V_{FB(OVP)}$, to shut down the system if the sampled voltage reaches the threshold continuously for 3 switching cycles, the SOVP will be triggered and the system will enter auto-recovery mode.

### Secondary-Side Under Voltage Protection (SUVP)

Like SOVP, the AP3981B also integrates the SUVP protection. If the detected voltage on FB pin is lower than $V_{FB(SUVP)}$ for 128ms, the SOVP will be triggered and the system will enter auto-recovery mode.

### Output Short Protection (SCP)

A much lower threshold is set on FB pin to protect the system when output short condition occurs. If the detected FB voltage is lower than 0.78V for 64ms, the SCP will be triggered and the system will enter auto-recovery mode.

### Transformer Anti-Saturation Protection

Under some fault conditions or bad system design, the transformer may approach saturation and the current increases dramatically. To avoid power device damage since of transformer saturation, the AP3981B integrated a maximum $V_{CS}$ threshold $V_{CS(MAX)}$ to protect the system. If there are 3 consecutive pulses where $V_{CS}$ exceeds the threshold, the controller will shut down and enter auto-recovery mode.
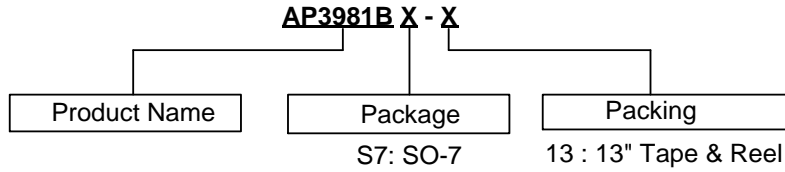
### Over Temperature Protection (OTP)

If the IC junction temperature exceeds the threshold of $T_{OTP}$, the AP3981B will shut down immediately and enter auto-recovery mode. Note that even when the $V_{CC}$ reaches $V_{TH\_ST}$, the IC will not output any drive pulse until the junction temperature falls of a hysteresis temperature of +30°C.

### Brown In / Brown Out Protection

The AP3981B detects the bus voltage at each switching cycle through FB pin during $t_{ONP}$ period. When the $V_{CC}$ reaches $V_{TH\_ST}$ after power-on, the AP3981B will output one switching pulse to check if the detected bus voltage on FB pin is higher than $V_{FB\_NEG\_H}$. If so, the system will start up normally, otherwise AP3981B will stop outputting following pulses, then the $V_{CC}$ will drop below $V_{OPR(MIN)}$ and the system will repeat the process described above until the detected FB voltage is higher than $V_{FB\_NEG\_H}$. When the power is off or there is a ditch in bus voltage, if the detected voltage is lower than $V_{FB\_NEG\_L}$ for 3 consecutive switching cycles, the IC will shut down and enter auto-recovery mode. This function is very useful when the bulk capacitor is open, or when the heavy load is suddenly released after power off.
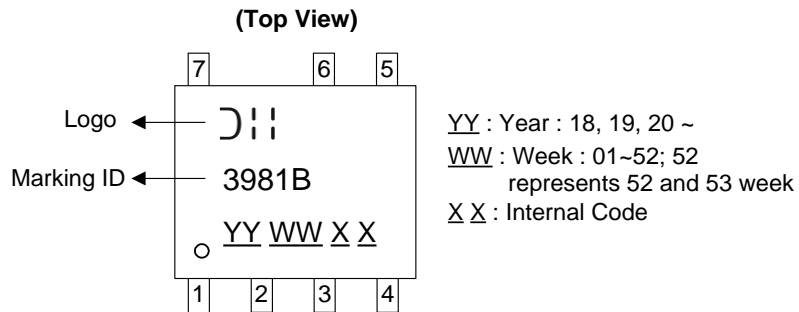
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## Ordering Information

AP3981B X - X

| Product Name | Package | Packing |
| --- | --- | --- |
| | S7: SO-7 | 13 : 13" Tape & Reel |

| Package | Part Number | Marking ID | 13"Tape and Reel | |
| --- | --- | --- | --- | --- |
| | | | Quantity | Part Number Suffix |
| SO-7 | AP3981BS7-13 | 3981B | 4000/Tape and Reel | -13 |

## Marking Information

Package Name: SO-7

**(Top View)**



YY : Year : 18, 19, 20 ~
WW : Week : 01~52; 52
 represents 52 and 53 week
X X : Internal Code

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## Package Outline Dimensions (All dimensions in mm (inch).)

**(1) Package Type: SO-7**



| | |
|---|---|
| 5.800(0.228) | |
| 6.200(0.244) | |

0.330(0.013)
0.510(0.020)

2.54(0.100)
TYP

1.270(0.050)
TYP

3.800(0.150)
4.000(0.157)

1.350(0.053)
1.750(0.069)

4.700(0.185)
5.100(0.201)

0.080(0.003)
0.250(0.010)

1.250(0.049)
1.500(0.059)

0°
8°

Option 1

0.450(0.017)
0.800(0.031)

0.150(0.006)
0.250(0.010)

0.350(0.014)
TYP

45°
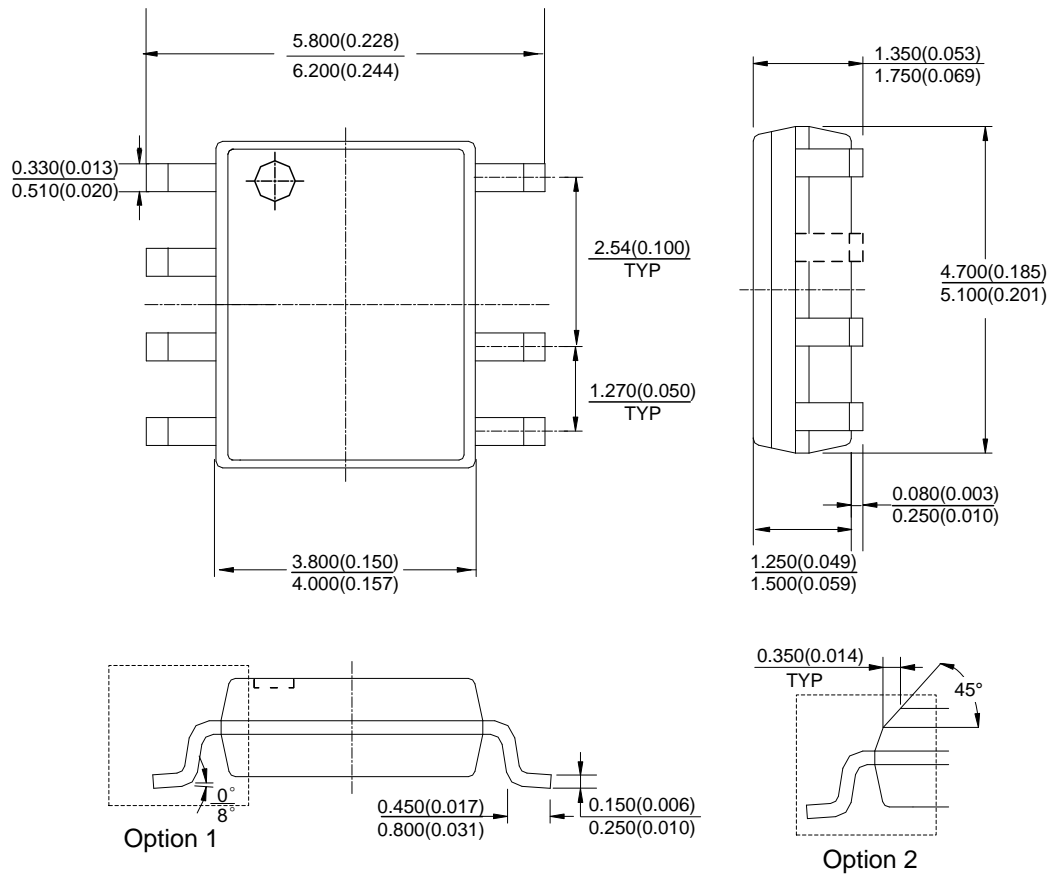
Option 2

Note: Eject hole, oriented hole and mold mark is optional.

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## Suggested Pad Layout

**(1) Package Type: SO-7**
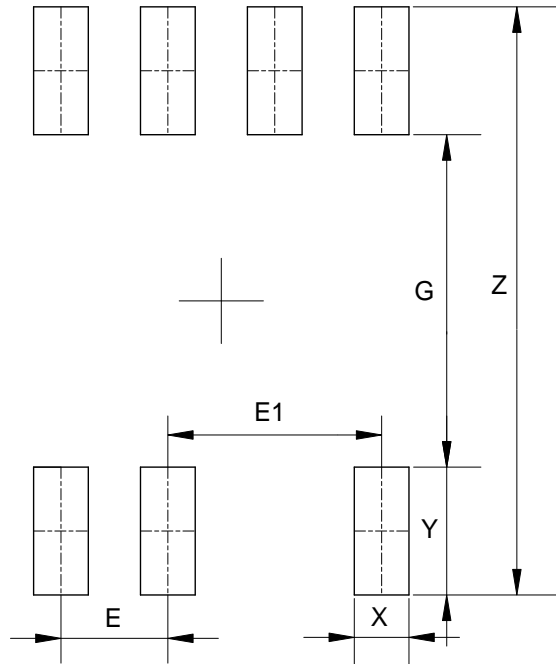


| Dimensions | Z<br>(mm)/(inch) | G<br>(mm)/(inch) | X<br>(mm)/(inch) | Y<br>(mm)/(inch) | E<br>(mm)/(inch) | E1<br>(mm)/(inch) |
|---|---|---|---|---|---|---|
| Value | 6.900/0.272 | 3.900/0.154 | 0.650/0.026 | 1.500/0.059 | 1.270/0.050 | 2.540/0.100 |

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