DUAL-CHANNEL USB TYPE-C PD3.1/PPS/QC5 PROTOCOL DECODER

Description

The DIODES™ AP43776 is a highly integrated, dual-channel, USB Type-C®, PD3.1 / PPS / QC5 protocol decoder. It passes certification of USB Type-C power delivery specification Rev 3.1 V1.1 with PPS and Quick Charge™ QC5 protocol.

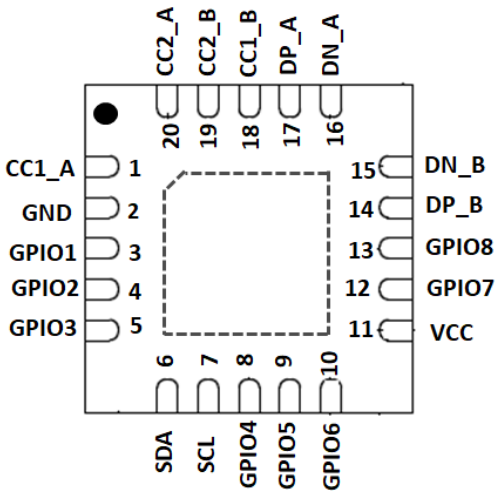
The device can support the full range of PPS APDO (augmented power data object) from 3.3V to 21V with 20mV/step voltage resolution and up to 6A current with 50mA/step resolution for power management. To enable output current beyond 3A, the AP43776 supports e-Marker cable detection with built-in VCONN switch with 30mA driving capability and overcurrent protection (OCP). Cable-loss compensations are also embedded.

The AP43776 provides an embedded MCU and built-in ADC converters for voltage and temperature measurement, where overtemperature protection (OTP) and other specific functions can be implemented through I2C pins and rich GPIO pins. Working in conjunction with two I2C-equipped Buck-Boost controllers or converters which have PD3.1 PPS output circuitry, the AP43776 serves as the I2C master and supports two independent PD3.1 PPS charging applications without using additional Output Enable MOS chips for each PD3.1 output port.

With built-in firmware, the AP43776 can support various smart power-management functions such as power-sharing scheme between two attached USB Type-C PD devices, low-battery power derating, thermal power derating, LED light indication, etc. Two AP43776 devices can also be interconnected through a UART (GPIO) pin to implement smart power-sharing scheme for all four connected USB Type-C ports attached to a fixed power source.

Pin Assignments

(Top View)



W-QFN4040-20

Features

- Dual-channel independent USB Type-C PD3.1/PPS decoder
- USB-IF PD3.1/PPS certificated TID: 6206
- Quick Charge™ QC5 certificated No.: QC20211008263
- Supports PD3.1/ full range of PPS VOUT (3.3V to 21V)
- Compliant with BC1.2 (DCP)
- Built-in MCU with 12KB OTP ROM for main application program with multi-time-programmable ROM (MTP ROM) blocks for customization
- Built-in Built-in 16-CH 8b 83KHz SAR ADC for voltage and temperature measurement
- Supports e-Marker detection and VCONN switch with 15Ω internal Rds_on
- Supports cable-loss compensations
- Supports I2C communication and GPIO controls
- Multi-purpose I/Os to support different applications
- Supports short protection between CC1/CC2 and VBUS (Up to 24V)
- Supports short detection between DP and DN
- Supports over-temperature protection (OTP)
- Support output power de-rating for low battery and thermal
- W-QFN4040-20 (4x4, 0.5mm pitch) package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Multi-port USB PD3.1 PPS car chargers
- Multi-port USB PD3.1 PPS power sources

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Quick Charge is a trademark of Qualcomm Incorporated.
USB Type-C and USB-C are registered trademarks of USB Implementers Forum.

Typical Applications Circuit

Application 1:
Two USB Type-C ports car charger based on one* AP43776 + two* DC/DC, where I2C bus is used for communications between AP43776 and two DC/DC controllers. It is shown that the USB Type-C output MOS switch is not needed.

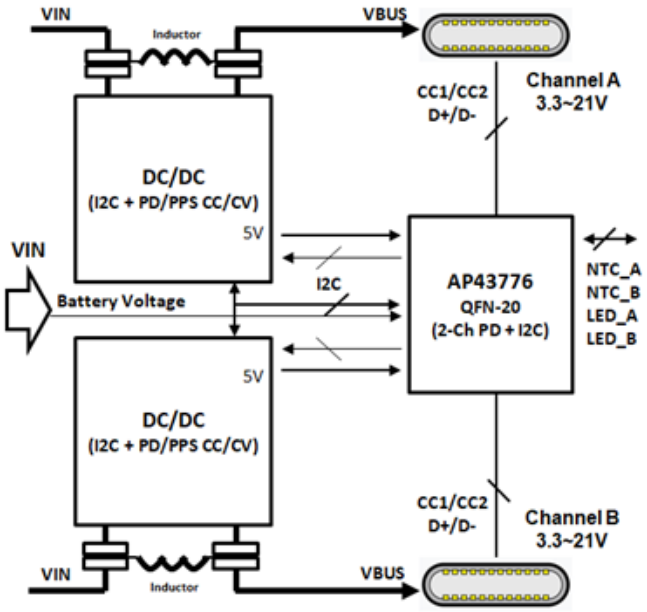


Figure 1. A two-channel car charger

Application 2:
Four USB Type-C ports car charger based on two* AP43776 + four* DC/DC controllers, where the smart power sharing is performed through I2C and UART buses.

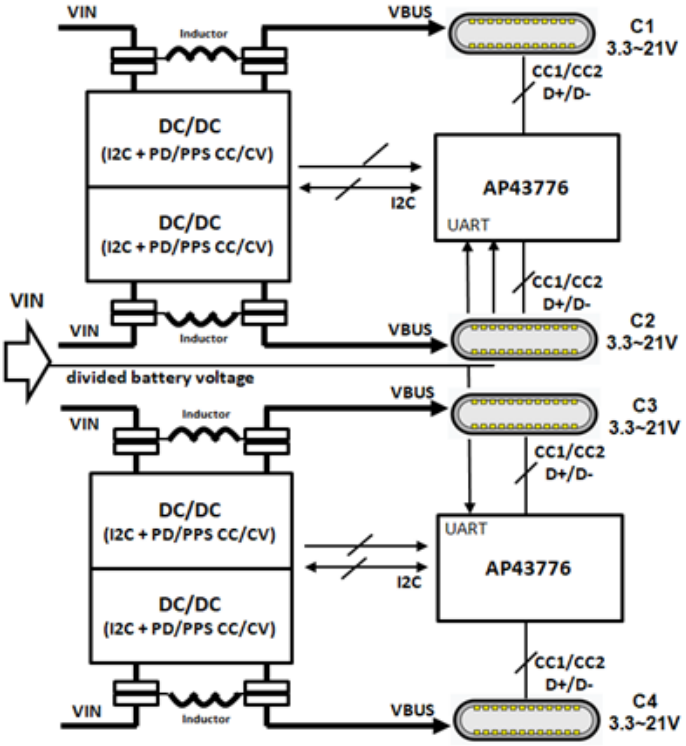


Figure 2. A four-channel car charger

Typical Applications Circuit (continued)

An example of 120W Dual-port Type C PD3.1 PPS car charger is shown Figure 3. Powered by the VREG pin (internal 5V Regulator output) for the attached DC-DC Controller, detecting Vin through GPIO1, the AP43776 could enter protection mode to disable DC/DC stage by controlling the GPIO2 pin. All PD decoded information through CC1 and CC2 pin as well as measured parameters of the operating coditions, the AP43776 conveys necessary actions, such as Constant Voltage output, Constant Current output and protection functions through I2C interface. With built-in application firmware of the AP43776, VBUS MOS switches are not needed, and GPIO pins are used to do battery detection, power sharing, temperature detection, LED indicator, and so on.

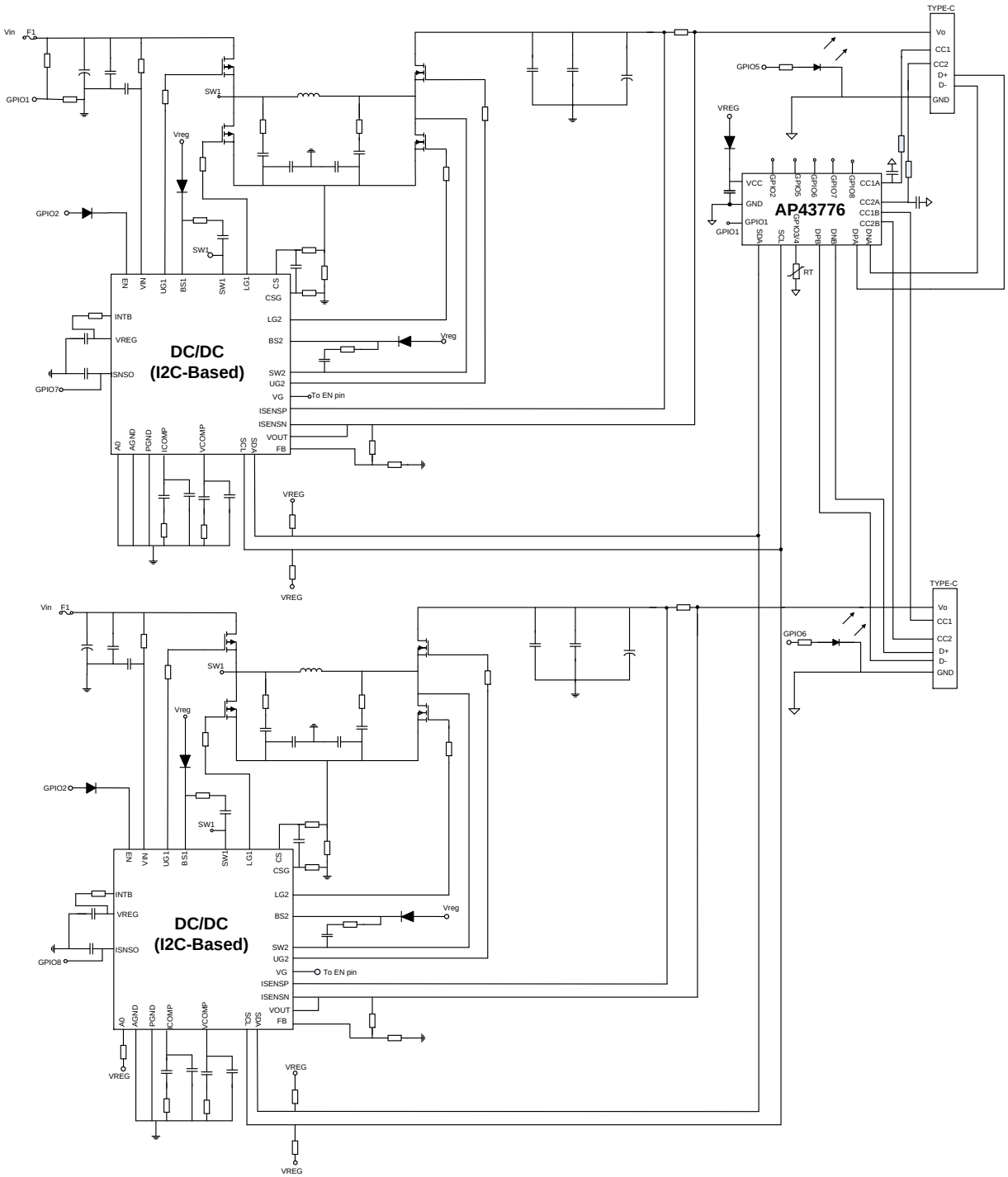


Figure 3. A 120W 2C PD3.1 PPS car charger design based on 2*DC/DC+1*AP43776

Pin Descriptions

Pin Number	Pin Name	Function
1	CC1_A	Output to channel A Type-C CC or VCONN pin.
2	GND	Ground pin.
3	GPIO1	Multipurpose I/O pin. (define for UART application)
4	GPIO2	Multipurpose I/O pin. (define for UART application)
5	GPIO3	Multipurpose I/O pin. (define for NTC application)
6	SDA	Data pin of I2C. (define for communication with I2C-based Buck-Boost or Buck IC)
7	SCL	Clock pin of I2C. (define for communication with I2C-based Buck-Boost or Buck IC)
8	GPIO4	Multi-purpose I/O pin with current source. (defined for NTC application)
9	GPIO5	Multipurpose I/O pin. (define for LED indicator light)
10	GPIO6	Multipurpose I/O pin. (define for LED indicator light)
11	VCC	Power supply pin
12	GPIO7	General-purpose I/O pin. (define for V/I report of Buck-Boost or Buck IC)
13	GPIO8	General-purpose I/O pin. (define for V/I report of Buck-Boost or Buck IC)
14	DP_B	Connected to channel B Type-C DP pin.
15	DN_B	Connected to channel B Type-C DN pin.
16	DN_A	Connected to channel A Type-C DN pin.
17	DP_A	Connected to channel A Type-C DP pin.
18	CC1_B	Output to channel B Type-C CC or VCONN pin.
19	CC2_B	Output to channel B Type-C CC or VCONN pin.
20	CC2_A	Output to channel A Type-C CC or VCONN pin.
—	Exposed Pad	Connected to PCB Ground.

Functional Block Diagram

The AP43776 is an MCU-based, dual-channel, USB Type-C, PD3.1/PPS and QC5 protocol decoder. The device's functional block diagram is shown below. With its hardware transceivers and multiplexed ADC, the rich multipurpose GPIOs can support many different kinds of applications.

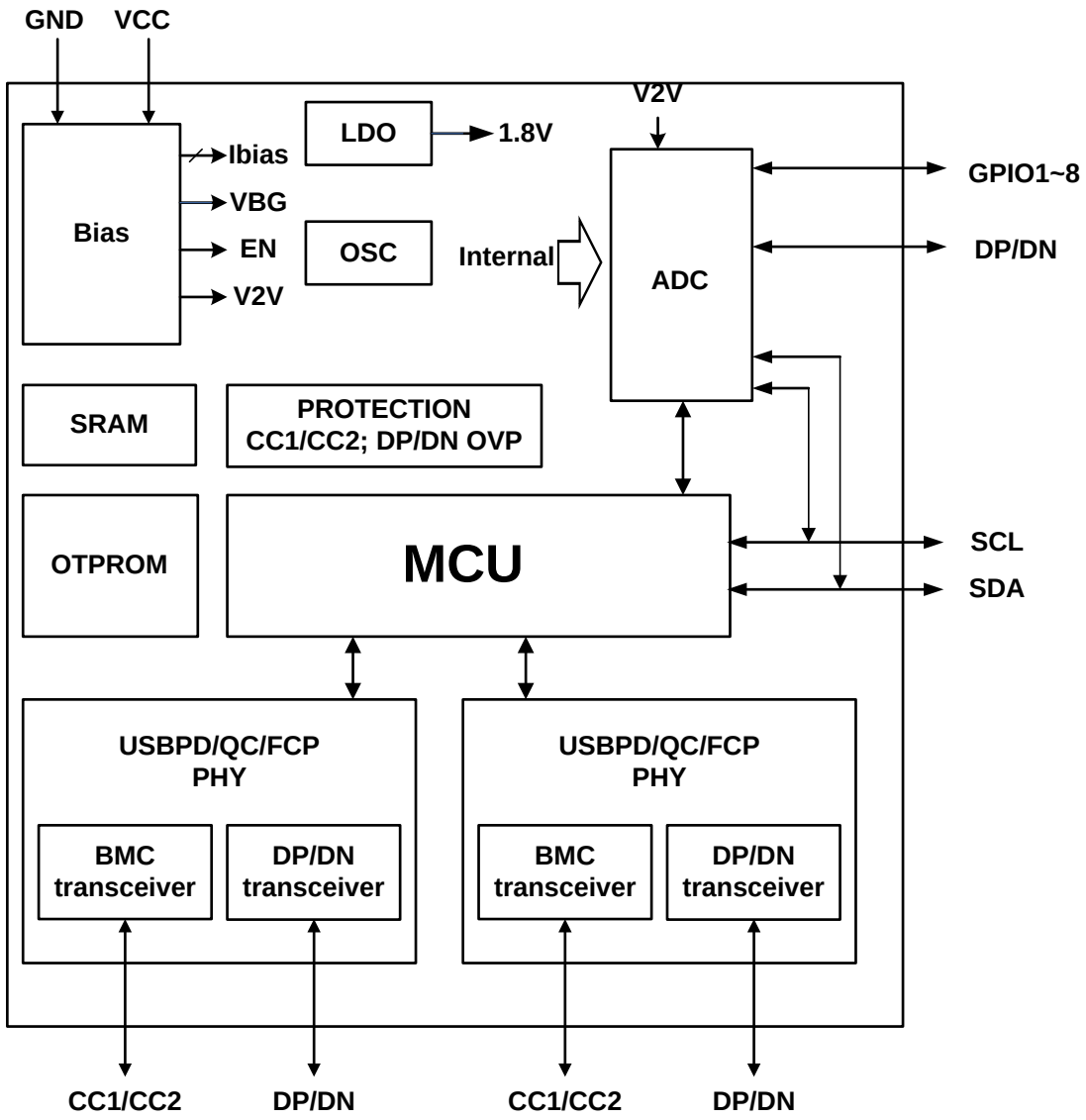


Figure 4. The functional block diagram of AP43776

Functional Overview

Function Description

The AP43776 is a highly integrated, dual-channel, USB Type-C PD3.1/ PPS/ QC5 protocol decoder, certified for USB-IF PD3.1/PPS Qualcomm™ QC5.0 compliance. To ensure two independent PD3.1 PPS protocol decoding operations are in full compliance with critical USB Power Delivery specification rev 3.1 v1.1, the AP43776 implements a combination of hardware and MCU firmware to leverage quick response times from the hardware and maintain software flexibility. To improve noise immunity during chip application, I2C communication is used between the PD controller and DC/DC converter.

Bias and Power

The AP43776 operates from a single external supply source, VCC. VCC is used for analog circuitry and goes through internal regulators to generate all of the voltage and current references for chip operation, without the need for external capacitor decoupling. The AP43776 has two different power modes: normal and sleep. During normal operation, the AP43771 consumes under 3mA. During sleep mode, its current can be reduced to around 0.5mA automatically.

PHY Transceiver

To leverage quick response times from the hardware circuitry, there are two sets of PHY transceivers embedded on the AP43776. Each PHY transceiver consists of a BMC transceiver for processing USB PD protocol, and a D+/D- transceiver for supporting QC and FCP protocols. All communications are half-duplex, and the Physical Layer provides collision avoidance to minimize communication errors during handshake. The PHY transceiver includes CC detection logic; termination resistors and their switches, as required by USB PD specifications to implement connection detection; plug orientation detection; and to establish USB DFP/UFP roles.

MCU and OTP/MTP ROM

The AP43776 has an MCU subsystem, which integrates an 8-bit 8051 processor, SRAM, and OTP ROM. The MCU subsystem is optimized for user configurability of different topologies, support of different protocols, and low-power consumption at a low cost. With the embedded hardware PHY transceivers offloading MCU processing, the AP43776 can handle two channels of PD handshakes efficiently through an MCU simultaneously, and be compliant with critical USB Power Delivery specifications.

An OTP ROM is provided to store PD, QC, and FCP protocol firmware, and an MTP ROM is provided for user configuration table. Either in-system programming or offline socket programming are provided for the OTP ROM and MTP ROM.

ADC

The AP43776 contains a 10-bit SAR (successive approximation register) ADC for analog to digital conversions. All GPIO inputs can be connected to the internal analog multiplex busses through a switch. With the ADC voltage reference, VREF, being set at 2V, any input voltage, Vin, on the GPIO can be digitized into a 10-bit digital code proportional to Vin/VREF. The sampling rate of ADC is 100KHz, but the firmware re-samples the ADC output by 1ms/time, and some longer de-glitch time is used to qualify the ADC output code. Meanwhile, ADC is used to detect and monitor analog signals on the non-GPIO pins like CC1/CC2/VCONN and DP/DN, and then come out the associated OVP protections.

I2C Interface

For USB Type-C PD charging system, the I2C interface pins (SCK, SDA) are used to communicate between the PD decoder and DC/DC controller/converter to replace analog signal feedback with much higher noise immunity. The AP43776 is in charge of the CC1/CC2 or DP/DN protocol handshake with the attached device, and deliver the voltage and current request to DC/DC controller/converter through I2C bus.

The AP43776, working as an I2C master device, keeps track of charging capability of each USB Type-C port through I2C interface pins at the same time. Based on the user-specified and desired smart power-sharing options for the two charging ports, the AP43776 decides the final charging profiles for each port.

GPIO Support

There are many GPIO pins that can be used to support customization features, like low voltage battery, power derating, thermal power derating, LED light indication, fault status, and so on. The GPIO pin can also be used for UART communication to support four USB Type-C ports, and some GPIOs support current sources for NTC temperature detection.

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Input Voltage at V_{CC} Pin	6.0	V
V_{CC1A}, V_{CC2A}, V_{CC1B}, V_{CC2B}	Input Voltage at CC1_A,CC2_A,CC1_B,CC2_B Pins	24	V
V_{DPA}, V_{DNA}, V_{DPB}, V_{DNB}, SDA, SCL and $GPIO_X$	Input Voltage at DPA, DNA, DPB, DNB, SDA, SCL, and GPIOx Pins	6.0	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	122	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	27	°C/W
ESD	ESD (Human Body Model) Voltage on D+, D- Pins	±6	kV
	ESD (Human Body Model) Voltage on other Pins	±4	kV
	ESD (Charged Device Model)	±1000	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power Supply Voltage	3	5.5	V
T_{OP}	Operating Temperature Range	-40	+85	°C

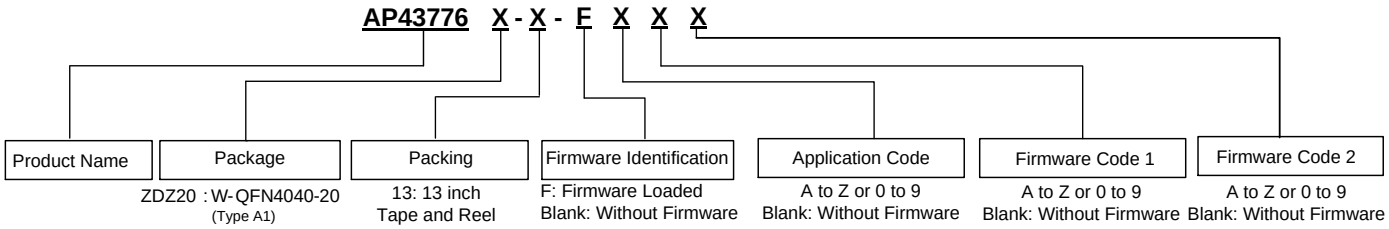
Electrical Characteristics (@ T_A = +25°C, V_{CC} = 5V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC PIN & INTERNAL BIAS SECTION						
V_{CC_OP}	VCC Operation Range	—	3	—	5.5	V
V_{CC_POR}	VCC Power-on Reset Voltage	—	2.0	—	3.1	V
$V_{CC\_POR\ HYS}$	VCC Power-on Hysteresis	—	—	0.1	—	V
I_{SM}	Sleep Mode Current	V_{CC} = 5V @ sleep mode	150	—	1200	μA
I_{CC_OP}	Operating Supply Current	—	1.1	—	3.0	mA
I_{S_SCL}	Sink Current of SCL for impedance check	V_{SCL} = 1V	760	840	920	μA
V_{2V}	Internal Reference Voltage	2.046±5%	1.944	2.046	2.148	V
CLK_{12M}	Internal Clock Frequency	12MHz±10%	10.8	12	13.2	MHz
CC1/CC2 PIN SECTION						
V_{OH_open}	Pull High Voltage of CCx	—	3.4	3.6	3.8	V
I_{rp_330}	Source Current of CCx	R_D = 5.1KΩ	305	330	355	μA
V_{SW_TxDC}	Voltage Swing of CCx for BMC Tx	R_D = 5.1KΩ	1.05	1.125	1.2	V
V_{SW_TxDCL}	Low Voltage Swing of CCx for BMC Tx	R_D = 5.1KΩ	0	--	75	mV
R_{VCONN}	Rds_on of internal Vconn switch			15		Ω
DN/DP PIN SECTION						
V_{DP_APP}	DP Apple mode output voltage	—	2.52	2.8	3.08	V
V_{DN_APP}	DN Apple mode output voltage	—	2.52	2.8	3.08	V
D_{P_DWM20K}	DP 20K pull down resistor	—	18	20	22	kΩ
D_{N_DWM20K}	DN 20K pull down resistor	—	18	20	22	kΩ
$D_{P\_DWM900K}$	DP 900K pull down resistor	—	600	—	1400	kΩ
$D_{N\_DWM900K}$	DN 900K pull down resistor	—	600	—	1400	kΩ
R_{DPDN_short}	DPDN short resistor	—	5	20	40	Ω
R_{DN_IMP}	Impedance check of DN for attach function	—	100	—	350	Ω
DIGITAL I/O PIN SECTION (DP/DN/GPIO1~GPIO8)						
V_{OH}	Logic Output High Level Voltage	Source Current 4mA	V_{CC}-0.2	—	—	V
V_{OL}	Logic Output Low Level Voltage	Sink Current 4mA	—	—	200	mV
I_{S_OTP}	Source Current for OTP Pins (GPIO3 and GPIO4)	—	126	140	154	μA

Electrical Characteristics (@ T_A = +25°C, V_{CC} = 5V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ADC SECTION						
V_{ADC_REF}	ADC Reference Voltage	—	—	2.046	—	V
V_{OFFSET}	ADC Offset Voltage	—	—	±4.0	—	mV
PROTECTION SECTION						
V_{DP_OVP}	$VABCV_{DP\_OVP}$	V_{DP_OVP}	4.1	4.35	4.6	V
V_{DN_OVP}	V_{DN_OVP}	V_{DN_OVP}	4.1	4.35	4.6	V
I_{VCONN_OCP}	VCONN Overcurrent Protection	—	32	48	56	mA

Ordering Information

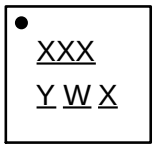


Part Number	Package (Note 6)	Marking ID	13'' Tape and Reel	
			Quantity	Part Number Suffix
AP43776ZDZ20-13	W-QFN4040-20	B4	3000/Tape and Reel	-13

Note: 6. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

(Top View)

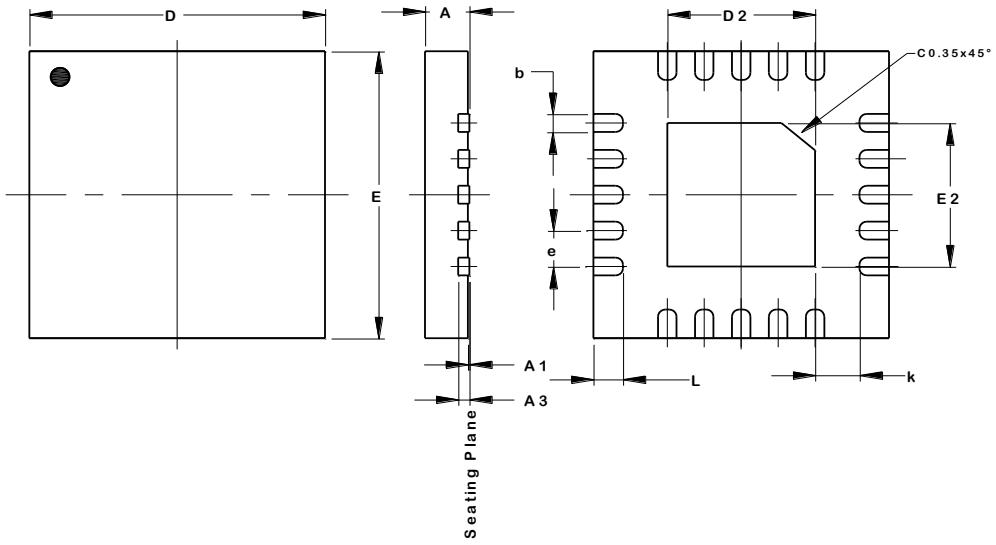


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-20 (Type A1)

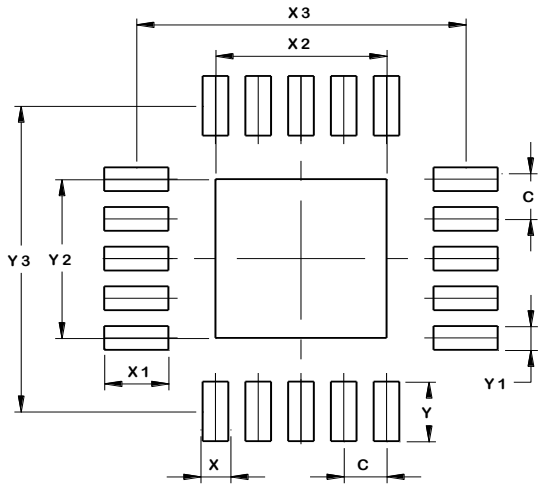


W-QFN4040-20 (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.20	0.30	0.25
D	4.00 BSC		
D2	1.95	2.05	2.00
E	4.00 BSC		
E2	1.95	2.05	2.00
e	0.50 BSC		
k	0.20	--	--
L	0.30	0.50	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-20 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.000
X3	3.850
Y	0.750
Y1	0.300
Y2	2.000
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 (e3)
- Weight: 0.0408 grams (Approximate)