3.8V TO 40V INPUT, 1A LOW IQ SYNCHRONOUS BUCK WITH ADJUSTABLE FREQUENCY

Description

The AP64100 is a 1A, synchronous buck converter with a wide input voltage range of 3.8V to 40V. The device fully integrates a 150mΩ high-side power MOSFET and an 80mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

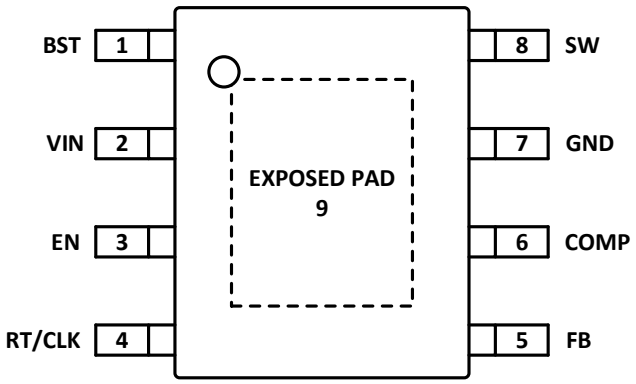
The AP64100 device is easily used by minimizing the external component count due to its adoption of peak current mode control.

The AP64100 design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching. The AP64100 also features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The device is available in an SO-8EP (Standard) package.

Pin Assignments

(Top View)



SO-8EP (Standard)

Features

- VIN: 3.8V to 40V
- Output Voltage (VOUT): 0.8V to VIN
- 1A Continuous Output Current
- 0.8V ± 1% Reference Voltage
- 25μA Low Quiescent Current (Pulse Frequency Modulation)
- Adjustable Switching Frequency: 100kHz to 2.2MHz
- External Clock Synchronization: 100kHz to 2.2MHz
- Up to 88% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Low-Dropout (LDO) Mode
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection (OVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Distributed Power Bus Supplies
- Power Tools and Laser Printers
- White Goods and Small Home Appliances
- Home Audio
- Network Systems
- Consumer Electronics
- General Purpose Point of Load

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

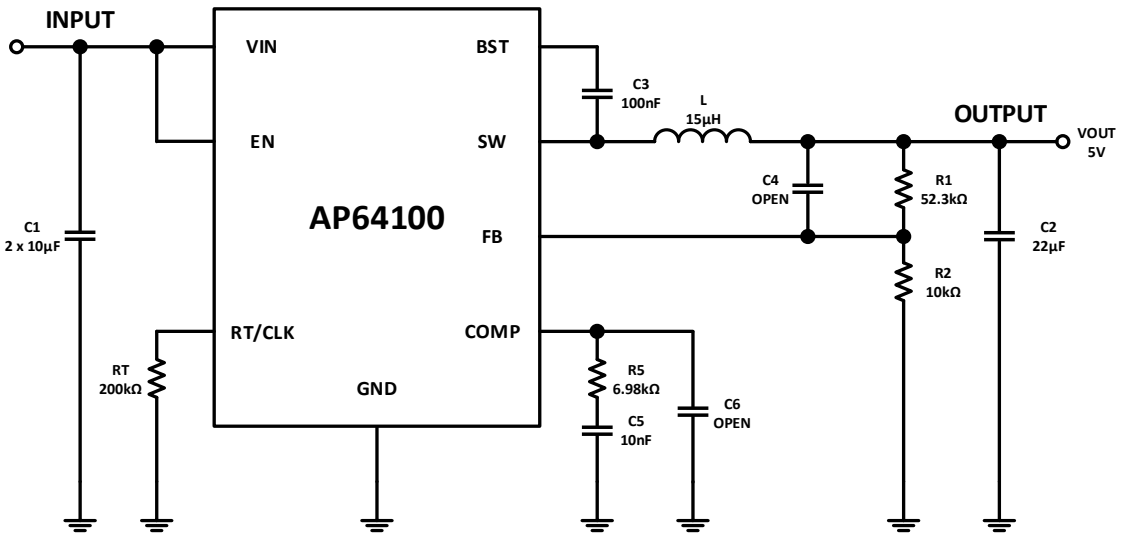


Figure 1. Typical Application Circuit

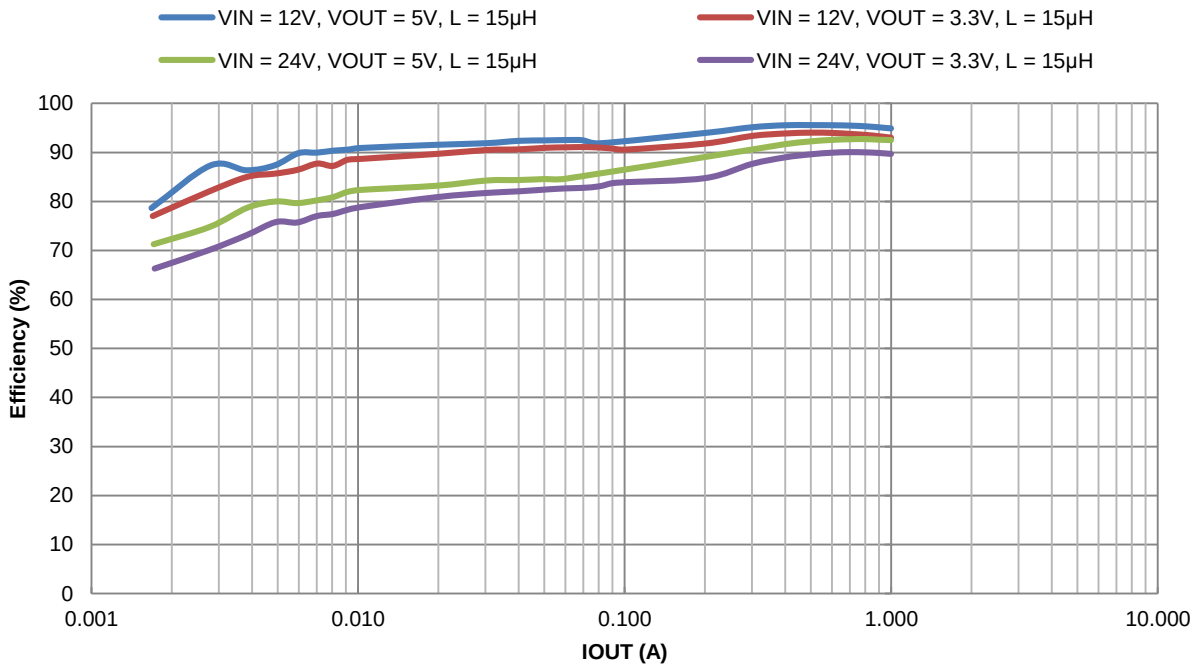


Figure 2. Efficiency vs. Output Current

Pin Descriptions

Pin Name	Pin Number	Function
BST	1	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel power MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.
VIN	2	Power Input. VIN supplies the power to the IC as well as the step-down converter power MOSFETs. Drive VIN with a 3.8V to 40V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
EN	3	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect to VIN or leave floating for automatic startup. The EN has a precision threshold of 1.18V for adjusting the UVLO. See **Enable** section for more details.
RT/CLK	4	Resistor Timing and External Clock. This pin can be used to control the switching frequency by setting the internal oscillator frequency or by synchronizing to an external clock. Connect a resistor from RT/CLK to GND to set the internal oscillator frequency. An external clock can be input directly to the RT/CLK pin and the internal oscillator synchronizes to the external clock frequency using a PLL. If the external clock edges stop, the operating mode automatically returns to the resistor frequency setting. See **Adjusting Switching Frequency** section for more details.
FB	5	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.
COMP	6	Compensation. Connect an external RC network to the COMP pin to adjust the loop response. See **External Loop Compensation Design** section for more details.
GND	7	Power Ground.
SW	8	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
EXPOSED PAD	9	Heat dissipation path of the die. The exposed thermal pad must be electrically connected to GND and must be connected to the ground plane of the PCB for proper operation and optimized thermal performance.

Functional Block Diagram

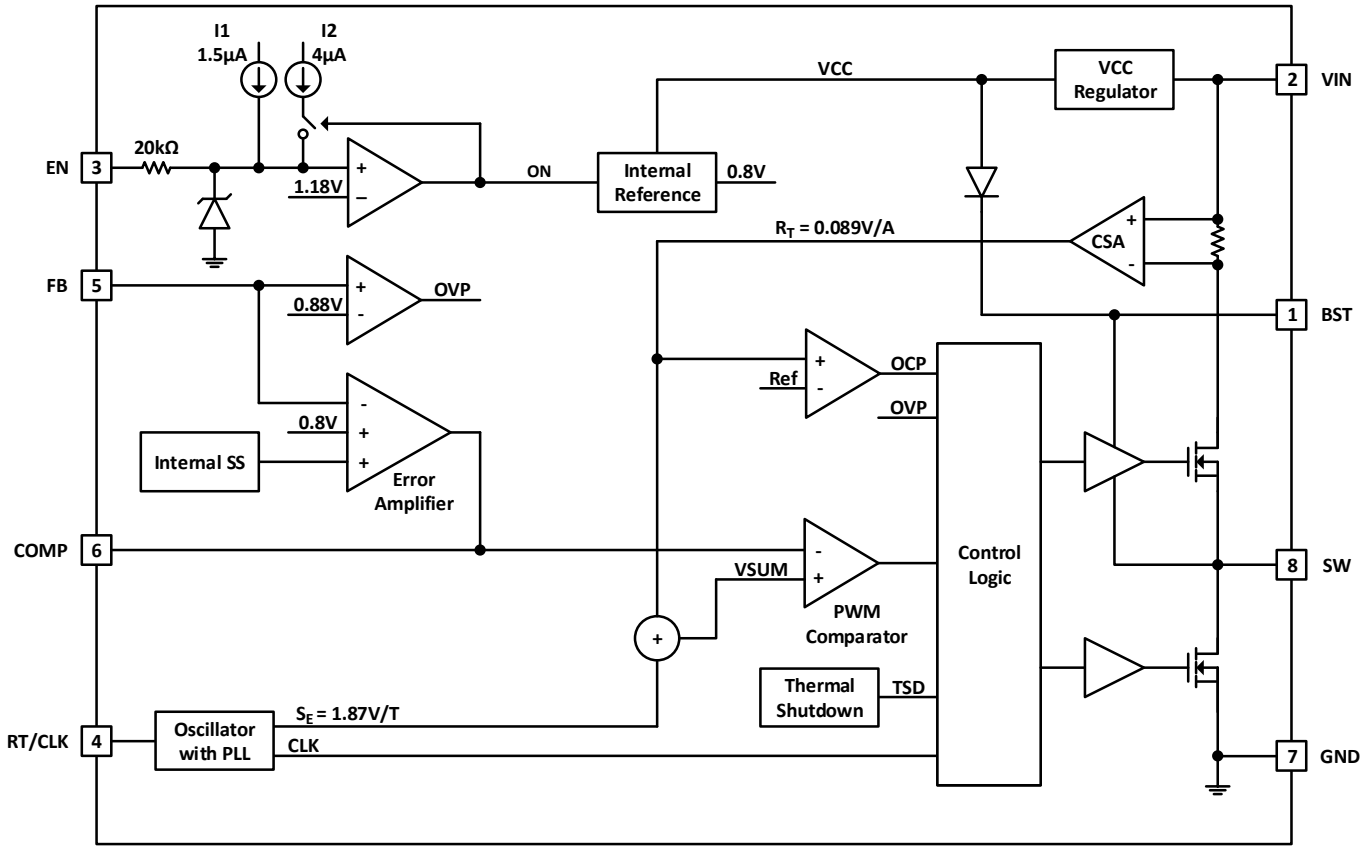


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +42.0 (DC)	V
		-0.3 to +45.0 (400ms)	
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +42.0	V
$V_{RT/CLK}$	RT/CLK Pin Voltage	-0.3 to +6.0	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
V_{COMP}	Compensation Pin Voltage	-0.3 to +6.0	V
V_{SW}	Switch Pin Voltage	-0.3 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±2000	V
CDM	Charged Device Model	±1000	V

Notes: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	SO-8EP (Standard)	45	°C/W
θ_{JC}	Junction to Case	SO-8EP (Standard)	5	°C/W

Note: 6. Test condition for SO-8EP (Standard): Device mounted on FR-4 substrate, four-layer PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	3.8	40	V
VOUT	Output Voltage	0.8	VIN	V
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature	-40	+125	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (@ T_J = +25°C, VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended operating junction temperature range, -40°C to +125°C, and input voltage range, 3.8V to 40V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1	—	μA
I_Q	Quiescent Supply Current	V_{EN} = Floating, R2 = OPEN, No Load, V_{BST} - V_{SW} = 5V	—	25	—	μA
POR	VIN Undervoltage Rising Threshold	—	—	3.5	3.7	V
UVLO	VIN Undervoltage Falling Threshold	—	—	3.1	—	V
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	150	—	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	80	—	mΩ
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 8)	—	1.5	2.2	3.5	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	—	—	2.2	—	A
I_{PFMPK}	PFM Peak Current Limit	—	—	400	—	mA
I_{ZC}	Zero Cross Current Threshold	—	—	60	—	mA
f_{RANGE_RT}	Frequency Range Using RT (Note 8)	—	100	—	2200	kHz
f_{SW}	Oscillator Frequency	RT = 200kΩ (±1%)	450	500	550	kHz
f_{RANGE_CLK}	Frequency Range Using External CLK (Note 8)	—	100	—	2200	kHz
t_{ON_MIN}	Minimum On-Time	—	—	100	—	ns
V_{FB}	Feedback Voltage	CCM	0.792	0.800	0.808	V
V_{EN_H}	EN Logic High Threshold	—	—	1.18	1.25	V
V_{EN_L}	EN Logic Low Threshold	—	1.03	1.09	—	V
I_{EN}	EN Input Current	V_{EN} = 1.5V	—	5.5	—	μA
		V_{EN} = 1V	1	1.5	2	μA
t_{SS}	Soft-Start Time	—	—	2	—	ms
T_{SD}	Thermal Shutdown (Note 8)	—	—	+160	—	°C
T_{Hys}	Thermal Shutdown Hysteresis (Note 8)	—	—	+25	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP64100 @ T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 500kHz (RT = 200kΩ ± 1%), BOM = Table 1, unless otherwise specified.)

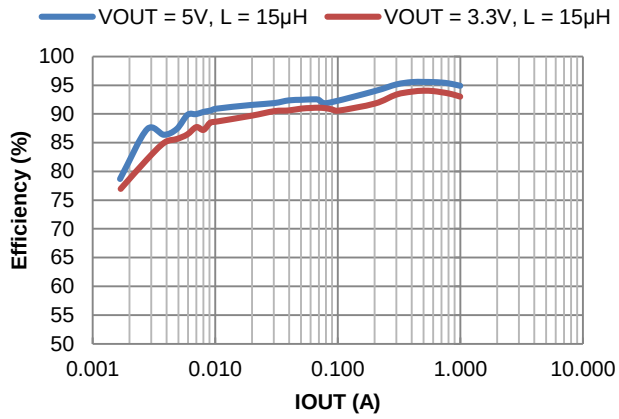


Figure 4. Efficiency vs. Output Current, VIN = 12V

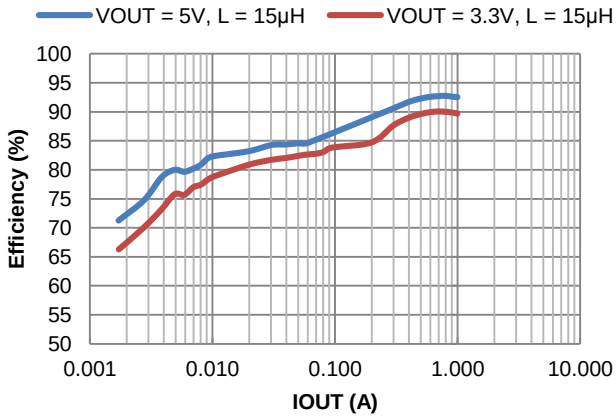


Figure 5. Efficiency vs. Output Current, VIN = 24V

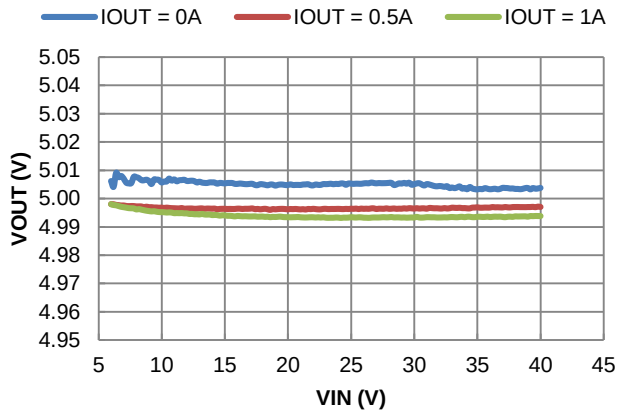


Figure 6. Line Regulation

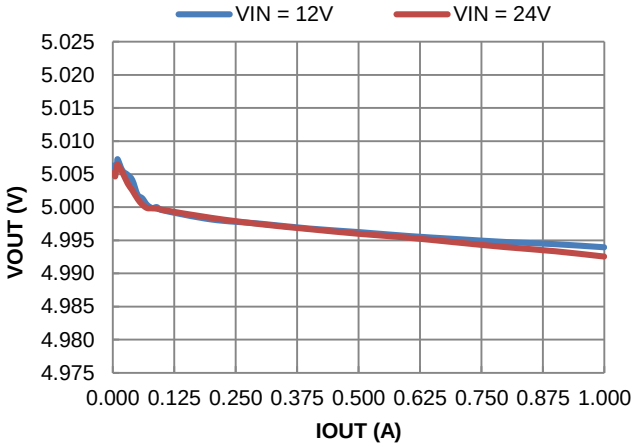


Figure 7. Load Regulation

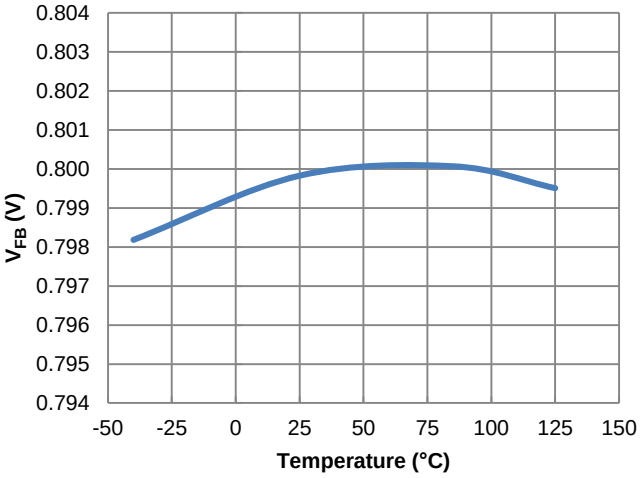


Figure 8. Feedback Voltage vs. Temperature, IOUT = 1A

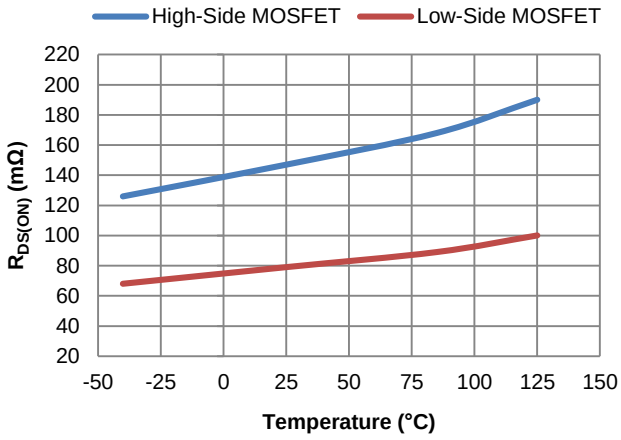


Figure 9. Power MOSFET $R_{DS(ON)}$ vs. Temperature

Typical Performance Characteristics (AP64100 @ T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 500kHz (RT = 200kΩ ± 1%), BOM = Table 1, unless otherwise specified.) (continued)

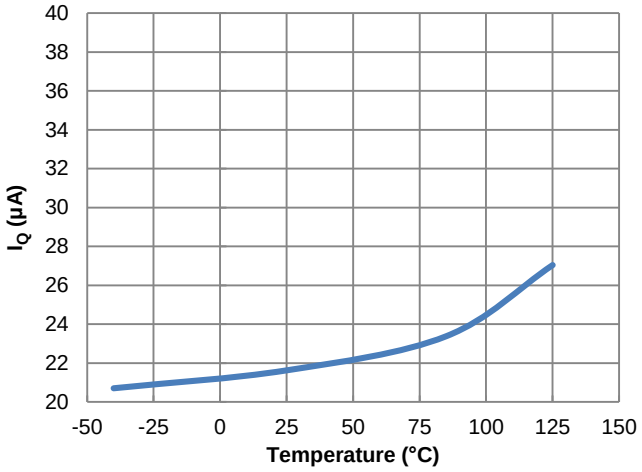


Figure 10. I_Q vs. Temperature

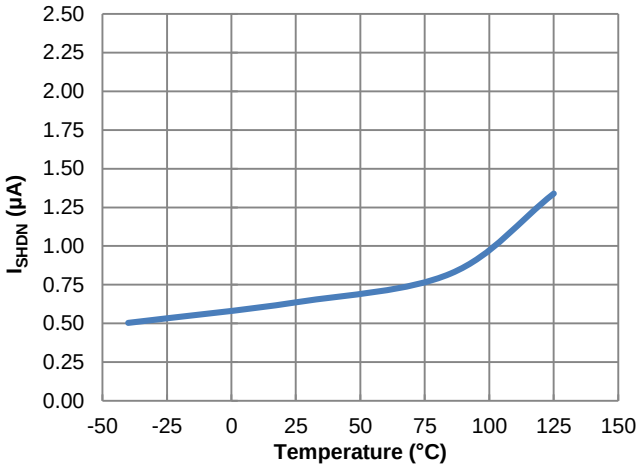


Figure 11. I_{SHDN} vs. Temperature

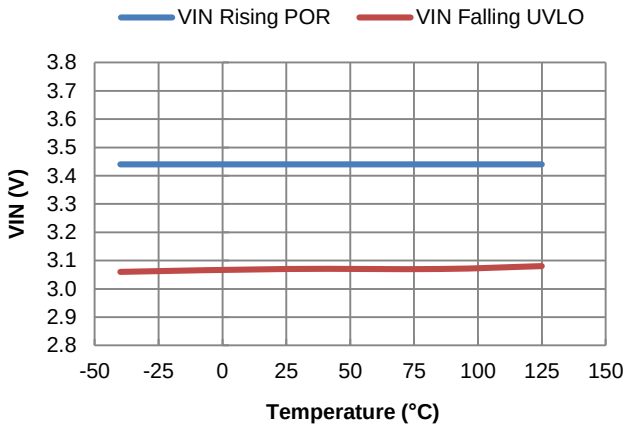


Figure 12. VIN Power-On Reset and UVLO vs. Temperature

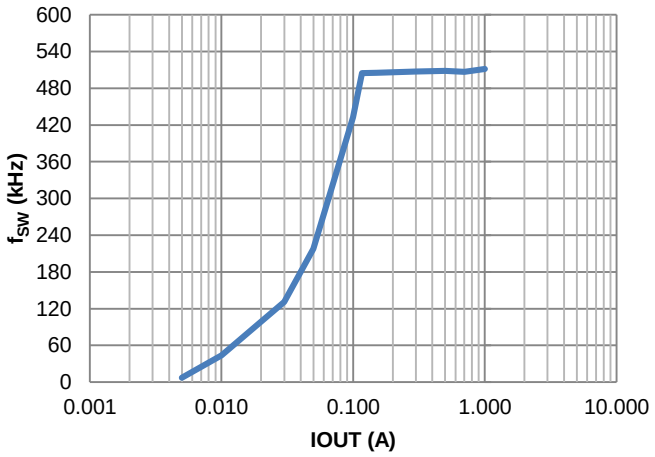


Figure 13. f_{SW} vs. Load

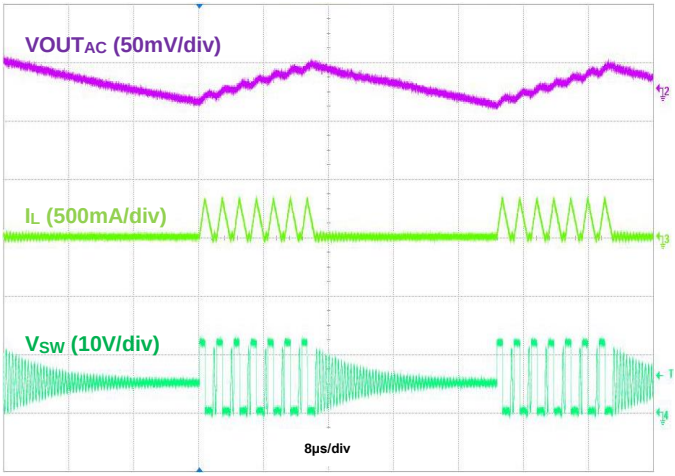


Figure 14. Output Voltage Ripple, VOUT = 5V, IOUT = 50mA

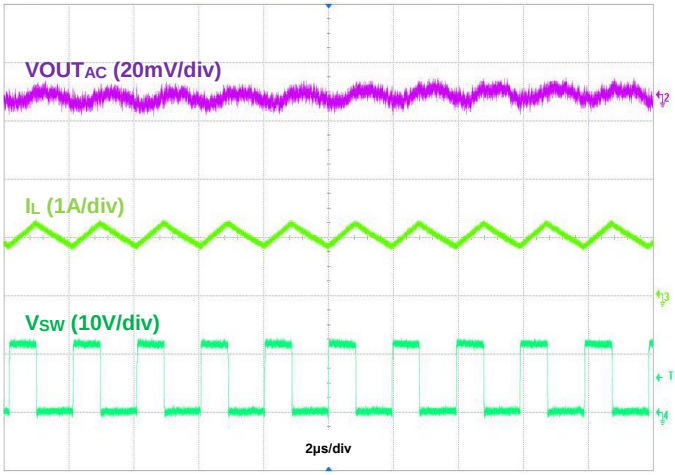


Figure 15. Output Voltage Ripple, VOUT = 5V, IOUT = 1A

Typical Performance Characteristics (AP64100 @ T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 500kHz (RT = 200kΩ ± 1%), BOM = Table 1, unless otherwise specified.) (continued)

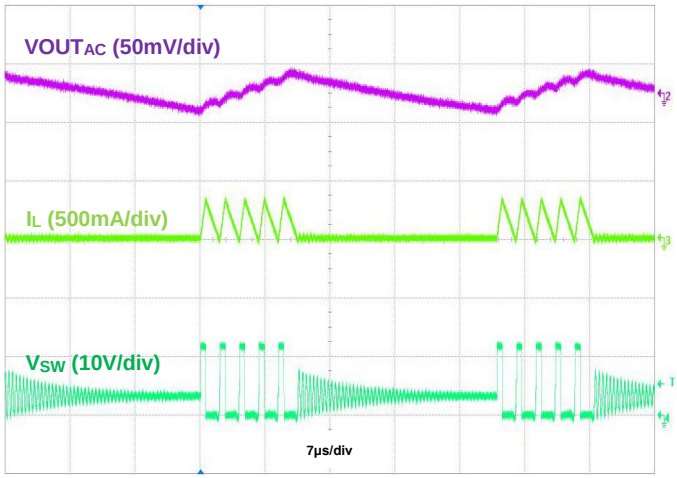


Figure 16. Output Voltage Ripple, VOUT = 3.3V, IOUT = 50mA

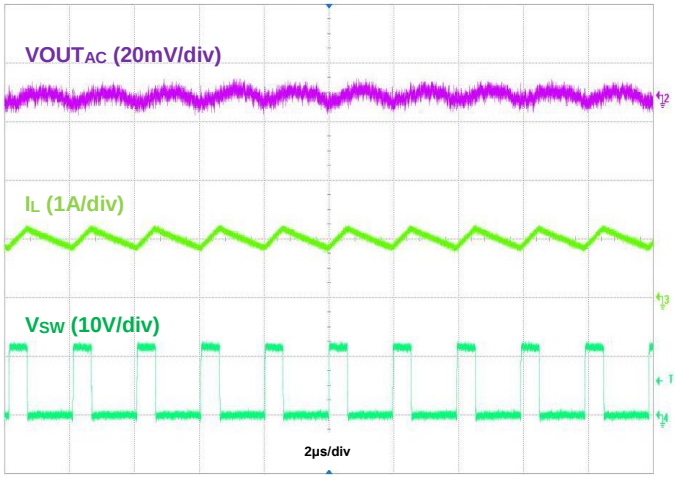


Figure 17. Output Voltage Ripple, VOUT = 3.3V, IOUT = 1A

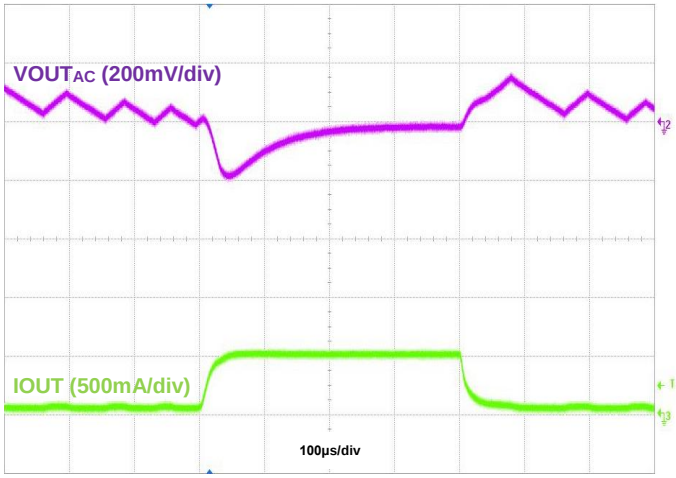


Figure 18. Load Transient, IOUT = 50mA to 500mA to 50mA

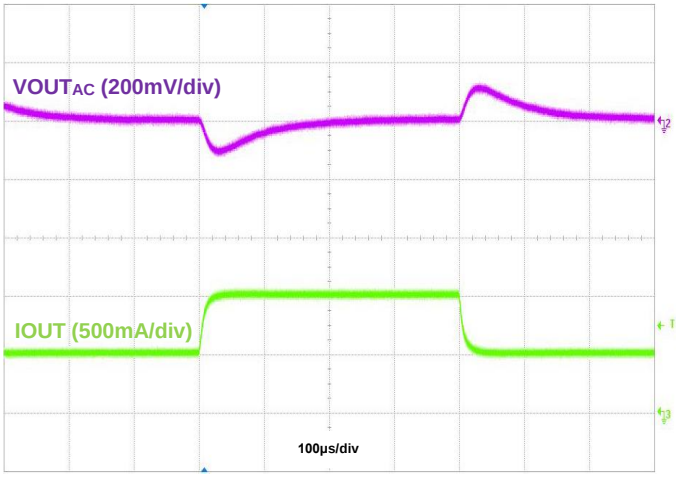


Figure 19. Load Transient, IOUT = 500mA to 1A to 500mA

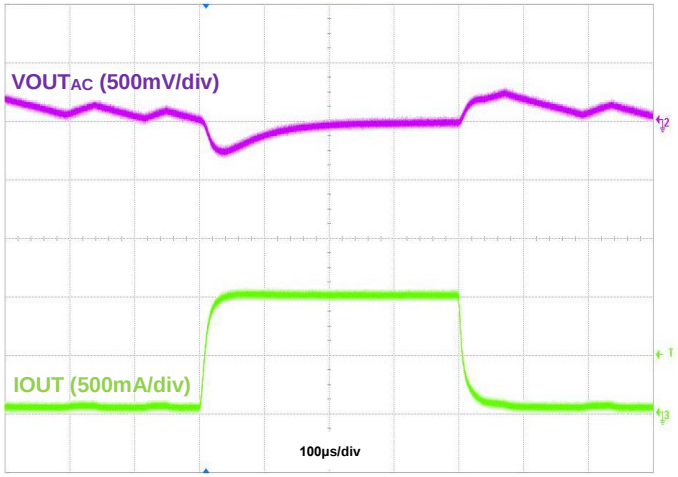


Figure 20. Load Transient, IOUT = 50mA to 1A to 50mA

Typical Performance Characteristics (AP64100 @ T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 500kHz (RT= 200kΩ ± 1%), BOM = Table 1, unless otherwise specified.) (continued)

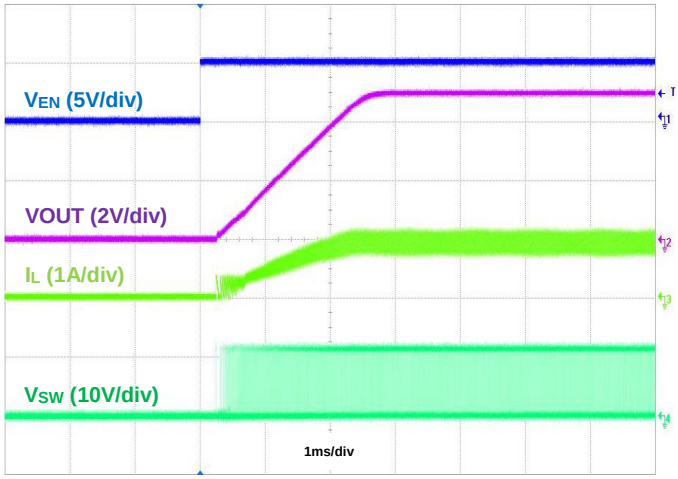


Figure 21. Startup Using EN, IOUT = 1A

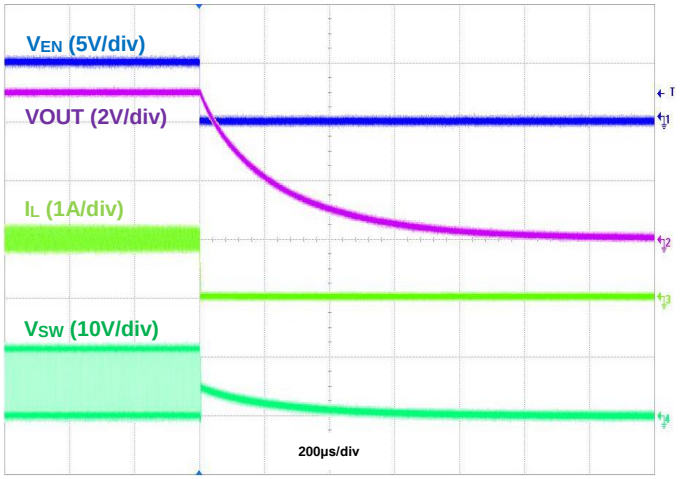


Figure 22. Shutdown Using EN, IOUT = 1A

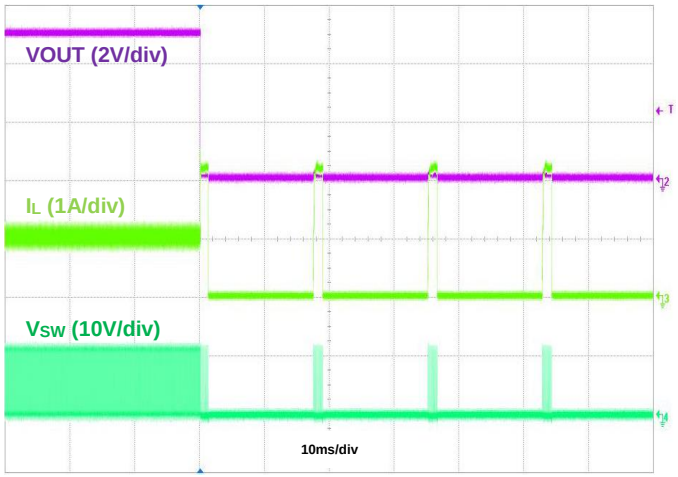


Figure 23. Output Short Protection, IOUT = 1A

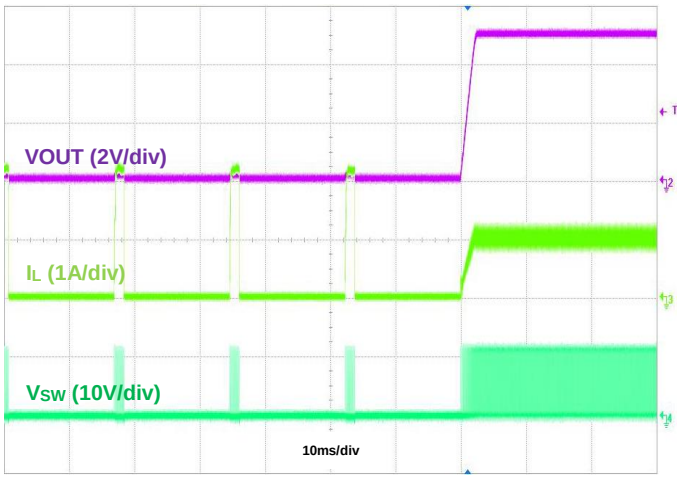


Figure 24. Output Short Recovery, IOUT = 1A

Application Information

1 Pulse Width Modulation (PWM) Operation

The AP64100 device is a 3.8V-to-40V input, 1A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 3. The device employs fixed-frequency peak current mode control. The switching frequency is adjustable from 100kHz to 2.2MHz through either of two modes, resistor timing or external clock synchronization, to allow optimizing either power efficiency or external component size. The internal clock's rising edge initiates turning on the integrated high-side power MOSFET, Q1, for each cycle. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. The current across Q1 is sensed and converted to a voltage with a ratio of R_T via the CSA block. The CSA output is combined with an internal slope compensation, S_E, resulting in V_{SUM}. When V_{SUM} rises higher than the COMP node, the device turns off Q1 and turns on the low-side power MOSFET, Q2. The inductor current decreases when Q2 is on. On the rising edge of next clock cycle, Q2 turns off and Q1 turns on. This sequence repeats every clock cycle.

The error amplifier generates the COMP voltage by comparing the voltage on the FB pin with an internal 0.8V reference. An increase in load current causes the feedback voltage to drop. The error amplifier thus raises the COMP voltage until the average inductor current matches the increased load current. This feedback loop regulates the output voltage. The internal slope compensation circuitry prevents subharmonic oscillation when the duty cycle is greater than 50% for peak current mode control.

The peak current mode control and built-in 2ms soft-start time simplify the AP64100 footprint.

2 Pulse Frequency Modulation (PFM) Operation

In heavy load conditions, the AP64100 operates in forced PWM mode. As the load current decreases, the internal COMP node voltage also decreases. At a certain limit, if the load current is low enough, the COMP node voltage is clamped and is prevented from decreasing any further. The voltage at which COMP is clamped corresponds to the 400mA PFM peak inductor current limit. As the load current approaches zero, the AP64100 enters PFM mode to increase the converter power efficiency at light load conditions. When the inductor current decreases to 60mA, zero cross detection circuitry on the low-side power MOSFET, Q2, forces it off. The buck converter does not sink current from the output when the output load is light and while the device is in PFM. Because the AP64100 works in PFM during light load conditions, it can achieve power efficiency of up to 88% at a 5mA load condition.

The quiescent current of the AP64100 is 25μA typical under a no-load, non-switching condition.

3 Enable

When disabled, the device shutdown supply current is only 1μA. When applying a voltage greater than the EN logic high threshold (typical 1.18V, rising), the AP64100 enables all functions and the device initiates the soft-start phase. The EN pin is a high-voltage pin and can be directly connected to VIN to automatically start up the device as VIN increases. An internal 1.5μA pull-up current source connected from the internal LDO-regulated VCC to the EN pin guarantees that if EN is left floating, the device still automatically enables once the voltage reaches the EN logic high threshold. The AP64100 has a built-in 2ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic low threshold (typical 1.09V, falling), the internal SS voltage discharges to ground and device operation disables.

The EN pin can also be used to adjust the undervoltage lockout thresholds. See **Undervoltage Lockout (UVLO)** section for more details.

Alternatively, a small ceramic capacitor can be added from EN to GND. When EN is not driven externally, this capacitor increases the time needed for the EN pin voltage to reach its logic high threshold, which delays the startup of the output voltage. This is useful when sequencing multiple power rails to minimize input inrush current. When the EN pin voltage starts from 0V, the amount of capacitance for a given delay time is approximated by:

$$C_d[nF] \approx 1.27 \cdot t_d[ms] \quad \text{Eq. 1}$$

Where:

- C_d is the time delay capacitance in nF
- t_d is the delay time in ms

Application Information (continued)

4 Electromagnetic Interference (EMI) Reduction with Ringing-Free Switching Node and Frequency Spread Spectrum (FSS)

In some applications, the system must meet EMI standards. In relation to high frequency radiation EMI noise, the switching node's (SW's) ringing amplitude is especially critical. To dampen high frequency radiated EMI noise, the AP64100 device implements a proprietary, multi-level gate driver scheme that achieves a ringing-free switching node without sacrificing the switching node's rise and fall slew rates as well as the converter's power efficiency.

To further improve EMI reduction, the AP64100 device also implements FSS with a switching frequency jitter of ±6%. FSS reduces conducted and radiated interference at a particular frequency by spreading the switching noise over a wider frequency band and by not allowing emitted energy to stay in any one frequency for a significant period of time.

5 Adjusting Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP64100 device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP64100 disables if the input voltage falls below 3.1V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

Some applications may desire higher VIN UVLO threshold voltages than is provided by the default setup. A 4µA hysteresis pull-up current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO threshold voltages as shown in Figure 25.

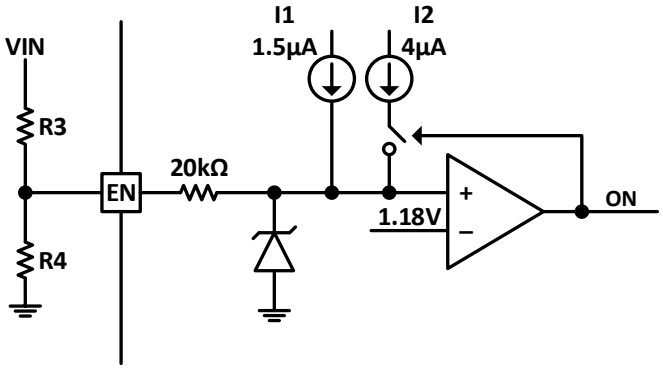


Figure 25. Adjusting UVLO

The resistive divider resistor values are calculated by:

$$R3 = \frac{0.924 \cdot V_{ON} - V_{OFF}}{4.114\mu A} \quad \text{Eq. 2}$$

$$R4 = \frac{1.09 \cdot R3}{V_{OFF} - 1.09V + 5.5\mu A \cdot R3} \quad \text{Eq. 3}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 3.7V
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 3.3V

6 Output Overvoltage Protection (OVP)

The AP64100 implements output OVP circuitry to minimize output voltage overshoots during decreasing load transients. The high-side power MOSFET turns off, and the low-side power MOSFET turns on, when the feedback voltage exceeds 110% of the 0.8V internal reference voltage in order to prevent the output voltage from continuing to increase.

Application Information (continued)

7 Overcurrent Protection (OCP)

The AP64100 has cycle-by-cycle peak current limit protection by sensing the current through the internal high-side power MOSFET, Q1. While Q1 is on, the internal sensing circuitry monitors its conduction current. Once the current through Q1 exceeds the peak current limit, Q1 immediately turns off. If Q1 consistently hits the peak current limit for 512 cycles, the buck converter enters hiccup mode and shuts down. After 8192 cycles of down time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

8 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of +160°C, the AP64100 shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+135°C typical), the device initiates a normal power-up cycle with soft-start.

9 Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$T_{RISE} = P_D \cdot (\theta_{JA}) \quad \text{Eq. 4}$$

Where:

- P_D is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE} \quad \text{Eq. 5}$$

Where:

- T_A is the ambient temperature of the environment

For the SO-8EP (Standard) package, the θ_{JA} is 45°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +125°C when considering the thermal design. Figure 26 shows a typical derating curve versus ambient temperature.

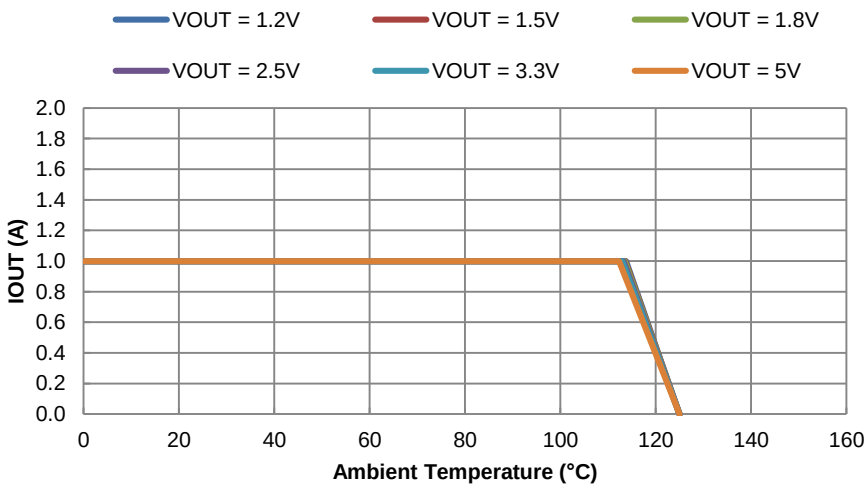


Figure 26. Output Current Derating Curve vs. Ambient Temperature, VIN = 12V, f_{SW} = 500kHz

Application Information (continued)

10 Setting the Output Voltage

The AP64100 has adjustable output voltages, starting from 0.8V, using an external resistive divider. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R1 can be determined by the following equation:

$$\mathbf{R1 = R2 \cdot \left(\frac{VOUT}{0.8V} - 1\right)} \quad \textbf{Eq. 6}$$

Table 1 shows a list of recommended component selections for common AP64100 output voltages referencing Figure 1.

Table 1. Recommended Components Selections, f_{SW} = 500kHz

AP64100										
Output Voltage (V)	**R1 (kΩ)**	**R2 (kΩ)**	**L (µH)**	**C1 (µF)**	**C2 (µF)**	**C3 (nF)**	**C4 (pF)**	**R5 (kΩ)**	**C5 (nF)**	**C6 (pF)**
1.2	4.99	10	6.8	2 x 10	22	100	OPEN	1.69	10	OPEN
1.5	8.66	10	8.2	2 x 10	22	100	OPEN	2.10	10	OPEN
1.8	12.40	10	10.0	2 x 10	22	100	OPEN	2.55	10	OPEN
2.5	21.50	10	10.0	2 x 10	22	100	OPEN	3.48	10	OPEN
3.3	31.60	10	15.0	2 x 10	22	100	OPEN	4.64	10	OPEN
5.0	52.30	10	15.0	2 x 10	22	100	OPEN	6.98	10	OPEN
12.0	140.00	10	33.0	2 x 10	22	100	OPEN	11.3	10	OPEN

11 Adjusting Switching Frequency

The switching frequency of the AP64100 can be set through either of two modes, Resistor Timing or External Clock Synchronization.

In Resistor Timing mode, a resistor is placed between the RT/CLK pin to ground and sets the switching frequency over a wide range from 100kHz to 2.2MHz. The RT/CLK pin voltage is typically 0.5V. The RT/CLK pin cannot be left floating. The RT resistance required for a given switching frequency is calculated by:

$$\mathbf{RT[k\Omega] = \frac{100000}{f_{SW}[kHz]}} \quad \textbf{Eq. 7}$$

Where:

- RT is the resistance in kΩ
- f_{SW} is the switching frequency in kHz between 100kHz to 2.2MHz

FSS is enabled when setting the switching frequency through Resistor Timing mode.

In External Clock Synchronization mode, the switching frequency synchronizes to an external clock applied to the RT/CLK pin. The synchronization frequency range is also 100kHz to 2.2MHz, and the rising edge of SW synchronizes to the falling edge of the external clock at the RT/CLK pin with a typical 66ns delay. An internal PLL locks the internal switching frequency to that of the external clock signal. An external square wave clock signal supplied at the RT/CLK pin must have a logic high level greater than 3.5V, a logic low level less than 0.4V, and a pulse width of at least 80ns.

FSS is disabled when setting the switching frequency through External Clock Synchronization mode.

Application Information (continued)

11 Adjusting Switching Frequency (continued)

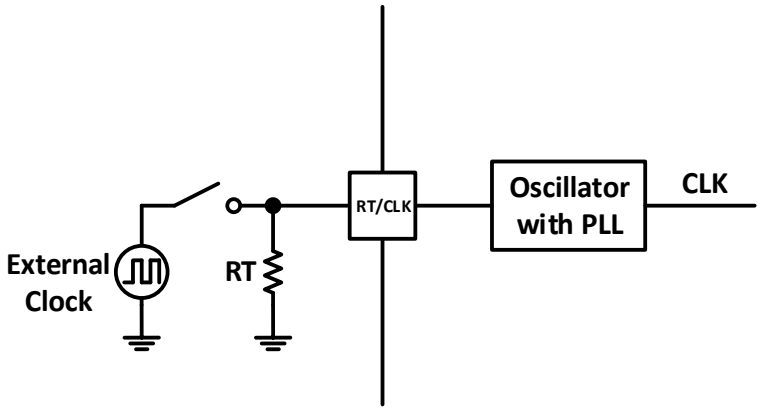


Figure 27. Switching Between Resistor Timing and External Clock Synchronization Modes

In applications where both Resistor Timing and External Clock Synchronization modes are required, the device can be configured as shown in Figure 27. Before an external clock signal is available at the RT/CLK pin, the device operates in Resistor Timing mode. When an external clock is supplied to the RT/CLK pin, the device automatically transitions from Resistor Timing mode to External Clock Synchronization mode typically within 85µs. When the external clock signal is disconnected from the RT/CLK pin, the device's switching frequency returns to being set in Resistor Timing mode. When switching between Resistor Timing and External Clock Synchronization modes, it is recommended that the external clock signal is within ±25% of the frequency controlling the device in Resistor Timing mode to prevent large changes in switching frequency within the device.

12 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{SW}}} \quad \textbf{Eq. 8}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For the AP64100, choose ΔI_L to be 30% to 40% of the maximum load current of 1A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2}} \quad \textbf{Eq. 9}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 6.8µH to 33µH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 50mΩ. Use a larger inductance for improved efficiency under light load conditions.

Application Information (continued)

13 Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor of 20µF or greater is sufficient for most applications.

14 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and enters 100% duty cycle to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and sets the on-time to minimum to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{SW}} \cdot \mathbf{COUT}} \right) \quad \textbf{Eq. 10}$$

Output capacitors with large capacitance and low ESR are the best option. For most applications, a total capacitance of 22µF using ceramic capacitors is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})} \right) \quad \textbf{Eq. 11}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

15 Bootstrap Capacitor and Low-Dropout (LDO) Operation

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins to supply the drive voltage for the high-side power MOSFET. A 100nF ceramic capacitor is sufficient. If the bootstrap capacitor voltage falls below 2.3V, the boot undervoltage protection circuit turns Q2 on for 300ns to refresh the bootstrap capacitor and raise its voltage back above 2.55V. The bootstrap capacitor threshold voltage is always maintained to ensure enough driving capability for Q1. This operation may arise during long periods of no switching such as in PFM with light load conditions. Another event that requires the refreshing of the bootstrap capacitor is when the input voltage drops close to the output voltage. Under this condition, the regulator enters low-dropout mode by holding Q1 on for multiple clock cycles. To prevent the bootstrap capacitor from discharging, Q2 is forced to refresh. The effective duty cycle is approximately 100% so that it acts as an LDO to maintain the output voltage regulation.

Application Information (continued)

16 External Loop Compensation Design

When the COMP pin is not connected to GND, the COMP pin is active for external loop compensation. The regulator uses a constant frequency, peak current mode control architecture to achieve a fast loop response. The inductor is not considered as a state variable since its peak current is constant. Thus, the system becomes a single-order system. For loop stabilization, it is simpler to design a Type II compensator for current mode control than it is to design a Type III compensator for voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 28 shows the small signal model of the synchronous buck regulator.

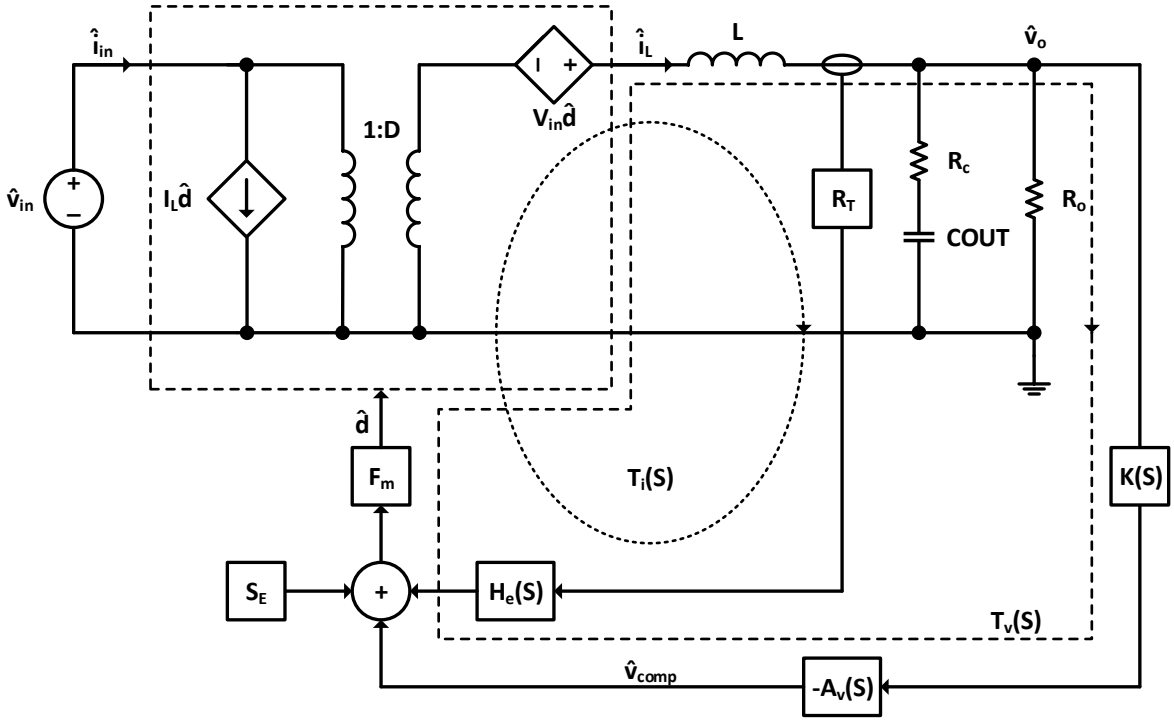


Figure 28. Small Signal Model of Buck Regulator

Where:

- $T_v(S)$ is the voltage loop
- $T_i(S)$ is the current loop
- K(S) is the voltage sense gain
- $-A_v(S)$ is the feedback compensation gain
- $H_e(S)$ is the current sampling function
- F_m is the PWM comparator gain
- V_{in} is the DC input voltage
- D is the duty cycle
- R_c is the ESR of the output capacitor, COUT
- R_o is the output load resistance
- $\hat{v}_{in}$ is the AC small-signal input voltage
- $\hat{i}_{in}$ is the AC small-signal input current
- $\hat{d}$ is the modulation of the duty cycle
- $\hat{i}_L$ is the AC small signal of the inductor current
- $\hat{v}_o$ is the AC small signal of output voltage
- $\hat{v}_{comp}$ is the AC small signal voltage of the compensation network

Application Information (continued)

16 External Loop Compensation Design (continued)

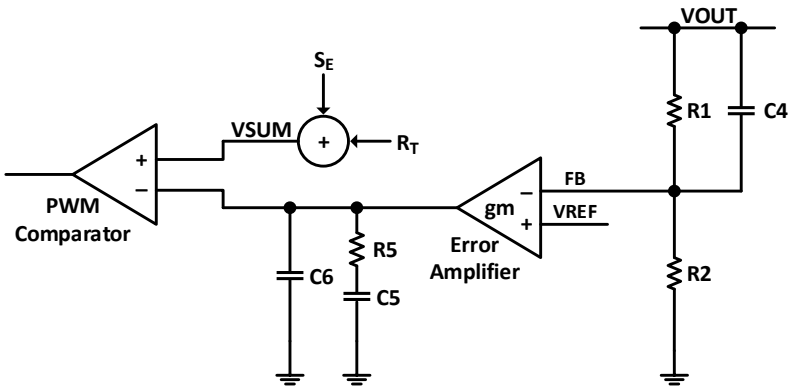


Figure 29. Type II Compensator

Figure 29 shows a Type II compensator. Its transfer function is expressed in the following equation:

$$\mathbf{A_v(S) \cdot K(S) = \frac{gm \cdot R5}{S \cdot (C5 + C6) \cdot (R1 + R2)} \frac{\left(1 + \frac{S}{\omega_{z1}}\right)\left(1 + \frac{S}{\omega_{z2}}\right)}{\left(1 + \frac{S}{\omega_{p1}}\right)\left(1 + \frac{S}{\omega_{p2}}\right)}} \quad \textbf{Eq. 12}$$

Where the poles and zeroes are:

$$\mathbf{\omega_{z1} = \frac{1}{R5 \cdot C5}} \quad \textbf{Eq. 13}$$

$$\mathbf{\omega_{z2} = \frac{1}{R1 \cdot C4}} \quad \textbf{Eq. 14}$$

$$\mathbf{\omega_{p1} = \frac{C5 + C6}{R5 \cdot C5 \cdot C6}} \quad \textbf{Eq. 15}$$

$$\mathbf{\omega_{p2} = \frac{R1 + R2}{R1 \cdot R2 \cdot C4}} \quad \textbf{Eq. 16}$$

The goal of loop compensation design is to achieve:

- High DC Gain
- Gain Margin less than -10dB
- Phase Margin greater than 45°
- Loop Bandwidth Crossover Frequency (f_C) less than 10% of f_{SW}

Application Information (continued)

16 External Loop Compensation Design (continued)

The loop gain at the crossover frequency has unity gain. Therefore, the compensator resistance, R5, is determined by:

$$R5 = \frac{2\pi \cdot f_C \cdot VOUT \cdot C_O \cdot R_T}{g_m \cdot V_{FB}} = 4.67x10^3[\frac{\Omega}{A}] \cdot f_C \cdot VOUT \cdot COUT \quad \text{Eq. 17}$$

Where:

- g_m is 0.15mS
- R_T is 0.089V/A
- V_{FB} is 0.8V
- f_C is the desired crossover frequency

Be aware that most ceramic capacitors will degrade with voltage stress or temperature extremes. Refer to its datasheet and use its worst case capacitance value for calculations.

The compensation capacitors C5 and C6 are then equal to:

$$C5 = \frac{VOUT \cdot COUT}{IOUT \cdot R5} \quad \text{Eq. 18}$$

$$C6 = \max\left(\frac{R_C \cdot C_O}{R5}, \frac{1}{\pi \cdot f_{SW} \cdot R5}\right) \quad \text{Eq. 19}$$

Where:

- IOUT is the output load current

The inclusion of C6 can increase gain margin and can decrease phase margin. In most cases, C6 is optional and may be omitted.

The zero, ω_{z2}, is optional as it can increase both the phase margin and gain bandwidth and can decrease gain margin. If used, place this zero at around two to five times f_C. Thus, C4 is in the approximate range of:

$$C4 = \left[\frac{1}{10\pi \cdot f_C \cdot R1}, \frac{1}{4\pi \cdot f_C \cdot R1}\right] \quad \text{Eq. 20}$$

Application Information (continued)

16 External Loop Compensation Design (continued)

The following is an example of how to choose component values for external loop compensation. Actual component values used in the application circuit may vary slightly from the calculated first-order approximation equations.

Let the following conditions be defined:

- VIN = 12V
- VOUT = 2.5V
- IOUT = 1A
- f_{SW} = 500kHz
- f_C = 20kHz
- R1 = 21.5kΩ
- R2 = 10kΩ
- L = 10µH
- C2 = 22µF (Effectively, COUT ≈ 15µF)
- R_C ≈ 5mΩ

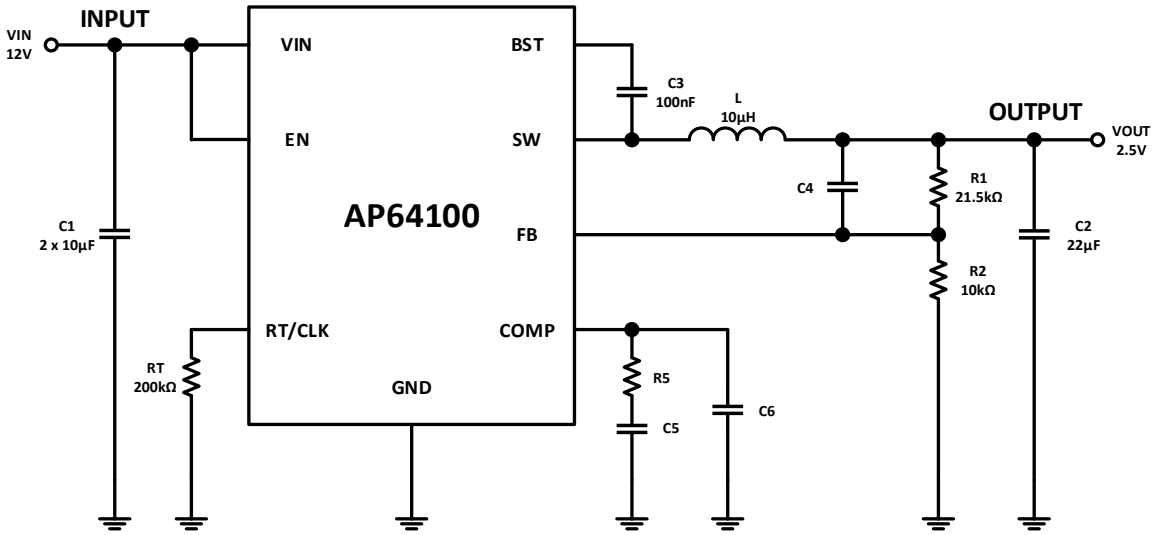


Figure 30. Example Circuit for Loop Compensation Calculations

The calculations of the main component values involved in the external loop compensation, R5 and C5, are required. If the optional C4 and C6 capacitors are used, their calculations are also required.

Application Information (continued)

16 External Loop Compensation Design (continued)

From Eq. 17, the value of R5 is calculated as:

$$\begin{aligned} \mathbf{R5} &= \mathbf{4.67x10^3}[\frac{\mathbf{\Omega}}{\mathbf{A}}] \cdot \mathbf{f_C} \cdot \mathbf{VOUT} \cdot \mathbf{COUT} \\ &= \mathbf{4.67x10^3}\left[\frac{\mathbf{\Omega}}{\mathbf{A}}\right] \cdot \mathbf{20kHz} \cdot \mathbf{2.5V} \cdot \mathbf{15\mu F} \\ &\approx \mathbf{3.50k\Omega} \end{aligned}$$

Choose a standard resistor value for R5 close to its calculated value. For example, choose R5 to be 3.48kΩ.

From Eq. 18, C5 is calculated as:

$$\begin{aligned} \mathbf{C5} &= \frac{\mathbf{VOUT} \cdot \mathbf{COUT}}{\mathbf{IOUT} \cdot \mathbf{R5}} \\ &= \frac{\mathbf{2.5V} \cdot \mathbf{15\mu F}}{\mathbf{1A} \cdot \mathbf{3.48k\Omega}} \\ &\approx \mathbf{10.78nF} \end{aligned}$$

Choose a standard capacitor value for C5 close to its calculated value. For example, choose C5 to be 10nF.

From Eq. 19, C6 is calculated as:

$$\begin{aligned} \mathbf{C6} &= \mathbf{max}\left(\frac{\mathbf{R_C} \cdot \mathbf{COUT}}{\mathbf{R5}}, \frac{\mathbf{1}}{\mathbf{\pi} \cdot \mathbf{f_{SW}} \cdot \mathbf{R5}}\right) \\ &= \mathbf{max}\left(\frac{\mathbf{5m\Omega} \cdot \mathbf{15\mu F}}{\mathbf{3.48k\Omega}}, \frac{\mathbf{1}}{\mathbf{\pi} \cdot \mathbf{500kHz} \cdot \mathbf{3.48k\Omega}}\right) \\ &\approx \mathbf{max}(\mathbf{21.55pF}, \mathbf{182.94pF}) \\ &= \mathbf{182.94pF} \end{aligned}$$

C6 is optional. If used, choose a standard capacitor value for C6 close to its calculated value. For example, choose C6 to be 180pF. However, use of C6 in the final example circuit will be omitted.

From Eq. 20, the approximate range of C4 is calculated as:

$$\begin{aligned} \mathbf{C4} &= \left[\frac{\mathbf{1}}{\mathbf{10\pi} \cdot \mathbf{f_C} \cdot \mathbf{R1}}, \frac{\mathbf{1}}{\mathbf{4\pi} \cdot \mathbf{f_C} \cdot \mathbf{R1}}\right] \\ &= \left[\frac{\mathbf{1}}{\mathbf{10\pi} \cdot \mathbf{20kHz} \cdot \mathbf{21.5k\Omega}}, \frac{\mathbf{1}}{\mathbf{4\pi} \cdot \mathbf{20kHz} \cdot \mathbf{21.5k\Omega}}\right] \\ &= [\mathbf{74.0pF}, \mathbf{185.1pF}] \end{aligned}$$

C4 is optional. If used, choose a standard capacitor value for C4 that is close to its calculated range. For example, choose C4 to be 180pF. However, use of C4 in the final example circuit will be omitted.

Application Information (continued)

16 External Loop Compensation Design (continued)

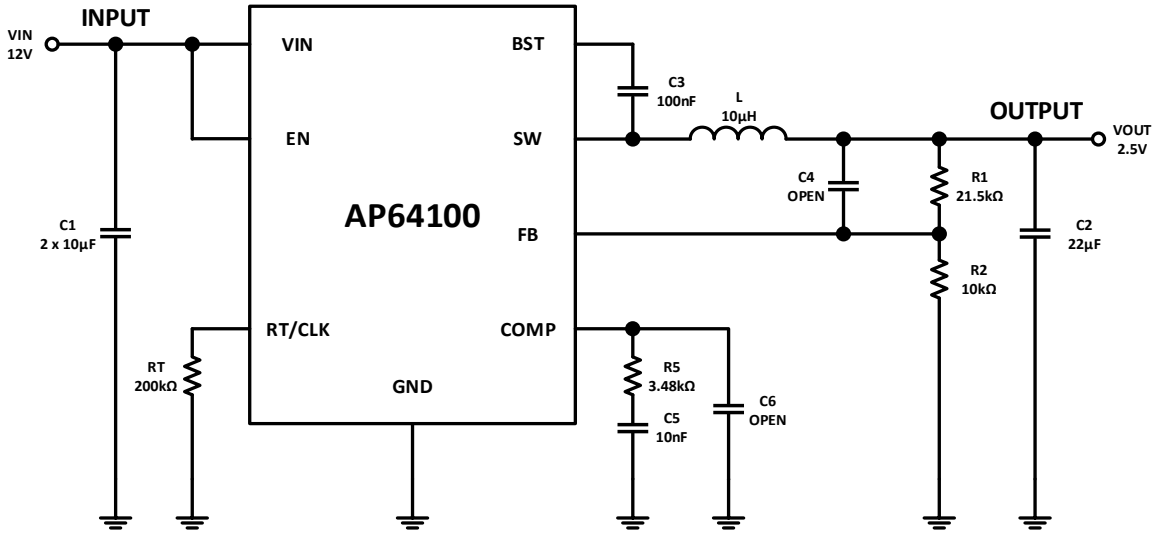


Figure 31. Example Circuit with Calculated Component Values for Loop Compensation

The first-order calculated loop response has the following characteristics:

- Bandwidth is around 13.2kHz
- Phase Margin is around 74.4°
- Gain Margin is around -12.6dB

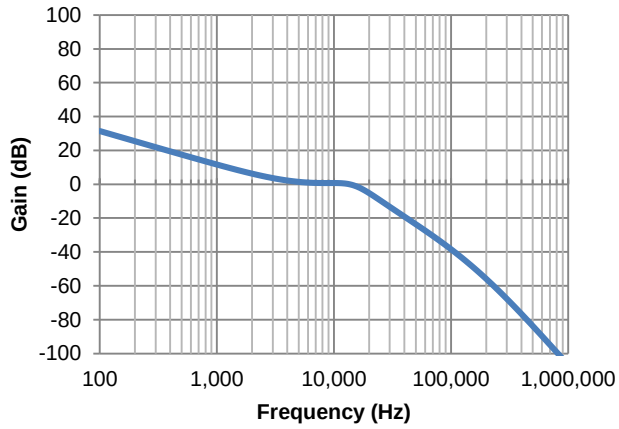


Figure 32. Closed-Loop Bandwidth

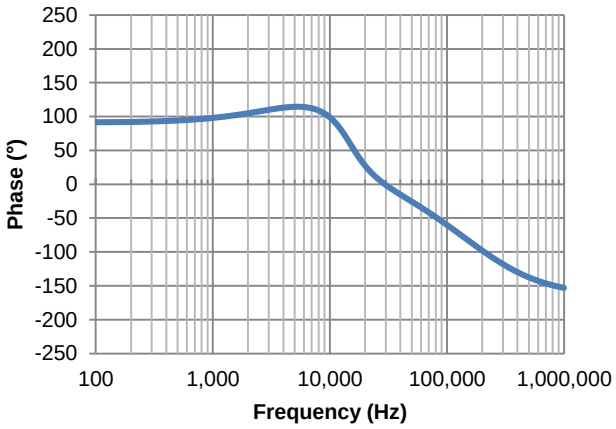


Figure 33. Closed-Loop Phase Margin

Layout

PCB Layout

1. The AP64100 works at 1A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 34 for more details.

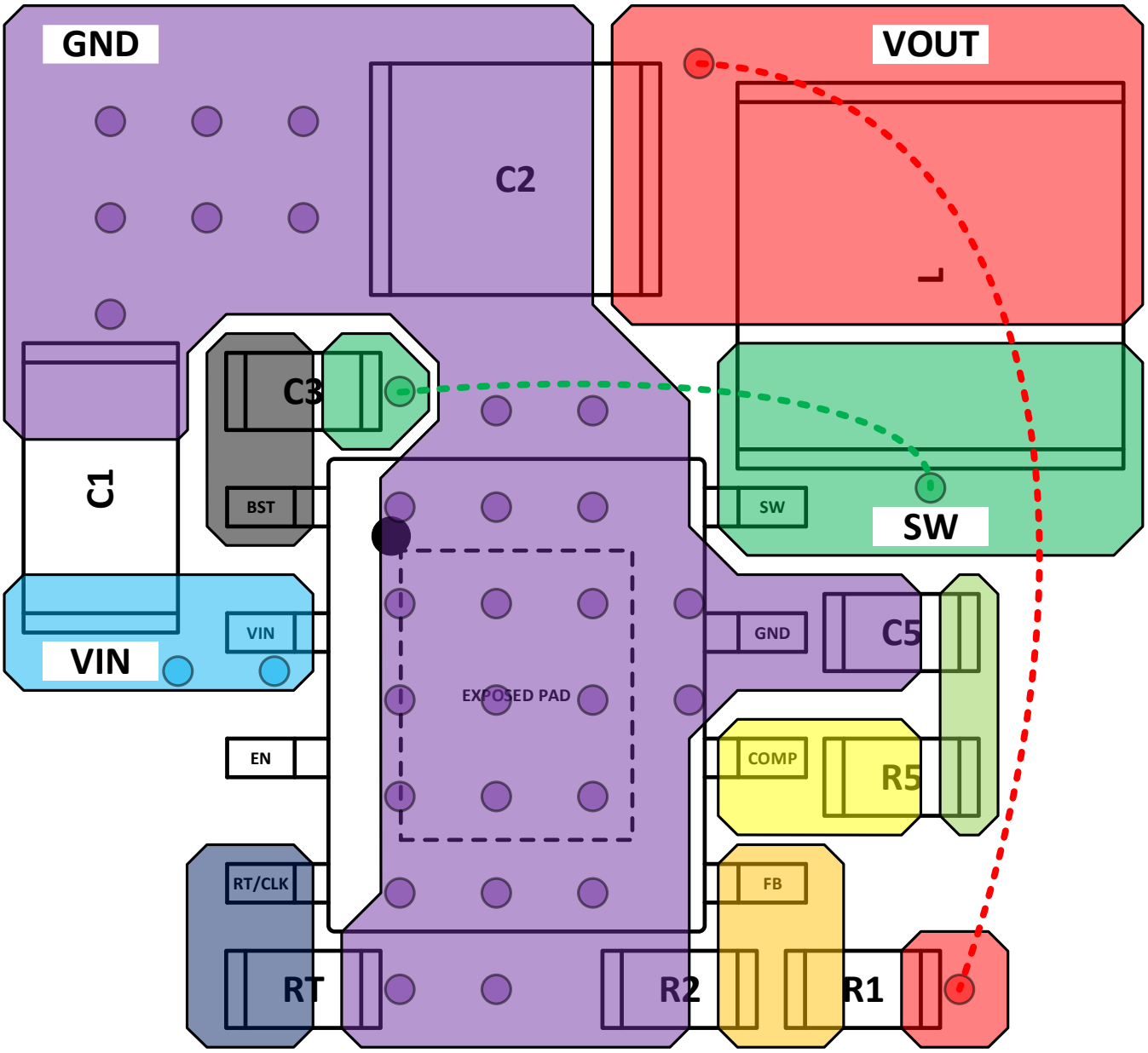
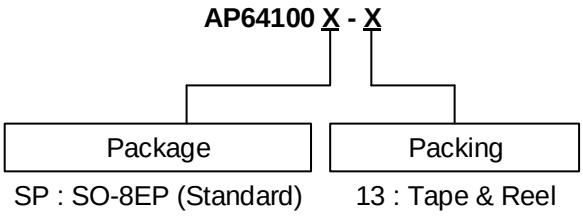


Figure 34. Recommended PCB Layout

Ordering Information

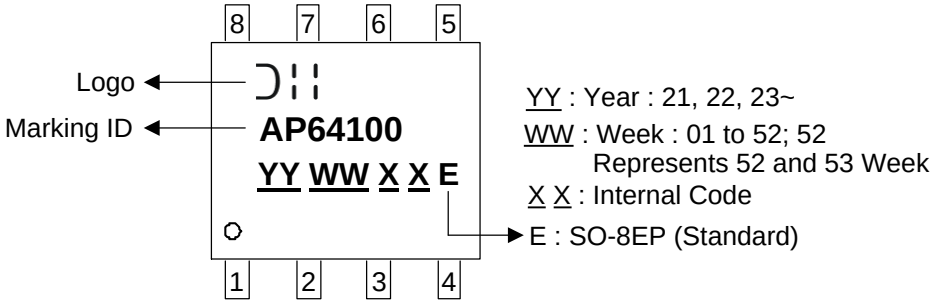


Part Number	Package Code	Tape and Reel	
		Quantity	Part Number Suffix
AP64100SP-13	SP	4,000	-13

Marking Information

SO-8EP (Standard)

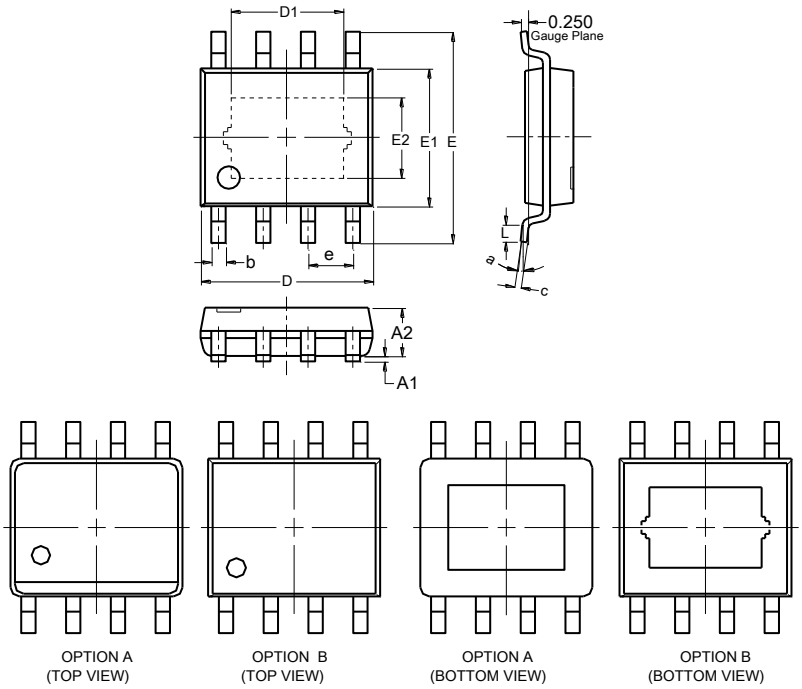
(Top View)



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP (Standard)

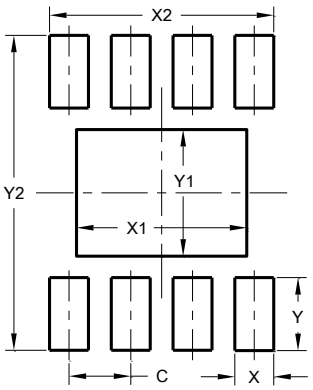


SO-8EP (Standard)			
Dim	**Min**	**Max**	**Typ**
A1	0.00	0.13	—
A2	1.35	1.55	1.45
b	0.30	0.51	0.40
c	0.15	0.25	0.20
D	4.70	5.10	4.90
D1	2.75	3.35	3.05
E	5.80	6.20	6.00
E1	3.80	4.00	3.85
E2	2.11	2.71	2.41
e	—	—	1.27
L	0.40	1.27	0.72
a	0°	8°	4°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP (Standard)



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.081 grams (Approximate)