ProASIC^PLUS® Flash Family FPGAs

FlashLock

Features and Benefits

High Capacity

Commercial and Industrial

- 75,000 to 1 Million System Gates
- 27 K to 198 Kbits of Two-Port SRAM
- 66 to 712 User I/Os

Military

- 300, 000 to 1 Million System Gates
- 72 K to 198 Kbits of Two Port SRAM
- 158 to 712 User I/Os

Reprogrammable Flash Technology

- 0.22 µm 4 LM Flash-Based CMOS Process
- Live At Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/Up Cycles
- Mil/Aero Devices Operate over Full Military Temperature Range

Performance

- 3.3 V, 32-Bit PCI, up to 50 MHz (33 MHz over military temperature)
- Two Integrated PLLs
- External System Performance up to 150 MHz

Secure Programming

- The Industry's Most Effective Security Key (FlashLock®)

Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

High Performance Routing Hierarchy

- Ultra-Fast Local and Long-Line Network
- High-Speed Very Long-Line Network
- High-Performance, Low Skew, Splittable Global Network
- 100% Routability and Utilization

I/O

- Schmitt-Trigger Option on Every Input
- 2.5 V / 3.3 V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin-Compatible Packages across the ProASIC^PLUS Family

Unique Clock Conditioning Circuitry

- PLL with Flexible Phase, Multiply/Divide, and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

Standard FPGA and ASIC Design Flow

- Flexibility with Choice of Industry-Standard Front-End Tools
- Efficient Design through Front-End Timing and Gate Optimization

ISP Support

- In-System Programming (ISP) via JTAG Port

SRAMs and FIFOs

- SmartGen Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- 24 SRAM and FIFO Configurations with Synchronous and Asynchronous Operation up to 150 MHz (typical)

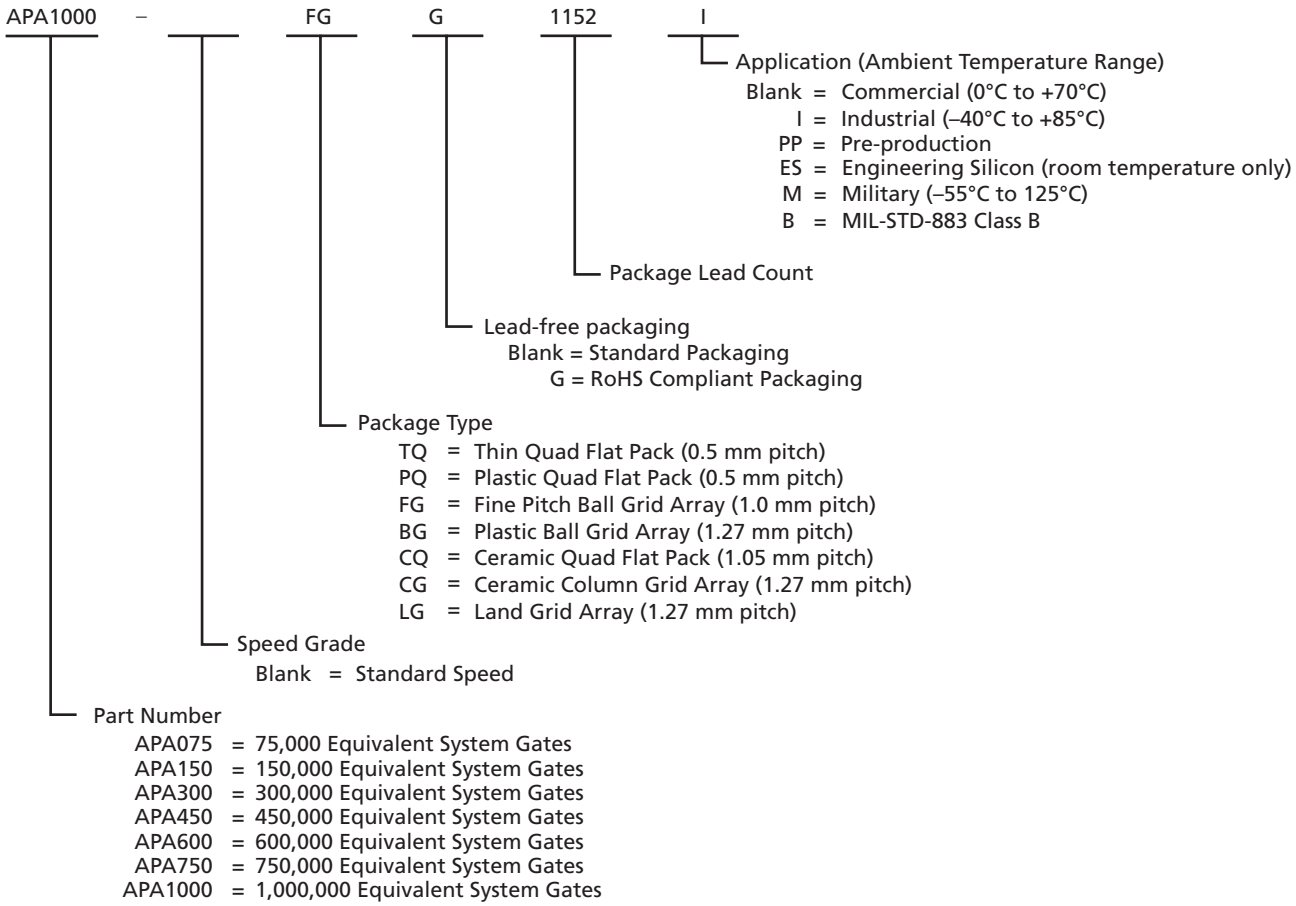
Table 1 • **ProASIC^PLUS Product Profile**

Device	APA075	APA150	APA300[1]	APA450	APA600[1]	APA750	APA1000[1]
Maximum System Gates	75,000	150,000	300,000	450,000	600,000	750,000	1,000,000
Tiles (Registers)	3,072	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM Bits (k=1,024 bits)	27 k	36k	72 k	108 k	126 k	144 k	198 k
Embedded RAM Blocks (256x9)	12	16	32	48	56	64	88
LVPECL	2	2	2	2	2	2	2
PLL	2	2	2	2	2	2	2
Global Networks	4	4	4	4	4	4	4
Maximum Clocks	24	32	32	48	56	64	88
Maximum User I/Os	158	242	290	344	454	562	712
JTAG ISP	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package (by pin count)							
TQFP	100, 144	100	–	–	–	–	–
PQFP	208	208	208	208	208	208	208
PBGA	–	456	456	456	456	456	456
FBGA	144	144, 256	144, 256	144, 256, 484	256, 484, 676	676, 896	896, 1152
CQFP[2]			208, 352		208, 352		208, 352
CCGA/LGA[2]					624		624

Notes:

1. *Available as Commercial/Industrial and Military/MIL-STD-883B devices.*
2. *These packages are available only for Military/MIL-STD-883B devices.*

Ordering Information



Device Resources

	User I/Os[2]												
	Commercial/Industrial										Military/MIL-STD-883B		
Device	TQFP[3] 100-Pin	TQFP[3] 144-Pin	PQFP[3] 208-Pin	PBGA[3] 456-Pin	FBGA[3] 144-Pin	FBGA[3] 256-Pin	FBGA[3] 484-Pin	FBGA[3] 676-Pin	FBGA[3] 896-Pin	FBGA[3] 1152-Pin	CQFP 208-Pin	CQFP 352-Pin	CCGA/ LGA 624-Pin
APA075	66	107	158		100								
APA150	66		158	242	100	186 [4]							
APA300			158 [5]	290 [5]	100 [5]	186 [4, 5]					158	248	
APA450			158	344	100	186 [4]	344 [4]						
APA600			158 [5]	356 [5]		186 [4, 5]	370 [4]	454			158	248	440
APA750			158	356				454	562 [6]				
APA1000			158 [5]	356 [5]					642 [5, 6]	712 [6]	158	248	440

Notes:

1. *Package Definitions: TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array, CQFP = Ceramic Quad Flat Pack, CCGA = Ceramic Column Grid Array, LGA = Land Grid Array*
2. *Each pair of PECL I/Os is counted as one user I/O.*
3. *Available in RoHS compatible packages. Ordering code is "G."*
4. *FG256 and FG484 are footprint-compatible packages.*
5. *Military Temperature Plastic Package Offering*
6. *FG896 and FG1152 are footprint-compatible packages.*

General Guideline

Maximum performance numbers in this datasheet are based on characterized data. Actel does not guarantee performance beyond the limits specified within the datasheet.

Temperature Grade Offerings

Package	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
TQ100	C, I	C, I					
TQ144	C, I						
PQ208	C, I	C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
BG456		C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
FG144	C, I	C, I	C, I, M	C, I			
FG256		C, I	C, I, M	C, I	C, I, M		
FG484				C, I	C, I, M		
FG676					C, I, M	C, I	
FG896						C, I	C, I, M
FG1152							C, I
CQ208			M, B		M, B		M, B
CQ352			M, B		M, B		M, B
CG624					M, B		M, B

Note: *C = Commercial*
I = Industrial
M = Military
B = MIL-STD-883

Speed Grade and Temperature Matrix

	Std.
C	✓
I	✓
M, B	✓

Note: *C = Commercial*
I = Industrial
M = Military
B = MIL-STD-883

Device Family Overview

The ProASIC^PLUS family of devices, Actel's second-generation family of flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC^PLUS family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to one million system gates, supported with up to 198 kbits of two-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of flash technology allows all functionality to be live at power-up. No external boot PROM is required to support device programming. While on-board security mechanisms prevent access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC^PLUS a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC^PLUS family achieves its nonvolatility and reprogrammability through an advanced flash-based 0.22 µm LVCMOS process with four layers of metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance compatible with gate arrays.

The ProASIC^PLUS architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles™. Each tile can be configured as a flip-flop, latch, or three-input/one-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant flash switches allows 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a four-level routing hierarchy.

Embedded two-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depths and widths. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The unique clock conditioning circuitry in each device includes two clock conditioning blocks. Each block provides a PLL core, delay lines, phase shifts (0° and 180°), and clock multipliers/dividers, as well as the circuitry needed to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 8 ns (in increments of 0.25 ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high-speed clock and data inputs.

To support customer needs for more comprehensive, lower-cost, board-level testing, Actel's ProASIC^PLUS devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information concerning the flash FPGA implementation, please refer to the "Boundary Scan (JTAG)" section on page 2-8.

ProASIC^PLUS devices are available in a variety of high-performance plastic packages. Those packages and the performance features discussed above are described in more detail in the following sections.

ProASIC^PLUS Architecture

The proprietary ProASIC^PLUS architecture provides granularity comparable to gate arrays.

The ProASIC^PLUS device core consists of a Sea-of-Tiles (Figure 1-1). Each tile can be configured as a three-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate flash switch interconnections (Figure 1-2 and Figure 1-3 on page 1-3). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^PLUS devices also contain embedded, two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user-defined depth and width, and parity generation or checking. Refer to the "Embedded Memory Specifications" section on page 2-54 for more information.

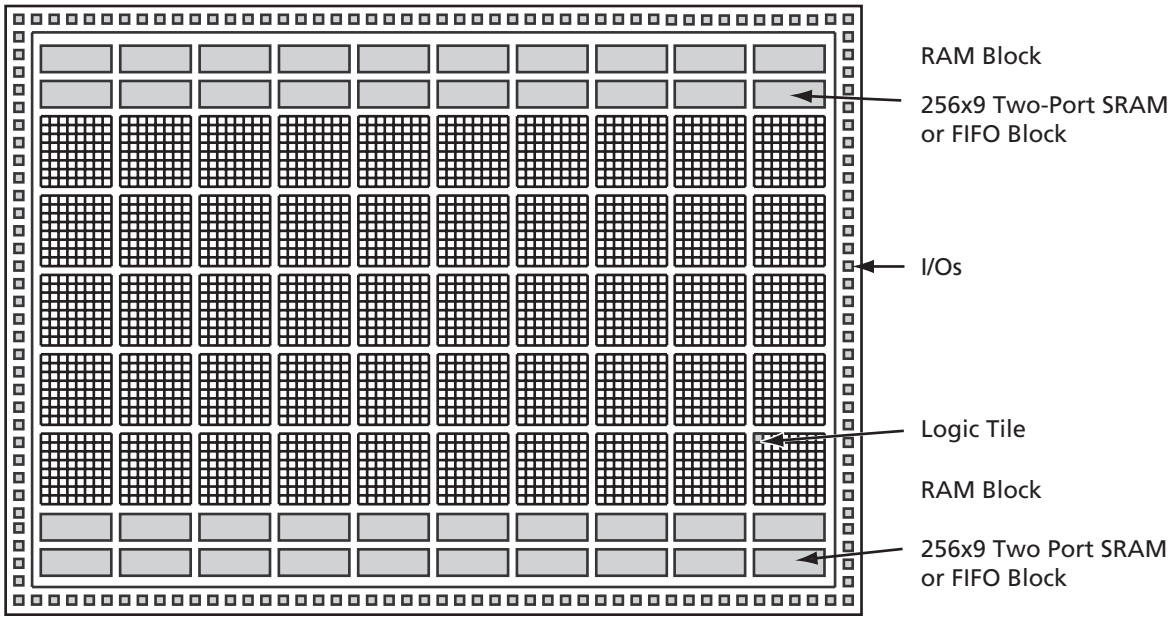


Figure 1-1 • **The ProASIC^PLUS Device Architecture**

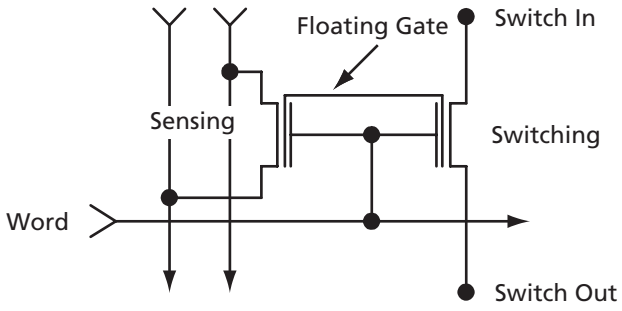


Figure 1-2 • **Flash Switch**

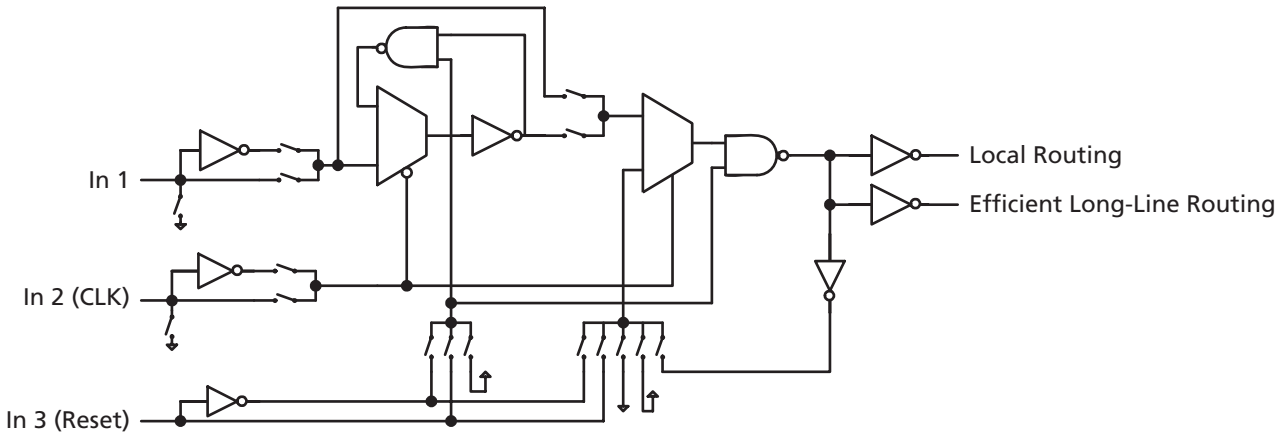


Figure 1-3 • **Core Logic Tile**

Live at Power-Up

The Actel flash-based ProASIC^PLUS devices support Level 0 of the live at power-up (LAPU) classification standard. This feature helps in system component initialization, executing critical tasks before the processor wakes up, setting up and configuring memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based ProASIC^PLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for complex programmable logic device (CPLD) and clock generation PLLs that are used for this purpose in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC^PLUS device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC^PLUS devices simplify total system design, and reduce cost and design risk, while increasing system reliability and improving system initialization time.

Flash Switch

Unlike SRAM FPGAs, ProASIC^PLUS uses a live-at-power-up ISP flash switch as its programming element.

In the ProASIC^PLUS flash switch, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 1-2 on page 1-2).

Logic Tile

The logic tile cell (Figure 1-3) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra-fast local and efficient long-line routing resources). Any three-input, one-output logic function (except a three-input XOR) can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.

Data Sheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advance

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

Export Administration Regulations (EAR)

The products described in this datasheet are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status datasheet may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.

Table of Contents

General Description

Routing Resources

The routing structure of ProASIC^PLUS devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very long-line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 2-1).

The efficient long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC^PLUS device (Figure 2-2 on page 2-2). Each tile can drive signals onto the efficient long-line resources, which can in turn access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed, very long-line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 2-3 on page 2-3).

The high-performance global networks are low-skew, high fanout nets that are accessible from external pins or from internal logic (Figure 2-4 on page 2-4). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.

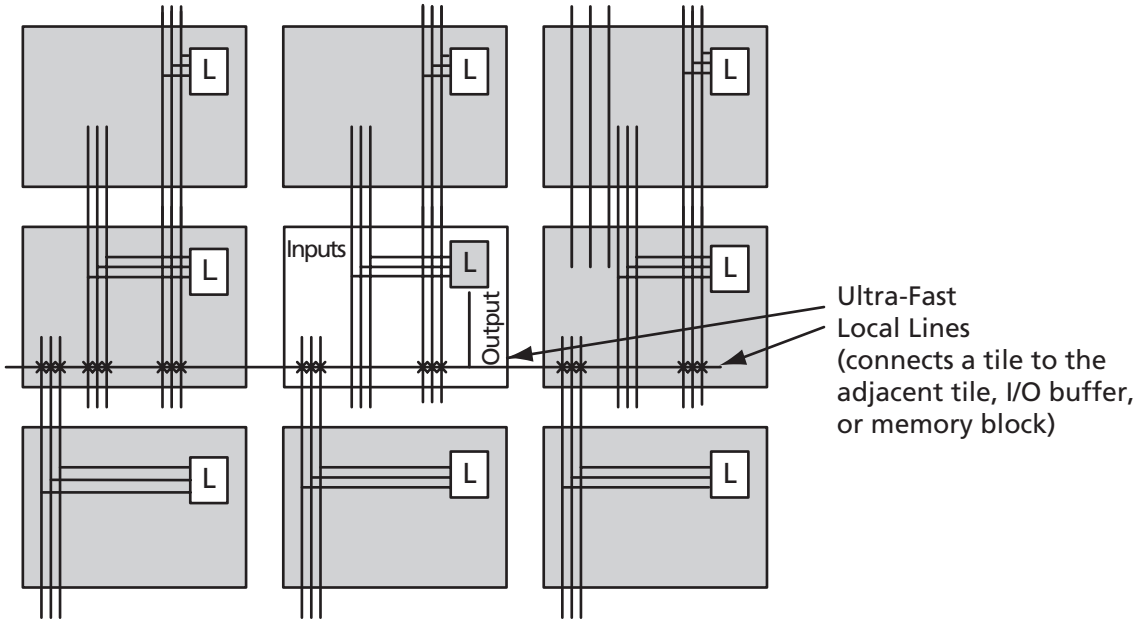


Figure 2-1 • **Ultra-Fast Local Resources**

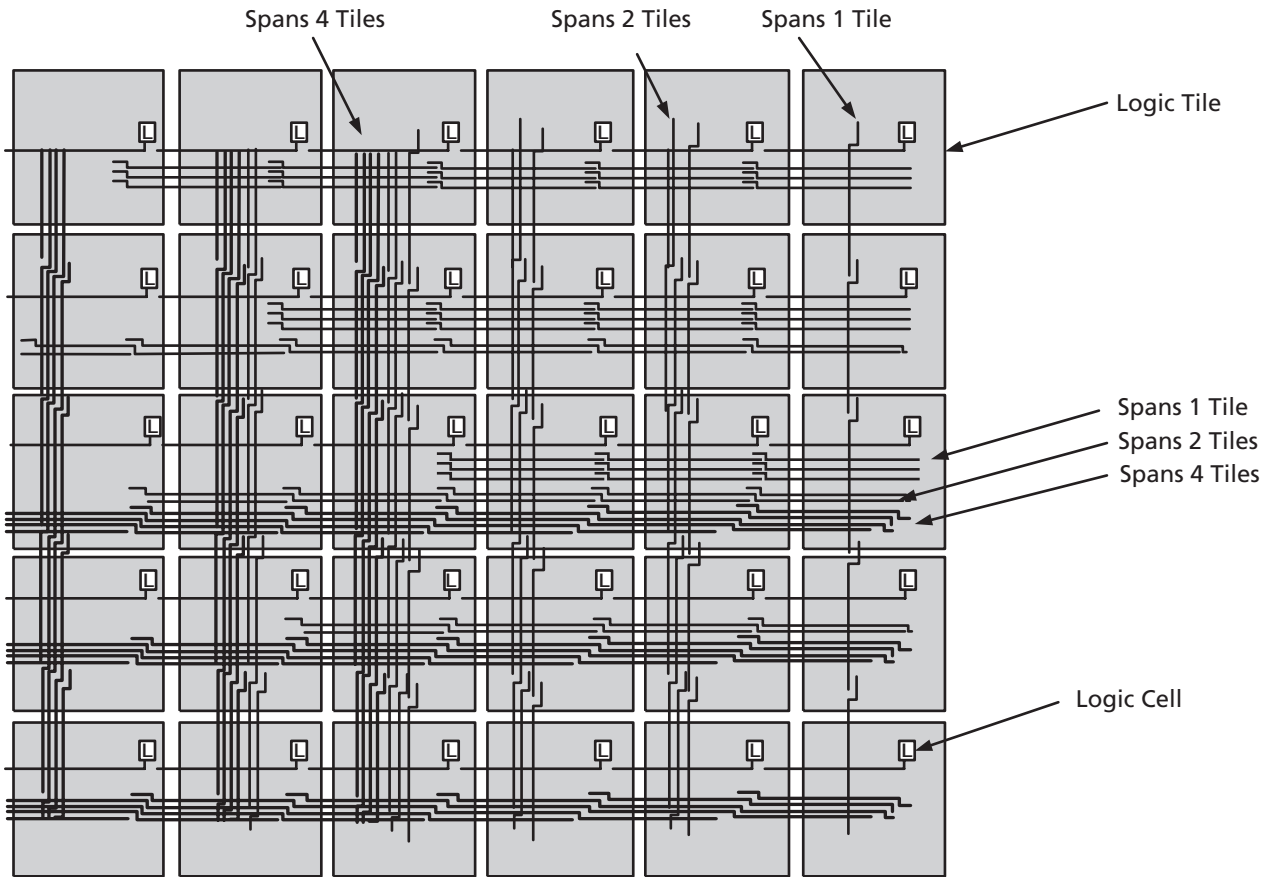


Figure 2-2 • **Efficient Long-Line Resources**

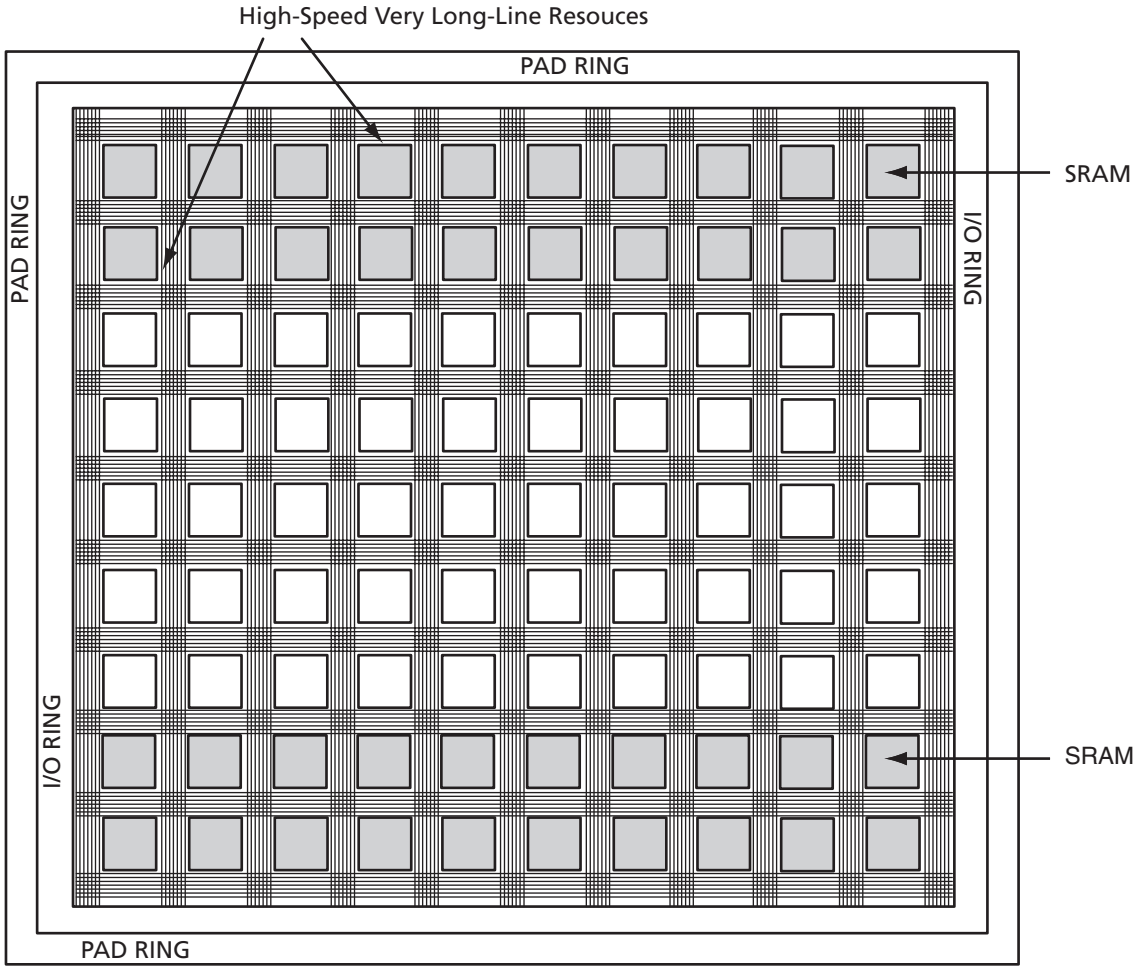


Figure 2-3 • **High-Speed, Very Long-Line Resources**

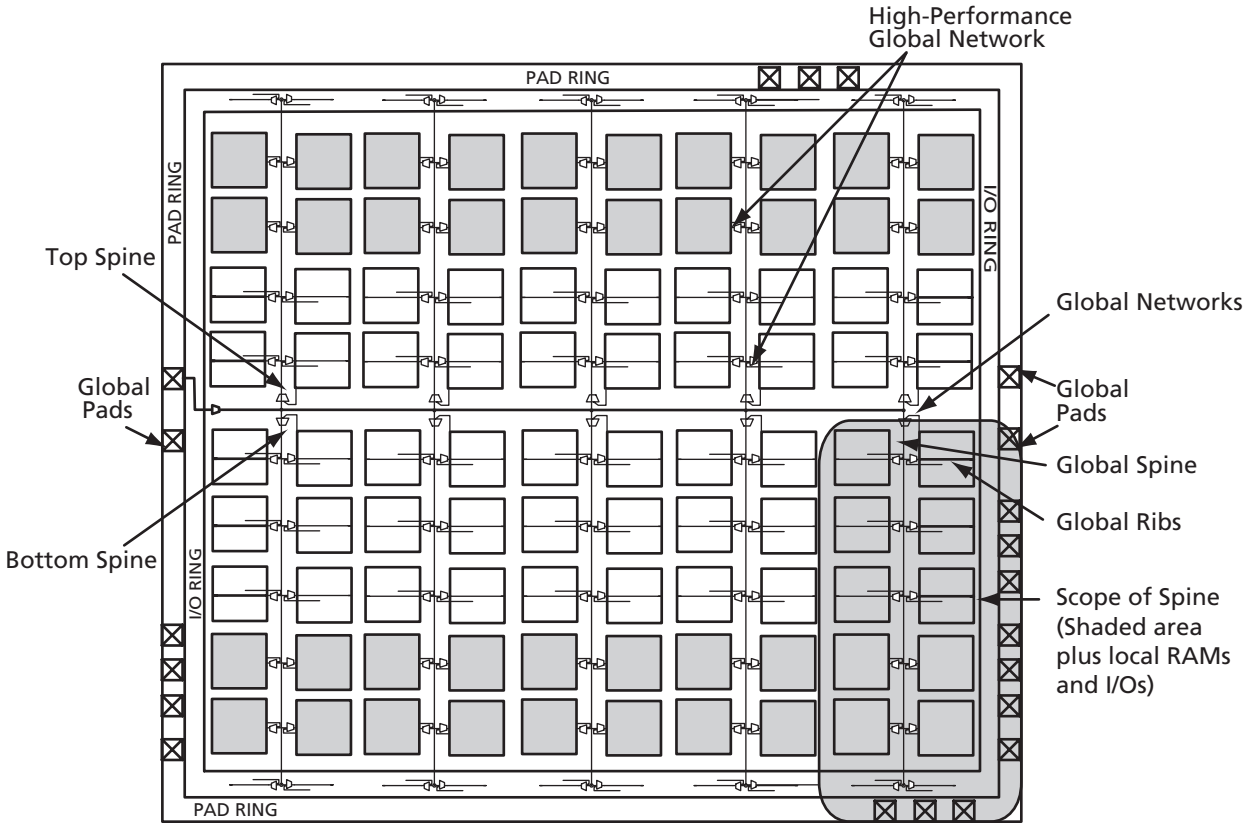
Clock Resources

The ProASIC^PLUS family offers powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has two clock conditioning blocks containing a phase-locked loop (PLL) core, delay lines, phase shifter (0° and 180°), clock multiplier/dividers, and all the circuitry needed for the selection and interconnection of inputs to the global network (thus providing bidirectional access to the PLL). This permits the PLL block to drive inputs and/or outputs via the two global lines on each side of the chip (four total lines). This circuitry is discussed in more detail in the "ProASIC^PLUS Clock Management System" section on page 2-10.

Clock Trees

One of the main architectural benefits of ProASIC^PLUS is the set of power- and delay-friendly global networks. ProASIC^PLUS offers four global trees. Each of these trees is based on a network of spines and ribs that reach all the tiles in their regions (Figure 2-4 on page 2-4). This flexible clock tree architecture allows users to map up to 88 different internal/external clocks in an APA1000 device. Details on the clock spines and various numbers of the family are given in Table 2-1 on page 2-4.

The flexible use of the ProASIC^PLUS clock spine allows the designer to cope with several design requirements. Users implementing clock-resource intensive applications can easily route external or gated internal clocks using global routing spines. Users can also drastically reduce delay penalties and save buffering resources by mapping critical high fanout nets to spines. For design hints on using these features, refer to Actel's *Efficient Use of ProASIC Clock Trees* application note.



Note: *This figure shows routing for only one global path.*

Figure 2-4 • **High-Performance Global Network**

Table 2-1 • **Clock Spines**

	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
Global Clock Networks (Trees)	4	4	4	4	4	4	4
Clock Spines/Tree	6	8	8	12	14	16	22
Total Spines	24	32	32	48	56	64	88
Top or Bottom Spine Height (Tiles)	16	24	32	32	48	64	80
Tiles in Each Top or Bottom Spine	512	768	1,024	1,024	1,536	2,048	2,560
Total Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320

Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 2-2 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups of core cells, I/Os, and RAM blocks. Wild cards are also allowed.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination.

Core cell coordinates start at the lower left corner (represented as (1,1)) or at (1,5) if memory blocks are present at the bottom. Memory coordinates use the same system and are indicated in Table 2-2. The memory coordinates for an APA1000 are illustrated in Figure 2-5. For more information on how to use constraints, see the *Designer User's Guide* or online help for ProASIC^PLUS software tools.

Table 2-2 • **Array Coordinates**

	Logic Tile				Memory Rows		All	
	Min.		Max.		Bottom	Top		
Device	**x**	**y**	**x**	**y**	**y**	**y**	**Min.**	**Max.**
APA075	1	1	96	32	–	(33,33) or (33, 35)	0,0	97, 37
APA150	1	1	128	48	–	(49,49) or (49, 51)	0,0	129, 53
APA300	1	5	128	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	129, 73
APA450	1	5	192	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	193, 73
APA600	1	5	224	100	(1,1) or (1,3)	(101,101) or (101, 103)	0,0	225, 105
APA750	1	5	256	132	(1,1) or (1,3)	(133,133) or (133, 135)	0,0	257, 137
APA1000	1	5	352	164	(1,1) or (1,3)	(165,165) or (165, 167)	0,0	353, 169

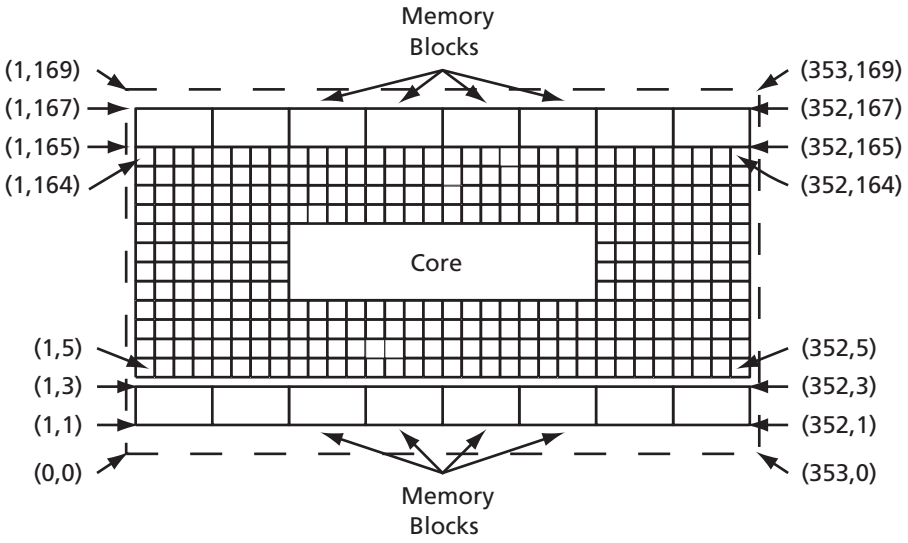


Figure 2-5 • **Core Cell Coordinates for the APA1000**

Input/Output Blocks

To meet complex system demands, the ProASIC^PLUS family offers devices with a large number of user I/O pins; up to 712 on the APA1000. Table 2-3 shows the available supply voltage configurations (the PLL block uses an independent 2.5 V supply on the AVDD and AGND pins). All I/Os include ESD protection circuits. Each I/O has been tested to 2000 V to the human body model (per JESD22 (HBM)).

Six or seven standard I/O pads are grouped with a GND pad and either a V_{DD} (core power) or V_{DDP} (I/O power) pad. Two reference bias signals circle the chip. One protects the cascaded output drivers, while the other creates a virtual V_{DD} supply for the I/O ring.

I/O pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a tristate driver, or a bidirectional buffer (Figure 2-6 and Table 2-4).

Table 2-3 • **ProASIC^PLUS I/O Power Supply Voltages**

	V_{DDP}	
	2.5 V	**3.3 V**
Input Compatibility	2.5 V	3.3 V
Output Drive	2.5 V	3.3 V

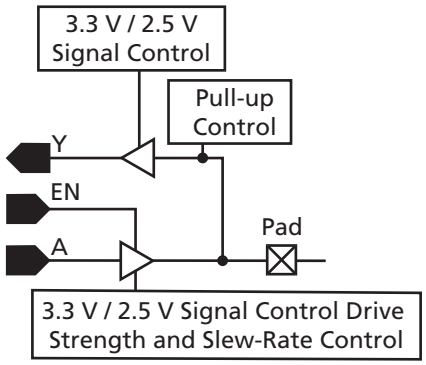


Figure 2-6 • **I/O Block Schematic Representation**

Table 2-4 • **I/O Features**

Function	Description
I/O pads configured as inputs	• Selectable 2.5 V or 3.3 V threshold levels • Optional pull-up resistor • Optionally configurable as Schmitt trigger input. The Schmitt trigger input option can be configured as an input only, not a bidirectional buffer. This input type may be slower than a standard input under certain conditions and has a typical hysteresis of 0.35 V. I/O macros with an "S" in the standard I/O library have added Schmitt capabilities. • 3.3 V PCI Compliant (except Schmitt trigger inputs)
I/O pads configured as outputs	• Selectable 2.5 V or 3.3 V compliant output signals • 2.5 V – JEDEC JESD 8-5 • 3.3 V – JEDEC JESD 8-A (LVTTL and LVCMOS) • 3.3 V PCI compliant • Ability to drive LVTTL and LVCMOS levels • Selectable drive strengths • Selectable slew rates • Tristate
I/O pads configured as bidirectional buffers	• Selectable 2.5 V or 3.3 V compliant output signals • 2.5 V – JEDEC JESD 8-5 • 3.3 V – JEDEC JESD 8-A (LVTTL and LVCMOS) • 3.3 V PCI compliant • Optional pull-up resistor • Selectable drive strengths • Selectable slew rates • Tristate

Power-Up Sequencing

While ProASIC^PLUS devices are live at power-up, the order of V_{DD} and V_{DDP} power-up is important during system start-up. V_{DD} should be powered up simultaneously with V_{DDP} on ProASIC^PLUS devices. Failure to follow these guidelines may result in undesirable pin behavior during system start-up. For more information, refer to Actel's *Power-Up Behavior of ProASIC^PLUS Devices* application note.

LVPECL Input Pads

In addition to standard I/O pads and power pads, ProASIC^PLUS devices have a single LVPECL input pad on both the east and west sides of the device, along with AVDD and AGND pins to power the PLL block. The LVPECL pad cell consists of an input buffer (containing a low voltage differential amplifier) and a signal and its complement, PPECL (I/P) (PECLN) and NPECL (PECLREF). The LVPECL input pad cell differs from the standard I/O cell in that it is operated from V_{DD} only.

Since it is exclusively an input, it requires no output signal, output enable signal, or output configuration bits. As a special high-speed differential input, it also does not require pull-ups. Recommended termination for LVPECL inputs is shown in Figure 2-7. The LVPECL pad cell compares voltages on the PPECL (I/P) pad (as illustrated in Figure 2-8) and the NPECL pad and sends the results to the global MUX (Figure 2-11 on page 2-11). This high-speed, low-skew output essentially controls the clock conditioning circuit.

LVPECLs are designed to meet LVPECL JEDEC receiver standard levels (Table 2-5).

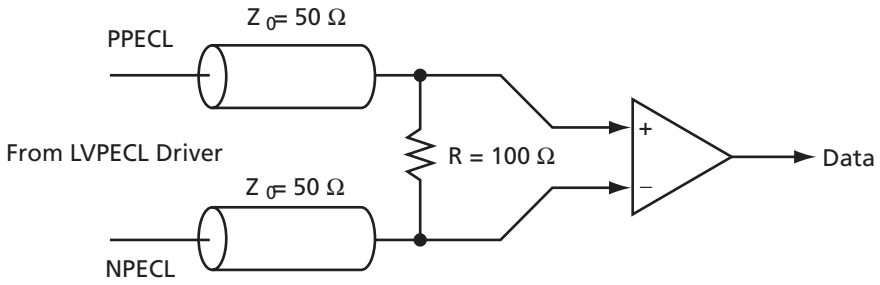


Figure 2-7 • **Recommended Termination for LVPECL Inputs**

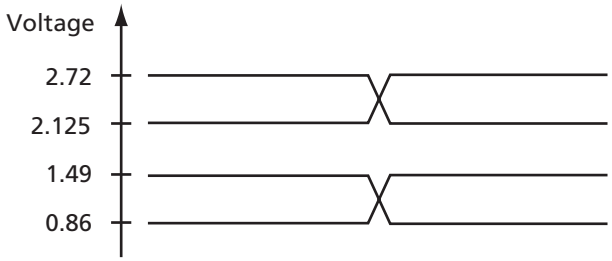


Figure 2-8 • **LVPECL High and Low Threshold Values**

Table 2-5 • **LVPECL Receiver Specifications**

Symbol	Parameter	Minimum	Maximum	Units
V_{IH}	Input High Voltage	1.49	2.72	V
V_{IL}	Input Low Voltage	0.86	2.125	V
V_{ID}	Differential Input Voltage	0.3	V_{DD}	V

Boundary Scan (JTAG)

ProASIC^PLUS devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective, board-level testing. The basic ProASIC^PLUS boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 2-9). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and the optional IDCODE instruction (Table 2-6).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI and TDO (test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage. Actel recommends that a nominal 20 kΩ pull-up resistor is added to TDO and TCK pins.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 2-10 on page 2-9. The 1s and 0s represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

ProASIC^PLUS devices have to be programmed at least once for complete boundary-scan functionality to be available. Prior to being programmed, EXTEST is not available. If boundary-scan functionality is required prior to programming, refer to online technical support on the Actel website and search for ProASIC^PLUS BSDL.

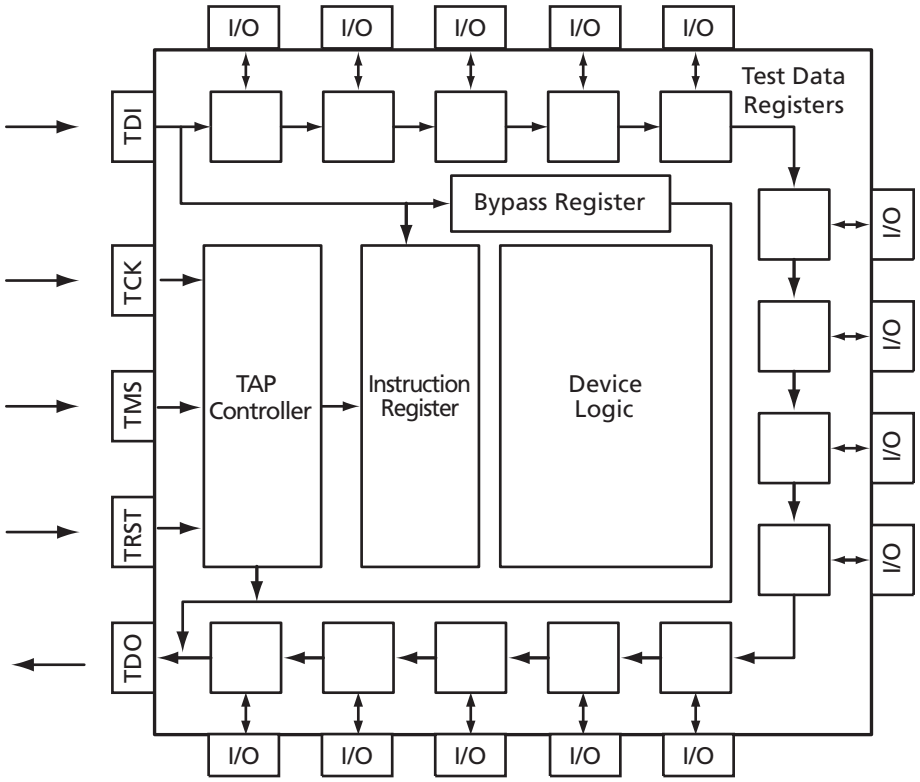


Figure 2-9 • **ProASIC^PLUS JTAG Boundary Scan Test Logic Circuit**

Table 2-6 • **Boundary-Scan Opcodes**

	Hex Opcode
EXTEST	00
SAMPLE/PRELOAD	01
IDCODE	0F

Table 2-6 • **Boundary-Scan Opcodes**

	Hex Opcode
CLAMP	05
BYPASS	FF

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC^PLUS devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

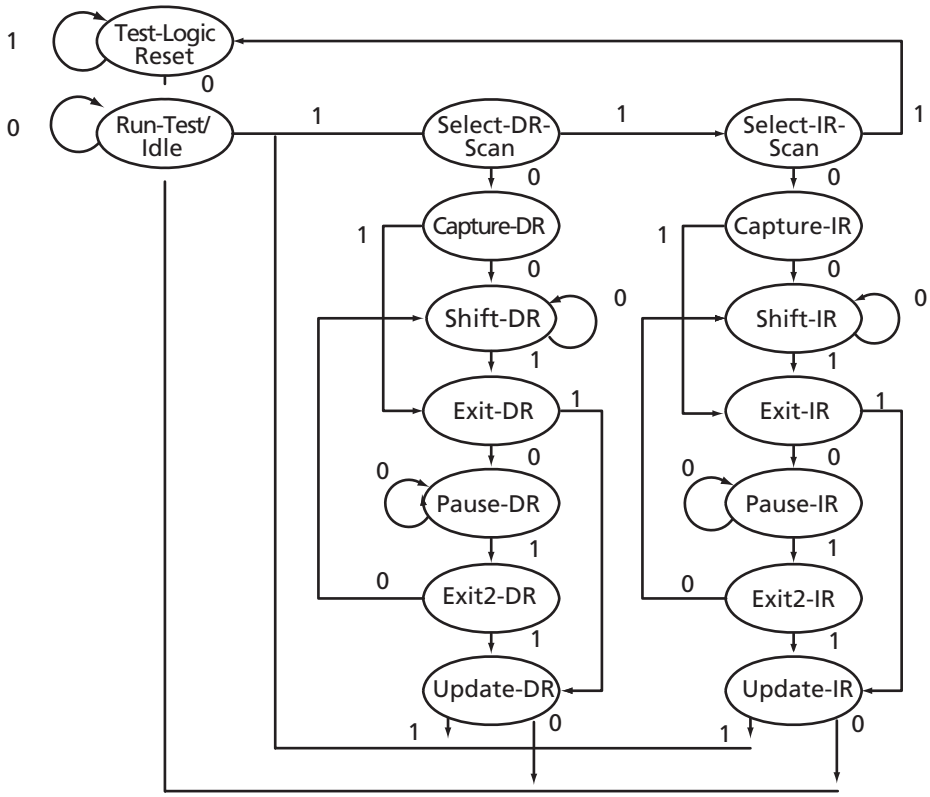


Figure 2-10 • **TAP Controller State Diagram**

Timing Control and Characteristics

ProASIC^PLUS Clock Management System

ProASIC^PLUS devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC^PLUS family contains two phase-locked loop (PLL) blocks which perform the following functions:

- Clock Phase Adjustment via Programmable Delay (250 ps steps from –7 ns to +8 ns)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range (f_{IN}) = 1.5 to 180 MHz
- Feedback Frequency Range (f_{VCO}) = 24 to 180 MHz
- Output Frequency Range (f_{OUT}) = 8 to 180 MHz
- Output Phase Shift = 0 ° and 180 °
- Output Duty Cycle = 50%
- Low Output Jitter (maximum at 25°C)
  - f_{VCO} <10 MHz. Jitter ±1% or better
  - 10 MHz < f_{VCO} < 60 MHz. Jitter ±2% or better
  - f_{VCO} > 60 MHz. Jitter ±1% or better

Note: Jitter (ps) = Jitter (%) × period

For Example:

Jitter in picoseconds at 100 MHz = 0.01 × (1/100E6) = 100 ps

- Maximum Acquisition Time = 80 µs for f_{VCO} > 40 MHz
  = 30 µs for f_{VCO} < 40 MHz
- Low Power Consumption – 6.9 mW (max. – analog supply) + 7.0 µW/MHz (max. – digital supply)

Physical Implementation

Each side of the chip contains a clock conditioning circuit based on a 180 MHz PLL block (Figure 2-11 on page 2-11). Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional LVPECL input pads (described below). The global lines may be driven by either the LVPECL global input pad or the outputs from the PLL block, or both. Each global line can be driven by a different output from the PLL. Unused global pins can be configured as regular I/Os or left unconnected. They default to an input with pull-up. The two signals available to drive the global networks are as follows (Figure 2-12 on page 2-12, Table 2-7 on page 2-12, and Table 2-8 on page 2-13):

Global A (secondary clock)

- Output from Global MUX A
- Conditioned version of PLL output (f_{OUT}) – delayed or advanced
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[1]

Global B

- Output from Global MUX B
- Delayed or advanced version of f_{OUT}
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[2]

Functional Description

Each PLL block contains four programmable dividers as shown in Figure 2-11 on page 2-11. These allow frequency scaling of the input clock signal as follows:

- The n divider divides the input clock by integer factors from 1 to 32.
- The m divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64.
- The two dividers together can implement any combination of multiplication and division resulting in a clock frequency between 24 and 180 MHz exiting the PLL core. This clock has a fixed 50% duty cycle.
- The output frequency of the PLL core is given by the formula in EQ 2-1 (f_{REF} is the reference clock frequency):

$$f_{OUT} = f_{REF} \times m \div n$$

EQ 2-1

- The third and fourth dividers (u and v) permit the signals applied to the global network to each be further divided by integer factors ranging from 1 to 4.

The implementations shown in EQ 2-2 and EQ 2-3 enable the user to define a wide range of frequency multiplier and divisors.

$$f_{GLB} = \frac{m}{(n \times u)}$$

EQ 2-2

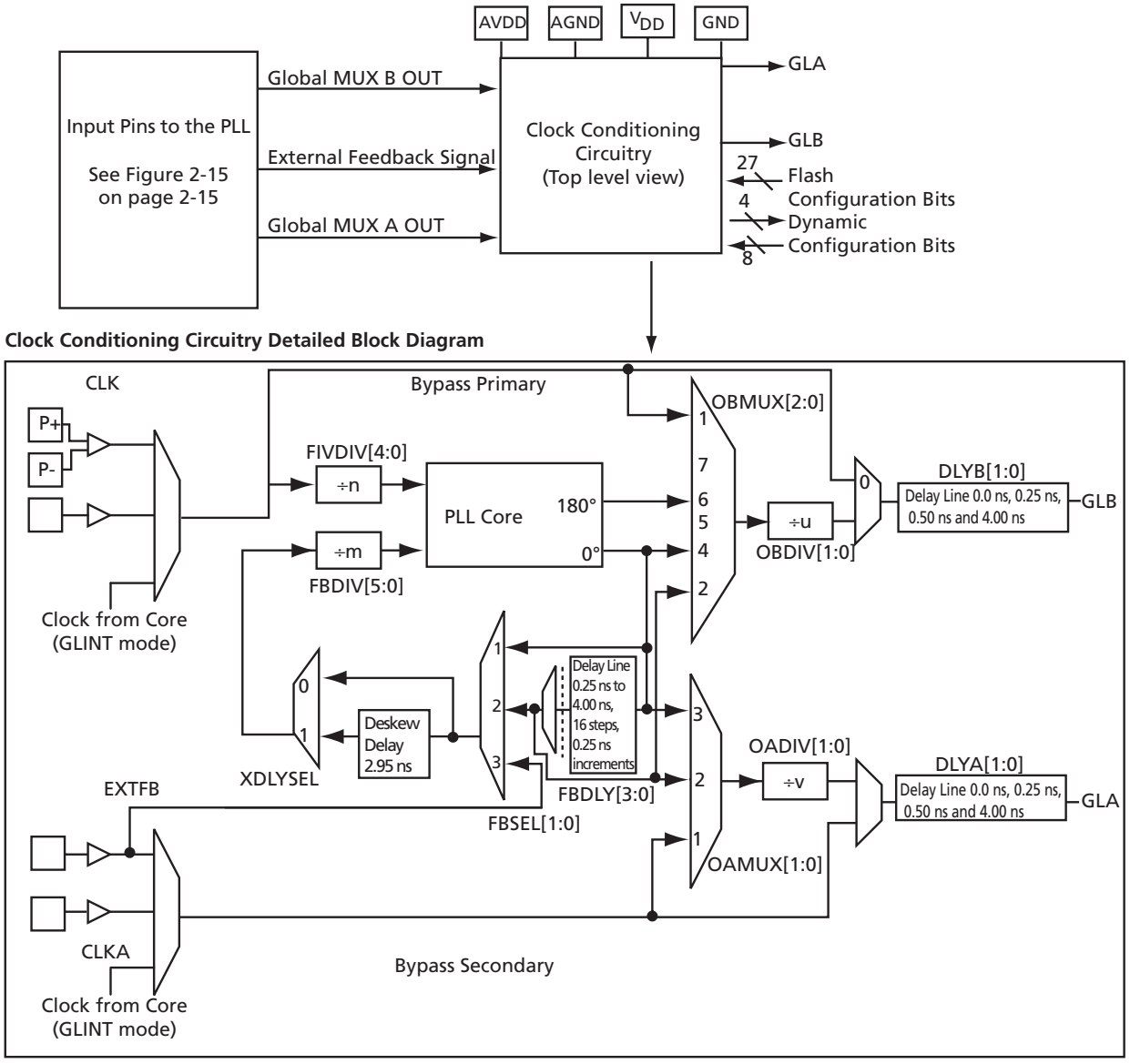
$$f_{GLA} = \frac{m}{(n \times v)}$$

EQ 2-3

1. *This mode is available through the delay feature of the global MUX driver.*

The clock conditioning circuit can advance or delay the clock up to 8 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0° and 180°.

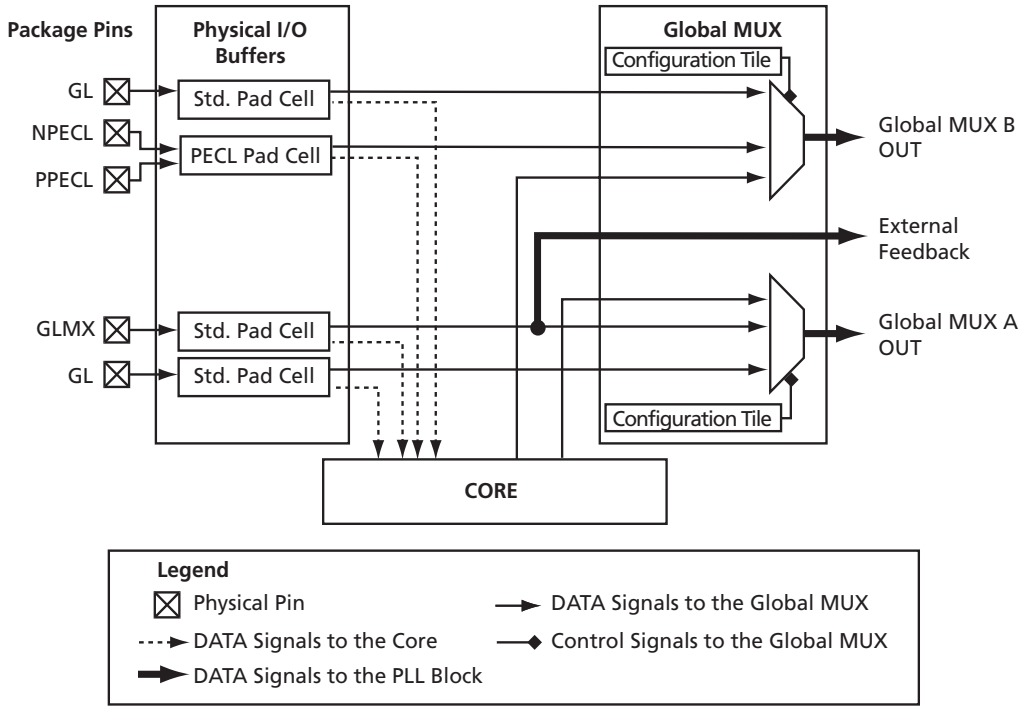
Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.



Notes:

1. *FBDLY is a programmable delay line from 0 to 4 ns in 250 ps increments.*
2. *DLYA and DLYB are programmable delay lines, each with selectable values 0 ps, 250 ps, 500 ps, and 4 ns.*
3. *OBDIV will also divide the phase-shift since it takes place after the PLL Core.*

Figure 2-11 • **PLL Block – Top-Level View and Detailed PLL Block Diagram**



Note: *When a signal from an I/O tile is connected to the core, it cannot be connected to the global MUX at the same time.*

Figure 2-12 • **Input Connectors to ProASIC^PLUS Clock Conditioning Circuitry**

Table 2-7 • **Clock-Conditioning Circuitry MUX Settings**

MUX	Datapath	Comments
FBSEL		
1	Internal Feedback	
2	Internal Feedback and Advance Clock Using FBDLY	–0.25 to –4 ns in 0.25 ns increments
3	External Feedback (EXTFB)	
XDLYSEL		
0	Feedback Unchanged	
1	Deskew feedback by advancing clock by system delay	Fixed delay of –2.95 ns
OBMUX	**GLB**	
0	Primary bypass, no divider	
1	Primary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
4	Phase Shift Clock by 0°	
5	Reserved	
6	Phase Shift Clock by +180°	
7	Reserved	
OAMUX	**GLA**	
0	Secondary bypass, no divider	
1	Secondary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
3	Phase Shift Clock by 0°	

Table 2-8 • **Clock Conditioning Circuitry Delay-Line Settings**

Delay Line	Delay Value (ns)
DLYB	
0	0
1	+0.25
2	+0.50
3	+4.0
DLYA	
0	0
1	+0.25
2	+0.50
3	+4.0

Lock Signal

An active high Lock signal (added via the SmartGen PLL development tool) indicates that the PLL has locked to the incoming clock signal. The PLL will acquire and maintain a lock even when there is jitter on the incoming clock signal. The PLL will maintain lock with an input jitter up to 5% of the input period, with a maximum of 5 ns. Users can employ the Lock signal as a soft reset of the logic driven by GLB and/or GLA. Note if F_{IN} is not within specified frequencies, then both the F_{OUT} and lock signal are indeterminate.

PLL Configuration Options

The PLL can be configured during design (via flash-configuration bits set in the programming bitstream) or dynamically during device operation, thus eliminating the need to reprogram the device. The dynamic configuration bits are loaded into a serial-in/parallel-out shift register provided in the clock conditioning circuit. The shift register can be accessed either from user logic within the device or via the JTAG port. Another option is internal dynamic configuration via user-designed hardware. Refer to Actel's *ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG* application note for more information.

For information on the clock conditioning circuit, refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note.

Sample Implementations

Frequency Synthesis

Figure 2-13 on page 2-14 illustrates an example where the PLL is used to multiply a 33 MHz external clock up to 133 MHz. Figure 2-14 on page 2-14 uses two dividers to synthesize a 50 MHz output clock from a 40 MHz input reference clock. The input frequency of 40 MHz is multiplied by five and divided by four, giving an output clock (GLB) frequency of 50 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL. For example, in this case the input divider could have been two and the output divider also two, giving us a division of the input frequency by four to go with the feedback loop division (effective multiplication) by five.

Adjustable Clock Delay

Figure 2-15 on page 2-15 illustrates the delay of the input clock by employing one of the adjustable delay lines. This is easily done in ProASIC^PLUS by bypassing the PLL core entirely and using the output delay line. Notice also that the output clock can be effectively advanced relative to the input clock by using the delay line in the feedback path. This is shown in Figure 2-16 on page 2-15.

Clock Skew Minimization

Figure 2-17 on page 2-16 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (GLA) feeds a clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note for more information.

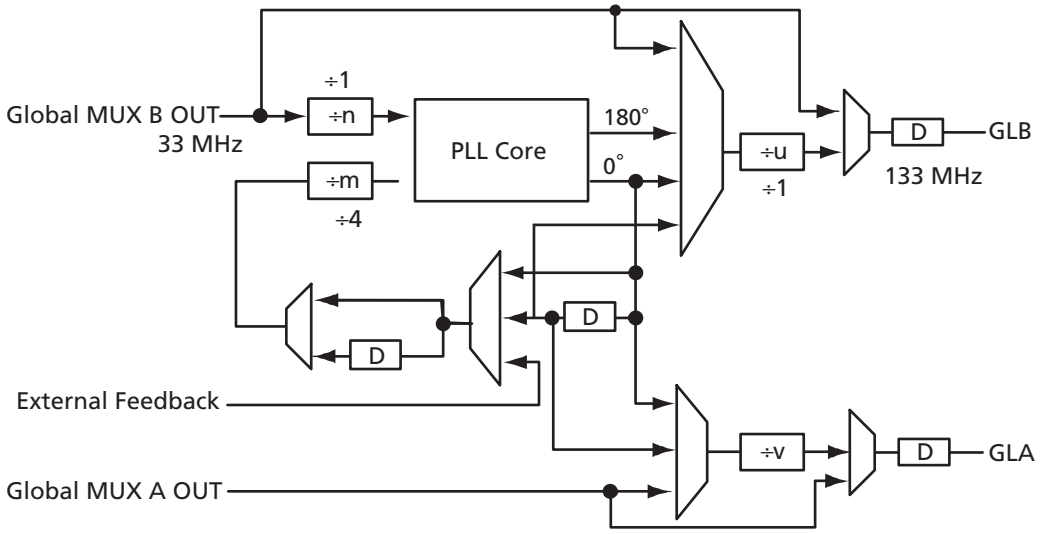


Figure 2-13 • **Using the PLL 33 MHz In, 133 MHz Out**

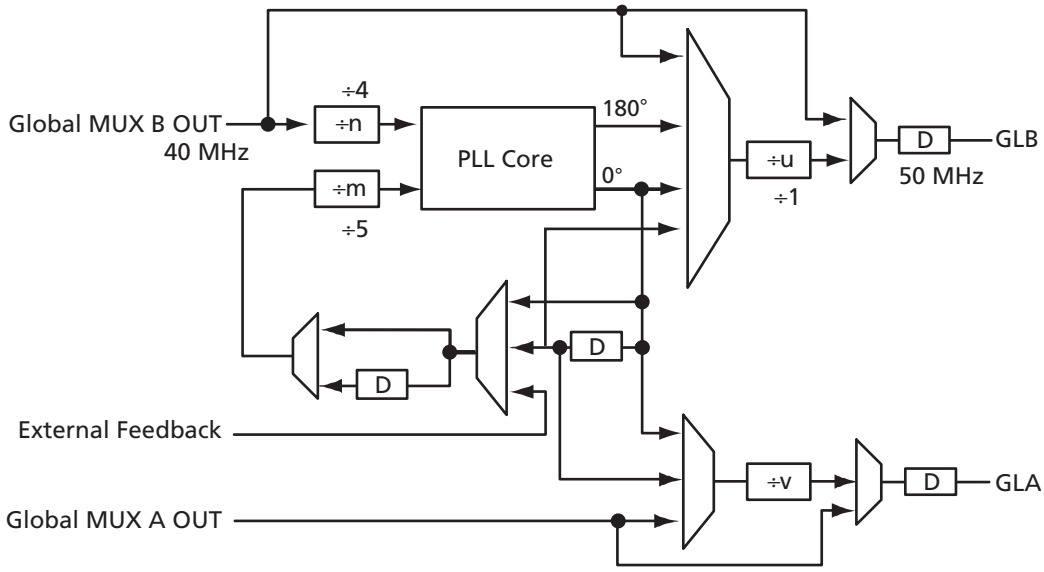


Figure 2-14 • **Using the PLL 40 MHz In, 50 MHz Out**

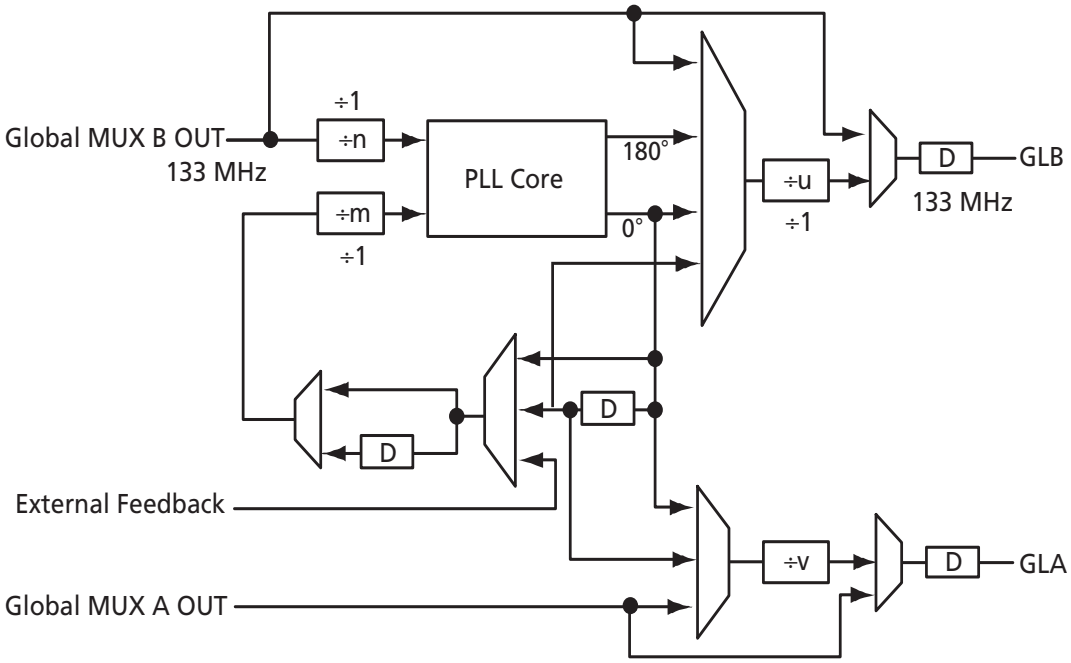


Figure 2-15 • **Using the PLL to Delay the Input Clock**

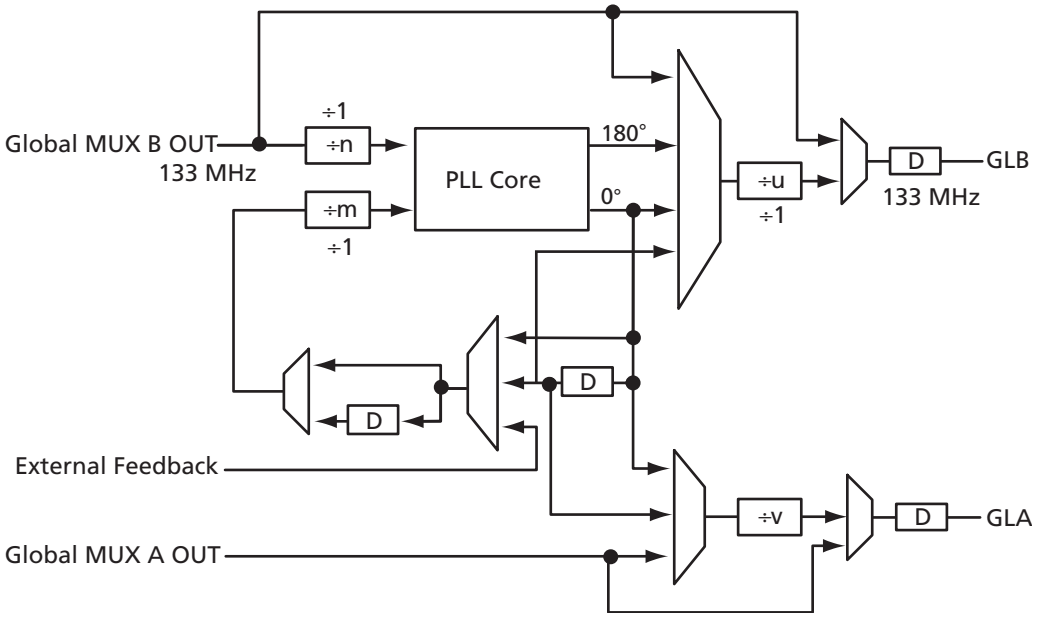


Figure 2-16 • **Using the PLL to Advance the Input Clock**

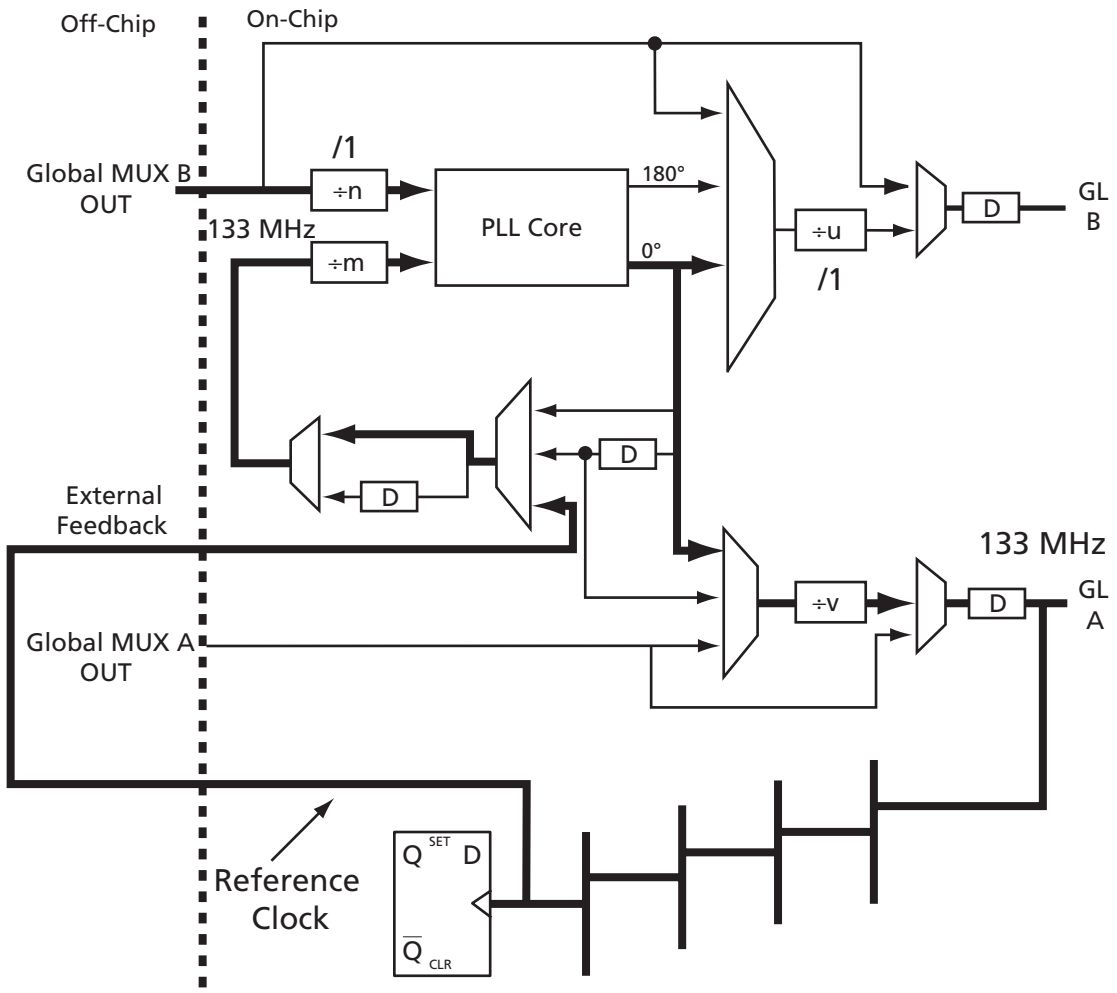


Figure 2-17 • **Using the PLL for Clock Deskewing**

Logic Tile Timing Characteristics

Timing characteristics for ProASIC^PLUS devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ProASIC^PLUS family members. Internal routing delays are device dependent. Design dependency means that actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or by performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to place-and-route. Refer to the Actel *Designer User's Guide* or online help for details on using constraints.

Timing Derating

Since ProASIC^PLUS devices are manufactured with a CMOS process, device performance will vary with temperature, voltage, and process. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and optimal process variations. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case process variations (within process specifications). The derating factors shown in Table 2-9 should be applied to all timing data contained within this datasheet.

All timing numbers listed in this datasheet represent sample timing characteristics of ProASIC^PLUS devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Actel's Designer software after place-and-route.

Table 2-9 • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{DD} = 2.3 V)**

	–55°C	–40°C	0°C	25°C	70°C	85°C	110°C	125°C	135°C	150°C
2.3 V	0.84	0.86	0.91	0.94	1.00	1.02	1.05	1.13	1.18	1.27
2.5 V	0.81	0.82	0.87	0.90	0.95	0.98	1.01	1.09	1.13	1.21
2.7 V	0.77	0.79	0.83	0.86	0.91	0.93	0.96	1.04	1.08	1.16

Notes:

1. *The user can set the junction temperature in Designer software to be any integer value in the range of –55°C to 175°C.*
2. *The user can set the core voltage in Designer software to be any value between 1.4 V and 1.6 V.*

PLL Electrical Specifications

Parameter	Value $T_J \leq$ –40°C	Value $T_J >$ –40°C	Notes
Frequency Ranges			
Reference Frequency f_{IN} (min.)	2.0 MHz	1.5 MHz	Clock conditioning circuitry (min.) lowest input frequency
Reference Frequency f_{IN} (max.)	180 MHz	180 MHz	Clock conditioning circuitry (max.) highest input frequency
OSC Frequency f_{VCO} (min.)	60	24 MHz	Lowest output frequency voltage controlled oscillator
OSC Frequency f_{VCO} (max.)	180	180 MHz	Highest output frequency voltage controlled oscillator
Clock Conditioning Circuitry f_{OUT} (min.)	$f_{IN} \leq 40$ = 18 MHz $f_{IN} > 40$ = 16 MHz	6 MHz	Lowest output frequency clock conditioning circuitry
Clock Conditioning Circuitry f_{OUT} (max.)	180	180 MHz	Highest output frequency clock conditioning circuitry
Acquisition Time from Cold Start			
Acquisition Time (max.)	80 µs	30 µs	$f_{VCO} \leq 40$ MHz
Acquisition Time (max.)	80 µs	80 µs	$f_{VCO} > 40$ MHz
Long Term Jitter Peak-to-Peak Max.*			
Temperature		**Frequency MHz**	
		f_{VCO}< 10 / **10<f_{VCO}<60** / **f_{VCO} >60**	
25°C (or higher)		±1% / ±2% / ±1%	Jitter(ps) = Jitter(%)*period For example: Jitter in picoseconds at 100 MHz = 0.01 * (1/100E6) = 100 ps
0°C		±1.5% / ±2.5% / ±1%	
–40°C		±2.5% / ±3.5% / ±1%	
–55°C		±2.5% / ±3.5% / ±1%	
Power Consumption			
Analog Supply Power (max.*)		6.9 mW per PLL	
Digital Supply Current (max.)		7 µW/MHz	
Duty Cycle		50% ±0.5%	
Input Jitter Tolerance		5% input period (max. 5 ns)	Maximum jitter allowable on an input clock to acquire and maintain lock.

Note: **High clock frequencies (>60 MHz) under typical setup conditions*

PLL I/O Constraints

PLL locking is guaranteed only when the following constraints are followed:

Table 2-10 • **PLL I/O Constraints**

	$T_J \leq -40°C$		Value $T_J > -40°C$
I/O Type	PLL locking is guaranteed only when using low drive strength and low slew rate I/O. PLL locking may be inconsistent when using high drive strength or high slew rate I/Os		No Constraints
SSO	APA300	Hermetic packages ≤ 8 SSO	With FIN ≤ 180 MHz and outputs switching simultaneously
		Plastic packages ≤ 16 SSO	
	APA600	Hermetic packages ≤ 16 SSO	
		Plastic packages ≤ 32 SSO	
	APA1000	Hermetic packages ≤ 16 SSO	
		Plastic packages ≤ 32 SSO	
	APA300	Hermetic packages ≤ 12 SSO	With FIN ≤ 50 MHz and half outputs switching on positive clock edge, half switching on the negative clock edge no less than 10 ns later
		Plastic packages ≤ 20 SSO	
	APA600	Hermetic packages ≤ 32 SSO	
		Plastic packages ≤ 64 SSO	
	APA1000	Hermetic packages ≤ 32 SSO	
		Plastic packages ≤ 64 SSO	

User Security

ProASIC^PLUS devices have FlashLock protection bits that, once programmed, block the entire programmed contents from being read externally. Refer to Table 2-11 for details on the number of bits in the key for each device. If locked, the user can only reprogram the device employing the user-defined security key. This protects the device from being read back and duplicated. Since programmed data is stored in nonvolatile memory cells (actually very small capacitors) rather than in the wiring, physical deconstruction cannot be used to compromise data. This type of security breach is further discouraged by the placement of the memory cells beneath the four metal layers (whose removal cannot be accomplished without disturbing the charge in the capacitor). This is the highest security provided in the industry. For more information, refer to Actel's *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper.

Table 2-11 • **Flashlock Key Size by Device**

Device	Key Size
APA075	79 bits
APA150	79 bits
APA300	79 bits
APA450	119 bits
APA600	167 bits
APA750	191 bits
APA1000	263 bits

Embedded Memory Floorplan

The embedded memory is located across the top and bottom of the device in 256x9 blocks (Figure 1-1 on page 1-2). Depending on the device, up to 88 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory array or combined (using dedicated memory routing resources) to form larger, more complex memory configurations. A single memory configuration could include blocks from both the top and bottom memory locations.

Embedded Memory Configurations

The embedded memory in the ProASIC^PLUS family provides great configuration flexibility (Table 2-12). Each ProASIC^PLUS block is designed and optimized as a two-port memory (one read, one write). This provides 198 kbits of two-port and/or single port memory in the APA1000 device.

Each memory block can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 2-13). Additional characteristics include programmable flags as well as parity checking and generation. Figure 2-18 on page 2-22 and Figure 2-19 on page 2-23 show the block diagrams of the basic SRAM and FIFO blocks. Table 2-14 on page 2-22 and Table 2-15 on page 2-23 describe memory block SRAM and FIFO interface signals, respectively. A single memory block is designed to operate at up to 150 MHz (standard speed grade typical conditions). Each block is comprised of 256 9-bit words (one read port, one write port). The memory blocks may be cascaded in width and/or depth to create the desired memory organization. (Figure 2-20 on page 2-24). This provides optimal bit widths of 9 (one block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1,024. Refer to Actel's *SmartGen User's Guide* for more information.

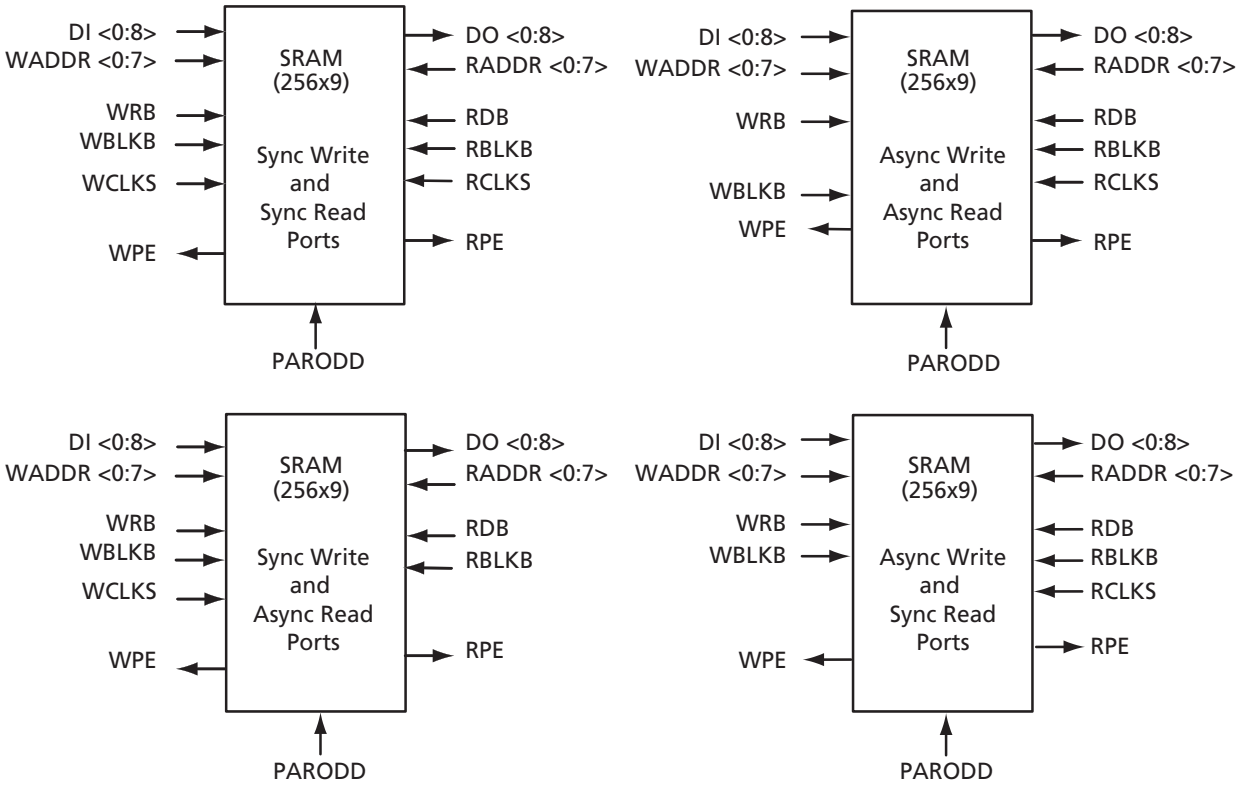
Figure 2-21 on page 2-24 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to generate three arrays of various widths and depths. Figure 2-22 on page 2-24 shows how RAM blocks can be used in parallel to create extra read ports. In this example, using only 10 of the 88 available blocks of the APA1000 yields an effective 6,912 bits of multiple port RAM. The Actel SmartGen software facilitates building wider and deeper memory configurations for optimal memory usage.

Table 2-12 • **ProASIC^PLUS Memory Configurations by Device**

Device	Bottom	Top	Maximum Width		Maximum Depth	
			D	W	D	W
APA075	0	12	256	108	1,536	9
APA150	0	16	256	144	2,048	9
APA300	16	16	256	144	2,048	9
APA450	24	24	256	216	3,072	9
APA600	28	28	256	252	3,584	9
APA750	32	32	256	288	4,096	9
APA1000	44	44	256	396	5,632	9

Table 2-13 • **Basic Memory Configurations**

Type	Write Access	Read Access	Parity	Library Cell Name
RAM	Asynchronous	Asynchronous	Checked	RAM256x9AA
RAM	Asynchronous	Asynchronous	Generated	RAM256x9AAP
RAM	Asynchronous	Synchronous Transparent	Checked	RAM256x9AST
RAM	Asynchronous	Synchronous Transparent	Generated	RAM256x9ASTP
RAM	Asynchronous	Synchronous Pipelined	Checked	RAM256x9ASR
RAM	Asynchronous	Synchronous Pipelined	Generated	RAM256x9ASRP
RAM	Synchronous	Asynchronous	Checked	RAM256x9SA
RAM	Synchronous	Asynchronous	Generated	RAM256xSAP
RAM	Synchronous	Synchronous Transparent	Checked	RAM256x9SST
RAM	Synchronous	Synchronous Transparent	Generated	RAM256x9SSTP
RAM	Synchronous	Synchronous Pipelined	Checked	RAM256x9SSR
RAM	Synchronous	Synchronous Pipelined	Generated	RAM256x9SSRP
FIFO	Asynchronous	Asynchronous	Checked	FIFO256x9AA
FIFO	Asynchronous	Asynchronous	Generated	FIFO256x9AAP
FIFO	Asynchronous	Synchronous Transparent	Checked	FIFO256x9AST
FIFO	Asynchronous	Synchronous Transparent	Generated	FIFO256x9ASTP
FIFO	Asynchronous	Synchronous Pipelined	Checked	FIFO256x9ASR
FIFO	Asynchronous	Synchronous Pipelined	Generated	FIFO256x9ASRP
FIFO	Synchronous	Asynchronous	Checked	FIFO256x9SA
FIFO	Synchronous	Asynchronous	Generated	FIFO256x9SAP
FIFO	Synchronous	Synchronous Transparent	Checked	FIFO256x9SST
FIFO	Synchronous	Synchronous Transparent	Generated	FIFO256x9SSTP
FIFO	Synchronous	Synchronous Pipelined	Checked	FIFO256x9SSR
FIFO	Synchronous	Synchronous Pipelined	Generated	FIFO256x9SSRP



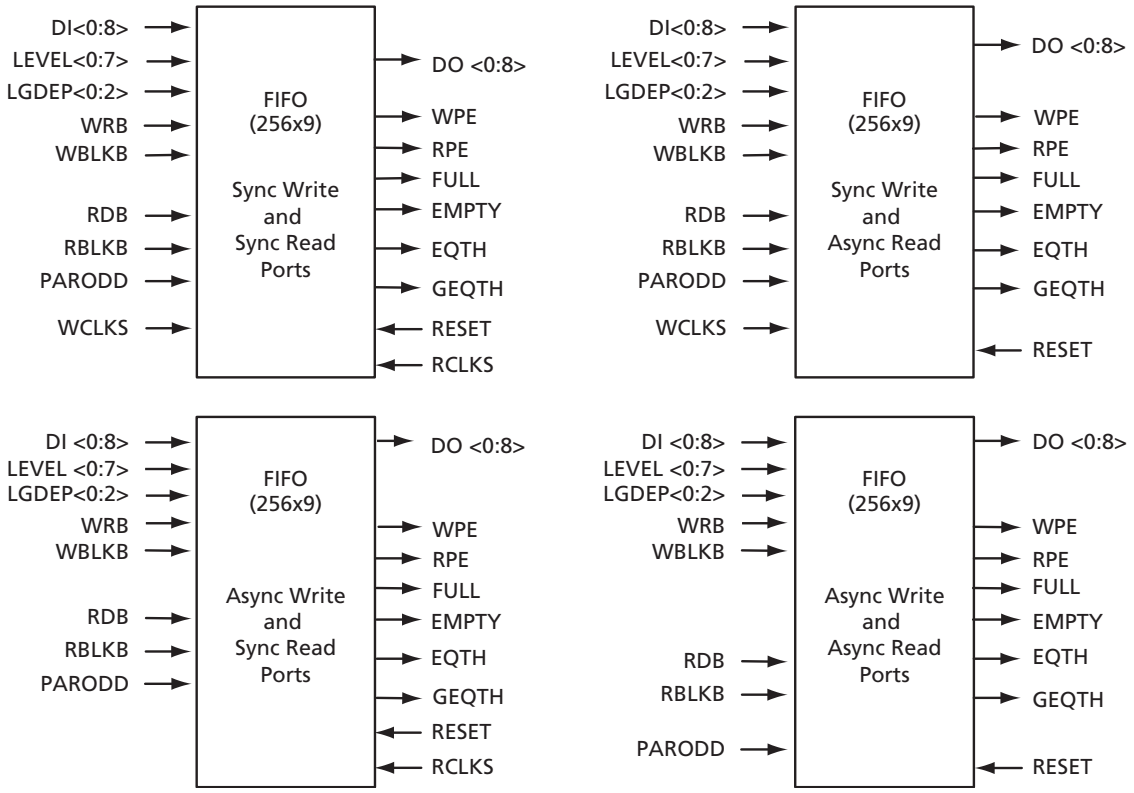
Note: *Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.*

Figure 2-18 • **Example SRAM Block Diagrams**

Table 2-14 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Write pulse (active Low)
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects odd parity generation/detect when High, even parity when Low

Note: *Not all signals shown are used in all modes.*



Note: *Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.*

Figure 2-19 • **Basic FIFO Block Diagrams**

Table 2-15 • **Memory Block FIFO Interface Signals**

FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated parity if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>. <8> will be parity output if PARGEN is true.
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Parity generation/detect – Even when Low, odd when High

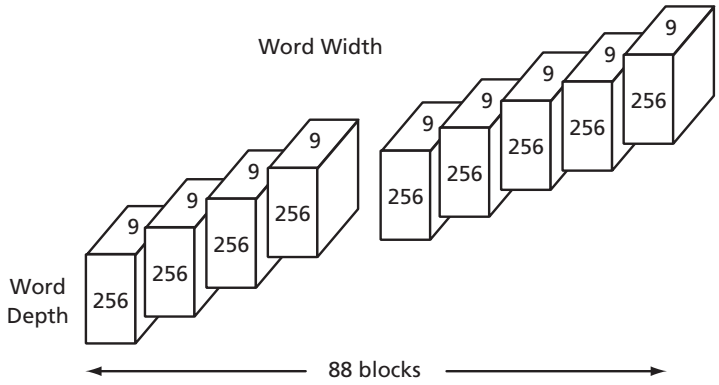


Figure 2-20 • **APA1000 Memory Block Architecture**

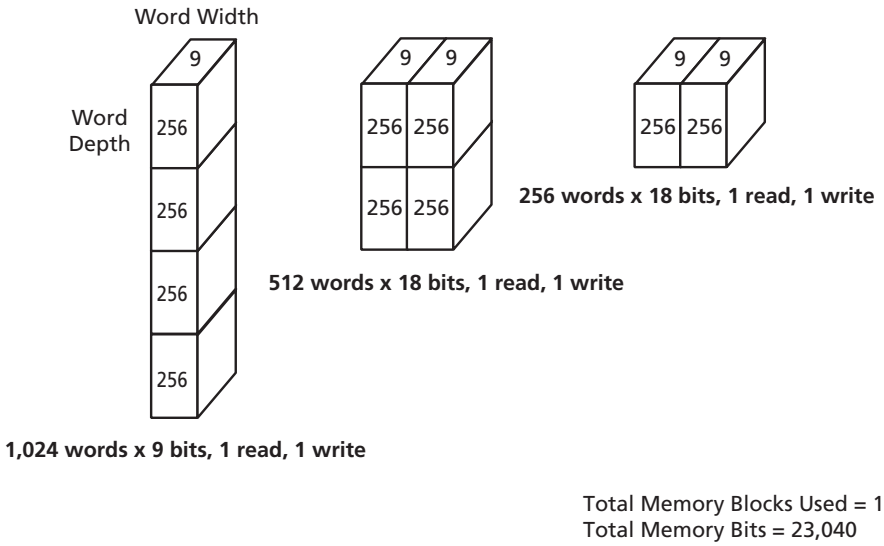


Figure 2-21 • **Example Showing Memory Arrays with Different Widths and Depths**

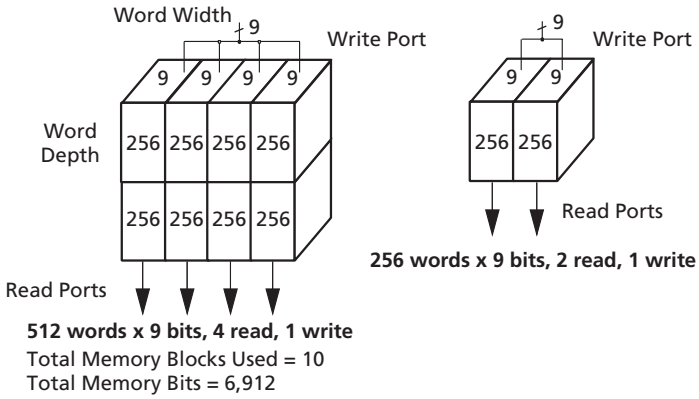


Figure 2-22 • **Multi-Port Memory Usage**

Design Environment

The ProASIC^PLUS family of FPGAs is fully supported by both Actel's Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see Actel's website for more information about *Libero IDE*). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, PALACE™ AE Physical Synthesis from Magma, and Designer software from Actel.

PALACE is an effective tool when designing with ProASIC^PLUS. PALACE AE Physical Synthesis from Magma takes an EDIF netlist and optimizes the performance of ProASIC^PLUS devices through a physical placement-driven process, ensuring that timing closure is easily achieved.

Actel's Designer software is a place-and-route tool that provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer – A world-class integrated static timing analyzer and constraints editor that supports timing-driven place-and-route
- NetlistViewer – A design netlist schematic viewer
- ChipPlanner – A graphical floorplanner viewer and editor
- SmartPower – Allows the designer to quickly estimate the power consumption of a design
- PinEditor – A graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – Displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel's back-annotation flow is compatible with all the major simulators. Another tool included in the Designer software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

ISP

The user can generate *.bit or *.stp programming files from the Designer software and can use these files to program a device.

ProASIC^PLUS devices can be programmed in-system. For more information on ISP of ProASIC^PLUS devices, refer to the *In-System Programming ProASIC^PLUS Devices* and *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application notes. Prior to being programmed for the first time, the ProASIC^PLUS device I/Os are in a tristate condition with the pull-up resistor option enabled.

Related Documents

Application Notes

Efficient Use of ProASIC Clock Trees
http://www.actel.com/documents/A500K_Clocktree_AN.pdf
I/O Features in ProASIC^PLUS Flash FPGAs
http://www.actel.com/documents/APA_LVPECL_AN.pdf
Power-Up Behavior of ProASIC^PLUS Devices
http://www.actel.com/documents/APA_PowerUp_AN.pdf
ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG
http://www.actel.com/documents/APA_PLLdynamic_AN.pdf
Using ProASIC^PLUS Clock Conditioning Circuits
http://www.actel.com/documents/APA_PLL_AN.pdf
In-System Programming ProASIC^PLUS Devices
http://www.actel.com/documents/APA_External_ISP_AN.pdf
Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices
http://www.actel.com/documents/APA_Microprocessor_AN.pdf
ProASIC^PLUS RAM and FIFO Blocks
http://www.actel.com/documents/APA_RAM_FIFO_AN.pdf

White Paper

Design Security in Nonvolatile Flash and Antifuse FPGAs
http://www.actel.com/documents/DesignSecurity_WP.pdf

User's Guides

Designer User's Guide
http://www.actel.com/documents/designer_UG.pdf
SmartGen Cores Reference Guide
http://www.actel.com/documents/gen_refguide_ug.pdf
ProASIC and ProASIC^PLUS Macro Library Guide
http://www.actel.com/documents/pa_libguide_UG.pdf

Additional Information

The following link contains additional information on ProASIC^PLUS devices.
http://www.actel.com/products/proasicplus/default.aspx

Package Thermal Characteristics

The ProASIC^PLUS family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the integrated circuit (IC) and is 110°C. P is defined as shown in EQ 2-4:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

EQ 2-4

Θ_{ja} is a function of the rate (in linear feet per minute (lfpm)) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used. The maximum power dissipation allowed for a Military temperature device is specified as a function of Θ_{jc}. The absolute maximum junction temperature is 150°C.

The calculation of the absolute maximum power dissipation allowed for a Military temperature application is illustrated in the following example for a 456-pin PBGA package:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. case temp. (°C)}}{\theta_{jc}\text{(°C/W)}} = \frac{150\text{°C} - 125\text{°C}}{3.0\text{°C/W}} = 8.333\text{W}$$

EQ 2-5

Table 2-16 • **Package Thermal Characteristics**

Plastic Packages	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	1.0 m/s 200 ft./min.	2.5 m/s 500 ft./min.	
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W
Thin Quad Flat Pack (TQFP)	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8.0	26.1	22.5	20.8	°C/W
PQFP with heat spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	456	3.0	15.6	12.5	11.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)[3]	484	3.2	18.0	14.7	13.6	°C/W
Fine Pitch Ball Grid Array (FBGA)[4]	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA/LGA)	624	6.5	8.9	8.5	8.0	°C/W

Notes:

1. *Valid for the following devices irrespective of temperature grade: APA075, APA150, and APA300*
2. *Valid for the following devices irrespective of temperature grade: APA450, APA600, APA750, and APA1000*
3. *Depopulated array*
4. *Full array*

Calculating Typical Power Dissipation

ProASIC^PLUS device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

Total Power Consumption—P_{total}

$$P_{total} = P_{dc} + P_{ac}$$

where:

P_{dc} = 7 mW for the APA075
8 mW for the APA150
11 mW for the APA300
12 mW for the APA450
12 mW for the APA600
13 mW for the APA750
19 mW for the APA1000
P_{dc} includes the static components of $P_{VDDP} + P_{VDD} + P_{AVDD}$

P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{outputs} + P_{inputs} + P_{pll} + P_{memory}$

Global Clock Contribution—P_{clock}

P_{clock}, the clock component of power dissipation, is given by the piece-wise model:

for R < 15000 the model is: (P1 + (P2*R) – (P7*R2)) * Fs (lightly-loaded clock trees)

for R > 15000 the model is: (P10 + P11*R) * Fs (heavily-loaded clock trees)

where:

P1 = 100 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P2 = 1.3 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

P7 = 0.00003 µW/MHz is a correction factor for partially-loaded clock trees

P10 = 6850 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P11 = 0.4 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

R = the number of storage tiles clocked by this clock

Fs = the clock frequency

Storage-Tile Contribution—$P_{storage}$

$P_{storage}$, the storage-tile (Register) component of AC power dissipation, is given by

$$P_{storage} = P5 * ms * Fs$$

where:

P5 = 1.1 µW/MHz is the average power consumption of a storage tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.

ms = the number of storage tiles (Register) switching during each Fs cycle

Fs = the clock frequency

Logic-Tile Contribution—P_{logic}

P_{logic}, the logic-tile component of AC power dissipation, is given by

$$P_{logic} = P3 * mc * Fs$$

where:

- P3 = 1.4 µW/MHz is the average power consumption of a logic tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.
- mc = the number of logic tiles switching during each Fs cycle
- Fs = the clock frequency

I/O Output Buffer Contribution—$P_{outputs}$

$P_{outputs}$, the I/O component of AC power dissipation, is given by

$$P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp$$

where:

- P4 = 326 µW/MHz is the intrinsic power consumption of an output pad normalized per MHz of the output frequency. This is the total I/O current V_{DDP}.
- C_{load} = the output load
- p = the number of outputs
- Fp = the average output frequency

I/O Input Buffer's Buffer Contribution—P_{inputs}

The input's component of AC power dissipation is given by

$$P_{inputs} = P8 * q * Fq$$

where:

- P8 = 29 µW/MHz is the intrinsic power consumption of an input pad normalized per MHz of the input frequency.
- q = the number of inputs
- Fq = the average input frequency

PLL Contribution—P_{pll}

$$P_{pll} = P9 * N_{pll}$$

where:

- P9 = 7.5 mW. This value has been estimated at maximum PLL clock frequency.
- N_{PII} = number of PLLs used

RAM Contribution—P_{memory}

Finally, P_{memory}, the memory component of AC power consumption, is given by

$$P_{memory} = P6 * N_{memory} * F_{memory} * E_{memory}$$

where:

- P6 = 175 µW/MHz is the average power consumption of a memory block per MHz of the clock
- N_{memory} = the number of RAM/FIFO blocks (1 block = 256 words * 9 bits)
- F_{memory} = the clock frequency of the memory
- E_{memory} = the average number of active blocks divided by the total number of blocks (N) of the memory.
  - Typical values for E_{memory} would be 1/4 for a 1k x 8,9,16, 32 memory and 1/16 for a 4kx8, 9, 16, and 32 memory configuration
  - In addition, an application-dependent component to E_{memory} can be considered. For example, for a 1kx8 memory configuration using only 1 cycle out of 2, E_{memory} = 1/4*1/2 = 1/8

The following is an APA750 example using a shift register design with 13,440 storage tiles (Register) and 0 logic tiles. This design has one clock at 10 MHz, and 24 outputs toggling at 5 MHz. We then calculate the various components as follows:

P_{clock}

Fs = 10 MHz

R = 13,440

=> $P_{clock} = (P1 + (P2*R) - (P7*R^2)) * Fs = 121.5$ mW

$P_{storage}$

ms = 13,440 (in a shift register 100% of storage tiles are toggling at each clock cycle and Fs = 10 MHz)

=> $P_{storage} = P5 * ms * Fs = 147.8$ mW

P_{logic}

mc = 0 (no logic tiles in this shift register)

=> $P_{logic} = 0$ mW

$P_{outputs}$

C_{load} = 40 pF

V_{DDP} = 3.3 V

p = 24

Fp = 5 MHz

=> $P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp = 91.4$ mW

P_{inputs}

q = 1

Fq = 10 MHz

=> $P_{inputs} = P8 * q * Fq = 0.3$ mW

P_{memory}

N_{memory} = 0 (no RAM/FIFO blocks in this shift register)

=> $P_{memory} = 0$ mW

P_{ac}

=> 361 mW

P_{total}

$P_{dc} + P_{ac} = 374$ mW (typical)

Operating Conditions

Table 2-17 and Table 2-18 delineate operating limits.

Table 2-17 • **Absolute Maximum Ratings***

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DD})		–0.3	3.0	V
Supply Voltage I/O Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–1.0	V_{DDP} + 1.0	V
PCI DC Input Clamp Current (absolute)	V_{IN} < –1 or V_{IN} = V_{DDP} + 1 V	10		mA
LVPECL Input Voltage		–0.3	V_{DDP} + 0.5	V
GND		0	0	V

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 2-18 • **Programming, Storage, and Operating Limits**

Product Grade	Programming Cycles (min.)	Program Retention (min.)	Storage Temperature		Operating
			Min.	Max.	T_J Max. Junction Temperature
Commercial	500	20 years	–55°C	110°C	110°C
Industrial	500	20 years	–55°C	110°C	110°C
Military	100	Refer to Table 2-19 on page 2-32	–65°C	150°C	150°C
MIL-STD-883	100	Refer to Table 2-19 on page 2-32	–65°C	150°C	150°C

Performance Retention

For devices operated and stored at 110°C or less, the performance retention period is 20 years after programming. For devices operated and stored at temperatures greater than 110°C, refer to Table 2-19 on page 2-32 to determine the performance retention period. Actel does not guarantee performance if the performance retention period is exceeded. Designers can determine the performance retention period from the following table.

Evaluate the percentage of time spent at the highest temperature, then determine the next highest temperature to which the device will be exposed. In Table 2-19 on page 2-32, find the temperature profile that most closely matches the application.

Example – the ambient temperature of a system cycles between 100°C (25% of the time) and 50°C (75% of the time). No forced ventilation cooling system is in use. An APA600-PQ208M FPGA operates in the system, dissipating 1 W. The package thermal resistance (junction-to-ambient) in still air Θ_{ja} is 20°C/W, indicating that the junction temperature of the FPGA will be 120°C (25% of the time) and 70°C (75% of the time). The entry in Table 2-19 on page 2-32, which most closely matches the application, is 25% at 125°C with 75% at 110°C. Performance retention in this example is at least 16.0 years.

Note that exceeding the stated retention period may result in a performance degradation in the FPGA below the worst-case performance indicated in the Actel Timer. To ensure that performance does not degrade below the worst-case values in the Actel Timer, the FPGA must be reprogrammed within the performance retention period. In addition, note that performance retention is independent of whether or not the FPGA is operating. The retention period of a device in storage at a given temperature will be the same as the retention period of a device operating at that junction temperature.

Table 2-19 • **Military Temperature Grade Product Performance Retention**

Minimum Time at T_J 110°C or Below	Minimum Time at T_J 125°C or Below	Minimum Time at T_J 135°C or Below	Minimum Time at T_J 150°C or Below	Minimum Performance Retention (Years)
100%				20.0
90%	10%			18.2
75%	25%			16
90%		10%		15.4
50%	50%			13.3
90%			10%	11.8
75%		25%		11.4
	100%			10
	90%	10%		9.1
50%		50%		8
	75%	25%		8
	90%		10%	7.7
75%			25%	7.3
	50%	50%		6.7
	75%		25%	5.7
		100%		5
		90%	10%	4.5
50%			50%	4.4
	50%		50%	4
		75%	25%	4
		50%	50%	3.3
			100%	2.5

Table 2-20 • **Recommended Maximum Operating Conditions Programming and PLL Supplies**

Parameter	Condition	Commercial/Industrial/Military/MIL-STD-883		Units
		Minimum	Maximum	
V_{PP}	During Programming	15.8	16.5	V
	Normal Operation[1]	0	16.5	V
V_{PN}	During Programming	–13.8	–13.2	V
	Normal Operation[2]	–13.8	0.5	V
I_{PP}	During Programming		25	mA
I_{PN}	During Programming		10	mA
AVDD		V_{DD}	V_{DD}	V
AGND		GND	GND	V

Notes:
1. *Please refer to the "V_{PP} Programming Supply Pin" section on page 2-74 for more information.*
2. *Please refer to the "V_{PN} Programming Supply Pin" section on page 2-74 for more information.*

Table 2-21 • **Recommended Operating Conditions**

Parameter	Symbol	Limits		
		Commercial	Industrial	Military/MIL-STD-883
DC Supply Voltage (2.5 V I/Os)	V_{DD} and V_{DDP}	2.5 V ± 0.2 V	2.5 V ± 0.2 V	2.5 V ± 0.2 V
DC Supply Voltage (3.3 V I/Os)	V_{DDP} V_{DD}	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V
Operating Ambient Temperature Range	T_A, T_C	0°C to 70°C	–40°C to 85°C	–55°C (T_A) to 125°C (T_C)
Maximum Operating Junction Temperature	T_J	110°C	110°C	150°C

Note: *For I/O long-term reliability, external pull-up resistors cannot be used to increase output voltage above V_{DDP}.*

Table 2-22 • **DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V)**

Symbol	Parameter	Conditions		Commercial/Industrial/ Military/MIL-STD-883[1, 2] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	 I_{OH} = –6 mA I_{OH} = –12 mA I_{OH} = –24 mA I_{OH} = –3 mA I_{OH} = –6 mA I_{OH} = –8 mA		 2.1 2.0 1.7 2.1 1.9 1.7			 V
V_{OL}	Output Low Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	 I_{OL} = 8 mA I_{OL} = 15 mA I_{OL} = 24 mA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 15 mA				 0.2 0.4 0.7 0.2 0.4 0.7	 V
V_{IH}[3]	Input High Voltage			1.7		V_{DDP} + 0.3	V
V_{IL}[4]	Input Low Voltage			–0.3		0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (OTB25LPU)	$V_{IN} \geq$ 1.25 V		6		56	kΩ
HYST	Input Hysteresis Schmitt	See Table 2-4 on page 2-6		0.3	0.35	0.45	V
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–240		– 20	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[5] or V_{DD}	Std.		5.0	15	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[5] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military/MIL-STD-883	V_{IN} = GND[5] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
I_{OSH}	Output Short Circuit Current High High Drive (OB25LPH) Low Drive (OB25LPL)	 V_{IN} = V_{SS} V_{IN} = V_{SS}		 –120 –100			mA

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All process conditions. Military: Junction Temperature: –55 to +150°C.*
3. *During transitions, the input signal may overshoot to V_{DDP} +1.0V for a limited time of no larger than 10% of the duty cycle.*
4. *During transitions, the input signal may undershoot to -1.0V for a limited time of no larger than 10% of the duty cycle.*
5. *No pull-up resistor.*

Table 2-22 • **DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V) (Continued)**

Symbol	Parameter	Conditions	Commercial/Industrial/ Military/MIL-STD-883[1, 2]			
			Min.	Typ.	Max.	Units
I_{OSL}	Output Short Circuit Current Low High Drive (OB25LPH) Low Drive (OB25LPL)	 $V_{IN} = V_{DDP}$ $V_{IN} = V_{DDP}$			 100 30	mA
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All process conditions. Military: Junction Temperature: –55 to +150°C.*
3. *During transitions, the input signal may overshoot to V_{DDP} +1.0V for a limited time of no larger than 10% of the duty cycle.*
4. *During transitions, the input signal may undershoot to -1.0V for a limited time of no larger than 10% of the duty cycle.*
5. *No pull-up resistor.*

Table 2-23 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Commercial and Industrial Temperature Only**

Symbol	Parameter	Conditions		Commercial/Industrial[1] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3 V I/O, High Drive (OB33P) 3.3 V I/O, Low Drive (OB33L)	 I_{OH} = –14 mA I_{OH} = –24 mA I_{OH} = –6 mA I_{OH} = –12 mA		 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive (OB33P) 3.3 V I/O, Low Drive (OB33L)	 I_{OL} = 15 mA I_{OL} = 20 mA I_{OL} = 28 mA I_{OL} = 7 mA I_{OL} = 10 mA I_{OL} = 15 mA				 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
V_{IH}[2]	Input High Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			 1.6 2 1.7		 V_{DDP} + 0.3 V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}[3]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			 –0.3 –0.3 –0.3		 0.8 0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	15	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[4] or V_{DD}	Std.		5.0	25	mA

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
3. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*
4. *No pull-up resistor required.*

Table 2-23 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Commercial and Industrial Temperature Only

Symbol	Parameter	Conditions	Commercial/Industrial[1]			Units
			Min.	Typ.	Max.	
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND	 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}			 200 100	
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
3. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*
4. *No pull-up resistor required.*

Table 2-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only**

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3 V I/O, High Drive, High Slew (OB33PH) 3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL) 3.3 V I/O, Low Drive, High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	 I_{OH} = –8 mA I_{OH} = –16 mA I_{OH} = –3mA I_{OH} = –8mA I_{OH} = –3 mA I_{OH} = –8 mA		 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive, High Slew (OB33PH) 3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL)) 3.3 V I/O, Low Drive, High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	 I_{OL} = 12 mA I_{OL} = 17 mA I_{OL} = 28 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA		 		 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
V_{IH}[2]	Input High Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			 1.6 2 1.7		 V_{DDP} + 0.3 V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}[3]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			 –0.3 –0.3 –0.3		 0.7 0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	15	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	20	mA

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
3. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*
4. *No pull-up resistor required.*

Table 2-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Military Temperature and MIL-STD-883B Temperature Only

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[4] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
3. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*
4. *No pull-up resistor required.*

Table 2-25 • **DC Specifications (3.3 V PCI Operation)[1]**

Symbol	Parameter	Condition		Commercial/ Industrial[2]		Military/MIL-STD- 883[2]		Units
				Min.	Max.	Min.	Max.	
V_{DD}	Supply Voltage for Core			2.3	2.7	2.3	2.7	V
V_{DDP}	Supply Voltage for I/O Ring			3.0	3.6	3.0	3.6	V
V_{IH}	Input High Voltage			$0.5V_{DDP}$	V_{DDP} + 0.5	$0.5V_{DDP}$	V_{DDP} + 0.5	V
V_{IL}	Input Low Voltage			–0.5	$0.3V_{DDP}$	–0.5	$0.3V_{DDP}$	V
I_{IPU}	Input Pull-up Voltage[3]			$0.7V_{DDP}$		$0.7V_{DDP}$		V
I_{IL}	Input Leakage Current[4]	$0 < V_{IN} < V_{DDP}$	Std.	–10	10	–50	50	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA		$0.9V_{DDP}$		$0.9V_{DDP}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA			$0.1V_{DDP}$		$0.1V_{DDP}$	V
C_{IN}	Input Pin Capacitance (except CLK)				10		10	pF
C_{CLK}	CLK Pin Capacitance			5	12	5	12	pF

Notes:

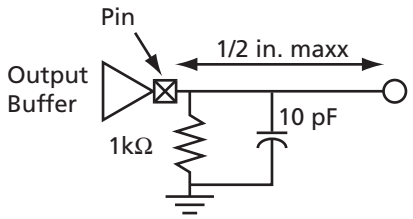
1. *For PCI operation, use GL33, OTB33PH, OB33PH, IOB33PH, IB33, or IB33S macro library cell only.*
2. *All process conditions. Junction Temperature: –40 to +110°C for Commercial and Industrial devices and –55 to +125°C for Military.*
3. *This specification is guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers with applications sensitive to static power utilization should ensure that the input buffer is conducting minimum current at this input voltage.*
4. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*

Table 2-26 • **AC Specifications (3.3 V PCI Revision 2.2 Operation)**

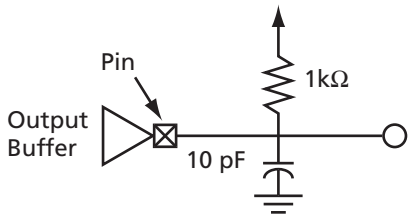
Symbol	Parameter	Condition	Commercial/Industrial/Military/MIL-STD- 883		Units
			Min.	Max.	
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{DDP}$*	$-12V_{DDP}$		mA
		$0.3V_{DDP} \le V_{OUT} < 0.9V_{DDP}$*	$(-17.1 + (V_{DDP} - V_{OUT}))$		mA
		$0.7V_{DDP} < V_{OUT} < V_{DDP}$*		See equation C – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.7V_{DDP}$*		$-32V_{DDP}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{DDP} > V_{OUT} \ge 0.6V_{DDP}$*	$16V_{DDP}$		mA
		$0.6V_{DDP} > V_{OUT} > 0.1V_{DDP}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{DDP} > V_{OUT} > 0$*		See equation D – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.18V_{DDP}$		$38V_{DDP}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{DDP} + 4 > V_{IN} \ge V_{DDP} + 1$	$25 + (V_{IN} - V_{DDP} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{DDP}$ to $0.6V_{DDP}$ load*	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{DDP}$ to $0.2V_{DDP}$ load*	1	4	V/ns

Note: ** Refer to the PCI Specification document rev. 2.2.*

Pad Loading Applicable to the Rising Edge PCI



Pad Loading Applicable to the Falling Edge PCI



Tristate Buffer Delays

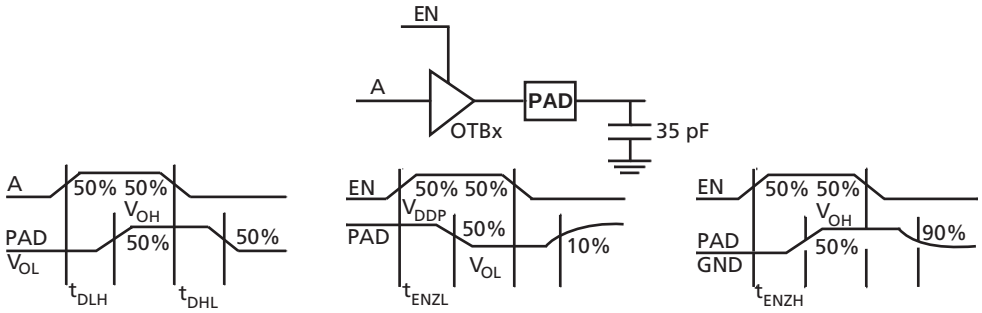


Figure 2-23 • **Tristate Buffer Delays**

Table 2-27 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Max. t_{ENZH}[3] Std.	Max. t_{ENZL}[4] Std.	Units
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.0	2.2	2.2	2.0	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.2	2.9	2.4	2.1	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.5	3.2	2.7	2.8	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.6	4.0	2.8	3.0	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	2.9	4.3	3.2	4.1	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.0	5.6	3.3	5.5	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*
3. *t_{ENZH} = Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*

Table 2-28 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Max. t_{ENZH}[3] Std.	Max. t_{ENZL}[4] Std.	Units
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[5]	2.0	2.1	2.3	2.0	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[5]	2.4	3.0	2.7	2.1	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[5]	2.9	3.2	3.1	2.7	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[5]	2.7	4.6	3.0	2.6	ns
OTB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[5]	3.5	4.2	3.8	3.8	ns
OTB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[5]	4.0	5.3	4.2	5.1	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*
3. *t_{ENZH} = Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP} = 2.5 V ±10% only. V_{DDP} = 2.3 V for delays.*

Table 2-29 • **Worst-Case Military Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Max. t_{ENZH}[3] Std.	Max. t_{ENZL}[4] Std.	Units
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.2	2.4	2.3	2.1	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.4	3.2	2.7	2.3	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.7	3.5	2.9	3.0	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.7	4.3	3.0	3.1	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	3.3	4.7	3.4	4.4	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.2	6.0	3.5	5.9	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*
3. *t_{ENZH} = Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*

Table 2-30 • **Worst-Case Military Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Max. t_{ENZH}[3] Std.	Max. t_{ENZL}[4] Std.	Units
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[5]	2.3	2.3	2.4	2.1	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[5]	2.7	3.2	2.8	2.1	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[5]	3.2	3.5	3.3	2.8	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[5]	3.0	5.0	3.2	2.8	ns
OTB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[5]	3.7	4.5	4.1	4.1	ns
OTB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[5]	4.4	5.8	4.4	5.4	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*
3. *t_{ENZH} = Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP} = 2.5 V ± 10% only. V_{DDP} = 2.3 V for delays.*

Output Buffer Delays

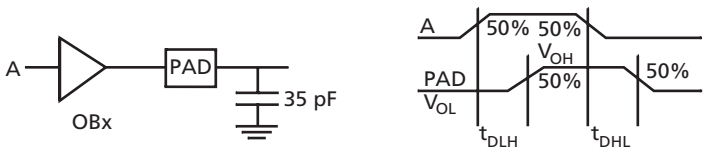


Figure 2-24 • **Output Buffer Delays**

Table 2-31 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB33PH	3.3 V, PCI Output Current, High Slew Rate	2.0	2.2	ns
OB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.2	2.9	ns
OB33PL	3.3 V, High Output Current, Low Slew Rate	2.5	3.2	ns
OB33LH	3.3 V, Low Output Current, High Slew Rate	2.6	4.0	ns
OB33LN	3.3 V, Low Output Current, Nominal Slew Rate	2.9	4.3	ns
OB33LL	3.3 V, Low Output Current, Low Slew Rate	3.0	5.6	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*

Table 2-32 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[3]	2.0	2.1	ns
OB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[3]	2.4	3.0	ns
OB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[3]	2.9	3.2	ns
OB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[3]	2.7	4.6	ns
OB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[3]	3.5	4.2	ns
OB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[3]	4.0	5.3	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*
3. *Low-power I/Os work with V_{DDP} = 2.5 V ±10% only. V_{DDP} = 2.3 V for delays.*

Table 2-33 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB33PH	3.3V, PCI Output Current, High Slew Rate	2.1	2.3	ns
OB33PN	3.3V, High Output Current, Nominal Slew Rate	2.5	3.2	ns

Table 2-33 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB33PL	3.3V, High Output Current, Low Slew Rate	2.7	3.5	ns
OB33LH	3.3V, Low Output Current, High Slew Rate	2.7	4.3	ns
OB33LN	3.3V, Low Output Current, Nominal Slew Rate	3.3	4.7	ns
OB33LL	3.3V, Low Output Current, Low Slew Rate	3.3	6.1	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*

Table 2-34 • **Worst-Case Military Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate[3]	2.3	2.4	ns
OB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate[3]	2.7	3.3	ns
OB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate[3]	3.2	3.5	ns
OB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate[3]	3.0	5.0	ns
OB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate[3]	3.9	4.6	ns
OB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate[3]	4.3	5.7	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*
3. *Low power I/O work with V_{DDP} = 2.5 V ±10% only. V_{DDP} = 2.3 V for delays.*

Input Buffer Delays

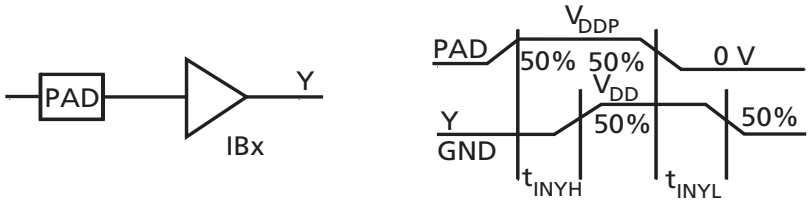


Figure 2-25 • **Input Buffer Delays**

Table 2-35 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1] Std.	Max. t_{INYL}[2] Std.	Units
IB33	3.3 V, CMOS Input Levels[3], No Pull-up Resistor	0.4	0.6	ns
IB33S	3.3 V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*

Table 2-36 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1] Std.	Max. t_{INYL}[2] Std.	Units
IB25LP	2.5 V, CMOS Input Levels[3], Low Power	0.9	0.6	ns
IB25LPS	2.5 V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.7	0.9	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP} = 2.3 V for delays.*

Table 2-37 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB33	3.3 V, CMOS Input Levels[3], No Pull-up Resistor	0.5	0.6	ns
IB33S	3.3 V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP} = 2.3 V for delays.*

Table 2-38 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB25LP	2.5 V, CMOS Input Levels[3], Low Power	0.9	0.7	ns
IB25LPS	2.5 V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.8	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP} = 2.3 V for delays.*

Global Input Buffer Delays

Table 2-39 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1] Std.[3]	Max. t_{INYL}[2] Std.[3]	Units
GL33	3.3 V, CMOS Input Levels[4], No Pull-up Resistor	1.0	1.1	ns
GL33S	3.3 V, CMOS Input Levels[4], No Pull-up Resistor, Schmitt Trigger	1.0	1.1	ns
PECL	PPECL Input Levels	1.0	1.1	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *Applies to Military ProASIC PLUS devices.*
4. *LVTTL delays are the same as CMOS delays.*
5. *For LP Macros, V_{DDP} = 2.3 V for delays.*

Table 2-40 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1] Std.[3]	Max. t_{INYL}[2] Std.[3]	Units
GL25LP	2.5 V, CMOS Input Levels[4], Low Power	1.1	1.0	ns
GL25LPS	2.5 V, CMOS Input Levels[4], Low Power, Schmitt Trigger	1.3	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *Applies to Military ProASIC PLUS devices.*
4. *LVTTL delays are the same as CMOS delays.*
5. *For LP Macros, V_{DDP} = 2.3 V for delays.*

Table 2-41 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]
		Std.	Std.
GL33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	1.1	1.1
GL33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	1.1	1.1
PECL	PPECL Input Levels	1.1	1.1

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP} = 2.3 V for delays.*

Table 2-42 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]
		Std.	Std.
GL25LP	2.5V, CMOS Input Levels[3], Low Power	1.0	1.1
GL25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	1.4	1.0

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP} = 2.3 V for delays.*

Predicted Global Routing Delay

Table 2-43 • **Worst-Case Commercial Conditions[1]**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Parameter	Description	Max. Std.	Units
t_{RCKH}	Input Low to High[2]	1.1	ns
t_{RCKL}	Input High to Low[2]	1.0	ns
t_{RCKH}	Input Low to High[3]	0.8	ns
t_{RCKL}	Input High to Low[3]	0.8	ns

Notes:

1. *The timing delay difference between tile locations is less than 15 ps.*
2. *Highly loaded row 50%.*
3. *Minimally loaded row.*

Table 2-44 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Parameter	Description	Max.	Units
t_{RCKH}	Input Low to High (high loaded row of 50%)	1.1	ns
t_{RCKL}	Input High to Low (high loaded row of 50%)	1.0	ns
t_{RCKH}	Input Low to High (minimally loaded row)	0.8	ns
t_{RCKL}	Input High to Low (minimally loaded row)	0.8	ns

Note: ** The timing delay difference between tile locations is less than 15 ps.*

Global Routing Skew

Table 2-45 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Parameter	Description	Max. Std.	Units
t_{RCKSWH}	Maximum Skew Low to High	270	ps
t_{RCKSHH}	Maximum Skew High to Low	270	ps

Table 2-46 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Parameter	Description	Max.	Units
t_{RCKSWH}	Maximum Skew Low to High	270	ps
t_{RCKSHH}	Maximum Skew High to Low	270	ps

Module Delays

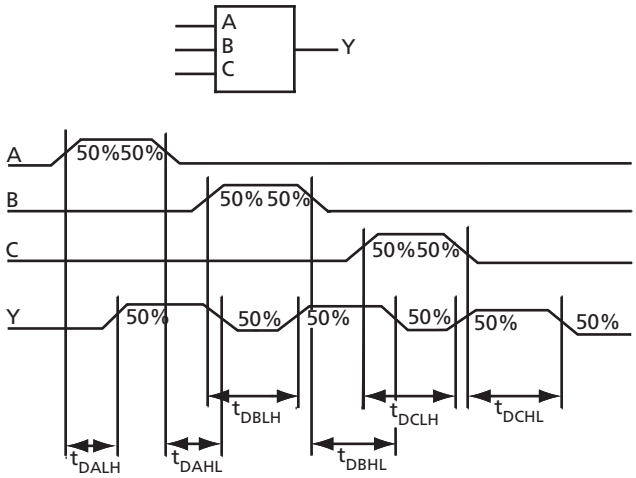


Figure 2-26 • **Module Delays**

Sample Macrocell Library Listing

Table 2-47 • **Worst-Case Military Conditions[1]**
V_{DD} = 2.3 V, T_J = 70° C, T_J = 70°C, T_J = 125°C for Military/MIL-STD-883

Cell Name	Description		Std. Max	Std. Min	Units
NAND2	2-Input NAND		0.5		ns
AND2	2-Input AND		0.7		ns
NOR3	3-Input NOR		0.8		ns
MUX2L	2-1 MUX with Active Low Select		0.5		ns
OA21	2-Input OR into a 2-Input AND		0.8		ns
XOR2	2-Input Exclusive OR		0.6		ns
LDL	Active Low Latch (LH/HL)				ns
	CLK-Q	LH[2]	0.9		
		HL[2]	0.8		ns
	t_{setup}			0.7	ns
	t_{hold}			0.1	ns
DFFL	Negative Edge-Triggered D-type Flip-Flop (LH/HL)				ns
	CLK-Q	LH[2]	0.9		
		HL[2]	0.8		ns
	t_{setup}			0.6	ns
	t_{hold}			0.0	ns

Notes:

1. *Intrinsic delays have a variable component, coupled to the input slope of the signal. These numbers assume an input slope typical of local interconnect.*
2. *LH and HL refer to the Q transitions from Low to High and High to Low, respectively.*

Table 2-48 • **Recommended Operating Conditions**

Parameter	Symbol	Limits	
		Commercial/Industrial	Military/MIL-STD-883
Maximum Clock Frequency*	f_{CLOCK}	180 MHz	180 MHz
Maximum RAM Frequency*	f_{RAM}	150 MHz	150 MHz
Maximum Rise/Fall Time on Inputs* • Schmitt Trigger Mode (10% to 90%) • Non-Schmitt Trigger Mode (10% to 90%)	 t_R/t_F t_R/t_F	 N/A 100 ns	 100 ns 10 ns
Maximum LVPECL Frequency*		180 MHz	180 MHz
Maximum TCK Frequency (JTAG)	f_{TCK}	10 MHz	10 MHz

Table 2-49 • **Slew Rates Measured at C = 30pF, Nominal Power Supplies and 25°C**

Type	Trig. Level	Rising Edge (ns)	Slew Rate (V/ns)	Falling Edge (ns)	Slew Rate (V/ns)	PCI Mode
OB33PH	10%-90%	1.60	1.65	1.65	1.60	Yes
OB33PN	10%-90%	1.57	1.68	3.32	0.80	No
OB33PL	10%-90%	1.57	1.68	1.99	1.32	No
OB33LH	10%-90%	3.80	0.70	4.84	0.55	No
OB33LN	10%-90%	4.19	0.63	3.37	0.78	No
OB33LL	10%-90%	5.49	0.48	2.98	0.89	No
OB25LPHH	10%-90%	1.55	1.29	1.56	1.28	No
OB25LPHN	10%-90%	1.70	1.18	2.08	0.96	No
OB25LPHL	10%-90%	1.97	1.02	2.09	0.96	No
OB25LPLH	10%-90%	3.57	0.56	3.93	0.51	No
OB25LPLN	10%-90%	4.65	0.43	3.28	0.61	No
OB25LPLL	10%-90%	5.52	0.36	3.44	0.58	No

Table 2-50 • **JTAG Switching Characteristics**

Description	Symbol	Min	Max	Unit
Output delay from TCK falling to TDI, TMS	t_{TCKTDI}	–4	4	ns
TDO Setup time before TCK rising	t_{TDOTCK}	10		ns
TDO Hold time after TCK rising	t_{TCKTDO}	0		ns
TCK period	t_{TCK}	100 [2]	1,000	ns
RCK period	t_{RCK}	100	1,000	ns

Notes:

1. *For DC electrical specifications of the JTAG pins (TCK, TDI, TMS, TDO, TRST), refer to Table 2-22 on page 2-34 when V_{DDP} = 2.5 V and Table 2-24 on page 2-38 when V_{DDP} = 3.3 V.*
2. *If RCK is being used, there is no minimum on the TCK period.*

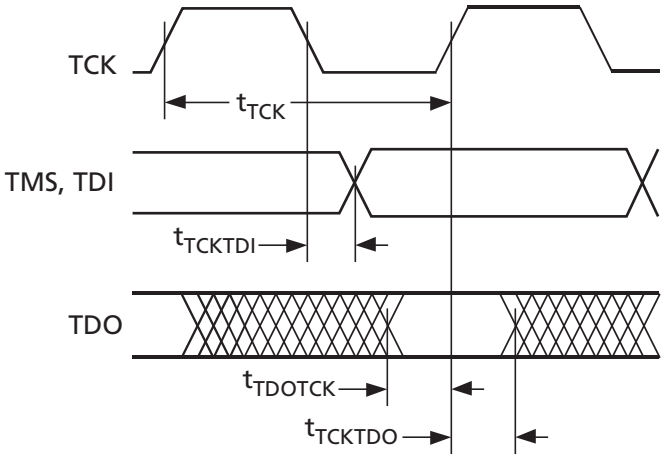


Figure 2-27 • **JTAG Operation Timing**

Embedded Memory Specifications

This section discusses ProASIC^PLUS SRAM/FIFO embedded memory and its interface signals, including timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 2-51). Table 2-13 on page 2-21 shows basic SRAM and FIFO configurations. Simultaneous read and write to the same location must be done with care. On such accesses the DI bus is output to the DO bus. Refer to the *ProASIC^PLUS RAM and FIFO Blocks* application note for more information.

Enclosed Timing Diagrams—SRAM Mode:

- "Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 2-55
- "Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 2-56
- "Asynchronous SRAM Write" section on page 2-57
- "Asynchronous SRAM Read, Address Controlled, RDB=0" section on page 2-58
- "Asynchronous SRAM Read, RDB Controlled" section on page 2-58
- "Synchronous SRAM Write"
- Embedded Memory Specifications

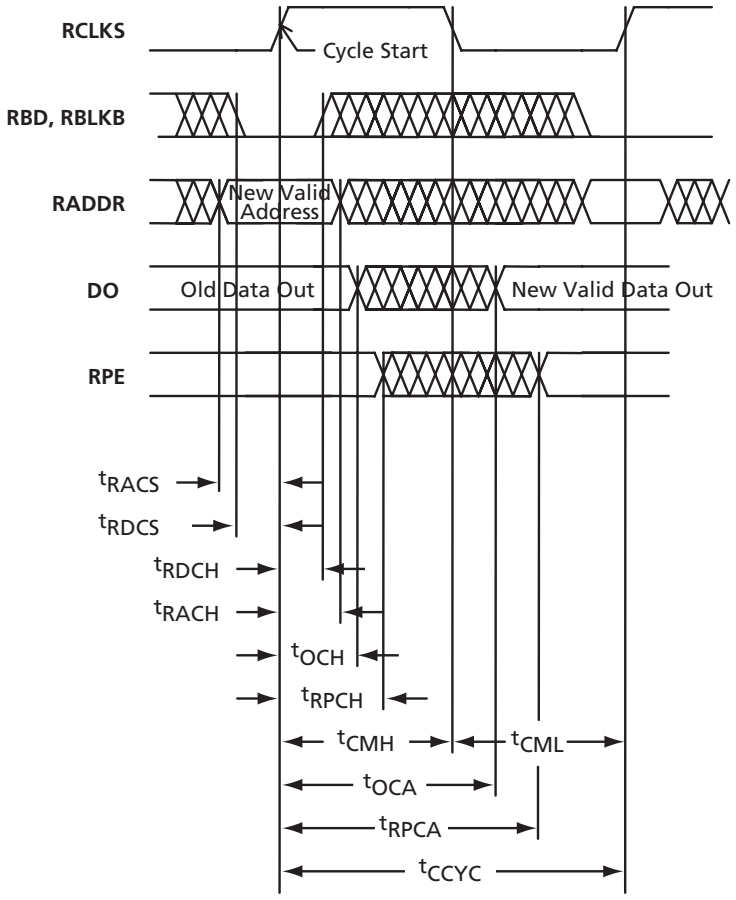
The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode, the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. If clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). Processing of this data in the same clock cycle is nearly impossible. Most designers add registers at all outputs of the memory to push the data processing into the next clock cycle. An entire clock cycle can then be used to process the data. To simplify use of this memory setup, suitable registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.

Table 2-51 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR[0:7]	8	In	Read address
RBLKB	1	In	True read block select (active Low)
RDB	1	In	True read pulse (active Low)
WADDR[0:7]	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI[0:8]	9	In	Input data bits [0:8], [8] can be used for parity In
WRB	1	In	Negative true write pulse
DO[0:8]	9	Out	Output data bits [0:8], [8] can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects odd parity generation/detect when high, even when low

Note: *Not all signals shown are used in all modes.*

Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)



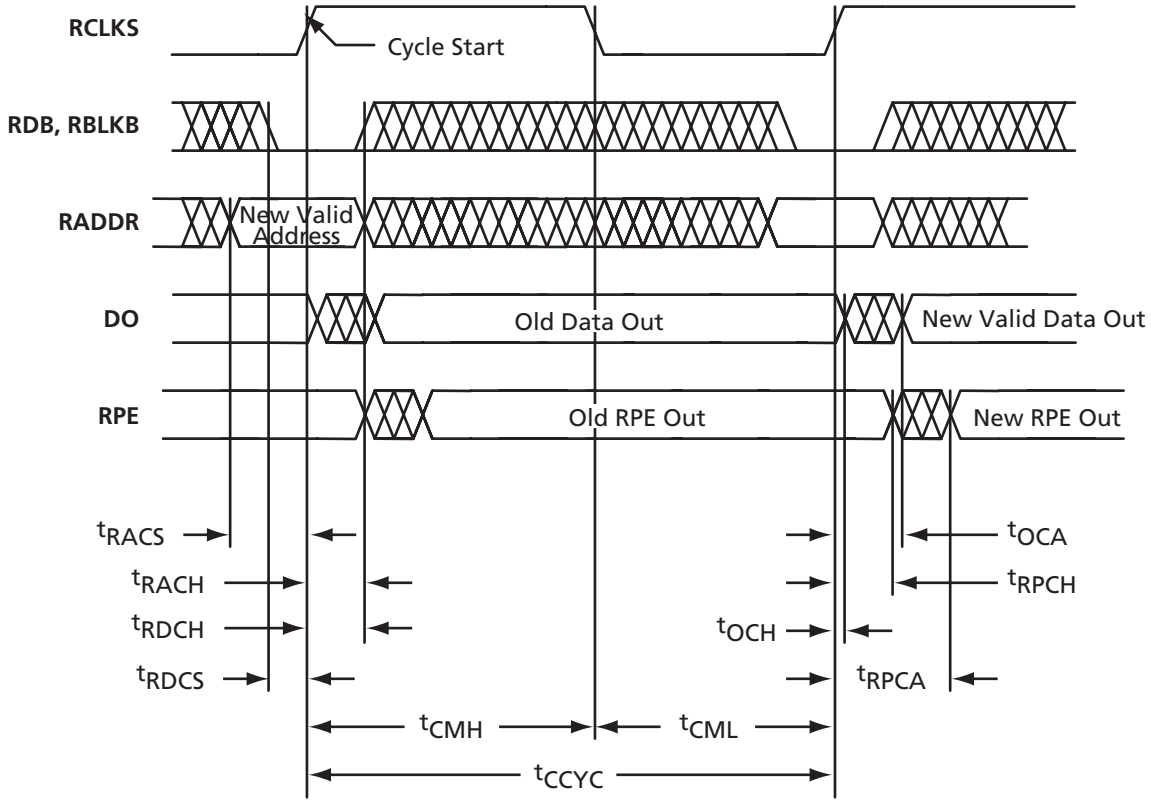
Note: *The plot shows the normal operation status.*

Figure 2-28 • **Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)**

Table 2-52 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	

Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)



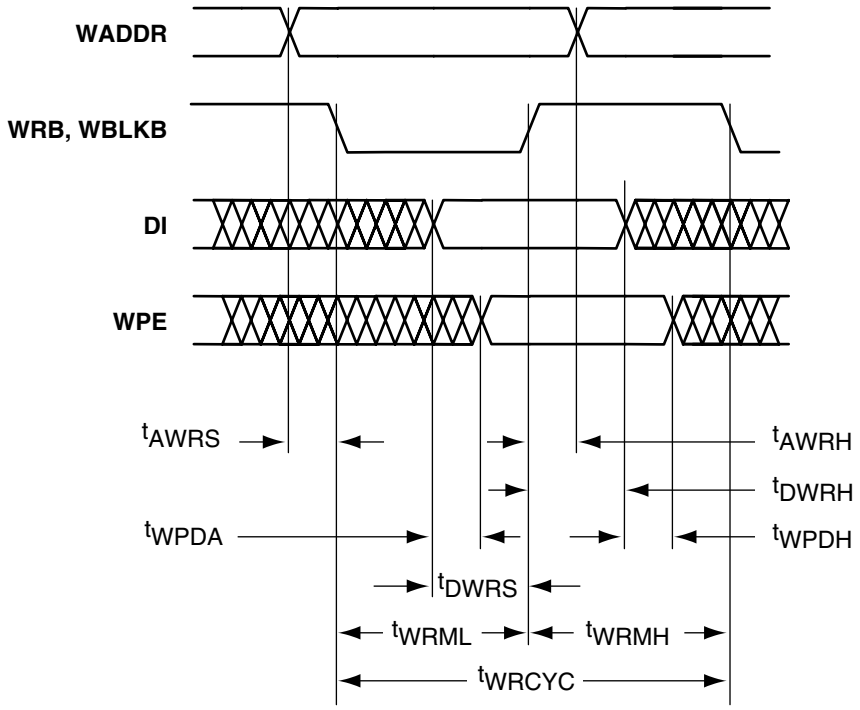
Note: *The plot shows the normal operation status.*

Figure 2-29 • **Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)**

Table 2-53 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = 0°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	

Asynchronous SRAM Write



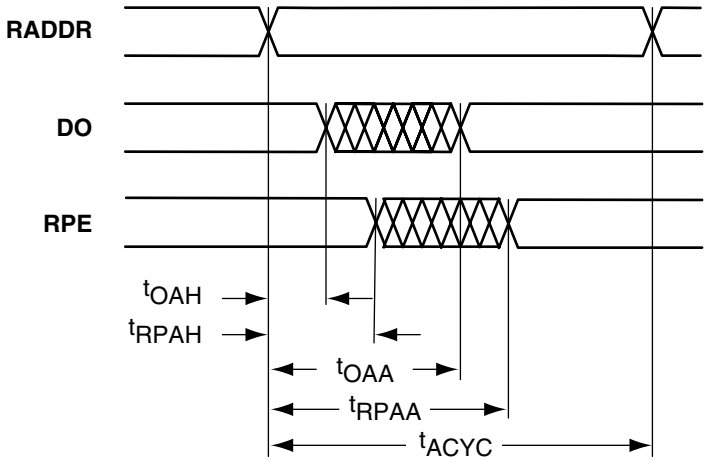
Note: *The plot shows the normal operation status.*

Figure 2-30 • **Asynchronous SRAM Write**

Table 2-54 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB ↑	1.0		ns	
AWRS	WADDR setup to WB ↓	0.5		ns	
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive.
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active.
WPDA	WPE access from DI	3.0		ns	WPE is invalid, while PARGEN is active.
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

Asynchronous SRAM Read, Address Controlled, RDB=0



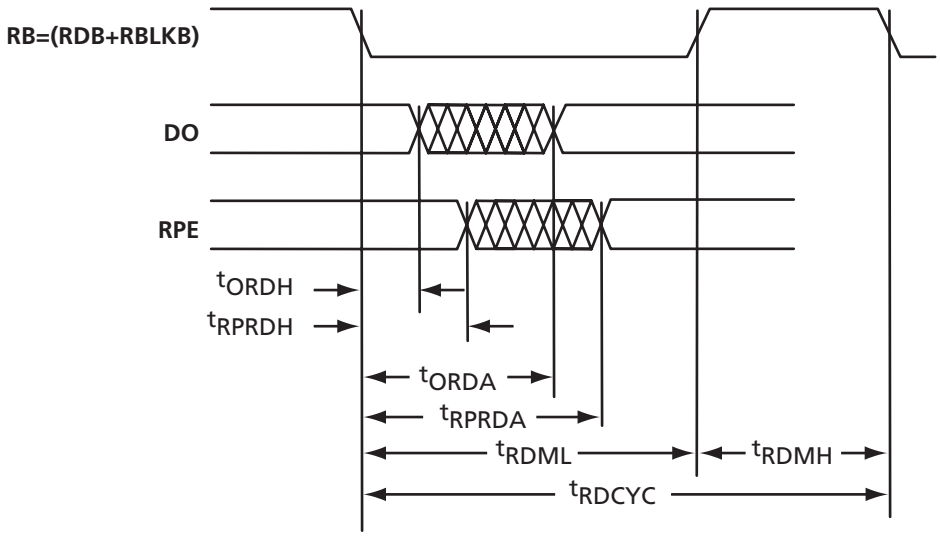
Note: *The plot shows the normal operation status.*

Figure 2-31 • **Asynchronous SRAM Read, Address Controlled, RDB = 0**

Table 2-55 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New DO access from RADDR stable	7.5		ns	
OAH	Old DO hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

Asynchronous SRAM Read, RDB Controlled



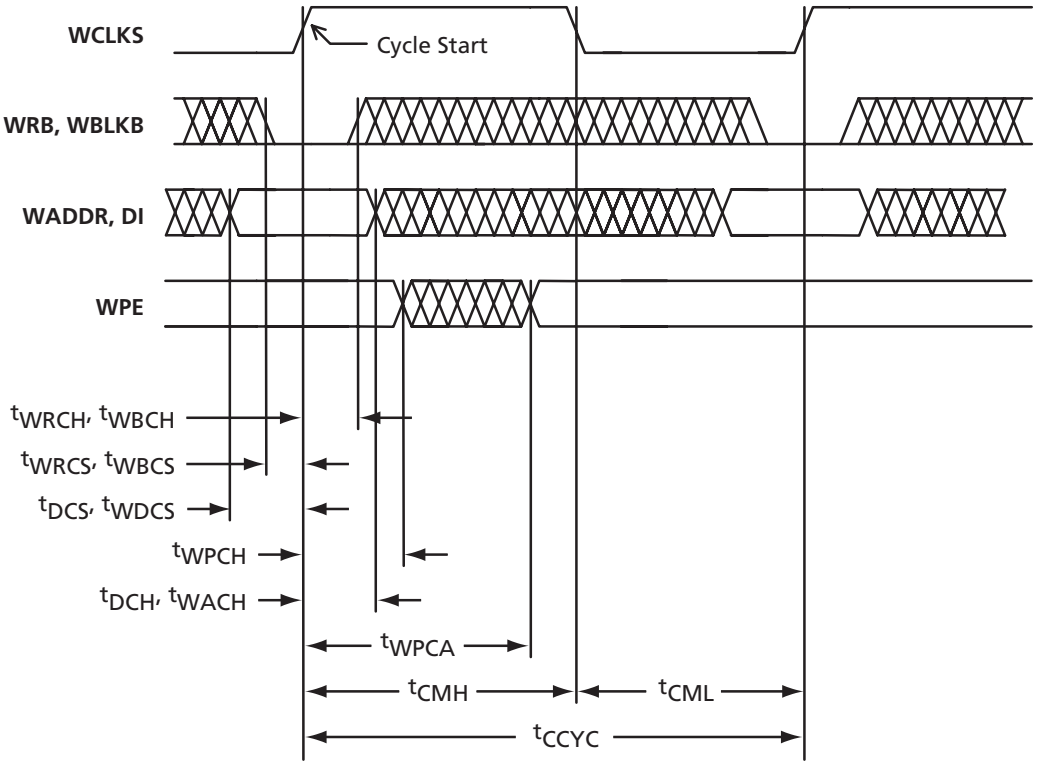
Note: *The plot shows the normal operation status.*

Figure 2-32 • **Asynchronous SRAM Read, RDB Controlled**

Table 2-56 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

Synchronous SRAM Write



Note: *The plot shows the normal operation status.*

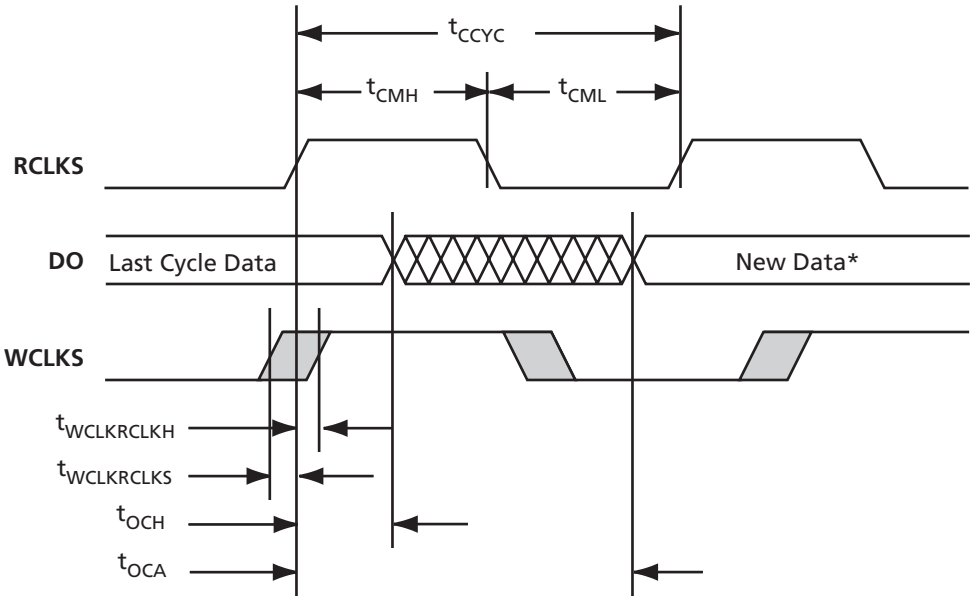
Figure 2-33 • **Synchronous SRAM Write**

Table 2-57 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
WACH	WADDR hold from WCLKS ↑	0.5		ns	
WDCS	WADDR setup to WCLKS ↑	1.0		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Note: *On simultaneous read and write accesses to the same location, DI is output to DO.*

Synchronous Write and Read to the Same Location



Note: ** New data is read if WCLKS ↑ occurs before setup time. The data stored is read if WCLKS ↑ occurs after hold time. The plot shows the normal operation status.*

Figure 2-34 • **Synchronous Write and Read to the Same Location**

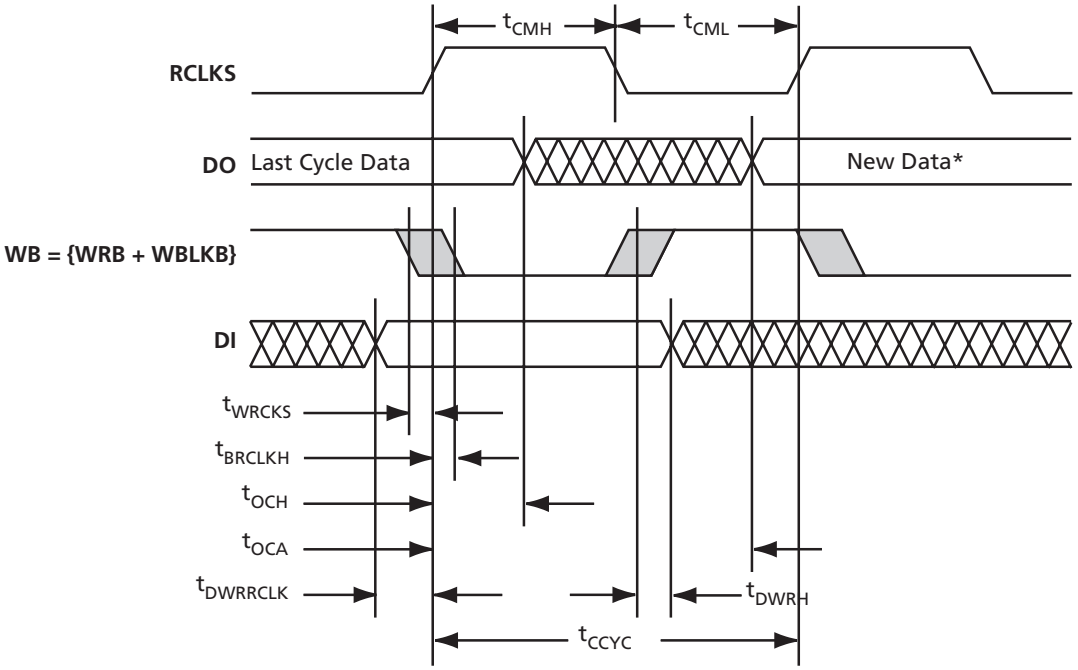
Table 2-58 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLKS ↑ to RCLKS ↑ setup time	– 0.1		ns	
WCLKRCLKH	WCLKS ↑ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLKS and RCLKS driven by the same design signal.*
3. *If WCLKS changes after the hold time, the data will be read.*
4. *A setup or hold time violation will result in unknown output data.*

Asynchronous Write and Synchronous Read to the Same Location



Note: **New data is read if WB ↓ occurs before setup time. The stored data is read if WB ↓ occurs after hold time. The plot shows the normal operation status.*

Figure 2-35 • **Asynchronous Write and Synchronous Read to the Same Location**

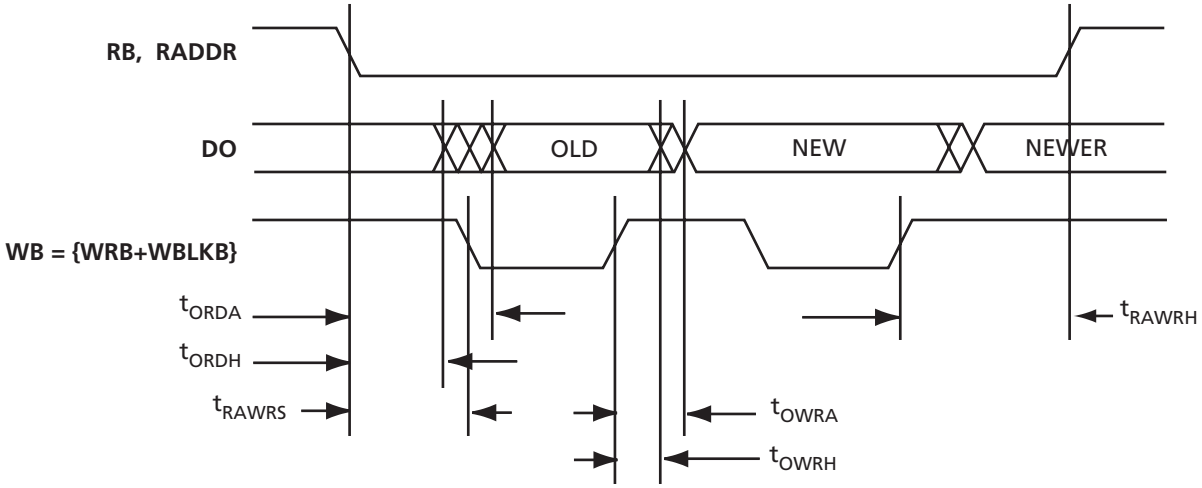
Table 2-59 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WBRCLKS	WB ↓ to RCLKS ↑ setup time	–0.1		ns	
WBRCLKH	WB ↓ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	
DWRRCLKS	DI to RCLKS ↑ setup time	0		ns	
DWRH	DI to WB ↑ hold time		1.5	ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.*
3. *A setup or hold time violation will result in unknown output data.*

Asynchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 2-36 • **Asynchronous Write and Read to the Same Location**

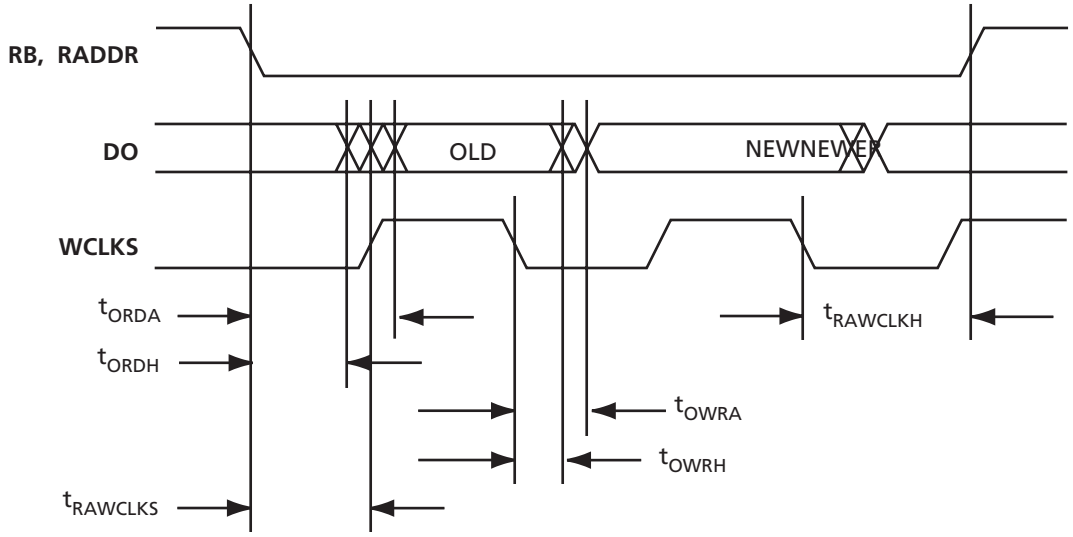
Table 2-60 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WB ↑	3.0		ns	
OWRH	Old DO valid from WB ↑		0.5	ns	
RAWRS	RB ↓ or RADDR from WB ↓	5.0		ns	
RAWRH	RB ↑ or RADDR from WB ↑	5.0		ns	

Notes:

1. *During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data. Refer to the ProASIC^PLUS RAM and FIFO Blocks application note for more information.*
2. *Violation or RAWRS will disturb access to the OLD data.*
3. *Violation of RAWRH will disturb access to the NEWER data.*

Synchronous Write and Asynchronous Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 2-37 • **Synchronous Write and Asynchronous Read to the Same Location**

Table 2-61 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WCLKS ↓	3.0		ns	
OWRH	Old DO valid from WCLKS ↓		0.5	ns	
RAWCLKS	RB ↓ or RADDR from WCLKS ↑	5.0		ns	
RAWCLKH	RB ↑ or RADDR from WCLKS ↓	5.0		ns	

Notes:

1. *During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.*
2. *Violation of RAWCLKS will disturb access to OLD data.*
3. *Violation of RAWCLKH will disturb access to NEWER data.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written to during the transition from full to not full, or read during the transition from empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. For slow cycles, this indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 2-1 on page 2-4).

The timing diagram for write is shown in Figure 2-35 on page 2-62. The timing diagram for read is shown in Figure 2-36 on page 2-63. For basic SRAM configurations, see Table 2-14 on page 2-22. When reset is asserted, the empty flag will be asserted, the counters will reset, the outputs go to zero, but the internal RAM is not erased.

Enclosed Timing Diagrams – FIFO Mode:

The following timing diagrams apply only to single cell; they are not applicable to cascaded cells. For more information, refer to the *ProASIC^PLUS RAM/FIFO Blocks* application note.

- "Asynchronous FIFO Read" section on page 2-67
- "Asynchronous FIFO Write" section on page 2-68
- "Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 2-69
- "Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 2-70
- "Synchronous FIFO Write" section on page 2-71
- "FIFO Reset" section on page 2-72

Table 2-62 • **Memory Block FIFO Interface Signals**

FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL [0:7]*	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI[0:8]	9	In	Input data bits [0:8], [8] will be generated if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH*	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO[0:8]	9	Out	Output data bits [0:8]
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP [0:2]	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: **LEVEL is always eight bits (0000.0000, 0000.0001). That means for values of DEPTH greater than 256, not all values will be possible, e.g. for DEPTH = 512, the LEVEL can only have the values 2, 4, . . ., 512. The LEVEL signal circuit will generate signals that indicate whether the FIFO is exactly filled to the value of LEVEL (EQTH) or filled equal or higher (GEQTH) than the specified LEVEL. Since counting starts at 0, EQTH will become true when the FIFO holds (LEVEL+1) words for 512-bit FIFOs.*

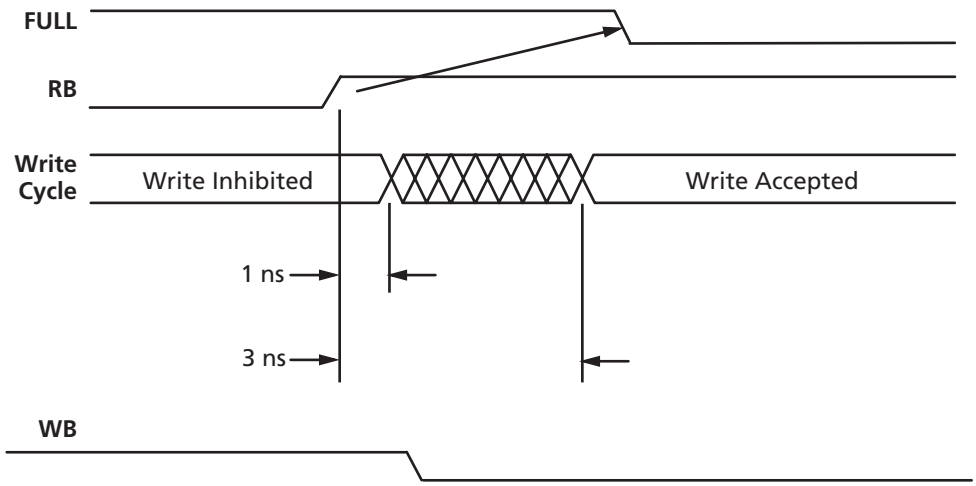


Figure 2-38 • **Write Timing Diagram**

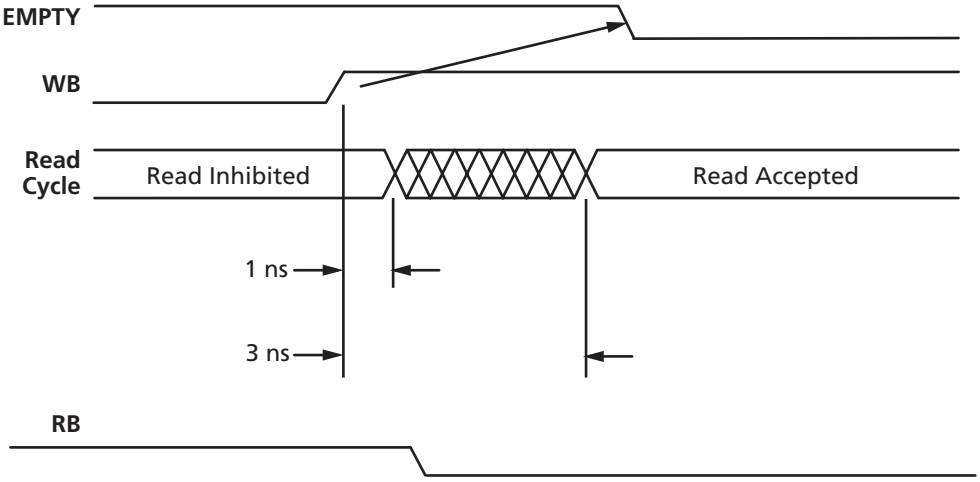
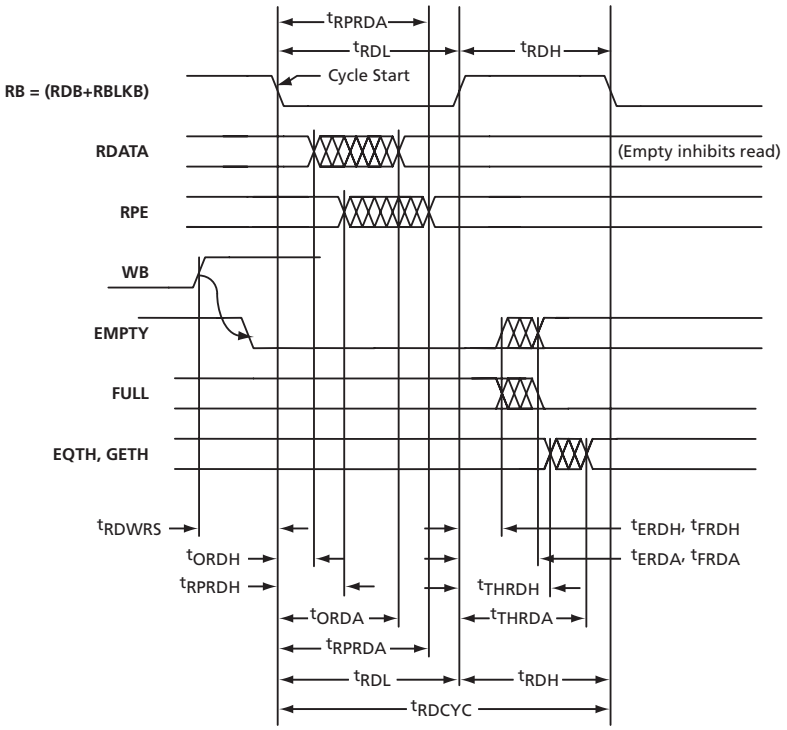


Figure 2-39 • **Read Timing Diagram**

Asynchronous FIFO Read



Note: *The plot shows the normal operation status.*

Figure 2-40 • **Asynchronous FIFO Read**

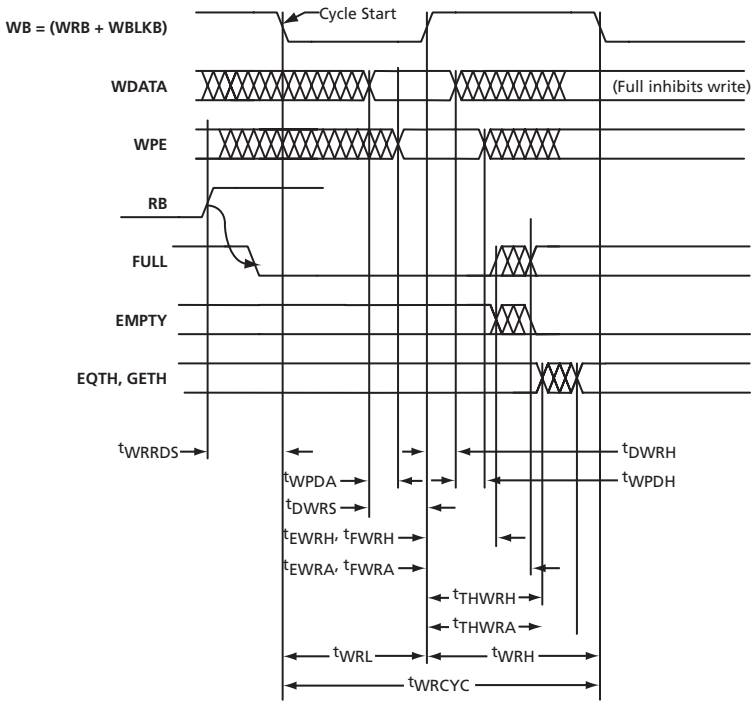
Table 2-63 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB ↑	3.0[1]		ns	
FRDA	FULL↓ access from RB ↑	3.0[1]		ns	
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	3.0[2]		ns	Enabling the read operation
			1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB↑	4.5		ns	

Notes:

1. *At fast cycles, ERDA and FRDA = MAX (7.5 ns – RDL), 3.0 ns.*
2. *At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns.*

Asynchronous FIFO Write



Note: *The plot shows the normal operation status.*

Figure 2-41 • **Asynchronous FIFO Write**

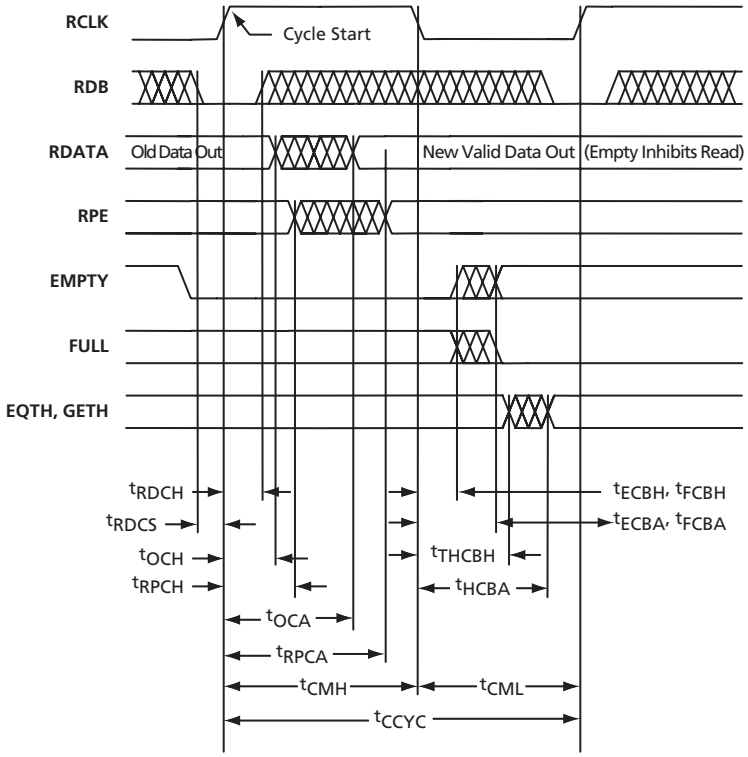
Table 2-64 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
EWRA	EMPTY ↓ access from WB ↑	3.0[1]		ns	
FWRA	New FULL access from WB ↑	3.0[1]		ns	
THWRA	EQTH or GETH access from WB ↑	4.5		ns	
WPDA	WPE access from DI	3.0		ns	WPE is invalid while PARGEN is active
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRRDS	RB ↑, clearing FULL, setup to WB ↓	3.0[2]		ns	Enabling the write operation
			1.0		Inhibiting the write operation
WRH	WB high phase	3.0		ns	Inactive
WRL	WB low phase	3.0		ns	Active

Notes:

1. *At fast cycles, EWRA, FWRA = MAX (7.5 ns – WRL), 3.0 ns.*
2. *At fast cycles, WRRDS (for enabling write) = MAX (7.5 ns – RDL), 3.0 ns.*
3. *After FIFO reset, WRB needs an initial falling edge prior to any write actions.*

Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

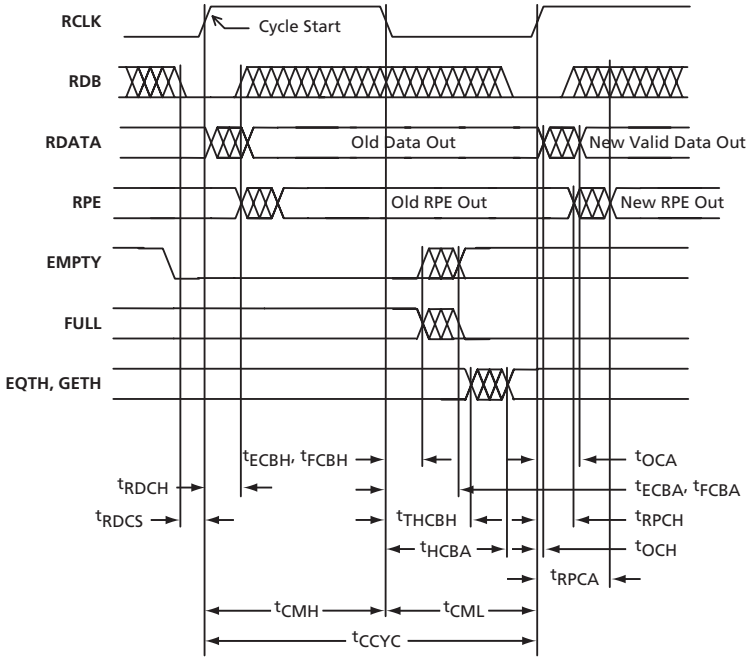
Figure 2-42 • **Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)**

Table 2-65 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0*		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0*		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Note: **At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.*

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: *The plot shows the normal operation status.*

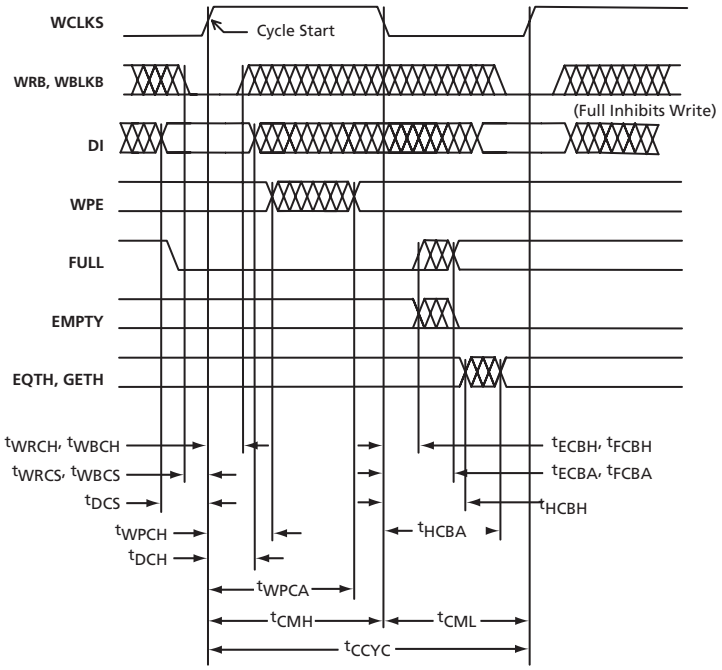
Figure 2-43 • **Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)**

Table 2-66 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0*		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0*		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Note: **At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMS), 3.0 ns.*

Synchronous FIFO Write



Note: *The plot shows the normal operation status.*

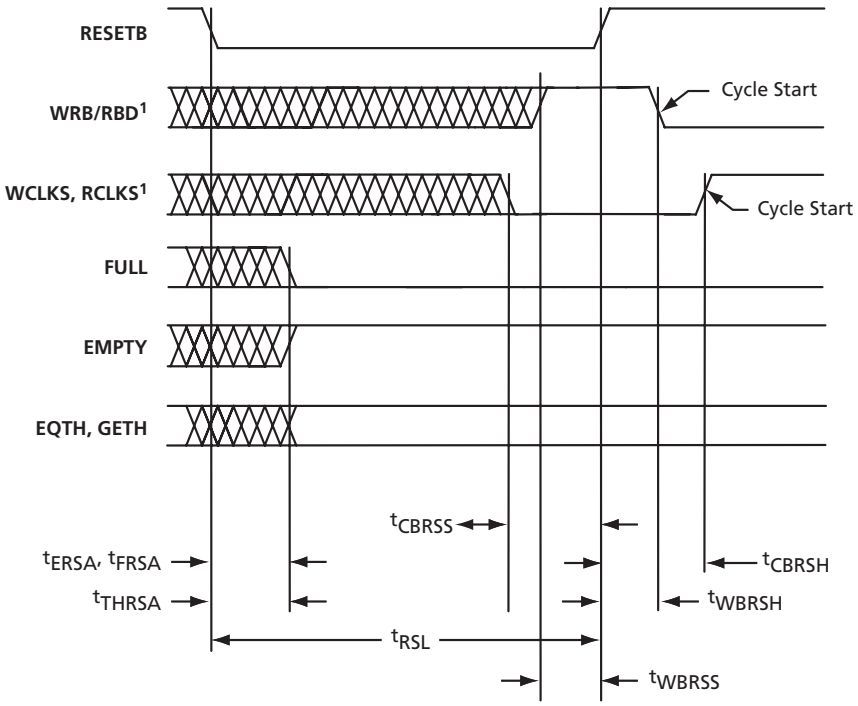
Figure 2-44 • **Synchronous FIFO Write**

Table 2-67 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
FCBA	New FULL access from WCLKS ↓	3.0*		ns	
ECBA	EMPTY↓ access from WCLKS ↓	3.0*		ns	
ECBH, FCBH, HCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
HCBA	EQTH or GETH access from WCLKS ↓	4.5		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid, while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Note: ** At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.*

FIFO Reset



Notes:

1. *During reset, either the enables (WRB and RBD) OR the clocks (WCLKS and RCKLS) must be low.*
2. *The plot shows the normal operation status.*

Figure 2-45 • **FIFO Reset**

Table 2-68 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CBRSH[1]	WCLKS or RCLKS ↑ hold from RESETB ↑	1.5		ns	Synchronous mode only
CBRSS[1]	WCLKS or RCLKS ↓ setup to RESETB ↑	1.5		ns	Synchronous mode only
ERSA	New EMPTY ↑ access from RESETB ↓	3.0		ns	
FRSA	FULL ↓ access from RESETB ↓	3.0		ns	
RSL	RESETB low phase	7.5		ns	
THRSA	EQTH or GETH access from RESETB ↓	4.5		ns	
WBRSH[1]	WB ↓ hold from RESETB ↑	1.5		ns	Asynchronous mode only
WBRSS[1]	WB ↑ setup to RESETB ↑	1.5		ns	Asynchronous mode only

Note: *During rest, the enables (WRB and RBD) must be high OR the clocks (WCLKS and RCKLS) must be low.*

Pin Description

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

NC **No Connect**

To maintain compatibility with other Actel ProASIC^PLUS products, it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Pin**

Low skew input pin for clock or other global signals. This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as a normal I/O.

GLMX **Global Multiplexing Pin**

Low skew input pin for clock or other global signals. This pin can be used in one of two special ways (refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits*).

When the external feedback option is selected for the PLL block, this pin is routed as the external feedback source to the clock conditioning circuit.

In applications where two different signals access the same global net at different times through the use of GLMXx and GLMXLx macros, this pin will be fixed as one of the source pins.

This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as any normal I/O. If not used, the GLMXx pin will be configured as an input with pull-up.

Dedicated Pins

GND **Ground**

Common ground supply voltage.

V_{DD} **Logic Array Power Supply Pin**

2.5 V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5 V or 3.3 V supply voltage.

TMS **Test Mode Select**

The TMS pin controls the use of boundary-scan circuitry. This pin has an internal pull-up resistor.

TCK **Test Clock**

Clock input pin for boundary scan (maximum 10 MHz). Actel recommends adding a nominal 20 kΩ pull-up resistor to this pin.

TDI **Test Data In**

Serial input for boundary scan. A dedicated pull-up resistor is included to pull this pin high when not being driven.

TDO **Test Data Out**

Serial output for boundary scan. Actel recommends adding a nominal 20kΩ pull-up resistor to this pin.

TRST **Test Reset Input**

Asynchronous, active low input pin for resetting boundary-scan circuitry. This pin has an internal pull-up resistor. For more information, please refer to *Power-up Behavior of ProASIC^PLUS Devices* application note.

Special Function Pins

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted. If not used, this pin has an internal pull-up and can be left floating.

NPECL **User Negative Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

PPECL **User Positive Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

AVDD **PLL Power Supply**

Analog V_{DD} should be V_{DD} (core voltage) 2.5 V (nominal) and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note. If the clock conditioning circuitry is not used in a design, AVDD can either be left floating or tied to 2.5 V.

AGND **PLL Power Ground**

The analog ground can be connected to the system ground. For more information, refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note. If the PLLs or clock conditioning circuitry are not used in a design, AGND should be tied to GND.

V_{PP} Programming Supply Pin

This pin may be connected to any voltage between GND and 16.5 V during normal operation, or it can be left unconnected.[2] For information on using this pin during programming, see the *In-System Programming ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to V_{DDP}.

V_{PN} Programming Supply Pin

This pin may be connected to any voltage between 0.5 V and –13.8 V during normal operation, or it can be left unconnected.[3] For information on using this pin during programming, see the *In-System Programming ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to GND.

Recommended Design Practice for V_{PN}/V_{PP}

ProASIC^PLUS Devices – APA450, APA600, APA750, APA1000

Bypass capacitors are required from V_{PP} to GND and V_{PN} to GND for all ProASIC^PLUS devices during programming. During the erase cycle, ProASIC^PLUS devices may have current surges on the V_{PP} and V_{PN} power supplies. The only way to maintain the integrity of the power distribution to the ProASIC^PLUS device during these current surges is to counteract the inductance of the finite length conductors that distribute the power to the device. This can be accomplished by providing sufficient bypass capacitance between the V_{PP} and V_{PN} pins and GND (using the shortest paths possible). Without sufficient bypass capacitance to counteract the inductance, the V_{PP} and V_{PN} pins may incur a voltage spike beyond the voltage that the device can withstand. This issue applies to all programming configurations.

The solution prevents spikes from damaging the ProASIC^PLUS devices. Bypass capacitors are required for the V_{PP} and V_{PN} pads. Use a 0.01 µF to 0.1 µF ceramic capacitor with a 25 V or greater rating. To filter low-frequency noise (decoupling), use a 4.7 µF (low ESR, <1 <Ω, tantalum, 25 V or greater rating) capacitor. The capacitors should be located as close to the device pins as possible (within 2.5 cm is desirable). The smaller, high-frequency capacitor should be placed closer to the device pins than the larger low-frequency capacitor. The same dual-capacitor circuit should be used on both the V_{PP} and V_{PN} pins (Figure 2-46).

ProASIC^PLUS Devices – APA075, APA150, APA300

These devices do not require bypass capacitors on the V_{PP} and V_{PN} pins as long as the total combined distance of the programming cable and the trace length on the board is less than or equal to 30 inches. Note: For trace lengths greater than 30 inches, use the bypass capacitor recommendations in the previous section.

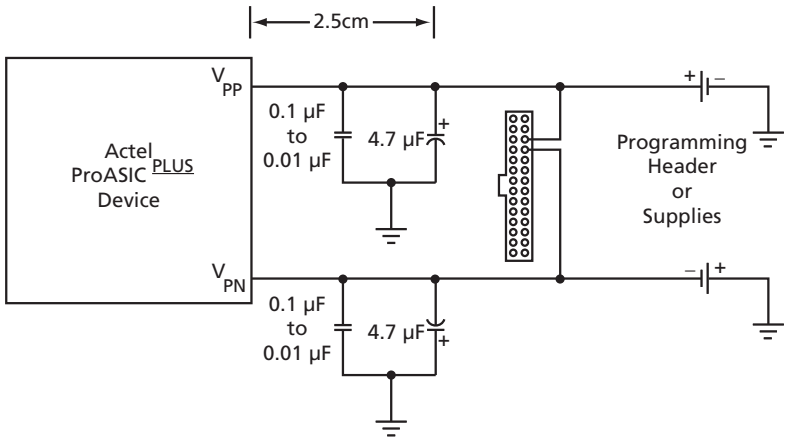
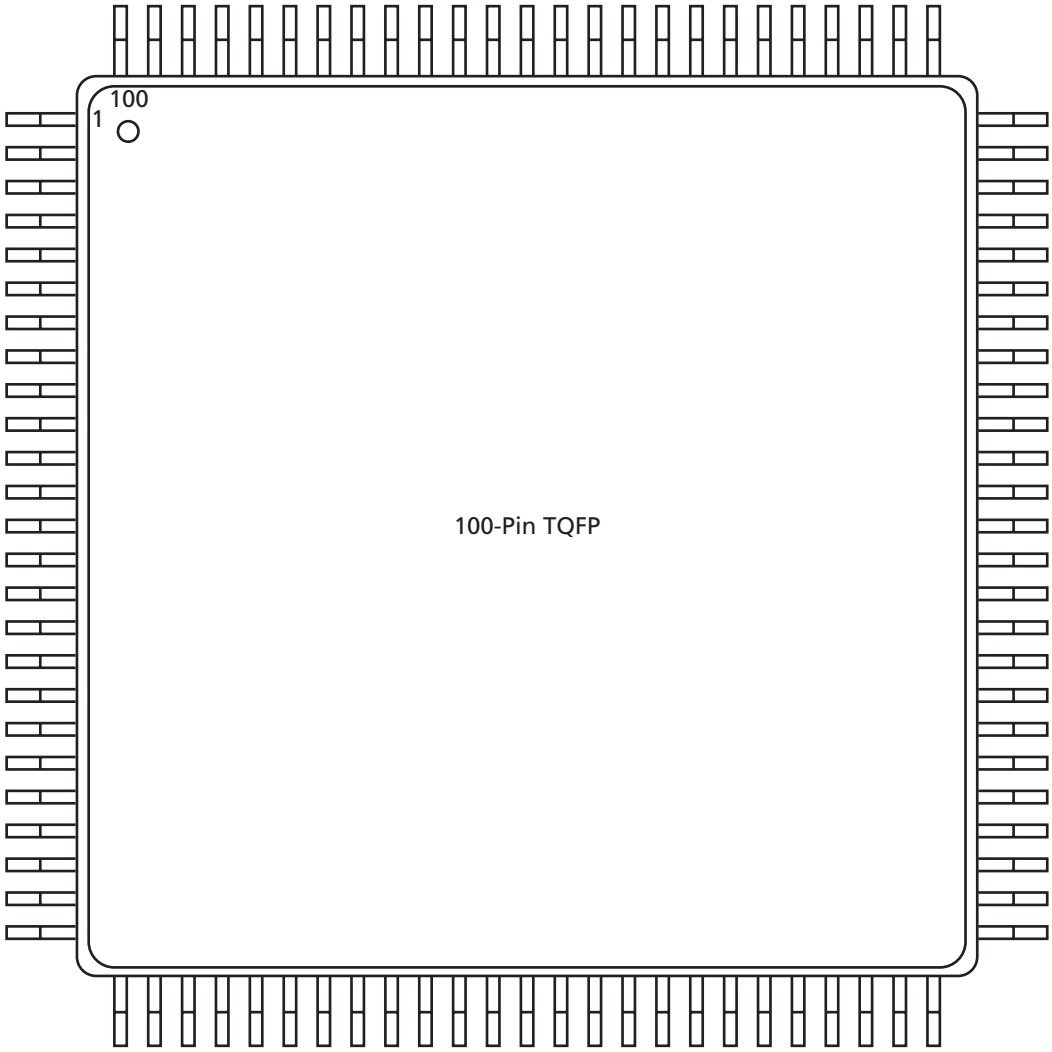


Figure 2-46 • **ProASIC^PLUS V_{PP} and V_{PN} Capacitor Requirements**

2. *There is a nominal 40 kΩ pull-up resistor on V_{PP}*
3. *There is a nominal 40 kΩ pull-down resistor on V_{PN}.*

Package Pin Assignments

100-Pin TQFP



Note

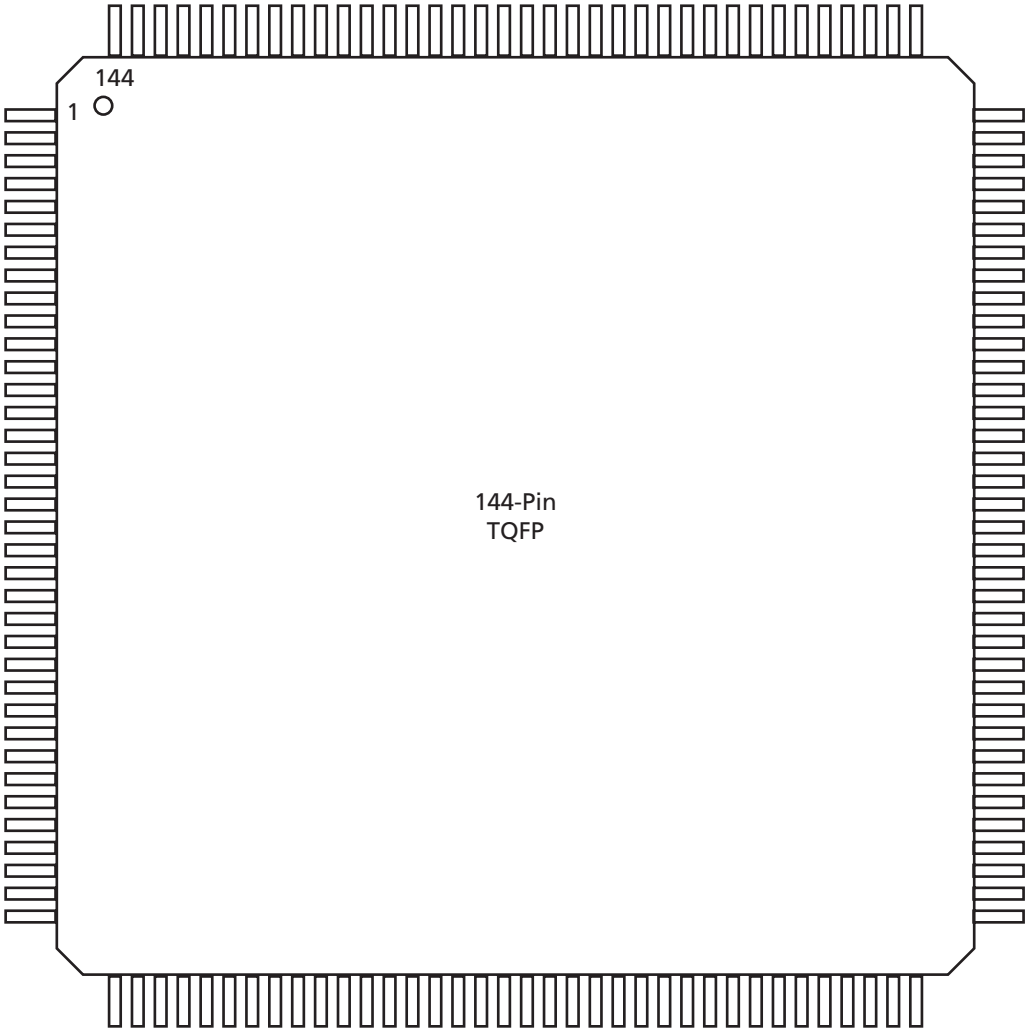
For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

100-Pin TQFP		
Pin Number	APA075 Function	APA150 Function
1	GND	GND
2	I/O	I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	GND	GND
10	I/O / GLMX1	I/O / GLMX1
11	I/O / GL1	I/O / GL1
12	AGND	AGND
13	NPECL1	NPECL1
14	AVDD	AVDD
15	PPECL1 / Input	PPECL1 / Input
16	I/O / GL2	I/O / GL2
17	V_{DD}	V_{DD}
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	GND	GND
26	V_{DDP}	V_{DDP}
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O

100-Pin TQFP		
Pin Number	APA075 Function	APA150 Function
36	I/O	I/O
37	V_{DD}	V_{DD}
38	GND	GND
39	V_{DDP}	V_{DDP}
40	GND	GND
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	TCK	TCK
48	TDI	TDI
49	TMS	TMS
50	V_{DDP}	V_{DDP}
51	GND	GND
52	V_{PP}	V_{PP}
53	V_{PN}	V_{PN}
54	TDO	TDO
55	TRST	TRST
56	RCK	RCK
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O / GL3	I/O / GL3
61	PPECL2 / Input	PPECL2 / Input
62	AVDD	AVDD
63	NPECL2	NPECL2
64	AGND	AGND
65	I/O / GL4	I/O / GL4
66	I/O / GLMX2	I/O / GLMX2
67	GND	GND
68	V_{DD}	V_{DD}
69	I/O	I/O
70	I/O	I/O

100-Pin TQFP		
Pin Number	APA075 Function	APA150 Function
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	GND	GND
76	V_{DDP}	V_{DDP}
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	GND	GND
87	V_{DDP}	V_{DDP}
88	GND	GND
89	V_{DD}	V_{DD}
90	I/O	I/O
91	I/O	I/O
92	I/O	I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	V_{DDP}	V_{DDP}

144-Pin TQFP



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

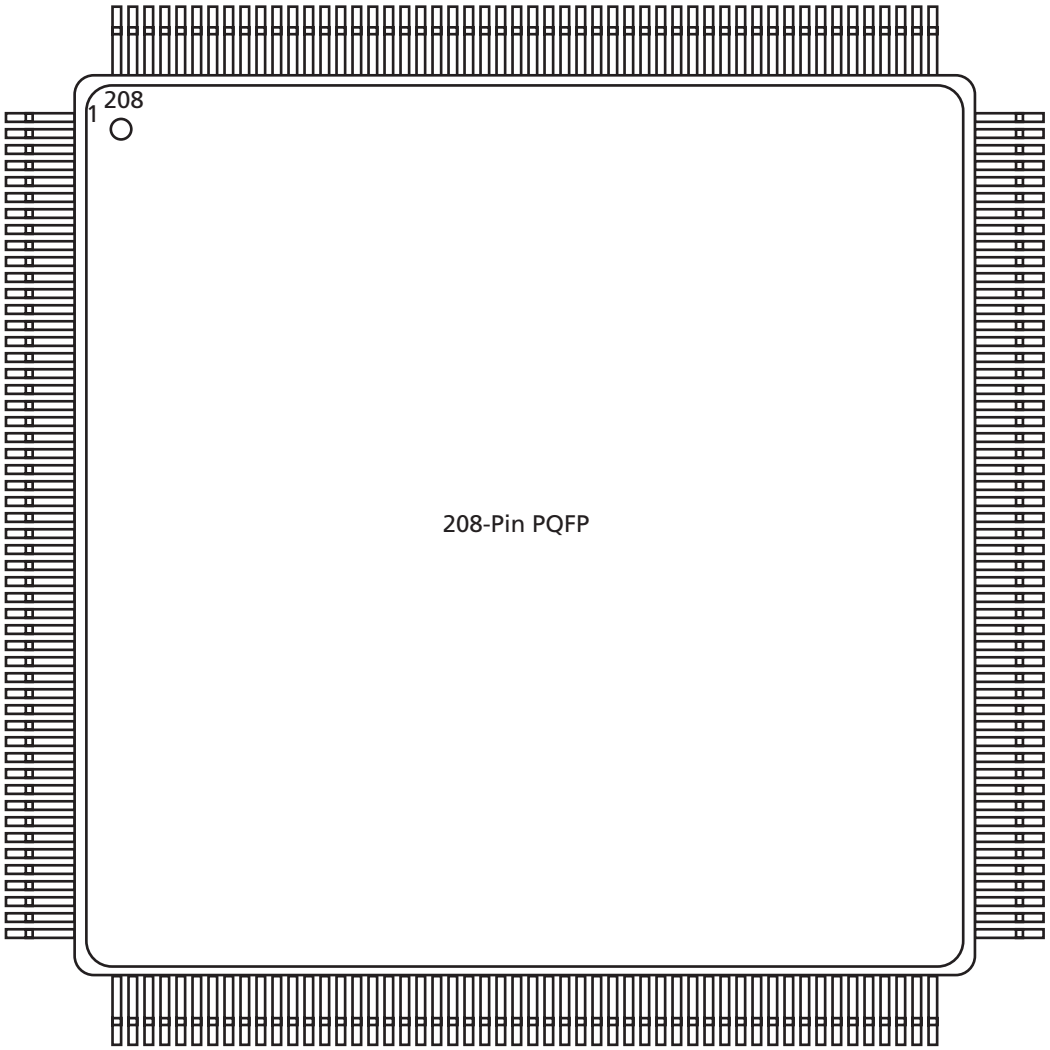
144-Pin TQFP	
Pin Number	**APA075 Function**
1	I/O
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	V_{DD}
10	GND
11	V_{DDP}
12	I/O
13	I/O
14	I/O
15	I/O / GLMX1
16	I/O / GL1
17	AGND
18	NPECL1
19	AVDD
20	PPECL1 / Input
21	I/O / GL2
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V_{DDP}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O

144-Pin TQFP	
Pin Number	**APA075 Function**
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	V_{DD}
46	GND
47	V_{DDP}
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	V_{DD}
63	GND
64	V_{DDP}
65	I/O
66	I/O
67	I/O
68	I/O
69	TCK
70	TDI
71	TMS
72	NC

144-Pin TQFP	
Pin Number	**APA075 Function**
73	V_{PP}
74	V_{PN}
75	TDO
76	TRST
77	RCK
78	I/O
79	I/O
80	I/O
81	V_{DDP}
82	GND
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O / GL3
89	PPECL2 / Input
90	AVDD
91	NPECL2
92	AGND
93	I/O / GL4
94	I/O / GLMX2
95	I/O
96	I/O
97	I/O
98	V_{DDP}
99	GND
100	V_{DD}
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O

144-Pin TQFP	
Pin Number	**APA075 Function**
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	V_{DDP}
118	GND
119	V_{DD}
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	I/O
134	V_{DDP}
135	GND
136	V_{DD}
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O

208-Pin PQFP



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

208-Pin PQFP							
Pin Number	**APA075 Function**	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
1	GND	GND	GND	GND	GND	GND	GND
2	I/O	I/O	I/O	I/O	I/O	I/O	I/O
3	I/O	I/O	I/O	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O	I/O	I/O	I/O
16	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
17	GND	GND	GND	GND	GND	GND	GND
18	I/O	I/O	I/O	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	I/O	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O	I/O	I/O	I/O
22	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
23	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1
24	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2
25	AGND	AGND	AGND	AGND	AGND	AGND	AGND
26	NPECL1	NPECL1	NPECL1	NPECL1	NPECL1	NPECL1	NPECL1
27	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
28	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input
29	GND	GND	GND	GND	GND	GND	GND
30	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1
31	I/O	I/O	I/O	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O	I/O	I/O	I/O
35	I/O	I/O	I/O	I/O	I/O	I/O	I/O

208-Pin PQFP							
Pin Number	**APA075 Function**	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
36	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
37	I/O	I/O	I/O	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O	I/O	I/O	I/O
40	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
41	GND	GND	GND	GND	GND	GND	GND
42	I/O	I/O	I/O	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O	I/O	I/O	I/O
48	I/O	I/O	I/O	I/O	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND	GND	GND	GND
53	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
54	I/O	I/O	I/O	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O	I/O	I/O	I/O
64	I/O	I/O	I/O	I/O	I/O	I/O	I/O
65	GND	GND	GND	GND	GND	GND	GND
66	I/O	I/O	I/O	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O	I/O	I/O	I/O
70	I/O	I/O	I/O	I/O	I/O	I/O	I/O

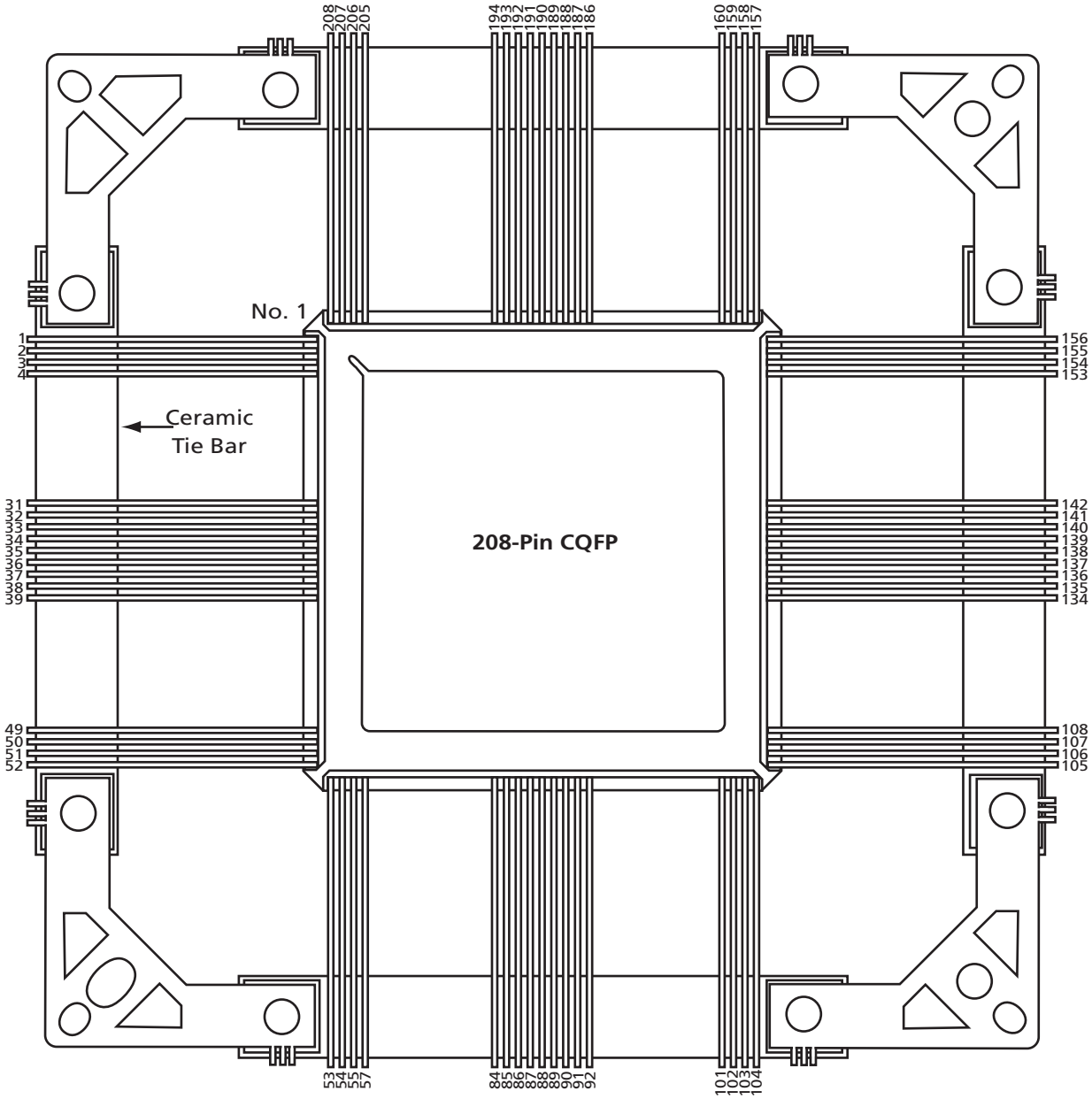
208-Pin PQFP							
Pin Number	**APA075 Function**	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
71	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
72	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
73	I/O	I/O	I/O	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O	I/O	I/O	I/O
77	I/O	I/O	I/O	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	I/O	I/O	I/O	I/O
79	I/O	I/O	I/O	I/O	I/O	I/O	I/O
80	I/O	I/O	I/O	I/O	I/O	I/O	I/O
81	GND	GND	GND	GND	GND	GND	GND
82	I/O	I/O	I/O	I/O	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O	I/O	I/O	I/O
88	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
89	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
90	I/O	I/O	I/O	I/O	I/O	I/O	I/O
91	I/O	I/O	I/O	I/O	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O	I/O	I/O	I/O
94	I/O	I/O	I/O	I/O	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O	I/O	I/O	I/O
97	GND	GND	GND	GND	GND	GND	GND
98	I/O	I/O	I/O	I/O	I/O	I/O	I/O
99	I/O	I/O	I/O	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O	I/O	I/O	I/O
101	TCK	TCK	TCK	TCK	TCK	TCK	TCK
102	TDI	TDI	TDI	TDI	TDI	TDI	TDI
103	TMS	TMS	TMS	TMS	TMS	TMS	TMS
104	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
105	GND	GND	GND	GND	GND	GND	GND

208-Pin PQFP							
Pin Number	**APA075 Function**	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
106	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}
107	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}
108	TDO	TDO	TDO	TDO	TDO	TDO	TDO
109	TRST	TRST	TRST	TRST	TRST	TRST	TRST
110	RCK	RCK	RCK	RCK	RCK	RCK	RCK
111	I/O	I/O	I/O	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O	I/O	I/O	I/O
114	I/O	I/O	I/O	I/O	I/O	I/O	I/O
115	I/O	I/O	I/O	I/O	I/O	I/O	I/O
116	I/O	I/O	I/O	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O	I/O	I/O	I/O
118	I/O	I/O	I/O	I/O	I/O	I/O	I/O
119	I/O	I/O	I/O	I/O	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O	I/O	I/O	I/O
122	GND	GND	GND	GND	GND	GND	GND
123	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
124	I/O	I/O	I/O	I/O	I/O	I/O	I/O
125	I/O	I/O	I/O	I/O	I/O	I/O	I/O
126	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
127	I/O	I/O	I/O	I/O	I/O	I/O	I/O
128	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3
129	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input
130	GND	GND	GND	GND	GND	GND	GND
131	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
132	NPECL2	NPECL2	NPECL2	NPECL2	NPECL2	NPECL2	NPECL2
133	AGND	AGND	AGND	AGND	AGND	AGND	AGND
134	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4
135	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2
136	I/O	I/O	I/O	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O	I/O	I/O	I/O
138	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
139	I/O	I/O	I/O	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O	I/O	I/O	I/O

208-Pin PQFP							
Pin Number	**APA075 Function**	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
141	GND	GND	GND	GND	GND	GND	GND
142	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
143	I/O	I/O	I/O	I/O	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O	I/O	I/O	I/O
145	I/O	I/O	I/O	I/O	I/O	I/O	I/O
146	I/O	I/O	I/O	I/O	I/O	I/O	I/O
147	I/O	I/O	I/O	I/O	I/O	I/O	I/O
148	I/O	I/O	I/O	I/O	I/O	I/O	I/O
149	I/O	I/O	I/O	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O	I/O	I/O	I/O
155	I/O	I/O	I/O	I/O	I/O	I/O	I/O
156	GND	GND	GND	GND	GND	GND	GND
157	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
158	I/O	I/O	I/O	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O	I/O	I/O	I/O
162	GND	GND	GND	GND	GND	GND	GND
163	I/O	I/O	I/O	I/O	I/O	I/O	I/O
164	I/O	I/O	I/O	I/O	I/O	I/O	I/O
165	I/O	I/O	I/O	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O	I/O	I/O	I/O
167	I/O	I/O	I/O	I/O	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O	I/O	I/O	I/O
170	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
171	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
172	I/O	I/O	I/O	I/O	I/O	I/O	I/O
173	I/O	I/O	I/O	I/O	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O	I/O	I/O	I/O

208-Pin PQFP							
Pin Number	**APA075 Function**	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
176	I/O	I/O	I/O	I/O	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O	I/O	I/O	I/O
178	GND	GND	GND	GND	GND	GND	GND
179	I/O	I/O	I/O	I/O	I/O	I/O	I/O
180	I/O	I/O	I/O	I/O	I/O	I/O	I/O
181	I/O	I/O	I/O	I/O	I/O	I/O	I/O
182	I/O	I/O	I/O	I/O	I/O	I/O	I/O
183	I/O	I/O	I/O	I/O	I/O	I/O	I/O
184	I/O	I/O	I/O	I/O	I/O	I/O	I/O
185	I/O	I/O	I/O	I/O	I/O	I/O	I/O
186	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
187	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
188	I/O	I/O	I/O	I/O	I/O	I/O	I/O
189	I/O	I/O	I/O	I/O	I/O	I/O	I/O
190	I/O	I/O	I/O	I/O	I/O	I/O	I/O
191	I/O	I/O	I/O	I/O	I/O	I/O	I/O
192	I/O	I/O	I/O	I/O	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O	I/O	I/O	I/O
195	GND	GND	GND	GND	GND	GND	GND
196	I/O	I/O	I/O	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O	I/O	I/O	I/O
198	I/O	I/O	I/O	I/O	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O	I/O	I/O	I/O
201	I/O	I/O	I/O	I/O	I/O	I/O	I/O
202	I/O	I/O	I/O	I/O	I/O	I/O	I/O
203	I/O	I/O	I/O	I/O	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O	I/O	I/O	I/O
205	I/O	I/O	I/O	I/O	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O	I/O	I/O	I/O
208	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

208-Pin CQFP



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

208-Pin CQFP			
Pin Number	**APA300 Function**	**APA600 Function**	**APA1000 Function**
1	GND	GND	GND
2	I/O	I/O	I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	V_{DD}	V_{DD}	V_{DD}
17	GND	GND	GND
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	I/O	I/O	I/O
22	V_{DDP}	V_{DDP}	V_{DDP}
23	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1
24	I/O / GL2	I/O / GL2	I/O / GL2
25	AGND	AGND	AGND
26	NPECL1	NPECL1	NPECL1
27	AVDD	AVDD	AVDD
28	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input
29	GND	GND	GND
30	I/O / GL1	I/O / GL1	I/O / GL1
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O

208-Pin CQFP			
Pin Number	**APA300 Function**	**APA600 Function**	**APA1000 Function**
36	V_{DD}	V_{DD}	V_{DD}
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	V_{DDP}	V_{DDP}	V_{DDP}
41	GND	GND	GND
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	V_{DDP}	V_{DDP}	V_{DDP}
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	GND	GND	GND
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	I/O	I/O	I/O

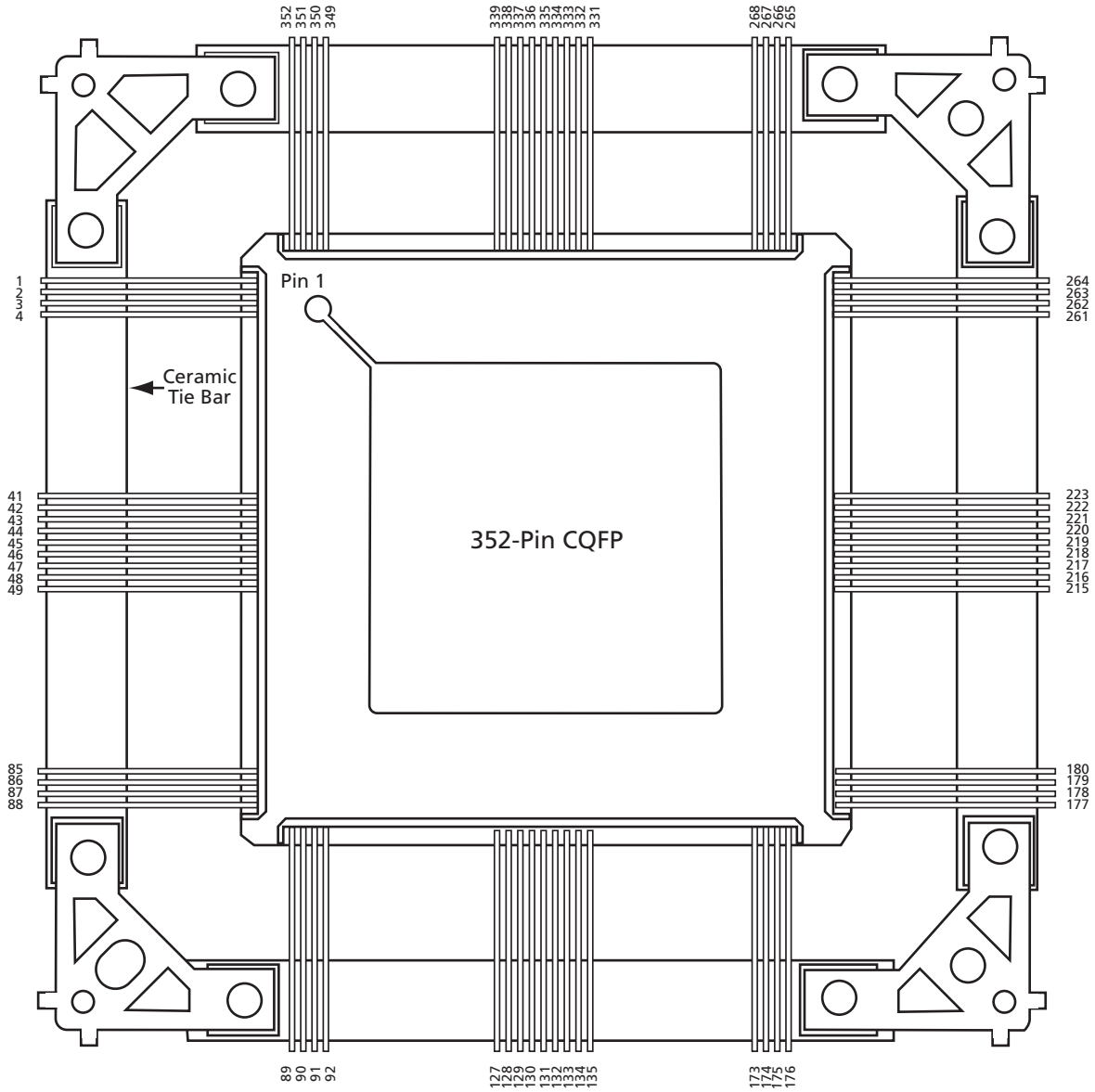
208-Pin CQFP			
Pin Number	**APA300 Function**	**APA600 Function**	**APA1000 Function**
71	V_{DD}	V_{DD}	V_{DD}
72	V_{DDP}	V_{DDP}	V_{DDP}
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	V_{DD}	V_{DD}	V_{DD}
89	V_{DDP}	V_{DDP}	V_{DDP}
90	I/O	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	GND	GND	GND
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	TCK	TCK	TCK
102	TDI	TDI	TDI
103	TMS	TMS	TMS
104	V_{DDP}	V_{DDP}	V_{DDP}
105	GND	GND	GND

208-Pin CQFP			
Pin Number	**APA300 Function**	**APA600 Function**	**APA1000 Function**
106	V_{PP}	V_{PP}	V_{PP}
107	V_{PN}	V_{PN}	V_{PN}
108	TDO	TDO	TDO
109	TRST	TRST	TRST
110	RCK	RCK	RCK
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	GND	GND	GND
123	V_{DDP}	V_{DDP}	V_{DDP}
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	V_{DD}	V_{DD}	V_{DD}
127	I/O	I/O	I/O
128	I/O / GL3	I/O / GL3	I/O / GL3
129	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input
130	GND	GND	GND
131	AVDD	AVDD	AVDD
132	NPECL2	NPECL2	NPECL2
133	AGND	AGND	AGND
134	I/O / GL4	I/O / GL4	I/O / GL4
135	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	V_{DDP}	V_{DDP}	V_{DDP}
139	I/O	I/O	I/O
140	I/O	I/O	I/O

208-Pin CQFP			
Pin Number	**APA300 Function**	**APA600 Function**	**APA1000 Function**
141	GND	GND	GND
142	V_{DD}	V_{DD}	V_{DD}
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	I/O	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	I/O	I/O	I/O
156	GND	]GND	GND
157	V_{DDP}	V_{DDP}	V_{DDP}
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	GND	GND	GND
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	I/O	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	V_{DDP}	V_{DDP}	V_{DDP}
171	V_{DD}	V_{DD}	V_{DD}
172	I/O	I/O	I/O
173	I/O	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O

208-Pin CQFP			
Pin Number	**APA300 Function**	**APA600 Function**	**APA1000 Function**
176	I/O	I/O	I/O
177	I/O	I/O	I/O
178	GND	GND	GND
179	I/O	I/O	I/O
180	I/O	I/O	I/O
181	I/O	I/O	I/O
182	I/O	I/O	I/O
183	I/O	I/O	I/O
184	I/O	I/O	I/O
185	I/O	I/O	I/O
186	V_{DDP}	V_{DDP}	V_{DDP}
187	V_{DD}	V_{DD}	V_{DD}
188	I/O	I/O	I/O
189	I/O	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	I/O	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	GND	GND	GND
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	I/O	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	I/O	I/O	I/O
202	I/O	I/O	I/O
203	I/O	I/O	I/O
204	I/O	I/O	I/O
205	I/O	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	V_{DDP}	V_{DDP}	V_{DDP}

352-Pin CQFP



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
1	I/O	I/O	I/O
2	I/O	I/O	I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	V_{DD}	V_{DD}	V_{DD}
8	GND	GND	GND
9	V_{DDP}	V_{DDP}	V_{DDP}
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	V_{DD}	V_{DD}	V_{DD}
19	GND	GND	GND
20	V_{DDP}	V_{DDP}	V_{DDP}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	V_{DD}	V_{DD}	V_{DD}
30	GND	GND	GND
31	V_{DDP}	V_{DDP}	V_{DDP}
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
38	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1
39	I/O / GL2	I/O / GL2	I/O / GL2
40	AGND	AGND	AGND
41	AVDD	AVDD	AVDD
42	NPECL1	NPECL1	NPECL1
43	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input
44	I/O / GL1	I/O / GL1	I/O / GL1
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	V_{DD}	V_{DD}	V_{DD}
48	GND	GND	GND
49	V_{DDP}	V_{DDP}	V_{DDP}
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	V_{DD}	V_{DD}	V_{DD}
59	GND	GND	GND
60	V_{DDP}	V_{DDP}	V_{DDP}
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	V_{DD}	V_{DD}	V_{DD}
70	GND	GND	GND
71	V_{DDP}	V_{DDP}	V_{DDP}
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	V_{DD}	V_{DD}	V_{DD}
81	GND	GND	GND
82	V_{DDP}	V_{DDP}	V_{DDP}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{DDP}	V_{DDP}	V_{DDP}
90	GND	GND	GND
91	V_{DD}	V_{DD}	V_{DD}
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	V_{DDP}	V_{DDP}	V_{DDP}
101	GND	GND	GND
102	V_{DD}	V_{DD}	V_{DD}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	V_{DDP}	V_{DDP}	V_{DDP}

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
112	GND	GND	GND
113	V_{DD}	V_{DD}	V_{DD}
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	V_{DDP}	V_{DDP}	V_{DDP}
123	GND	GND	GND
124	V_{DD}	V_{DD}	V_{DD}
125	I/O	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	I/O	I/O	I/O
132	I/O	I/O	I/O
133	V_{DDP}	V_{DDP}	V_{DDP}
134	GND	GND	GND
135	V_{DD}	V_{DD}	V_{DD}
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	V_{DDP}	V_{DDP}	V_{DDP}
145	GND	GND	GND
146	V_{DD}	V_{DD}	V_{DD}
147	I/O	I/O	I/O
148	I/O	I/O	I/O

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	V_{DDP}	V_{DDP}	V_{DDP}
156	GND	GND	GND
157	V_{DD}	V_{DD}	V_{DD}
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	I/O	I/O	I/O
166	V_{DDP}	V_{DDP}	V_{DDP}
167	GND	GND	GND
168	V_{DD}	V_{DD}	V_{DD}
169	I/O	I/O	I/O
170	I/O	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	TCK	TCK	TCK
174	TDI	TDI	TDI
175	TMS	TMS	TMS
176	I/O	I/O	I/O
177	VPP	VPP	VPP
178	VPN	VPN	VPN
179	TDO	TDO	TDO
180	TRST	TRST	TRST
181	RCK	RCK	RCK
182	I/O	I/O	I/O
183	V_{DDP}	V_{DDP}	V_{DDP}
184	GND	GND	GND
185	V_{DD}	V_{DD}	V_{DD}

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
186	I/O	I/O	I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	I/O	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	I/O	I/O	I/O
193	I/O	I/O	I/O
194	V_{DDP}	V_{DDP}	V_{DDP}
195	GND	GND	GND
196	V_{DD}	V_{DD}	V_{DD}
197	I/O	I/O	I/O
198	I/O	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	I/O	I/O	I/O
202	I/O	I/O	I/O
203	I/O	I/O	I/O
204	I/O	I/O	I/O
205	V_{DDP}	V_{DDP}	V_{DDP}
206	GND	GND	GND
207	V_{DD}	V_{DD}	V_{DD}
208	I/O	I/O	I/O
209	I/O	I/O	I/O
210	I/O	I/O	I/O
211	I/O	I/O	I/O
212	I/O	I/O	I/O
213	I/O	I/O	I/O
214	I/O	I/O	I/O
215	I/O	I/O	I/O
216	V_{DDP}	V_{DDP}	V_{DDP}
217	GND	GND	GND
218	V_{DD}	V_{DD}	V_{DD}
219	I/O	I/O	I/O
220	I/O	I/O	I/O
221	I/O / GL3	I/O / GL3	I/O / GL3
222	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input

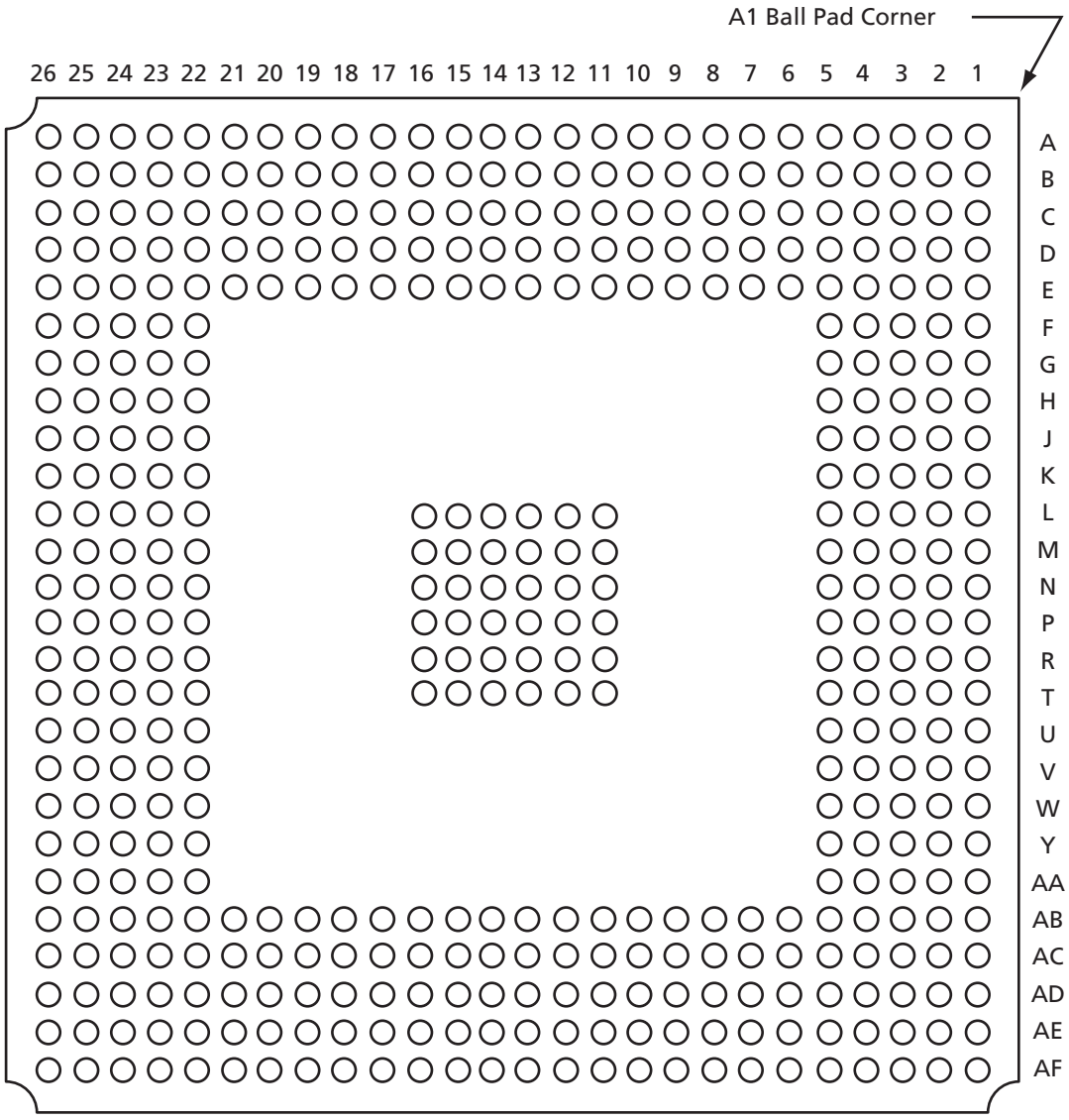
352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
223	NPECL2	NPECL2	NPECL2
224	AVDD	AVDD	AVDD
225	AGND	AGND	AGND
226	I/O / GL4	I/O / GL4	I/O / GL4
227	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2
228	I/O	I/O	I/O
229	I/O	I/O	I/O
230	I/O	I/O	I/O
231	I/O	I/O	I/O
232	I/O	I/O	I/O
233	I/O	I/O	I/O
234	V_{DDP}	V_{DDP}	V_{DDP}
235	GND	GND	GND
236	V_{DD}	V_{DD}	V_{DD}
237	I/O	I/O	I/O
238	I/O	I/O	I/O
239	I/O	I/O	I/O
240	I/O	I/O	I/O
241	I/O	I/O	I/O
242	I/O	I/O	I/O
243	I/O	I/O	I/O
244	I/O	I/O	I/O
245	V_{DDP}	V_{DDP}	V_{DDP}
246	GND	GND	GND
247	V_{DD}	V_{DD}	V_{DD}
248	I/O	I/O	I/O
249	I/O	I/O	I/O
250	I/O	I/O	I/O
251	I/O	I/O	I/O
252	I/O	I/O	I/O
253	I/O	I/O	I/O
254	I/O	I/O	I/O
255	I/O	I/O	I/O
256	V_{DDP}	V_{DDP}	V_{DDP}
257	GND	GND	GND
258	V_{DD}	V_{DD}	V_{DD}
259	I/O	I/O	I/O

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
260	I/O	I/O	I/O
261	I/O	I/O	I/O
262	I/O	I/O	I/O
263	I/O	I/O	I/O
264	I/O	I/O	I/O
265	I/O	I/O	I/O
266	I/O	I/O	I/O
267	I/O	I/O	I/O
268	I/O	I/O	I/O
269	I/O	I/O	I/O
270	I/O	I/O	I/O
271	I/O	I/O	I/O
272	I/O	I/O	I/O
273	V_{DD}	V_{DD}	V_{DD}
274	GND	GND	GND
275	V_{DDP}	V_{DDP}	V_{DDP}
276	I/O	I/O	I/O
277	I/O	I/O	I/O
278	I/O	I/O	I/O
279	I/O	I/O	I/O
280	I/O	I/O	I/O
281	I/O	I/O	I/O
282	I/O	I/O	I/O
283	I/O	I/O	I/O
284	V_{DD}	V_{DD}	V_{DD}
285	GND	GND	GND
286	V_{DDP}	V_{DDP}	V_{DDP}
287	I/O	I/O	I/O
288	I/O	I/O	I/O
289	I/O	I/O	I/O
290	I/O	I/O	I/O
291	I/O	I/O	I/O
292	I/O	I/O	I/O
293	I/O	I/O	I/O
294	I/O	I/O	I/O
295	V_{DD}	V_{DD}	V_{DD}
296	GND	GND	GND

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
297	V_{DDP}	V_{DDP}	V_{DDP}
298	I/O	I/O	I/O
299	I/O	I/O	I/O
300	I/O	I/O	I/O
301	I/O	I/O	I/O
302	I/O	I/O	I/O
303	I/O	I/O	I/O
304	I/O	I/O	I/O
305	I/O	I/O	I/O
306	V_{DD}	V_{DD}	V_{DD}
307	GND	GND	GND
308	V_{DDP}	V_{DDP}	V_{DDP}
309	I/O	I/O	I/O
310	I/O	I/O	I/O
311	I/O	I/O	I/O
312	I/O	I/O	I/O
313	I/O	I/O	I/O
314	I/O	I/O	I/O
315	I/O	I/O	I/O
316	I/O	I/O	I/O
317	V_{DD}	V_{DD}	V_{DD}
318	GND	GND	GND
319	V_{DDP}	V_{DDP}	V_{DDP}
320	I/O	I/O	I/O
321	I/O	I/O	I/O
322	I/O	I/O	I/O
323	I/O	I/O	I/O
324	I/O	I/O	I/O
325	I/O	I/O	I/O
326	I/O	I/O	I/O
327	I/O	I/O	I/O
328	V_{DD}	V_{DD}	V_{DD}
329	GND	GND	GND
330	V_{DDP}	V_{DDP}	V_{DDP}
331	I/O	I/O	I/O
332	I/O	I/O	I/O
333	I/O	I/O	I/O

352-Pin CQFP			
Pin Number	APA300 Function	APA600 Function	APA1000 Function
334	I/O	I/O	I/O
335	I/O	I/O	I/O
336	I/O	I/O	I/O
337	I/O	I/O	I/O
338	I/O	I/O	I/O
339	V_{DD}	V_{DD}	V_{DD}
340	GND	GND	GND
341	V_{DDP}	V_{DDP}	V_{DDP}
342	I/O	I/O	I/O
343	I/O	I/O	I/O
344	I/O	I/O	I/O
345	I/O	I/O	I/O
346	I/O	I/O	I/O
347	I/O	I/O	I/O
348	I/O	I/O	I/O
349	I/O	I/O	I/O
350	V_{DD}	V_{DD}	V_{DD}
351	GND	GND	GND
352	V_{DDP}	V_{DDP}	V_{DDP}

456-Pin PBGA



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
A1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
A2	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
A3	NC	NC	I/O	I/O	I/O	I/O
A4	NC	NC	I/O	I/O	I/O	I/O
A5	NC	NC	I/O	I/O	I/O	I/O
A6	NC	NC	I/O	I/O	I/O	I/O
A7	NC	NC	I/O	I/O	I/O	I/O
A8	I/O	I/O	I/O	I/O	I/O	I/O
A9	I/O	I/O	I/O	I/O	I/O	I/O
A10	I/O	I/O	I/O	I/O	I/O	I/O
A11	I/O	I/O	I/O	I/O	I/O	I/O
A12	I/O	I/O	I/O	I/O	I/O	I/O
A13	I/O	I/O	I/O	I/O	I/O	I/O
A14	I/O	I/O	I/O	I/O	I/O	I/O
A15	I/O	I/O	I/O	I/O	I/O	I/O
A16	I/O	I/O	I/O	I/O	I/O	I/O
A17	I/O	I/O	I/O	I/O	I/O	I/O
A18	I/O	I/O	I/O	I/O	I/O	I/O
A19	I/O	I/O	I/O	I/O	I/O	I/O
A20	NC	NC	I/O	I/O	I/O	I/O
A21	NC	NC	I/O	I/O	I/O	I/O
A22	NC	NC	I/O	I/O	I/O	I/O
A23	NC	NC	I/O	I/O	I/O	I/O
A24	NC	NC	I/O	I/O	I/O	I/O
A25	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
A26	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
B1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
B2	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
B3	NC	NC	NC	I/O	I/O	I/O
B4	NC	NC	I/O	I/O	I/O	I/O
B5	NC	NC	I/O	I/O	I/O	I/O
B6	NC	NC	I/O	I/O	I/O	I/O
B7	NC	NC	I/O	I/O	I/O	I/O
B8	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
B9	I/O	I/O	I/O	I/O	I/O	I/O
B10	I/O	I/O	I/O	I/O	I/O	I/O
B11	I/O	I/O	I/O	I/O	I/O	I/O
B12	I/O	I/O	I/O	I/O	I/O	I/O
B13	I/O	I/O	I/O	I/O	I/O	I/O
B14	I/O	I/O	I/O	I/O	I/O	I/O
B15	I/O	I/O	I/O	I/O	I/O	I/O
B16	I/O	I/O	I/O	I/O	I/O	I/O
B17	I/O	I/O	I/O	I/O	I/O	I/O
B18	I/O	I/O	I/O	I/O	I/O	I/O
B19	I/O	I/O	I/O	I/O	I/O	I/O
B20	NC	NC	I/O	I/O	I/O	I/O
B21	NC	NC	I/O	I/O	I/O	I/O
B22	NC	NC	I/O	I/O	I/O	I/O
B23	NC	NC	I/O	I/O	I/O	I/O
B24	NC	NC	I/O	I/O	I/O	I/O
B25	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
B26	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
C1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
C2	NC	I/O	I/O	I/O	I/O	I/O
C3	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
C4	NC	NC	NC	I/O	I/O	I/O
C5	NC	NC	I/O	I/O	I/O	I/O
C6	NC	NC	I/O	I/O	I/O	I/O
C7	I/O	I/O	I/O	I/O	I/O	I/O
C8	I/O	I/O	I/O	I/O	I/O	I/O
C9	I/O	I/O	I/O	I/O	I/O	I/O
C10	I/O	I/O	I/O	I/O	I/O	I/O
C11	I/O	I/O	I/O	I/O	I/O	I/O
C12	I/O	I/O	I/O	I/O	I/O	I/O
C13	I/O	I/O	I/O	I/O	I/O	I/O
C14	I/O	I/O	I/O	I/O	I/O	I/O
C15	I/O	I/O	I/O	I/O	I/O	I/O
C16	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
C17	I/O	I/O	I/O	I/O	I/O	I/O
C18	I/O	I/O	I/O	I/O	I/O	I/O
C19	I/O	I/O	I/O	I/O	I/O	I/O
C20	I/O	I/O	I/O	I/O	I/O	I/O
C21	NC	NC	I/O	I/O	I/O	I/O
C22	NC	NC	I/O	I/O	I/O	I/O
C23	NC	NC	I/O	I/O	I/O	I/O
C24	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
C25	NC	NC	NC	I/O	I/O	I/O
C26	NC	NC	NC	I/O	I/O	I/O
D1	NC	NC	NC	I/O	I/O	I/O
D2	NC	NC	NC	I/O	I/O	I/O
D3	NC	I/O	I/O	I/O	I/O	I/O
D4	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
D5	NC	NC	I/O	I/O	I/O	I/O
D6	NC	NC	I/O	I/O	I/O	I/O
D7	I/O	I/O	I/O	I/O	I/O	I/O
D8	I/O	I/O	I/O	I/O	I/O	I/O
D9	I/O	I/O	I/O	I/O	I/O	I/O
D10	I/O	I/O	I/O	I/O	I/O	I/O
D11	I/O	I/O	I/O	I/O	I/O	I/O
D12	I/O	I/O	I/O	I/O	I/O	I/O
D13	I/O	I/O	I/O	I/O	I/O	I/O
D14	I/O	I/O	I/O	I/O	I/O	I/O
D15	I/O	I/O	I/O	I/O	I/O	I/O
D16	I/O	I/O	I/O	I/O	I/O	I/O
D17	I/O	I/O	I/O	I/O	I/O	I/O
D18	I/O	I/O	I/O	I/O	I/O	I/O
D19	I/O	I/O	I/O	I/O	I/O	I/O
D20	I/O	I/O	I/O	I/O	I/O	I/O
D21	I/O	I/O	I/O	I/O	I/O	I/O
D22	NC	NC	I/O	I/O	I/O	I/O
D23	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
D24	NC	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
D25	NC	NC	NC	I/O	I/O	I/O
D26	NC	NC	NC	I/O	I/O	I/O
E1	NC	I/O	I/O	I/O	I/O	I/O
E2	NC	I/O	I/O	I/O	I/O	I/O
E3	NC	I/O	I/O	I/O	I/O	I/O
E4	NC	I/O	I/O	I/O	I/O	I/O
E5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E6	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E8	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E9	I/O	I/O	I/O	I/O	I/O	I/O
E10	I/O	I/O	I/O	I/O	I/O	I/O
E11	I/O	I/O	I/O	I/O	I/O	I/O
E12	I/O	I/O	I/O	I/O	I/O	I/O
E13	I/O	I/O	I/O	I/O	I/O	I/O
E14	I/O	I/O	I/O	I/O	I/O	I/O
E15	I/O	I/O	I/O	I/O	I/O	I/O
E16	I/O	I/O	I/O	I/O	I/O	I/O
E17	I/O	I/O	I/O	I/O	I/O	I/O
E18	I/O	I/O	I/O	I/O	I/O	I/O
E19	I/O	I/O	I/O	I/O	I/O	I/O
E20	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E21	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E23	NC	I/O	I/O	I/O	I/O	I/O
E24	NC	I/O	I/O	I/O	I/O	I/O
E25	NC	I/O	I/O	I/O	I/O	I/O
E26	NC	I/O	I/O	I/O	I/O	I/O
F1	NC	I/O	I/O	I/O	I/O	I/O
F2	NC	I/O	I/O	I/O	I/O	I/O
F3	NC	I/O	I/O	I/O	I/O	I/O
F4	NC	I/O	I/O	I/O	I/O	I/O
F5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
F23	NC	I/O	I/O	I/O	I/O	I/O
F24	NC	I/O	I/O	I/O	I/O	I/O
F25	NC	I/O	I/O	I/O	I/O	I/O
F26	NC	I/O	I/O	I/O	I/O	I/O
G1	I/O	I/O	I/O	I/O	I/O	I/O
G2	I/O	I/O	I/O	I/O	I/O	I/O
G3	NC	I/O	I/O	I/O	I/O	I/O
G4	NC	I/O	I/O	I/O	I/O	I/O
G5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
G22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
G23	NC	I/O	I/O	I/O	I/O	I/O
G24	NC	I/O	I/O	I/O	I/O	I/O
G25	NC	I/O	I/O	I/O	I/O	I/O
G26	I/O	I/O	I/O	I/O	I/O	I/O
H1	I/O	I/O	I/O	I/O	I/O	I/O
H2	I/O	I/O	I/O	I/O	I/O	I/O
H3	I/O	I/O	I/O	I/O	I/O	I/O
H4	I/O	I/O	I/O	I/O	I/O	I/O
H5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H23	I/O	I/O	I/O	I/O	I/O	I/O
H24	I/O	I/O	I/O	I/O	I/O	I/O
H25	I/O	I/O	I/O	I/O	I/O	I/O
H26	I/O	I/O	I/O	I/O	I/O	I/O
J1	I/O	I/O	I/O	I/O	I/O	I/O
J2	I/O	I/O	I/O	I/O	I/O	I/O
J3	I/O	I/O	I/O	I/O	I/O	I/O
J4	I/O	I/O	I/O	I/O	I/O	I/O
J5	I/O	I/O	I/O	I/O	I/O	I/O
J22	I/O	I/O	I/O	I/O	I/O	I/O
J23	I/O	I/O	I/O	I/O	I/O	I/O
J24	I/O	I/O	I/O	I/O	I/O	I/O
J25	I/O	I/O	I/O	I/O	I/O	I/O
J26	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
K1	I/O	I/O	I/O	I/O	I/O	I/O
K2	I/O	I/O	I/O	I/O	I/O	I/O
K3	I/O	I/O	I/O	I/O	I/O	I/O
K4	I/O	I/O	I/O	I/O	I/O	I/O
K5	I/O	I/O	I/O	I/O	I/O	I/O
K22	I/O	I/O	I/O	I/O	I/O	I/O
K23	I/O	I/O	I/O	I/O	I/O	I/O
K24	I/O	I/O	I/O	I/O	I/O	I/O
K25	I/O	I/O	I/O	I/O	I/O	I/O
K26	I/O	I/O	I/O	I/O	I/O	I/O
L1	I/O	I/O	I/O	I/O	I/O	I/O
L2	I/O	I/O	I/O	I/O	I/O	I/O
L3	I/O	I/O	I/O	I/O	I/O	I/O
L4	I/O	I/O	I/O	I/O	I/O	I/O
L5	I/O	I/O	I/O	I/O	I/O	I/O
L11	GND	GND	GND	GND	GND	GND
L12	GND	GND	GND	GND	GND	GND
L13	GND	GND	GND	GND	GND	GND
L14	GND	GND	GND	GND	GND	GND
L15	GND	GND	GND	GND	GND	GND
L16	GND	GND	GND	GND	GND	GND
L22	I/O	I/O	I/O	I/O	I/O	I/O
L23	I/O	I/O	I/O	I/O	I/O	I/O
L24	I/O	I/O	I/O	I/O	I/O	I/O
L25	I/O	I/O	I/O	I/O	I/O	I/O
L26	I/O	I/O	I/O	I/O	I/O	I/O
M1	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1
M2	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2
M3	I/O	I/O	I/O	I/O	I/O	I/O
M4	I/O	I/O	I/O	I/O	I/O	I/O
M5	I/O	I/O	I/O	I/O	I/O	I/O
M11	GND	GND	GND	GND	GND	GND
M12	GND	GND	GND	GND	GND	GND
M13	GND	GND	GND	GND	GND	GND

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
M14	GND	GND	GND	GND	GND	GND
M15	GND	GND	GND	GND	GND	GND
M16	GND	GND	GND	GND	GND	GND
M22	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4
M23	I/O	I/O	I/O	I/O	I/O	I/O
M24	I/O	I/O	I/O	I/O	I/O	I/O
M25	I/O	I/O	I/O	I/O	I/O	I/O
M26	I/O	I/O	I/O	I/O	I/O	I/O
N1	I/O	I/O	I/O	I/O	I/O	I/O
N2	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1
N3	AGND	AGND	AGND	AGND	AGND	AGND
N4	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input
N5	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
N11	GND	GND	GND	GND	GND	GND
N12	GND	GND	GND	GND	GND	GND
N13	GND	GND	GND	GND	GND	GND
N14	GND	GND	GND	GND	GND	GND
N15	GND	GND	GND	GND	GND	GND
N16	GND	GND	GND	GND	GND	GND
N22	NPECL2	NPECL2	NPECL2	NPECL2	NPECL2	NPECL2
N23	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3
N24	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
N25	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2
N26	AGND	AGND	AGND	AGND	AGND	AGND
P1	I/O	I/O	I/O	I/O	I/O	I/O
P2	I/O	I/O	I/O	I/O	I/O	I/O
P3	I/O	I/O	I/O	I/O	I/O	I/O
P4	I/O	I/O	I/O	I/O	I/O	I/O
P5	NPECL1	NPECL1	NPECL1	NPECL1	NPECL1	NPECL1
P11	GND	GND	GND	GND	GND	GND
P12	GND	GND	GND	GND	GND	GND
P13	GND	GND	GND	GND	GND	GND
P14	GND	GND	GND	GND	GND	GND
P15	GND	GND	GND	GND	GND	GND

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
P16	GND	GND	GND	GND	GND	GND
P22	I/O	I/O	I/O	I/O	I/O	I/O
P23	I/O	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O	I/O
P26	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input
R1	I/O	I/O	I/O	I/O	I/O	I/O
R2	I/O	I/O	I/O	I/O	I/O	I/O
R3	I/O	I/O	I/O	I/O	I/O	I/O
R4	I/O	I/O	I/O	I/O	I/O	I/O
R5	I/O	I/O	I/O	I/O	I/O	I/O
R11	GND	GND	GND	GND	GND	GND
R12	GND	GND	GND	GND	GND	GND
R13	GND	GND	GND	GND	GND	GND
R14	GND	GND	GND	GND	GND	GND
R15	GND	GND	GND	GND	GND	GND
R16	GND	GND	GND	GND	GND	GND
R22	I/O	I/O	I/O	I/O	I/O	I/O
R23	I/O	I/O	I/O	I/O	I/O	I/O
R24	I/O	I/O	I/O	I/O	I/O	I/O
R25	I/O	I/O	I/O	I/O	I/O	I/O
R26	I/O	I/O	I/O	I/O	I/O	I/O
T1	I/O	I/O	I/O	I/O	I/O	I/O
T2	I/O	I/O	I/O	I/O	I/O	I/O
T3	I/O	I/O	I/O	I/O	I/O	I/O
T4	I/O	I/O	I/O	I/O	I/O	I/O
T5	I/O	I/O	I/O	I/O	I/O	I/O
T11	GND	GND	GND	GND	GND	GND
T12	GND	GND	GND	GND	GND	GND
T13	GND	GND	GND	GND	GND	GND
T14	GND	GND	GND	GND	GND	GND
T15	GND	GND	GND	GND	GND	GND
T16	GND	GND	GND	GND	GND	GND
T22	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
T23	I/O	I/O	I/O	I/O	I/O	I/O
T24	I/O	I/O	I/O	I/O	I/O	I/O
T25	I/O	I/O	I/O	I/O	I/O	I/O
T26	I/O	I/O	I/O	I/O	I/O	I/O
U1	I/O	I/O	I/O	I/O	I/O	I/O
U2	I/O	I/O	I/O	I/O	I/O	I/O
U3	I/O	I/O	I/O	I/O	I/O	I/O
U4	I/O	I/O	I/O	I/O	I/O	I/O
U5	I/O	I/O	I/O	I/O	I/O	I/O
U22	I/O	I/O	I/O	I/O	I/O	I/O
U23	I/O	I/O	I/O	I/O	I/O	I/O
U24	I/O	I/O	I/O	I/O	I/O	I/O
U25	I/O	I/O	I/O	I/O	I/O	I/O
U26	I/O	I/O	I/O	I/O	I/O	I/O
V1	I/O	I/O	I/O	I/O	I/O	I/O
V2	I/O	I/O	I/O	I/O	I/O	I/O
V3	I/O	I/O	I/O	I/O	I/O	I/O
V4	I/O	I/O	I/O	I/O	I/O	I/O
V5	I/O	I/O	I/O	I/O	I/O	I/O
V22	I/O	I/O	I/O	I/O	I/O	I/O
V23	I/O	I/O	I/O	I/O	I/O	I/O
V24	I/O	I/O	I/O	I/O	I/O	I/O
V25	I/O	I/O	I/O	I/O	I/O	I/O
V26	I/O	I/O	I/O	I/O	I/O	I/O
W1	I/O	I/O	I/O	I/O	I/O	I/O
W2	I/O	I/O	I/O	I/O	I/O	I/O
W3	I/O	I/O	I/O	I/O	I/O	I/O
W4	I/O	I/O	I/O	I/O	I/O	I/O
W5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
W22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
W23	I/O	I/O	I/O	I/O	I/O	I/O
W24	I/O	I/O	I/O	I/O	I/O	I/O
W25	I/O	I/O	I/O	I/O	I/O	I/O
W26	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
Y1	I/O	I/O	I/O	I/O	I/O	I/O
Y2	I/O	I/O	I/O	I/O	I/O	I/O
Y3	I/O	I/O	I/O	I/O	I/O	I/O
Y4	NC	I/O	I/O	I/O	I/O	I/O
Y5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
Y22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
Y23	NC	I/O	I/O	I/O	I/O	I/O
Y24	NC	I/O	I/O	I/O	I/O	I/O
Y25	NC	I/O	I/O	I/O	I/O	I/O
Y26	NC	I/O	I/O	I/O	I/O	I/O
AA1	I/O	I/O	I/O	I/O	I/O	I/O
AA2	NC	I/O	I/O	I/O	I/O	I/O
AA3	NC	I/O	I/O	I/O	I/O	I/O
AA4	NC	I/O	I/O	I/O	I/O	I/O
AA5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AA22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AA23	NC	I/O	I/O	I/O	I/O	I/O
AA24	NC	I/O	I/O	I/O	I/O	I/O
AA25	NC	I/O	I/O	I/O	I/O	I/O
AA26	NC	I/O	I/O	I/O	I/O	I/O
AB1	NC	I/O	I/O	I/O	I/O	I/O
AB2	NC	I/O	I/O	I/O	I/O	I/O
AB3	NC	I/O	I/O	I/O	I/O	I/O
AB4	NC	I/O	I/O	I/O	I/O	I/O
AB5	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB6	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB8	I/O	I/O	I/O	I/O	I/O	I/O
AB9	I/O	I/O	I/O	I/O	I/O	I/O
AB10	I/O	I/O	I/O	I/O	I/O	I/O
AB11	I/O	I/O	I/O	I/O	I/O	I/O
AB12	I/O	I/O	I/O	I/O	I/O	I/O
AB13	I/O	I/O	I/O	I/O	I/O	I/O
AB14	I/O	I/O	I/O	I/O	I/O	I/O

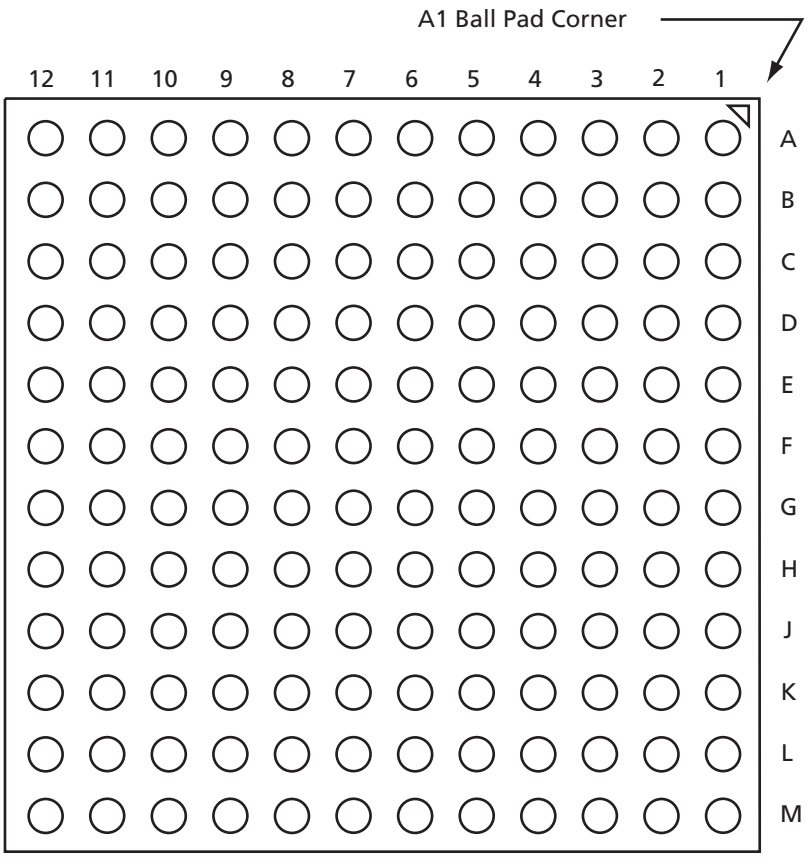
456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
AB15	I/O	I/O	I/O	I/O	I/O	I/O
AB16	I/O	I/O	I/O	I/O	I/O	I/O
AB17	I/O	I/O	I/O	I/O	I/O	I/O
AB18	I/O	I/O	I/O	I/O	I/O	I/O
AB19	I/O	I/O	I/O	I/O	I/O	I/O
AB20	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB21	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB22	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
AB23	NC	I/O	I/O	I/O	I/O	I/O
AB24	NC	I/O	I/O	I/O	I/O	I/O
AB25	NC	I/O	I/O	I/O	I/O	I/O
AB26	NC	NC	NC	I/O	I/O	I/O
AC1	NC	I/O	I/O	I/O	I/O	I/O
AC2	NC	I/O	I/O	I/O	I/O	I/O
AC3	NC	I/O	I/O	I/O	I/O	I/O
AC4	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AC5	NC	NC	I/O	I/O	I/O	I/O
AC6	I/O	I/O	I/O	I/O	I/O	I/O
AC7	I/O	I/O	I/O	I/O	I/O	I/O
AC8	I/O	I/O	I/O	I/O	I/O	I/O
AC9	I/O	I/O	I/O	I/O	I/O	I/O
AC10	I/O	I/O	I/O	I/O	I/O	I/O
AC11	I/O	I/O	I/O	I/O	I/O	I/O
AC12	I/O	I/O	I/O	I/O	I/O	I/O
AC13	I/O	I/O	I/O	I/O	I/O	I/O
AC14	I/O	I/O	I/O	I/O	I/O	I/O
AC15	I/O	I/O	I/O	I/O	I/O	I/O
AC16	I/O	I/O	I/O	I/O	I/O	I/O
AC17	I/O	I/O	I/O	I/O	I/O	I/O
AC18	I/O	I/O	I/O	I/O	I/O	I/O
AC19	I/O	I/O	I/O	I/O	I/O	I/O
AC20	I/O	I/O	I/O	I/O	I/O	I/O
AC21	TMS	TMS	TMS	TMS	TMS	TMS
AC22	TDO	TDO	TDO	TDO	TDO	TDO

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
AC23	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AC24	RCK	RCK	RCK	RCK	RCK	RCK
AC25	NC	NC	I/O	I/O	I/O	I/O
AC26	NC	I/O	I/O	I/O	I/O	I/O
AD1	NC	NC	NC	I/O	I/O	I/O
AD2	NC	I/O	I/O	I/O	I/O	I/O
AD3	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AD4	NC	NC	I/O	I/O	I/O	I/O
AD5	NC	NC	I/O	I/O	I/O	I/O
AD6	NC	NC	I/O	I/O	I/O	I/O
AD7	I/O	I/O	I/O	I/O	I/O	I/O
AD8	I/O	I/O	I/O	I/O	I/O	I/O
AD9	I/O	I/O	I/O	I/O	I/O	I/O
AD10	I/O	I/O	I/O	I/O	I/O	I/O
AD11	I/O	I/O	I/O	I/O	I/O	I/O
AD12	I/O	I/O	I/O	I/O	I/O	I/O
AD13	I/O	I/O	I/O	I/O	I/O	I/O
AD14	I/O	I/O	I/O	I/O	I/O	I/O
AD15	I/O	I/O	I/O	I/O	I/O	I/O
AD16	I/O	I/O	I/O	I/O	I/O	I/O
AD17	I/O	I/O	I/O	I/O	I/O	I/O
AD18	I/O	I/O	I/O	I/O	I/O	I/O
AD19	I/O	I/O	I/O	I/O	I/O	I/O
AD20	NC	NC	I/O	I/O	I/O	I/O
AD21	TCK	TCK	TCK	TCK	TCK	TCK
AD22	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}
AD23	NC	NC	NC	I/O	I/O	I/O
AD24	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AD25	NC	NC	I/O	I/O	I/O	I/O
AD26	NC	NC	I/O	I/O	I/O	I/O
AE1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AE2	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AE3	NC	NC	I/O	I/O	I/O	I/O
AE4	NC	NC	I/O	I/O	I/O	I/O

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
AE5	NC	NC	I/O	I/O	I/O	I/O
AE6	NC	NC	I/O	I/O	I/O	I/O
AE7	NC	NC	I/O	I/O	I/O	I/O
AE8	I/O	I/O	I/O	I/O	I/O	I/O
AE9	I/O	I/O	I/O	I/O	I/O	I/O
AE10	I/O	I/O	I/O	I/O	I/O	I/O
AE11	I/O	I/O	I/O	I/O	I/O	I/O
AE12	I/O	I/O	I/O	I/O	I/O	I/O
AE13	I/O	I/O	I/O	I/O	I/O	I/O
AE14	I/O	I/O	I/O	I/O	I/O	I/O
AE15	I/O	I/O	I/O	I/O	I/O	I/O
AE16	I/O	I/O	I/O	I/O	I/O	I/O
AE17	I/O	I/O	I/O	I/O	I/O	I/O
AE18	I/O	I/O	I/O	I/O	I/O	I/O
AE19	I/O	I/O	I/O	I/O	I/O	I/O
AE20	NC	NC	I/O	I/O	I/O	I/O
AE21	NC	NC	I/O	I/O	I/O	I/O
AE22	NC	NC	I/O	I/O	I/O	I/O
AE23	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}
AE24	TRST	TRST	TRST	TRST	TRST	TRST
AE25	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AE26	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AF1	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AF2	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AF3	NC	NC	I/O	I/O	I/O	I/O
AF4	NC	NC	I/O	I/O	I/O	I/O
AF5	NC	NC	I/O	I/O	I/O	I/O
AF6	NC	NC	I/O	I/O	I/O	I/O
AF7	NC	NC	I/O	I/O	I/O	I/O
AF8	NC	NC	NC	I/O	I/O	I/O
AF9	I/O	I/O	I/O	I/O	I/O	I/O
AF10	I/O	I/O	I/O	I/O	I/O	I/O
AF11	I/O	I/O	I/O	I/O	I/O	I/O
AF12	I/O	I/O	I/O	I/O	I/O	I/O

456-Pin PBGA						
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**	**APA750 Function**	**APA1000 Function**
AF13	I/O	I/O	I/O	I/O	I/O	I/O
AF14	I/O	I/O	I/O	I/O	I/O	I/O
AF15	I/O	I/O	I/O	I/O	I/O	I/O
AF16	I/O	I/O	I/O	I/O	I/O	I/O
AF17	I/O	I/O	I/O	I/O	I/O	I/O
AF18	NC	NC	I/O	I/O	I/O	I/O
AF19	NC	NC	I/O	I/O	I/O	I/O
AF20	NC	NC	I/O	I/O	I/O	I/O
AF21	NC	NC	I/O	I/O	I/O	I/O
AF22	NC	NC	I/O	I/O	I/O	I/O
AF23	TDI	TDI	TDI	TDI	TDI	TDI
AF24	NC	NC	I/O	I/O	I/O	I/O
AF25	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
AF26	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

144-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

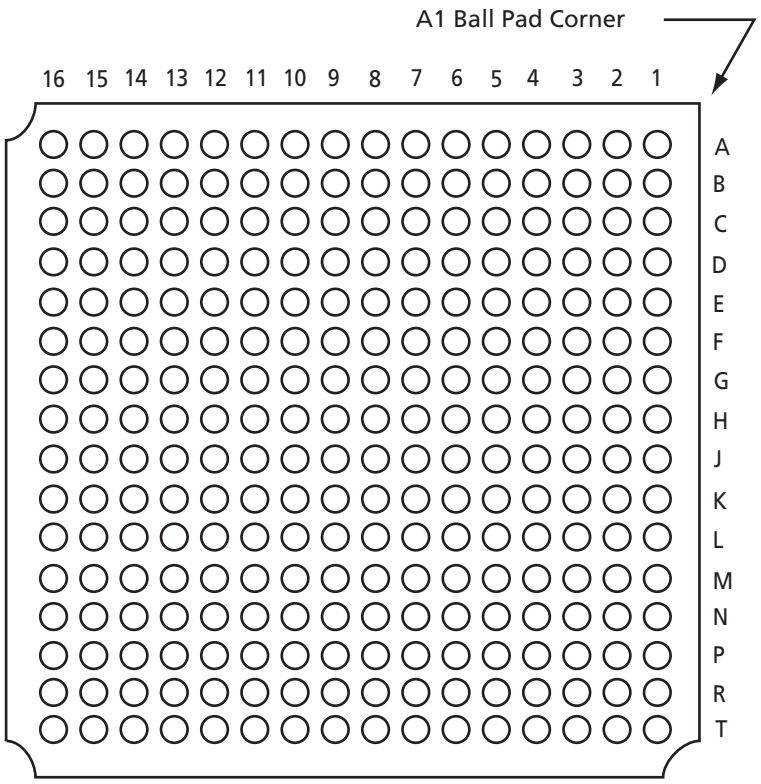
144-FBGA Pin				
Pin Number	APA075 Function	APA150 Function	APA300 Function	APA450 Function
A1	I/O	I/O	I/O	I/O
A2	I/O	I/O	I/O	I/O
A3	I/O	I/O	I/O	I/O
A4	I/O	I/O	I/O	I/O
A5	I/O	I/O	I/O	I/O
A6	GND	GND	GND	GND
A7	I/O	I/O	I/O	I/O
A8	V_{DD}	V_{DD}	V_{DD}	V_{DD}
A9	I/O	I/O	I/O	I/O
A10	I/O	I/O	I/O	I/O
A11	I/O	I/O	I/O	I/O
A12	I/O	I/O	I/O	I/O
B1	I/O	I/O	I/O	I/O
B2	GND	GND	GND	GND
B3	I/O	I/O	I/O	I/O
B4	I/O	I/O	I/O	I/O
B5	I/O	I/O	I/O	I/O
B6	I/O	I/O	I/O	I/O
B7	I/O	I/O	I/O	I/O
B8	I/O	I/O	I/O	I/O
B9	I/O	I/O	I/O	I/O
B10	I/O	I/O	I/O	I/O
B11	GND	GND	GND	GND
B12	I/O	I/O	I/O	I/O
C1	I/O	I/O	I/O	I/O
C2	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1
C3	I/O	I/O	I/O	I/O
C4	V_{DD}	V_{DD}	V_{DD}	V_{DD}
C5	I/O	I/O	I/O	I/O
C6	I/O	I/O	I/O	I/O
C7	I/O	I/O	I/O	I/O
C8	I/O	I/O	I/O	I/O
C9	I/O	I/O	I/O	I/O
C10	I/O	I/O	I/O	I/O
C11	I/O	I/O	I/O	I/O
C12	I/O	I/O	I/O	I/O
D1	I/O	I/O	I/O	I/O

144-FBGA Pin				
Pin Number	APA075 Function	APA150 Function	APA300 Function	APA450 Function
D2	I/O	I/O	I/O	I/O
D3	I/O	I/O	I/O	I/O
D4	I/O	I/O	I/O	I/O
D5	I/O	I/O	I/O	I/O
D6	I/O	I/O	I/O	I/O
D7	I/O	I/O	I/O	I/O
D8	I/O	I/O	I/O	I/O
D9	I/O	I/O	I/O	I/O
D10	I/O	I/O	I/O	I/O
D11	I/O	I/O	I/O	I/O
D12	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2
E1	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E2	I/O	I/O	I/O	I/O
E3	I/O	I/O	I/O	I/O
E4	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E5	I/O	I/O	I/O	I/O
E6	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E7	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E8	AVDD	AVDD	AVDD	AVDD
E9	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E10	V_{DD}	V_{DD}	V_{DD}	V_{DD}
E11	NPECL2	NPECL2	NPECL2	NPECL2
E12	AGND	AGND	AGND	AGND
F1	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2
F2	AGND	AGND	AGND	AGND
F3	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1
F4	I/O	I/O	I/O	I/O
F5	GND	GND	GND	GND
F6	GND	GND	GND	GND
F7	GND	GND	GND	GND
F8	I/O	I/O	I/O	I/O
F9	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4
F10	GND	GND	GND	GND
F11	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input
F12	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3

144-FBGA Pin				
Pin Number	**APA075 Function**	**APA150 Function**	**APA300 Function**	**APA450 Function**
G1	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input
G2	GND	GND	GND	GND
G3	AVDD	AVDD	AVDD	AVDD
G4	NPECL1	NPECL1	NPECL1	NPECL1
G5	GND	GND	GND	GND
G6	GND	GND	GND	GND
G7	GND	GND	GND	GND
G8	I/O	I/O	I/O	I/O
G9	I/O	I/O	I/O	I/O
G10	I/O	I/O	I/O	I/O
G11	I/O	I/O	I/O	I/O
G12	I/O	I/O	I/O	I/O
H1	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H2	I/O	I/O	I/O	I/O
H3	I/O	I/O	I/O	I/O
H4	I/O	I/O	I/O	I/O
H5	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H6	I/O	I/O	I/O	I/O
H7	I/O	I/O	I/O	I/O
H8	I/O	I/O	I/O	I/O
H9	I/O	I/O	I/O	I/O
H10	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
H11	I/O	I/O	I/O	I/O
H12	V_{DD}	V_{DD}	V_{DD}	V_{DD}
J1	I/O	I/O	I/O	I/O
J2	I/O	I/O	I/O	I/O
J3	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
J4	I/O	I/O	I/O	I/O
J5	I/O	I/O	I/O	I/O
J6	I/O	I/O	I/O	I/O
J7	V_{DD}	V_{DD}	V_{DD}	V_{DD}
J8	TCK	TCK	TCK	TCK
J9	I/O	I/O	I/O	I/O
J10	TDO	TDO	TDO	TDO
J11	I/O	I/O	I/O	I/O
J12	I/O	I/O	I/O	I/O

144-FBGA Pin				
Pin Number	**APA075 Function**	**APA150 Function**	**APA300 Function**	**APA450 Function**
K1	I/O	I/O	I/O	I/O
K2	I/O	I/O	I/O	I/O
K3	I/O	I/O	I/O	I/O
K4	I/O	I/O	I/O	I/O
K5	I/O	I/O	I/O	I/O
K6	I/O	I/O	I/O	I/O
K7	GND	GND	GND	GND
K8	I/O	I/O	I/O	I/O
K9	I/O	I/O	I/O	I/O
K10	GND	GND	GND	GND
K11	I/O	I/O	I/O	I/O
K12	I/O	I/O	I/O	I/O
L1	GND	GND	GND	GND
L2	I/O	I/O	I/O	I/O
L3	I/O	I/O	I/O	I/O
L4	I/O	I/O	I/O	I/O
L5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
L6	I/O	I/O	I/O	I/O
L7	I/O	I/O	I/O	I/O
L8	I/O	I/O	I/O	I/O
L9	TMS	TMS	TMS	TMS
L10	RCK	RCK	RCK	RCK
L11	I/O	I/O	I/O	I/O
L12	TRST	TRST	TRST	TRST
M1	I/O	I/O	I/O	I/O
M2	I/O	I/O	I/O	I/O
M3	I/O	I/O	I/O	I/O
M4	I/O	I/O	I/O	I/O
M5	I/O	I/O	I/O	I/O
M6	I/O	I/O	I/O	I/O
M7	I/O	I/O	I/O	I/O
M8	I/O	I/O	I/O	I/O
M9	TDI	TDI	TDI	TDI
M10	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M11	V_{PP}	V_{PP}	V_{PP}	V_{PP}
M12	V_{PN}	V_{PN}	V_{PN}	V_{PN}

256-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

256-Pin FBGA				
Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
A1	GND	GND	GND	GND
A2	I/O	I/O	I/O	I/O
A3	I/O	I/O	I/O	I/O
A4	I/O	I/O	I/O	I/O
A5	I/O	I/O	I/O	I/O
A6	I/O	I/O	I/O	I/O
A7	I/O	I/O	I/O	I/O
A8	I/O	I/O	I/O	I/O
A9	I/O	I/O	I/O	I/O
A10	I/O	I/O	I/O	I/O
A11	I/O	I/O	I/O	I/O
A12	I/O	I/O	I/O	I/O
A13	I/O	I/O	I/O	I/O
A14	I/O	I/O	I/O	I/O
A15	I/O	I/O	I/O	I/O
A16	GND	GND	GND	GND
B1	I/O	I/O	I/O	I/O
B2	I/O	I/O	I/O	I/O
B3	I/O	I/O	I/O	I/O
B4	I/O	I/O	I/O	I/O
B5	I/O	I/O	I/O	I/O
B6	I/O	I/O	I/O	I/O
B7	I/O	I/O	I/O	I/O
B8	I/O	I/O	I/O	I/O
B9	I/O	I/O	I/O	I/O
B10	I/O	I/O	I/O	I/O
B11	I/O	I/O	I/O	I/O
B12	I/O	I/O	I/O	I/O
B13	I/O	I/O	I/O	I/O
B14	I/O	I/O	I/O	I/O
B15	I/O	I/O	I/O	I/O
B16	I/O	I/O	I/O	I/O
C1	I/O	I/O	I/O	I/O
C2	I/O	I/O	I/O	I/O
C3	I/O	I/O	I/O	I/O

256-Pin FBGA				
Pin Number	APA150 Function	APA300 Function	APA450 Function	APA600 Function
C4	I/O	I/O	I/O	I/O
C5	I/O	I/O	I/O	I/O
C6	I/O	I/O	I/O	I/O
C7	I/O	I/O	I/O	I/O
C8	I/O	I/O	I/O	I/O
C9	I/O	I/O	I/O	I/O
C10	I/O	I/O	I/O	I/O
C11	I/O	I/O	I/O	I/O
C12	I/O	I/O	I/O	I/O
C13	I/O	I/O	I/O	I/O
C14	I/O	I/O	I/O	I/O
C15	I/O	I/O	I/O	I/O
C16	I/O	I/O	I/O	I/O
D1	I/O	I/O	I/O	I/O
D2	I/O	I/O	I/O	I/O
D3	I/O	I/O	I/O	I/O
D4	I/O	I/O	I/O	I/O
D5	I/O	I/O	I/O	I/O
D6	I/O	I/O	I/O	I/O
D7	I/O	I/O	I/O	I/O
D8	I/O	I/O	I/O	I/O
D9	I/O	I/O	I/O	I/O
D10	I/O	I/O	I/O	I/O
D11	I/O	I/O	I/O	I/O
D12	I/O	I/O	I/O	I/O
D13	I/O	I/O	I/O	I/O
D14	I/O	I/O	I/O	I/O
D15	I/O	I/O	I/O	I/O
D16	I/O	I/O	I/O	I/O
E1	I/O	I/O	I/O	I/O
E2	I/O	I/O	I/O	I/O
E3	I/O	I/O	I/O	I/O
E4	I/O	I/O	I/O	I/O
E5	I/O	I/O	I/O	I/O
E6	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

256-Pin FBGA				
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**
E7	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E8	I/O	I/O	I/O	I/O
E9	I/O	I/O	I/O	I/O
E10	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E11	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
E12	I/O	I/O	I/O	I/O
E13	I/O	I/O	I/O	I/O
E14	I/O	I/O	I/O	I/O
E15	I/O	I/O	I/O	I/O
E16	I/O	I/O	I/O	I/O
F1	I/O	I/O	I/O	I/O
F2	I/O	I/O	I/O	I/O
F3	I/O	I/O	I/O	I/O
F4	I/O	I/O	I/O	I/O
F5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
F6	GND	GND	GND	GND
F7	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F8	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F9	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F10	V_{DD}	V_{DD}	V_{DD}	V_{DD}
F11	GND	GND	GND	GND
F12	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
F13	I/O	I/O	I/O	I/O
F14	I/O	I/O	I/O	I/O
F15	I/O	I/O	I/O	I/O
F16	I/O	I/O	I/O	I/O
G1	I/O	I/O	I/O	I/O
G2	I/O	I/O	I/O	I/O
G3	I/O	I/O	I/O	I/O
G4	I/O	I/O	I/O	I/O
G5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
G6	V_{DD}	V_{DD}	V_{DD}	V_{DD}
G7	GND	GND	GND	GND
G8	GND	GND	GND	GND
G9	GND	GND	GND	GND

256-Pin FBGA				
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**
G10	GND	GND	GND	GND
G11	V_{DD}	V_{DD}	V_{DD}	V_{DD}
G12	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
G13	I/O	I/O	I/O	I/O
G14	I/O	I/O	I/O	I/O
G15	I/O	I/O	I/O	I/O
G16	I/O	I/O	I/O	I/O
H1	I/O / GL1	I/O / GL1	I/O / GL1	I/O / GL1
H2	NPECL1	NPECL1	NPECL1	NPECL1
H3	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1	I/O / GLMX1
H4	AGND	AGND	AGND	AGND
H5	I/O	I/O	I/O	I/O
H6	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H7	GND	GND	GND	GND
H8	GND	GND	GND	GND
H9	GND	GND	GND	GND
H10	GND	GND	GND	GND
H11	V_{DD}	V_{DD}	V_{DD}	V_{DD}
H12	I/O	I/O	I/O	I/O
H13	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2	I/O / GLMX2
H14	NPECL2	NPECL2	NPECL2	NPECL2
H15	AGND	AGND	AGND	AGND
H16	I/O / GL4	I/O / GL4	I/O / GL4	I/O / GL4
J1	I/O / GL2	I/O / GL2	I/O / GL2	I/O / GL2
J2	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input	PPECL1 / Input
J3	AVDD	AVDD	AVDD	AVDD
J4	I/O	I/O	I/O	I/O
J5	I/O	I/O	I/O	I/O
J6	V_{DD}	V_{DD}	V_{DD}	V_{DD}
J7	GND	GND	GND	GND
J8	GND	GND	GND	GND
J9	GND	GND	GND	GND
J10	GND	GND	GND	GND
J11	V_{DD}	V_{DD}	V_{DD}	V_{DD}

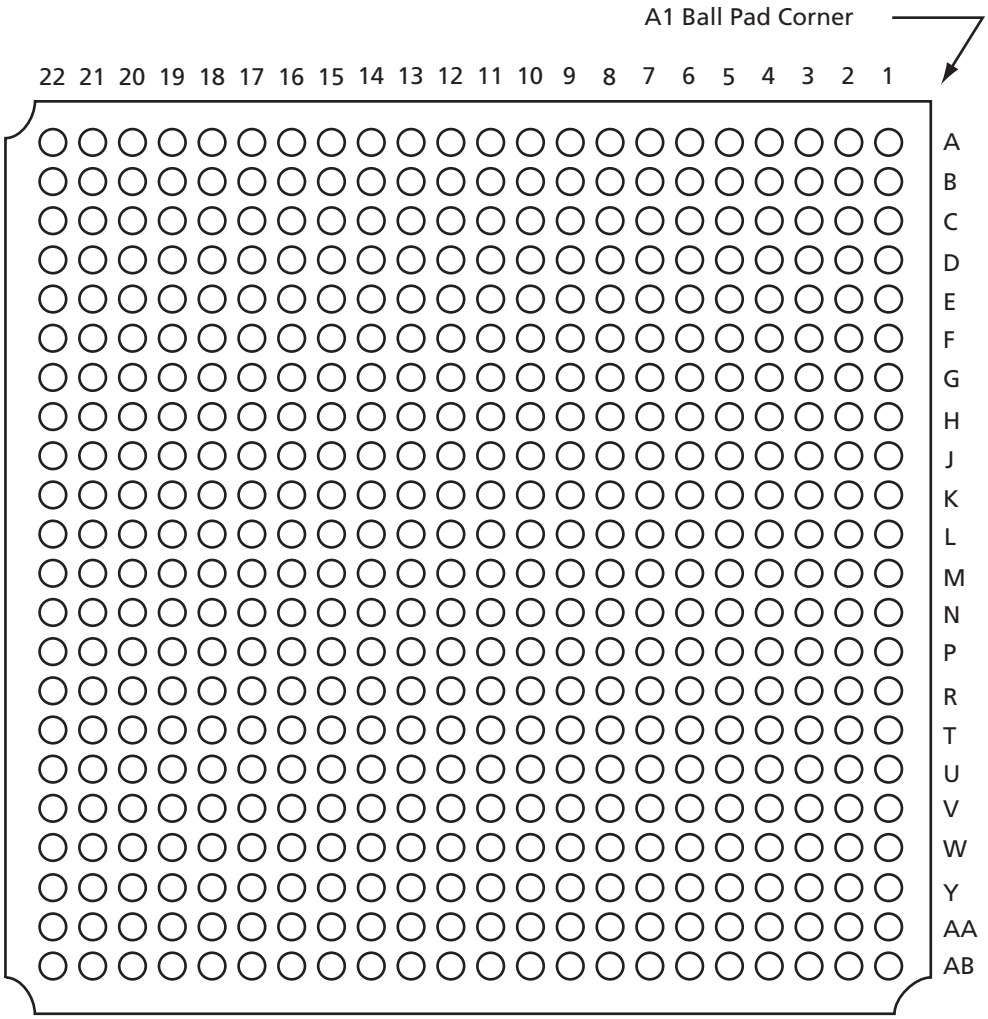
256-Pin FBGA				
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**
J12	I/O	I/O	I/O	I/O
J13	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input	PPECL2 / Input
J14	I/O	I/O	I/O	I/O
J15	AVDD	AVDD	AVDD	AVDD
J16	I/O / GL3	I/O / GL3	I/O / GL3	I/O / GL3
K1	I/O	I/O	I/O	I/O
K2	I/O	I/O	I/O	I/O
K3	I/O	I/O	I/O	I/O
K4	I/O	I/O	I/O	I/O
K5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
K6	V_{DD}	V_{DD}	V_{DD}	V_{DD}
K7	GND	GND	GND	GND
K8	GND	GND	GND	GND
K9	GND	GND	GND	GND
K10	GND	GND	GND	GND
K11	V_{DD}	V_{DD}	V_{DD}	V_{DD}
K12	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
K13	I/O	I/O	I/O	I/O
K14	I/O	I/O	I/O	I/O
K15	I/O	I/O	I/O	I/O
K16	I/O	I/O	I/O	I/O
L1	I/O	I/O	I/O	I/O
L2	I/O	I/O	I/O	I/O
L3	I/O	I/O	I/O	I/O
L4	I/O	I/O	I/O	I/O
L5	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
L6	GND	GND	GND	GND
L7	V_{DD}	V_{DD}	V_{DD}	V_{DD}
L8	V_{DD}	V_{DD}	V_{DD}	V_{DD}
L9	V_{DD}	V_{DD}	V_{DD}	V_{DD}
L10	V_{DD}	V_{DD}	V_{DD}	V_{DD}
L11	GND	GND	GND	GND
L12	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
L13	I/O	I/O	I/O	I/O

256-Pin FBGA				
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**
L14	I/O	I/O	I/O	I/O
L15	I/O	I/O	I/O	I/O
L16	I/O	I/O	I/O	I/O
M1	I/O	I/O	I/O	I/O
M2	I/O	I/O	I/O	I/O
M3	I/O	I/O	I/O	I/O
M4	I/O	I/O	I/O	I/O
M5	I/O	I/O	I/O	I/O
M6	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M7	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M8	I/O	I/O	I/O	I/O
M9	I/O	I/O	I/O	I/O
M10	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M11	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
M12	I/O	I/O	I/O	I/O
M13	I/O	I/O	I/O	I/O
M14	I/O	I/O	I/O	I/O
M15	I/O	I/O	I/O	I/O
M16	I/O	I/O	I/O	I/O
N1	I/O	I/O	I/O	I/O
N2	I/O	I/O	I/O	I/O
N3	I/O	I/O	I/O	I/O
N4	I/O	I/O	I/O	I/O
N5	I/O	I/O	I/O	I/O
N6	I/O	I/O	I/O	I/O
N7	I/O	I/O	I/O	I/O
N8	I/O	I/O	I/O	I/O
N9	I/O	I/O	I/O	I/O
N10	I/O	I/O	I/O	I/O
N11	I/O	I/O	I/O	I/O
N12	I/O	I/O	I/O	I/O
N13	I/O	I/O	I/O	I/O
N14	RCK	RCK	RCK	RCK
N15	I/O	I/O	I/O	I/O
N16	I/O	I/O	I/O	I/O

256-Pin FBGA				
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**
P1	I/O	I/O	I/O	I/O
P2	I/O	I/O	I/O	I/O
P3	I/O	I/O	I/O	I/O
P4	I/O	I/O	I/O	I/O
P5	I/O	I/O	I/O	I/O
P6	I/O	I/O	I/O	I/O
P7	I/O	I/O	I/O	I/O
P8	I/O	I/O	I/O	I/O
P9	I/O	I/O	I/O	I/O
P10	I/O	I/O	I/O	I/O
P11	I/O	I/O	I/O	I/O
P12	I/O	I/O	I/O	I/O
P13	TCK	TCK	TCK	TCK
P14	V_{PP}	V_{PP}	V_{PP}	V_{PP}
P15	TRST	TRST	TRST	TRST
P16	I/O	I/O	I/O	I/O
R1	I/O	I/O	I/O	I/O
R2	I/O	I/O	I/O	I/O
R3	I/O	I/O	I/O	I/O
R4	I/O	I/O	I/O	I/O
R5	I/O	I/O	I/O	I/O
R6	I/O	I/O	I/O	I/O
R7	I/O	I/O	I/O	I/O
R8	I/O	I/O	I/O	I/O
R9	I/O	I/O	I/O	I/O
R10	I/O	I/O	I/O	I/O
R11	I/O	I/O	I/O	I/O
R12	I/O	I/O	I/O	I/O
R13	I/O	I/O	I/O	I/O
R14	TDI	TDI	TDI	TDI
R15	V_{PN}	V_{PN}	V_{PN}	V_{PN}
R16	TDO	TDO	TDO	TDO
T1	GND	GND	GND	GND
T2	I/O	I/O	I/O	I/O
T3	I/O	I/O	I/O	I/O

256-Pin FBGA				
Pin Number	**APA150 Function**	**APA300 Function**	**APA450 Function**	**APA600 Function**
T4	I/O	I/O	I/O	I/O
T5	I/O	I/O	I/O	I/O
T6	I/O	I/O	I/O	I/O
T7	I/O	I/O	I/O	I/O
T8	I/O	I/O	I/O	I/O
T9	I/O	I/O	I/O	I/O
T10	I/O	I/O	I/O	I/O
T11	I/O	I/O	I/O	I/O
T12	I/O	I/O	I/O	I/O
T13	I/O	I/O	I/O	I/O
T14	I/O	I/O	I/O	I/O
T15	TMS	TMS	TMS	TMS
T16	GND	GND	GND	GND

484-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
A1	GND	GND
A2	GND	GND
A3	V_{DDP}	V_{DDP}
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
A16	I/O	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	V_{DDP}	V_{DDP}
A21	GND	GND
A22	GND	GND
B1	GND	GND
B2	V_{DDP}	V_{DDP}
B3	I/O	I/O
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O	I/O
B20	I/O	I/O
B21	V_{DDP}	V_{DDP}
B22	GND	GND
C1	V_{DDP}	V_{DDP}
C2	NC	I/O
C3	I/O	I/O
C4	I/O	I/O
C5	GND	GND
C6	I/O	I/O
C7	I/O	I/O
C8	V_{DD}	V_{DD}
C9	V_{DD}	V_{DD}
C10	I/O	I/O
C11	I/O	I/O
C12	NC	I/O
C13	NC	I/O
C14	V_{DD}	V_{DD}
C15	V_{DD}	V_{DD}
C16	NC	I/O
C17	I/O	I/O
C18	GND	GND
C19	I/O	I/O
C20	I/O	I/O
C21	I/O	I/O
C22	V_{DDP}	V_{DDP}
D1	I/O	I/O
D2	I/O	I/O
D3	NC	I/O
D4	GND	GND
D5	I/O	I/O
D6	I/O	I/O

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	GND	GND
D20	I/O	I/O
D21	I/O	I/O
D22	I/O	I/O
E1	I/O	I/O
E2	NC	I/O
E3	GND	GND
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	GND	GND

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
E21	I/O	I/O
E22	I/O	I/O
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	I/O	I/O
F6	I/O	I/O
F7	I/O	I/O
F8	I/O	I/O
F9	I/O	I/O
F10	I/O	I/O
F11	I/O	I/O
F12	I/O	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
F16	I/O	I/O
F17	I/O	I/O
F18	I/O	I/O
F19	I/O	I/O
F20	I/O	I/O
F21	I/O	I/O
F22	NC	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	NC	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	I/O	I/O
G8	I/O	I/O
G9	I/O	I/O
G10	I/O	I/O
G11	I/O	I/O
G12	I/O	I/O

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
G16	I/O	I/O
G17	I/O	I/O
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
G21	I/O	I/O
G22	I/O	I/O
H1	I/O	I/O
H2	I/O	I/O
H3	V_{DD}	V_{DD}
H4	I/O	I/O
H5	I/O	I/O
H6	I/O	I/O
H7	I/O	I/O
H8	I/O	I/O
H9	V_{DDP}	V_{DDP}
H10	V_{DDP}	V_{DDP}
H11	I/O	I/O
H12	I/O	I/O
H13	V_{DDP}	V_{DDP}
H14	V_{DDP}	V_{DDP}
H15	I/O	I/O
H16	I/O	I/O
H17	I/O	I/O
H18	I/O	I/O
H19	I/O	I/O
H20	V_{DD}	V_{DD}
H21	I/O	I/O
H22	I/O	I/O
J1	I/O	I/O
J2	I/O	I/O
J3	NC	I/O
J4	I/O	I/O

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
J5	I/O	I/O
J6	I/O	I/O
J7	I/O	I/O
J8	V_{DDP}	V_{DDP}
J9	GND	GND
J10	V_{DD}	V_{DD}
J11	V_{DD}	V_{DD}
J12	V_{DD}	V_{DD}
J13	V_{DD}	V_{DD}
J14	GND	GND
J15	V_{DDP}	V_{DDP}
J16	I/O	I/O
J17	I/O	I/O
J18	I/O	I/O
J19	I/O	I/O
J20	NC	I/O
J21	I/O	I/O
J22	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	NC	I/O
K4	I/O	I/O
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	V_{DDP}	V_{DDP}
K9	V_{DD}	V_{DD}
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	V_{DD}	V_{DD}
K15	V_{DDP}	V_{DDP}
K16	I/O	I/O
K17	I/O	I/O
K18	I/O	I/O

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
K19	I/O	I/O
K20	I/O	I/O
K21	I/O	I/O
K22	I/O	I/O
L1	NC	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	I/O / GL1	I/O / GL1
L5	NPECL1	NPECL1
L6	I/O / GLMX1	I/O / GLMX1
L7	AGND	AGND
L8	I/O	I/O
L9	V_{DD}	V_{DD}
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	V_{DD}	V_{DD}
L15	I/O	I/O
L16	I/O / GLMX2	I/O / GLMX2
L17	NPECL2	NPECL2
L18	AGND	AGND
L19	I/O / GL4	I/O / GL4
L20	I/O	I/O
L21	I/O	I/O
L22	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I/O / GL2	I/O / GL2
M5	PPECL1 / Input	PPECL1 / Input
M6	AVDD	AVDD
M7	I/O	I/O
M8	I/O	I/O
M9	V_{DD}	V_{DD}

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	V_{DD}	V_{DD}
M15	I/O	I/O
M16	PPECL2 / Input	PPECL2 / Input
M17	I/O	I/O
M18	AVDD	AVDD
M19	I/O / GL3	I/O / GL3
M20	I/O	I/O
M21	I/O	I/O
M22	I/O	I/O
N1	I/O	I/O
N2	I/O	I/O
N3	NC	I/O
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	I/O	I/O
N8	V_{DDP}	V_{DDP}
N9	V_{DD}	V_{DD}
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	V_{DD}	V_{DD}
N15	V_{DDP}	V_{DDP}
N16	I/O	I/O
N17	I/O	I/O
N18	I/O	I/O
N19	I/O	I/O
N20	NC	I/O
N21	I/O	I/O
N22	I/O	I/O

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	I/O	I/O
P5	I/O	I/O
P6	I/O	I/O
P7	I/O	I/O
P8	V_{DDP}	V_{DDP}
P9	GND	GND
P10	V_{DD}	V_{DD}
P11	V_{DD}	V_{DD}
P12	V_{DD}	V_{DD}
P13	V_{DD}	V_{DD}
P14	GND	GND
P15	V_{DDP}	V_{DDP}
P16	I/O	I/O
P17	I/O	I/O
P18	I/O	I/O
P19	I/O	I/O
P20	NC	I/O
P21	I/O	I/O
P22	I/O	I/O
R1	I/O	I/O
R2	I/O	I/O
R3	V_{DD}	V_{DD}
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	I/O	I/O
R9	V_{DDP}	V_{DDP}
R10	V_{DDP}	V_{DDP}
R11	I/O	I/O
R12	I/O	I/O
R13	V_{DDP}	V_{DDP}
R14	V_{DDP}	V_{DDP}

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
R15	I/O	I/O
R16	I/O	I/O
R17	I/O	I/O
R18	I/O	I/O
R19	I/O	I/O
R20	V_{DD}	V_{DD}
R21	I/O	I/O
R22	I/O	I/O
T1	I/O	I/O
T2	I/O	I/O
T3	NC	I/O
T4	I/O	I/O
T5	I/O	I/O
T6	I/O	I/O
T7	I/O	I/O
T8	I/O	I/O
T9	I/O	I/O
T10	I/O	I/O
T11	I/O	I/O
T12	I/O	I/O
T13	I/O	I/O
T14	I/O	I/O
T15	I/O	I/O
T16	I/O	I/O
T17	RCK	RCK
T18	I/O	I/O
T19	I/O	I/O
T20	NC	I/O
T21	I/O	I/O
T22	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U6	I/O	I/O

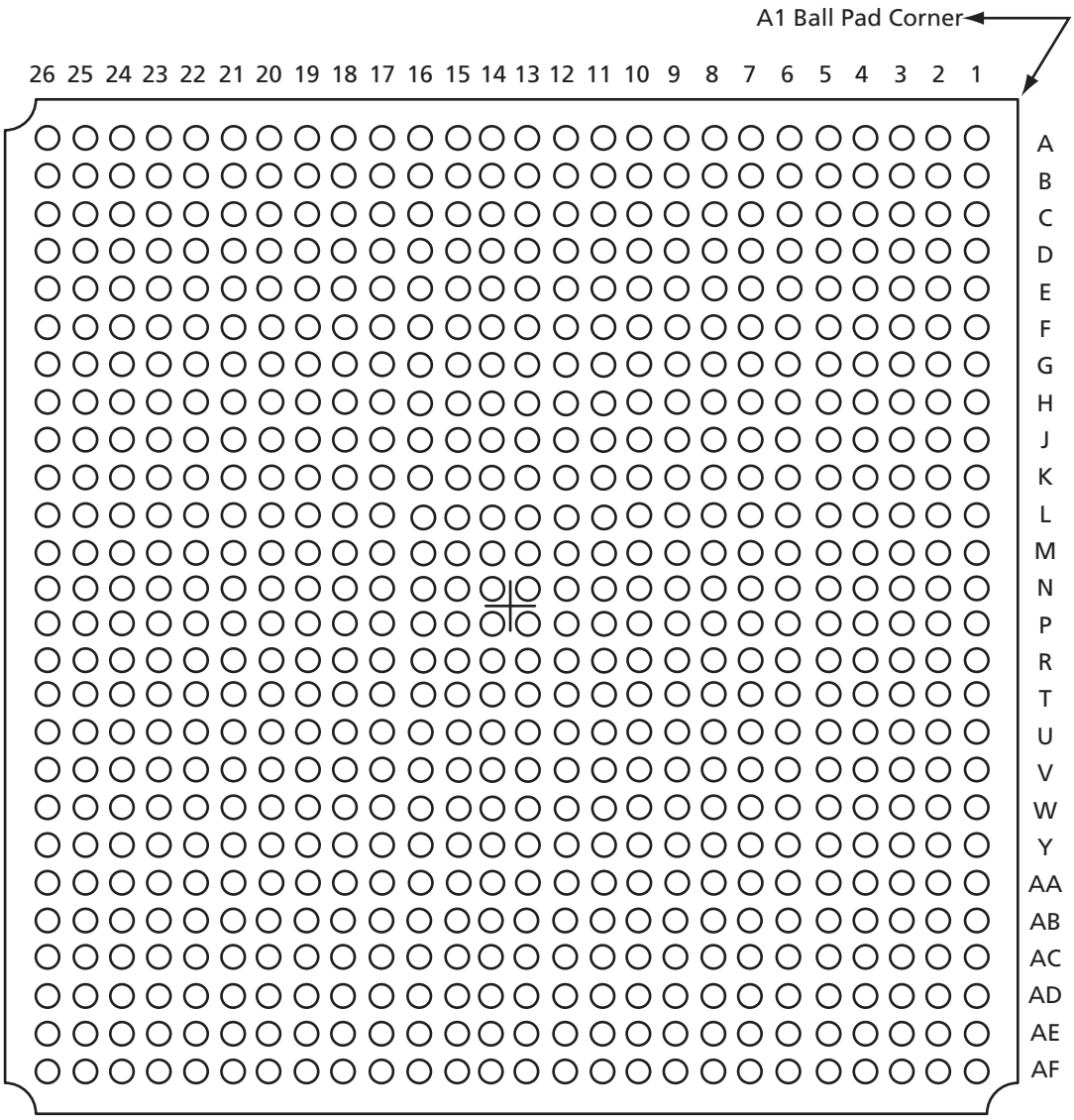
484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
U7	I/O	I/O
U8	I/O	I/O
U9	I/O	I/O
U10	I/O	I/O
U11	I/O	I/O
U12	I/O	I/O
U13	I/O	I/O
U14	I/O	I/O
U15	I/O	I/O
U16	TCK	TCK
U17	V_{PP}	V_{PP}
U18	TRST	TRST
U19	I/O	I/O
U20	NC	I/O
U21	I/O	I/O
U22	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O
V3	GND	GND
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	I/O	I/O
V10	I/O	I/O
V11	I/O	I/O
V12	I/O	I/O
V13	I/O	I/O
V14	I/O	I/O
V15	I/O	I/O
V16	I/O	I/O
V17	TDI	TDI
V18	V_{PN}	V_{PN}
V19	TDO	TDO
V20	GND	GND

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
V21	NC	I/O
V22	I/O	I/O
W1	NC	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	GND	GND
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O
W8	I/O	I/O
W9	I/O	I/O
W10	I/O	I/O
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O
W15	I/O	I/O
W16	I/O	I/O
W17	I/O	I/O
W18	TMS	TMS
W19	GND	GND
W20	NC	I/O
W21	NC	I/O
W22	I/O	I/O
Y1	V_{DDP}	V_{DDP}
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	GND	GND
Y6	I/O	I/O
Y7	I/O	I/O
Y8	V_{DD}	V_{DD}
Y9	V_{DD}	V_{DD}
Y10	I/O	I/O
Y11	I/O	I/O
Y12	I/O	I/O

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
Y13	I/O	I/O
Y14	V_{DD}	V_{DD}
Y15	V_{DD}	V_{DD}
Y16	I/O	I/O
Y17	I/O	I/O
Y18	GND	GND
Y19	I/O	I/O
Y20	I/O	I/O
Y21	NC	I/O
Y22	V_{DDP}	V_{DDP}
AA1	GND	GND
AA2	V_{DDP}	V_{DDP}
AA3	I/O	I/O
AA4	I/O	I/O
AA5	I/O	I/O
AA6	I/O	I/O
AA7	I/O	I/O
AA8	I/O	I/O
AA9	I/O	I/O
AA10	I/O	I/O
AA11	I/O	I/O
AA12	I/O	I/O
AA13	I/O	I/O
AA14	I/O	I/O
AA15	I/O	I/O
AA16	I/O	I/O
AA17	I/O	I/O
AA18	NC	I/O
AA19	NC	I/O
AA20	I/O	I/O
AA21	V_{DDP}	V_{DDP}
AA22	GND	GND
AB1	GND	GND
AB2	GND	GND
AB3	V_{DDP}	V_{DDP}
AB4	I/O	I/O

484-Pin FBGA		
Pin Number	APA450 Function	APA600 Function
AB5	I/O	I/O
AB6	I/O	I/O
AB7	I/O	I/O
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	I/O	I/O
AB13	I/O	I/O
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	NC	I/O
AB19	I/O	I/O
AB20	V_{DDP}	V_{DDP}
AB21	GND	GND
AB22	GND	GND

676-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
A1	GND	GND
A2	GND	GND
A3	I/O	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
A16	I/O	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	I/O	I/O
A22	I/O	I/O
A23	I/O	I/O
A24	I/O	I/O
A25	GND	GND
A26	GND	GND
B1	GND	GND
B2	GND	GND
B3	GND	GND
B4	GND	GND
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O	I/O
B20	I/O	I/O
B21	I/O	I/O
B22	I/O	I/O
B23	I/O	I/O
B24	I/O	I/O
B25	GND	GND
B26	GND	GND
C1	GND	GND
C2	GND	GND
C3	GND	GND
C4	GND	GND
C5	I/O	I/O
C6	I/O	I/O
C7	I/O	I/O
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
C19	I/O	I/O
C20	I/O	I/O
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	I/O	I/O
C26	I/O	I/O
D1	I/O	I/O
D2	I/O	I/O
D3	GND	GND
D4	I/O	I/O
D5	I/O	I/O
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	I/O	I/O
D22	I/O	I/O
D23	I/O	I/O
D24	I/O	I/O
D25	I/O	I/O
D26	I/O	I/O
E1	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
E2	I/O	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	I/O	I/O
E26	I/O	I/O
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	GND	GND
F6	I/O	I/O
F7	NC	NC
F8	I/O	I/O
F9	I/O	I/O
F10	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
F11	I/O	I/O
F12	I/O	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
F16	I/O	I/O
F17	I/O	I/O
F18	I/O	I/O
F19	I/O	I/O
F20	I/O	I/O
F21	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	I/O	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	I/O	I/O
G8	V_{DD}	V_{DD}
G9	NC	NC
G10	I/O	I/O
G11	NC	NC
G12	I/O	I/O
G13	NC	NC
G14	I/O	I/O
G15	NC	NC
G16	I/O	I/O
G17	NC	NC
G18	I/O	I/O
G19	V_{DDP}	V_{DDP}

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
G20	NC	NC
G21	I/O	I/O
G22	I/O	I/O
G23	I/O	I/O
G24	I/O	I/O
G25	I/O	I/O
G26	I/O	I/O
H1	I/O	I/O
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	I/O	I/O
H7	V_{DDP}	V_{DDP}
H8	V_{DD}	V_{DD}
H9	V_{DDP}	V_{DDP}
H10	V_{DDP}	V_{DDP}
H11	V_{DDP}	V_{DDP}
H12	V_{DDP}	V_{DDP}
H13	V_{DDP}	V_{DDP}
H14	V_{DDP}	V_{DDP}
H15	V_{DDP}	V_{DDP}
H16	V_{DDP}	V_{DDP}
H17	V_{DDP}	V_{DDP}
H18	V_{DDP}	V_{DDP}
H19	V_{DD}	V_{DD}
H20	V_{DD}	V_{DD}
H21	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	I/O	I/O
H26	I/O	I/O
J1	I/O	I/O
J2	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J6	I/O	I/O
J7	NC	NC
J8	V_{DDP}	V_{DDP}
J9	V_{DD}	V_{DD}
J10	V_{DD}	V_{DD}
J11	V_{DD}	V_{DD}
J12	V_{DD}	V_{DD}
J13	V_{DD}	V_{DD}
J14	V_{DD}	V_{DD}
J15	V_{DD}	V_{DD}
J16	V_{DD}	V_{DD}
J17	V_{DD}	V_{DD}
J18	V_{DD}	V_{DD}
J19	V_{DDP}	V_{DDP}
J20	NC	NC
J21	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	I/O	I/O
J26	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	I/O	I/O
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	V_{DDP}	V_{DDP}
K9	V_{DD}	V_{DD}
K10	GND	GND
K11	GND	GND

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
K12	GND	GND
K13	GND	GND
K14	GND	GND
K15	GND	GND
K16	GND	GND
K17	GND	GND
K18	V_{DD}	V_{DD}
K19	V_{DDP}	V_{DDP}
K20	I/O	I/O
K21	I/O	I/O
K22	I/O	I/O
K23	I/O	I/O
K24	I/O	I/O
K25	I/O	I/O
K26	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	I/O	I/O
L7	NC	NC
L8	V_{DDP}	V_{DDP}
L9	V_{DD}	V_{DD}
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GND	GND
L15	GND	GND
L16	GND	GND
L17	GND	GND
L18	V_{DD}	V_{DD}
L19	V_{DDP}	V_{DDP}
L20	NC	NC

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
L21	I/O	I/O
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	V_{DDP}	V_{DDP}
M9	V_{DD}	V_{DD}
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M18	V_{DD}	V_{DD}
M19	V_{DDP}	V_{DDP}
M20	I/O	I/O
M21	I/O	I/O
M22	I/O	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	I/O	I/O
M26	I/O	I/O
N1	I/O / GL1	I/O / GL1
N2	AGND	AGND
N3	I/O / GLMX1	I/O / GLMX1

676-Pin FBGA		
Pin Number	**APA600 Function**	**APA750 Function**
N4	I/O	I/O
N5	NPECL1	NPECL1
N6	I/O	I/O
N7	NC	NC
N8	V_{DDP}	V_{DDP}
N9	V_{DD}	V_{DD}
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N18	V_{DD}	V_{DD}
N19	V_{DDP}	V_{DDP}
N20	NC	NC
N21	I/O	I/O
N22	I/O / GL3	I/O / GL3
N23	I/O	I/O
N24	NPECL2	NPECL2
N25	I/O / GL4	I/O / GL4
N26	I/O	I/O
P1	I/O / GL2	I/O / GL2
P2	AVDD	AVDD
P3	I/O	I/O
P4	I/O	I/O
P5	PPECL1 / Input	PPECL1 / Input
P6	I/O	I/O
P7	I/O	I/O
P8	V_{DDP}	V_{DDP}
P9	V_{DD}	V_{DD}
P10	GND	GND
P11	GND	GND

676-Pin FBGA		
Pin Number	**APA600 Function**	**APA750 Function**
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P18	V_{DD}	V_{DD}
P19	V_{DDP}	V_{DDP}
P20	I/O	I/O
P21	I/O	I/O
P22	I/O / GLMX2	I/O / GLMX2
P23	I/O	I/O
P24	PPECL2 / Input	PPECL2 / Input
P25	AVDD	AVDD
P26	AGND	AGND
R1	I/O	I/O
R2	I/O	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	NC	NC
R8	V_{DDP}	V_{DDP}
R9	V_{DD}	V_{DD}
R10	GND	GND
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R18	V_{DD}	V_{DD}
R19	V_{DDP}	V_{DDP}

676-Pin FBGA		
Pin Number	**APA600 Function**	**APA750 Function**
R20	NC	NC
R21	I/O	I/O
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	I/O	I/O
R26	I/O	I/O
T1	I/O	I/O
T2	I/O	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T6	I/O	I/O
T7	I/O	I/O
T8	V_{DDP}	V_{DDP}
T9	V_{DD}	V_{DD}
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T18	V_{DD}	V_{DD}
T19	V_{DDP}	V_{DDP}
T20	I/O	I/O
T21	I/O	I/O
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	I/O	I/O
T26	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U6	I/O	I/O
U7	NC	NC
U8	V_{DDP}	V_{DDP}
U9	V_{DD}	V_{DD}
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U18	V_{DD}	V_{DD}
U19	V_{DDP}	V_{DDP}
U20	NC	NC
U21	I/O	I/O
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	I/O	I/O
U26	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	V_{DDP}	V_{DDP}
V9	V_{DD}	V_{DD}
V10	V_{DD}	V_{DD}
V11	V_{DD}	V_{DD}

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
V12	V_{DD}	V_{DD}
V13	V_{DD}	V_{DD}
V14	V_{DD}	V_{DD}
V15	V_{DD}	V_{DD}
V16	V_{DD}	V_{DD}
V17	V_{DD}	V_{DD}
V18	V_{DD}	V_{DD}
V19	V_{DDP}	V_{DDP}
V20	I/O	I/O
V21	I/O	I/O
V22	I/O	I/O
V23	I/O	I/O
V24	I/O	I/O
V25	I/O	I/O
V26	I/O	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	V_{DD}	V_{DD}
W8	V_{DD}	V_{DD}
W9	V_{DDP}	V_{DDP}
W10	V_{DDP}	V_{DDP}
W11	V_{DDP}	V_{DDP}
W12	V_{DDP}	V_{DDP}
W13	V_{DDP}	V_{DDP}
W14	V_{DDP}	V_{DDP}
W15	V_{DDP}	V_{DDP}
W16	V_{DDP}	V_{DDP}
W17	V_{DDP}	V_{DDP}
W18	V_{DDP}	V_{DDP}
W19	V_{DD}	V_{DD}
W20	V_{DDP}	V_{DDP}

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
W21	I/O	I/O
W22	I/O	I/O
W23	I/O	I/O
W24	I/O	I/O
W25	I/O	I/O
W26	I/O	I/O
Y1	I/O	I/O
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	I/O	I/O
Y6	I/O	I/O
Y7	I/O	I/O
Y8	V_{DDP}	V_{DDP}
Y9	NC	NC
Y10	I/O	I/O
Y11	NC	NC
Y12	I/O	I/O
Y13	NC	NC
Y14	I/O	I/O
Y15	NC	NC
Y16	I/O	I/O
Y17	NC	NC
Y18	I/O	I/O
Y19	V_{DD}	V_{DD}
Y20	V_{PP}	V_{PP}
Y21	I/O	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	I/O	I/O
Y25	I/O	I/O
Y26	I/O	I/O
AA1	I/O	I/O
AA2	I/O	I/O
AA3	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
AA4	I/O	I/O
AA5	I/O	I/O
AA6	GND	GND
AA7	I/O	I/O
AA8	I/O	I/O
AA9	I/O	I/O
AA10	I/O	I/O
AA11	I/O	I/O
AA12	I/O	I/O
AA13	I/O	I/O
AA14	I/O	I/O
AA15	I/O	I/O
AA16	I/O	I/O
AA17	I/O	I/O
AA18	I/O	I/O
AA19	I/O	I/O
AA20	I/O	I/O
AA21	TDO	TDO
AA22	GND	GND
AA23	GND	GND
AA24	I/O	I/O
AA25	I/O	I/O
AA26	I/O	I/O
AB1	I/O	I/O
AB2	I/O	I/O
AB3	I/O	I/O
AB4	I/O	I/O
AB5	I/O	I/O
AB6	GND	GND
AB7	GND	GND
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	I/O	I/O

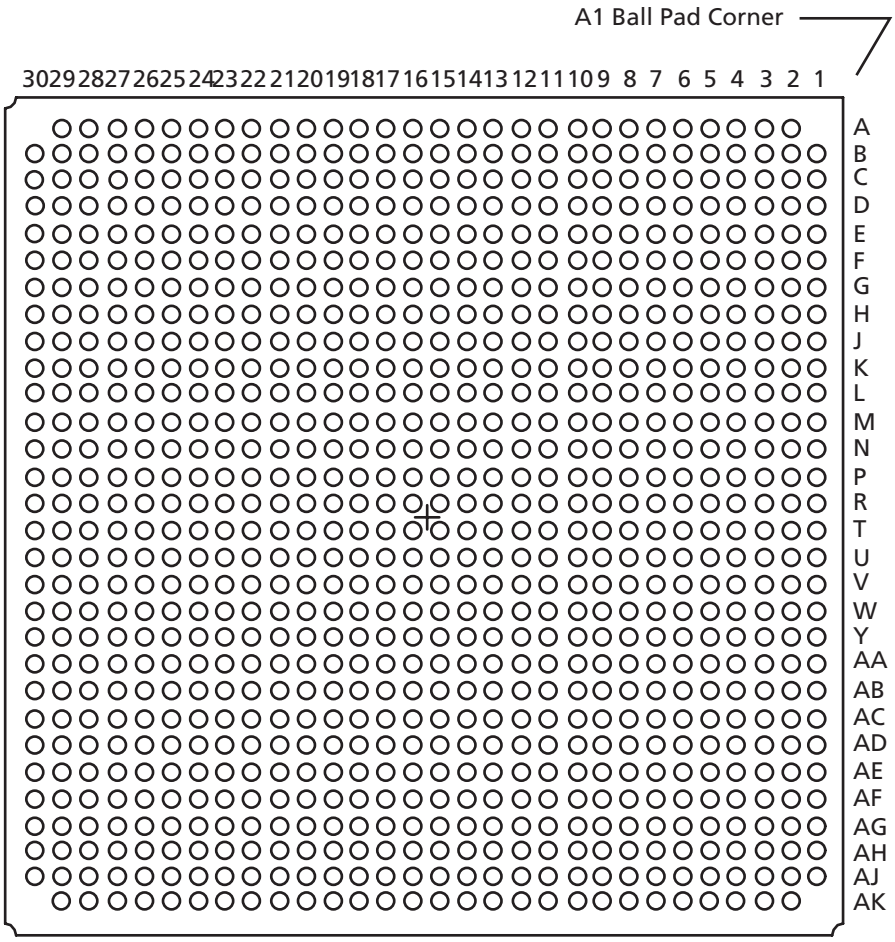
676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
AB13	I/O	I/O
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	I/O	I/O
AB21	TCK	TCK
AB22	TRST	TRST
AB23	I/O	I/O
AB24	I/O	I/O
AB25	I/O	I/O
AB26	I/O	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	I/O	I/O
AC5	GND	GND
AC6	I/O	I/O
AC7	I/O	I/O
AC8	I/O	I/O
AC9	GND	GND
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	I/O
AC13	I/O	I/O
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	I/O	I/O
AC20	I/O	I/O
AC21	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
AC22	TMS	TMS
AC23	RCK	RCK
AC24	I/O	I/O
AC25	I/O	I/O
AC26	I/O	I/O
AD1	I/O	I/O
AD2	I/O	I/O
AD3	I/O	I/O
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	I/O	I/O
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	I/O	I/O
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	I/O	I/O
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	I/O	I/O
AD23	TDI	TDI
AD24	V_{PN}	V_{PN}
AD25	I/O	I/O
AD26	I/O	I/O
AE1	GND	GND
AE2	GND	GND
AE3	GND	GND
AE4	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
AE5	I/O	I/O
AE6	I/O	I/O
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	I/O	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	I/O	I/O
AE16	I/O	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	I/O	I/O
AE22	I/O	I/O
AE23	I/O	I/O
AE24	I/O	I/O
AE25	GND	GND
AE26	GND	GND
AF1	GND	GND
AF2	GND	GND
AF3	GND	GND
AF4	GND	GND
AF5	I/O	I/O
AF6	I/O	I/O
AF7	I/O	I/O
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	I/O	I/O
AF12	I/O	I/O
AF13	I/O	I/O

676-Pin FBGA		
Pin Number	APA600 Function	APA750 Function
AF14	I/O	I/O
AF15	I/O	I/O
AF16	I/O	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	I/O	I/O
AF21	I/O	I/O
AF22	I/O	I/O
AF23	I/O	I/O
AF24	I/O	I/O
AF25	GND	GND
AF26	GND	GND

896-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
A2	GND	GND
A3	GND	GND
A4	I/O	I/O
A5	GND	GND
A6	I/O	I/O
A7	GND	GND
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
A16	I/O	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	I/O	I/O
A22	I/O	I/O
A23	I/O	I/O
A24	GND	GND
A25	I/O	I/O
A26	GND	GND
A27	I/O	I/O
A28	GND	GND
A29	GND	GND
B1	GND	GND
B2	GND	GND
B3	I/O	I/O
B4	V_{DD}	V_{DD}
B5	I/O	I/O
B6	V_{DD}	V_{DD}

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O	I/O
B20	I/O	I/O
B21	I/O	I/O
B22	I/O	I/O
B23	I/O	I/O
B24	I/O	I/O
B25	V_{DD}	V_{DD}
B26	I/O	I/O
B27	V_{DD}	V_{DD}
B28	I/O	I/O
B29	GND	GND
B30	GND	GND
C1	GND	GND
C2	I/O	I/O
C3	V_{DD}	V_{DD}
C4	I/O	I/O
C5	V_{DDP}	V_{DDP}
C6	I/O	I/O
C7	I/O	I/O
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O
C19	I/O	I/O
C20	I/O	I/O
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	I/O	I/O
C26	V_{DDP}	V_{DDP}
C27	I/O	I/O
C28	V_{DD}	V_{DD}
C29	NC	I/O
C30	GND	GND
D1	I/O	I/O
D2	V_{DD}	V_{DD}
D3	I/O	I/O
D4	GND	GND
D5	I/O	I/O
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O
D14	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	I/O	I/O
D22	I/O	I/O
D23	I/O	I/O
D24	I/O	I/O
D25	I/O	I/O
D26	I/O	I/O
D27	GND	GND
D28	I/O	I/O
D29	V_{DD}	V_{DD}
D30	I/O	I/O
E1	GND	GND
E2	I/O	I/O
E3	V_{DDP}	V_{DDP}
E4	I/O	I/O
E5	V_{DD}	V_{DD}
E6	I/O	I/O
E7	V_{DDP}	V_{DDP}
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	V_{DDP}	V_{DDP}
E25	I/O	I/O
E26	V_{DD}	V_{DD}
E27	I/O	I/O
E28	V_{DDP}	V_{DDP}
E29	I/O	I/O
E30	GND	GND
F1	I/O	I/O
F2	V_{DD}	V_{DD}
F3	I/O	I/O
F4	I/O	I/O
F5	I/O	I/O
F6	GND	GND
F7	I/O	I/O
F8	I/O	I/O
F9	I/O	I/O
F10	I/O	I/O
F11	I/O	I/O
F12	I/O	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
F16	I/O	I/O
F17	I/O	I/O
F18	I/O	I/O
F19	I/O	I/O
F20	I/O	I/O
F21	I/O	I/O
F22	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
F23	I/O	I/O
F24	I/O	I/O
F25	GND	GND
F26	I/O	I/O
F27	I/O	I/O
F28	I/O	I/O
F29	V_{DD}	V_{DD}
F30	I/O	I/O
G1	GND	GND
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	V_{DDP}	V_{DDP}
G6	I/O	I/O
G7	V_{DD}	V_{DD}
G8	I/O	I/O
G9	V_{DDP}	V_{DDP}
G10	I/O	I/O
G11	I/O	I/O
G12	I/O	I/O
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
G16	I/O	I/O
G17	I/O	I/O
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
G21	I/O	I/O
G22	V_{DDP}	V_{DDP}
G23	I/O	I/O
G24	V_{DD}	V_{DD}
G25	I/O	I/O
G26	V_{DDP}	V_{DDP}

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
G27	I/O	I/O
G28	I/O	I/O
G29	I/O	I/O
G30	GND	GND
H1	I/O	I/O
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	I/O	I/O
H7	I/O	I/O
H8	GND	GND
H9	NC	I/O
H10	NC	I/O
H11	NC	I/O
H12	NC	I/O
H13	NC	I/O
H14	NC	I/O
H15	NC	I/O
H16	NC	I/O
H17	NC	I/O
H18	NC	I/O
H19	NC	I/O
H20	NC	I/O
H21	NC	I/O
H22	NC	I/O
H23	GND	GND
H24	I/O	I/O
H25	I/O	I/O
H26	I/O	I/O
H27	I/O	I/O
H28	I/O	I/O
H29	I/O	I/O
H30	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J6	I/O	I/O
J7	V_{DDP}	V_{DDP}
J8	I/O	I/O
J9	V_{DD}	V_{DD}
J10	NC	I/O
J11	NC	I/O
J12	NC	I/O
J13	NC	I/O
J14	NC	I/O
J15	NC	I/O
J16	NC	I/O
J17	NC	I/O
J18	NC	I/O
J19	NC	I/O
J20	NC	I/O
J21	NC	I/O
J22	V_{DD}	V_{DD}
J23	I/O	I/O
J24	V_{DDP}	V_{DDP}
J25	I/O	I/O
J26	I/O	I/O
J27	I/O	I/O
J28	I/O	I/O
J29	I/O	I/O
J30	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	I/O	I/O
K9	NC	I/O
K10	V_{DD}	V_{DD}
K11	NC	I/O
K12	V_{DDP}	V_{DDP}
K13	V_{DDP}	V_{DDP}
K14	V_{DDP}	V_{DDP}
K15	V_{DDP}	V_{DDP}
K16	V_{DDP}	V_{DDP}
K17	V_{DDP}	V_{DDP}
K18	V_{DDP}	V_{DDP}
K19	V_{DDP}	V_{DDP}
K20	NC	I/O
K21	V_{DD}	V_{DD}
K22	NC	I/O
K23	I/O	I/O
K24	I/O	I/O
K25	I/O	I/O
K26	I/O	I/O
K27	I/O	I/O
K28	I/O	I/O
K29	I/O	I/O
K30	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	I/O	I/O
L7	I/O	I/O
L8	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
L9	NC	I/O
L10	NC	I/O
L11	V_{DD}	V_{DD}
L12	V_{DD}	V_{DD}
L13	V_{DD}	V_{DD}
L14	V_{DD}	V_{DD}
L15	V_{DD}	V_{DD}
L16	V_{DD}	V_{DD}
L17	V_{DD}	V_{DD}
L18	V_{DD}	V_{DD}
L19	V_{DD}	V_{DD}
L20	V_{DD}	V_{DD}
L21	NC	I/O
L22	NC	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
L27	I/O	I/O
L28	I/O	I/O
L29	I/O	I/O
L30	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	I/O	I/O
M9	NC	I/O
M10	V_{DDP}	V_{DDP}
M11	V_{DD}	V_{DD}
M12	GND	GND

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M18	GND	GND
M19	GND	GND
M20	V_{DD}	V_{DD}
M21	V_{DDP}	V_{DDP}
M22	NC	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	I/O	I/O
M26	I/O	I/O
M27	I/O	I/O
M28	I/O	I/O
M29	I/O	I/O
M30	I/O	I/O
N1	I/O	I/O
N2	I/O	I/O
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	I/O	I/O
N8	I/O	I/O
N9	NC	I/O
N10	V_{DDP}	V_{DDP}
N11	V_{DD}	V_{DD}
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
N17	GND	GND
N18	GND	GND
N19	GND	GND
N20	V_{DD}	V_{DD}
N21	V_{DDP}	V_{DDP}
N22	NC	I/O
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
N26	I/O	I/O
N27	I/O	I/O
N28	I/O	I/O
N29	I/O	I/O
N30	I/O	I/O
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	I/O	I/O
P5	I/O	I/O
P6	I/O	I/O
P7	I/O	I/O
P8	I/O	I/O
P9	I/O	I/O
P10	V_{DDP}	V_{DDP}
P11	V_{DD}	V_{DD}
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P18	GND	GND
P19	GND	GND
P20	V_{DD}	V_{DD}

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
P21	V_{DDP}	V_{DDP}
P22	I/O	I/O
P23	I/O	I/O
P24	I/O	I/O
P25	I/O	I/O
P26	I/O	I/O
P27	I/O	I/O
P28	I/O	I/O
P29	I/O	I/O
P30	I/O	I/O
R1	I/O	I/O
R2	I/O / GLMX1	I/O / GLMX1
R3	AGND	AGND
R4	NPECL1	NPECL1
R5	I/O / GL1	I/O / GL1
R6	I/O	I/O
R7	I/O	I/O
R8	I/O	I/O
R9	NC	I/O
R10	V_{DDP}	V_{DDP}
R11	V_{DD}	V_{DD}
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R18	GND	GND
R19	GND	GND
R20	V_{DD}	V_{DD}
R21	V_{DDP}	V_{DDP}
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
R25	I/O	I/O
R26	I/O	I/O
R27	NPECL2	NPECL2
R28	AGND	AGND
R29	I/O / GLMX2	I/O / GLMX2
R30	I/O	I/O
T1	I/O	I/O
T2	AVDD	AVDD
T3	I/O / GL2	I/O / GL2
T4	PPECL1 / Input	PPECL1 / Input
T5	I/O	I/O
T6	I/O	I/O
T7	I/O	I/O
T8	I/O	I/O
T9	I/O	I/O
T10	V_{DDP}	V_{DDP}
T11	V_{DD}	V_{DD}
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T18	GND	GND
T19	GND	GND
T20	V_{DD}	V_{DD}
T21	V_{DDP}	V_{DDP}
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	I/O	I/O
T26	PPECL2 / Input	PPECL2 / Input
T27	I/O / GL4	I/O / GL4
T28	I/O / GL3	I/O / GL3

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
T29	AVDD	AVDD
T30	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U6	I/O	I/O
U7	I/O	I/O
U8	I/O	I/O
U9	NC	I/O
U10	V_{DDP}	V_{DDP}
U11	V_{DD}	V_{DD}
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U18	GND	GND
U19	GND	GND
U20	V_{DD}	V_{DD}
U21	V_{DDP}	V_{DDP}
U22	NC	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	I/O	I/O
U26	I/O	I/O
U27	I/O	I/O
U28	I/O	I/O
U29	I/O	I/O
U30	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	NC	I/O
V10	V_{DDP}	V_{DDP}
V11	V_{DD}	V_{DD}
V12	GND	GND
V13	GND	GND
V14	GND	GND
V15	GND	GND
V16	GND	GND
V17	GND	GND
V18	GND	GND
V19	GND	GND
V20	V_{DD}	V_{DD}
V21	V_{DDP}	V_{DDP}
V22	NC	I/O
V23	I/O	I/O
V24	I/O	I/O
V25	I/O	I/O
V26	I/O	I/O
V27	I/O	I/O
V28	I/O	I/O
V29	I/O	I/O
V30	I/O	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
W7	I/O	I/O
W8	I/O	I/O
W9	NC	I/O
W10	V_{DDP}	V_{DDP}
W11	V_{DD}	V_{DD}
W12	GND	GND
W13	GND	GND
W14	GND	GND
W15	GND	GND
W16	GND	GND
W17	GND	GND
W18	GND	GND
W19	GND	GND
W20	V_{DD}	V_{DD}
W21	V_{DDP}	V_{DDP}
W22	NC	I/O
W23	I/O	I/O
W24	I/O	I/O
W25	I/O	I/O
W26	I/O	I/O
W27	I/O	I/O
W28	I/O	I/O
W29	I/O	I/O
W30	I/O	I/O
Y1	I/O	I/O
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	I/O	I/O
Y6	I/O	I/O
Y7	I/O	I/O
Y8	I/O	I/O
Y9	NC	I/O
Y10	NC	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
Y11	V_{DD}	V_{DD}
Y12	V_{DD}	V_{DD}
Y13	V_{DD}	V_{DD}
Y14	V_{DD}	V_{DD}
Y15	V_{DD}	V_{DD}
Y16	V_{DD}	V_{DD}
Y17	V_{DD}	V_{DD}
Y18	V_{DD}	V_{DD}
Y19	V_{DD}	V_{DD}
Y20	V_{DD}	V_{DD}
Y21	NC	I/O
Y22	NC	I/O
Y23	I/O	I/O
Y24	I/O	I/O
Y25	I/O	I/O
Y26	I/O	I/O
Y27	I/O	I/O
Y28	I/O	I/O
Y29	I/O	I/O
Y30	I/O	I/O
AA1	I/O	I/O
AA2	I/O	I/O
AA3	I/O	I/O
AA4	I/O	I/O
AA5	I/O	I/O
AA6	I/O	I/O
AA7	I/O	I/O
AA8	I/O	I/O
AA9	NC	I/O
AA10	V_{DD}	V_{DD}
AA11	NC	I/O
AA12	V_{DDP}	V_{DDP}
AA13	V_{DDP}	V_{DDP}
AA14	V_{DDP}	V_{DDP}

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AA15	V_{DDP}	V_{DDP}
AA16	V_{DDP}	V_{DDP}
AA17	V_{DDP}	V_{DDP}
AA18	V_{DDP}	V_{DDP}
AA19	V_{DDP}	V_{DDP}
AA20	NC	I/O
AA21	V_{DD}	V_{DD}
AA22	NC	I/O
AA23	I/O	I/O
AA24	I/O	I/O
AA25	I/O	I/O
AA26	I/O	I/O
AA27	I/O	I/O
AA28	I/O	I/O
AA29	I/O	I/O
AA30	I/O	I/O
AB1	I/O	I/O
AB2	I/O	I/O
AB3	I/O	I/O
AB4	I/O	I/O
AB5	I/O	I/O
AB6	I/O	I/O
AB7	V_{DDP}	V_{DDP}
AB8	I/O	I/O
AB9	V_{DD}	V_{DD}
AB10	NC	I/O
AB11	NC	I/O
AB12	NC	I/O
AB13	NC	I/O
AB14	NC	I/O
AB15	NC	I/O
AB16	NC	I/O
AB17	NC	I/O
AB18	NC	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AB19	NC	I/O
AB20	NC	I/O
AB21	NC	I/O
AB22	V_{DD}	V_{DD}
AB23	I/O	I/O
AB24	V_{DDP}	V_{DDP}
AB25	I/O	I/O
AB26	I/O	I/O
AB27	I/O	I/O
AB28	I/O	I/O
AB29	I/O	I/O
AB30	I/O	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	I/O	I/O
AC5	I/O	I/O
AC6	I/O	I/O
AC7	I/O	I/O
AC8	GND	GND
AC9	NC	I/O
AC10	NC	I/O
AC11	NC	I/O
AC12	NC	I/O
AC13	NC	I/O
AC14	NC	I/O
AC15	NC	I/O
AC16	NC	I/O
AC17	NC	I/O
AC18	NC	I/O
AC19	NC	I/O
AC20	NC	I/O
AC21	NC	I/O
AC22	NC	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AC23	GND	GND
AC24	I/O	I/O
AC25	I/O	I/O
AC26	I/O	I/O
AC27	I/O	I/O
AC28	I/O	I/O
AC29	I/O	I/O
AC30	I/O	I/O
AD1	GND	GND
AD2	I/O	I/O
AD3	I/O	I/O
AD4	I/O	I/O
AD5	V_{DDP}	V_{DDP}
AD6	I/O	I/O
AD7	V_{DD}	V_{DD}
AD8	I/O	I/O
AD9	V_{DDP}	V_{DDP}
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	I/O	I/O
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	I/O	I/O
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	V_{DDP}	V_{DDP}
AD23	TCK	TCK
AD24	V_{DD}	V_{DD}
AD25	TRST	TRST
AD26	V_{DDP}	V_{DDP}

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AD27	I/O	I/O
AD28	I/O	I/O
AD29	I/O	I/O
AD30	GND	GND
AE1	I/O	I/O
AE2	V_{DD}	V_{DD}
AE3	I/O	I/O
AE4	I/O	I/O
AE5	I/O	I/O
AE6	GND	GND
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	I/O	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	I/O	I/O
AE16	I/O	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	I/O	I/O
AE22	I/O	I/O
AE23	I/O	I/O
AE24	I/O	I/O
AE25	GND	GND
AE26	I/O	I/O
AE27	I/O	I/O
AE28	I/O	I/O
AE29	V_{DD}	V_{DD}
AE30	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AF1	GND	GND
AF2	I/O	I/O
AF3	V_{DDP}	V_{DDP}
AF4	I/O	I/O
AF5	V_{DD}	V_{DD}
AF6	I/O	I/O
AF7	V_{DDP}	V_{DDP}
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	I/O	I/O
AF12	I/O	I/O
AF13	I/O	I/O
AF14	I/O	I/O
AF15	I/O	I/O
AF16	I/O	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	I/O	I/O
AF21	I/O	I/O
AF22	I/O	I/O
AF23	I/O	I/O
AF24	V_{DDP}	V_{DDP}
AF25	I/O	I/O
AF26	V_{DD}	V_{DD}
AF27	TDO	TDO
AF28	V_{DDP}	V_{DDP}
AF29	V_{PN}	V_{PN}
AF30	GND	GND
AG1	I/O	I/O
AG2	V_{DD}	V_{DD}
AG3	I/O	I/O
AG4	GND	GND

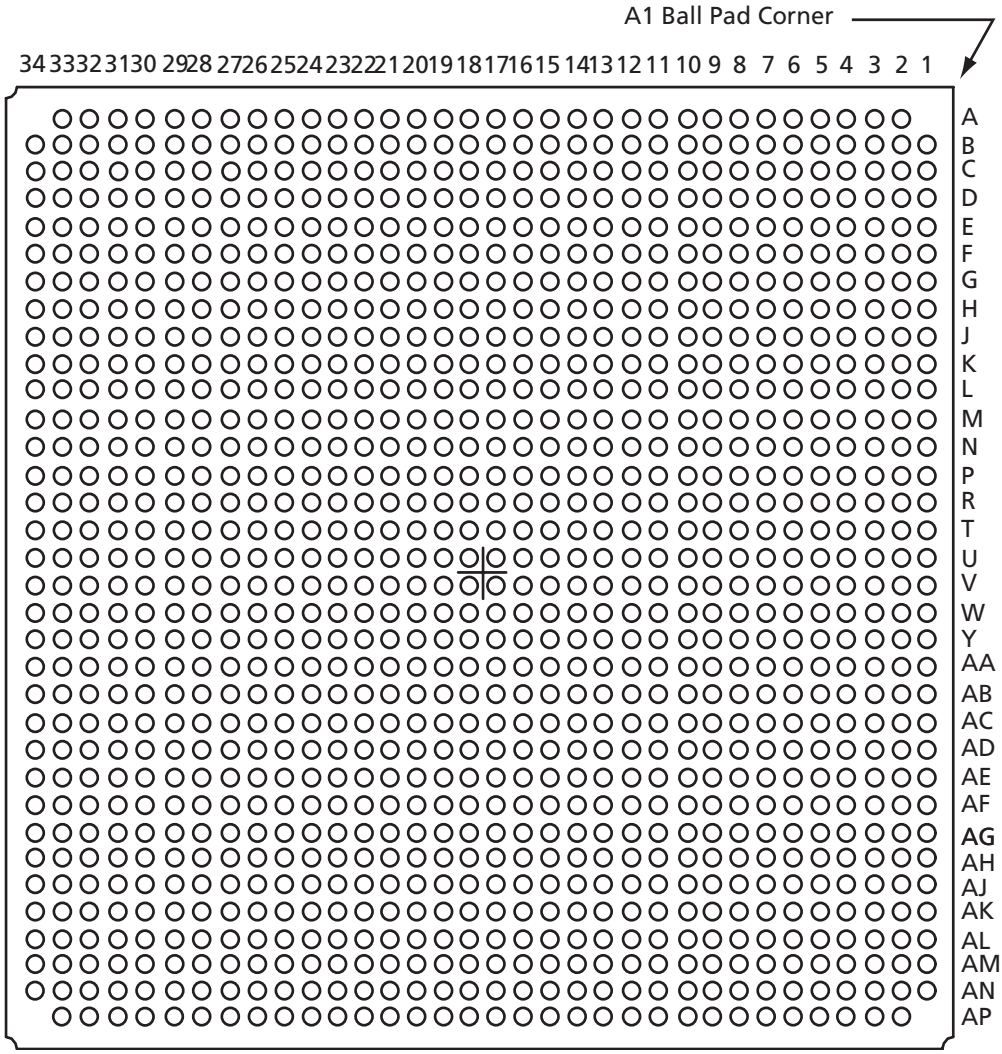
896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AG5	I/O	I/O
AG6	I/O	I/O
AG7	I/O	I/O
AG8	I/O	I/O
AG9	I/O	I/O
AG10	I/O	I/O
AG11	I/O	I/O
AG12	I/O	I/O
AG13	I/O	I/O
AG14	I/O	I/O
AG15	I/O	I/O
AG16	I/O	I/O
AG17	I/O	I/O
AG18	I/O	I/O
AG19	I/O	I/O
AG20	I/O	I/O
AG21	I/O	I/O
AG22	I/O	I/O
AG23	I/O	I/O
AG24	I/O	I/O
AG25	I/O	I/O
AG26	I/O	I/O
AG27	GND	GND
AG28	RCK	RCK
AG29	V_{DD}	V_{DD}
AG30	I/O	I/O
AH1	GND	GND
AH2	I/O	I/O
AH3	V_{DD}	V_{DD}
AH4	I/O	I/O
AH5	V_{DDP}	V_{DDP}
AH6	I/O	I/O
AH7	I/O	I/O
AH8	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AH9	I/O	I/O
AH10	I/O	I/O
AH11	I/O	I/O
AH12	I/O	I/O
AH13	I/O	I/O
AH14	I/O	I/O
AH15	I/O	I/O
AH16	I/O	I/O
AH17	I/O	I/O
AH18	I/O	I/O
AH19	I/O	I/O
AH20	I/O	I/O
AH21	I/O	I/O
AH22	I/O	I/O
AH23	I/O	I/O
AH24	I/O	I/O
AH25	I/O	I/O
AH26	V_{DDP}	V_{DDP}
AH27	TDI	TDI
AH28	V_{DD}	V_{DD}
AH29	V_{PP}	V_{PP}
AH30	GND	GND
AJ1	GND	GND
AJ2	GND	GND
AJ3	I/O	I/O
AJ4	V_{DD}	V_{DD}
AJ5	I/O	I/O
AJ6	V_{DD}	V_{DD}
AJ7	I/O	I/O
AJ8	I/O	I/O
AJ9	I/O	I/O
AJ10	I/O	I/O
AJ11	I/O	I/O
AJ12	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AJ13	I/O	I/O
AJ14	I/O	I/O
AJ15	I/O	I/O
AJ16	I/O	I/O
AJ17	I/O	I/O
AJ18	I/O	I/O
AJ19	I/O	I/O
AJ20	I/O	I/O
AJ21	I/O	I/O
AJ22	I/O	I/O
AJ23	I/O	I/O
AJ24	I/O	I/O
AJ25	V_{DD}	V_{DD}
AJ26	I/O	I/O
AJ27	V_{DD}	V_{DD}
AJ28	TMS	TMS
AJ29	GND	GND
AJ30	GND	GND
AK2	GND	GND
AK3	GND	GND
AK4	I/O	I/O
AK5	GND	GND
AK6	I/O	I/O
AK7	GND	GND
AK8	I/O	I/O
AK9	I/O	I/O
AK10	I/O	I/O
AK11	I/O	I/O
AK12	I/O	I/O
AK13	I/O	I/O
AK14	I/O	I/O
AK15	I/O	I/O
AK16	I/O	I/O
AK17	I/O	I/O

896-Pin FBGA		
Pin Number	APA750 Function	APA1000 Function
AK18	I/O	I/O
AK19	I/O	I/O
AK20	I/O	I/O
AK21	I/O	I/O
AK22	I/O	I/O
AK23	I/O	I/O
AK24	GND	GND
AK25	I/O	I/O
AK26	GND	GND
AK27	I/O	I/O
AK28	GND	GND
AK29	GND	GND

1152-Pin FBGA



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

1152-Pin FBGA	
Pin Number	APA1000 Function
A2	NC
A3	GND
A4	GND
A5	GND
A6	I/O
A7	V_{DD}
A8	V_{DD}
A9	V_{DD}
A10	V_{DD}
A11	I/O
A12	GND
A13	I/O
A14	V_{DDP}
A15	V_{DDP}
A16	I/O
A17	GND
A18	GND
A19	I/O
A20	V_{DDP}
A21	V_{DDP}
A22	I/O
A23	GND
A24	I/O
A25	V_{DD}
A26	V_{DD}
A27	V_{DD}
A28	V_{DD}
A29	I/O
A30	GND
A31	GND
A32	GND
A33	NC
B1	NC
B2	NC
B3	GND
B4	GND
B5	GND

1152-Pin FBGA	
Pin Number	APA1000 Function
B6	NC
B7	I/O
B8	NC
B9	I/O
B10	NC
B11	I/O
B12	GND
B13	I/O
B14	V_{DDP}
B15	V_{DDP}
B16	I/O
B17	GND
B18	GND
B19	I/O
B20	V_{DDP}
B21	V_{DDP}
B22	I/O
B23	GND
B24	I/O
B25	NC
B26	I/O
B27	NC
B28	I/O
B29	NC
B30	GND
B31	GND
B32	GND
B33	NC
B34	NC
C1	GND
C2	GND
C3	NC
C4	GND
C5	GND
C6	I/O
C7	GND
C8	I/O

1152-Pin FBGA	
Pin Number	APA1000 Function
C9	GND
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	I/O
C22	I/O
C23	I/O
C24	I/O
C25	I/O
C26	GND
C27	I/O
C28	GND
C29	I/O
C30	GND
C31	GND
C32	NC
C33	GND
C34	GND
D1	GND
D2	GND
D3	GND
D4	GND
D5	I/O
D6	V_{DD}
D7	I/O
D8	V_{DD}
D9	I/O
D10	I/O
D11	I/O

1152-Pin FBGA	
Pin Number	APA1000 Function
D12	I/O
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
D24	I/O
D25	I/O
D26	I/O
D27	V_{DD}
D28	I/O
D29	V_{DD}
D30	I/O
D31	GND
D32	GND
D33	GND
D34	GND
E1	GND
E2	GND
E3	GND
E4	I/O
E5	V_{DD}
E6	I/O
E7	V_{DDP}
E8	I/O
E9	I/O
E10	I/O
E11	I/O
E12	I/O
E13	I/O
E14	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
E15	I/O
E16	I/O
E17	I/O
E18	I/O
E19	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
E24	I/O
E25	I/O
E26	I/O
E27	I/O
E28	V_{DDP}
E29	I/O
E30	V_{DD}
E31	I/O
E32	GND
E33	GND
E34	GND
F1	I/O
F2	NC
F3	I/O
F4	V_{DD}
F5	I/O
F6	GND
F7	I/O
F8	I/O
F9	I/O
F10	I/O
F11	I/O
F12	I/O
F13	I/O
F14	I/O
F15	I/O
F16	I/O
F17	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
F18	I/O
F19	I/O
F20	I/O
F21	I/O
F22	I/O
F23	I/O
F24	I/O
F25	I/O
F26	I/O
F27	I/O
F28	I/O
F29	GND
F30	I/O
F31	V_{DD}
F32	I/O
F33	NC
F34	NC
G1	V_{DD}
G2	I/O
G3	GND
G4	I/O
G5	V_{DDP}
G6	I/O
G7	V_{DD}
G8	I/O
G9	V_{DDP}
G10	I/O
G11	I/O
G12	I/O
G13	I/O
G14	I/O
G15	I/O
G16	I/O
G17	I/O
G18	I/O
G19	I/O
G20	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
G21	I/O
G22	I/O
G23	I/O
G24	I/O
G25	I/O
G26	V_{DDP}
G27	I/O
G28	V_{DD}
G29	I/O
G30	V_{DDP}
G31	I/O
G32	GND
G33	I/O
G34	V_{DD}
H1	V_{DD}
H2	NC
H3	I/O
H4	V_{DD}
H5	I/O
H6	I/O
H7	I/O
H8	GND
H9	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
H14	I/O
H15	I/O
H16	I/O
H17	I/O
H18	I/O
H19	I/O
H20	I/O
H21	I/O
H22	I/O
H23	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
H24	I/O
H25	I/O
H26	I/O
H27	GND
H28	I/O
H29	I/O
H30	I/O
H31	V_{DD}
H32	I/O
H33	NC
H34	V_{DD}
J1	V_{DD}
J2	I/O
J3	GND
J4	I/O
J5	I/O
J6	I/O
J7	V_{DDP}
J8	I/O
J9	V_{DD}
J10	I/O
J11	V_{DDP}
J12	I/O
J13	I/O
J14	I/O
J15	I/O
J16	I/O
J17	I/O
J18	I/O
J19	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
J24	V_{DDP}
J25	I/O
J26	V_{DD}

1152-Pin FBGA	
Pin Number	**APA1000 Function**
J27	I/O
J28	V_{DDP}
J29	I/O
J30	I/O
J31	I/O
J32	GND
J33	I/O
J34	V_{DD}
K1	V_{DD}
K2	NC
K3	I/O
K4	I/O
K5	I/O
K6	I/O
K7	I/O
K8	I/O
K9	I/O
K10	GND
K11	I/O
K12	I/O
K13	I/O
K14	I/O
K15	I/O
K16	I/O
K17	I/O
K18	I/O
K19	I/O
K20	I/O
K21	I/O
K22	I/O
K23	I/O
K24	I/O
K25	GND
K26	I/O
K27	I/O
K28	I/O
K29	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
K30	I/O
K31	I/O
K32	I/O
K33	NC
K34	V_{DD}
L1	I/O
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	I/O
L8	I/O
L9	V_{DDP}
L10	I/O
L11	V_{DD}
L12	I/O
L13	I/O
L14	I/O
L15	I/O
L16	I/O
L17	I/O
L18	I/O
L19	I/O
L20	I/O
L21	I/O
L22	I/O
L23	I/O
L24	V_{DD}
L25	I/O
L26	V_{DDP}
L27	I/O
L28	I/O
L29	I/O
L30	I/O
L31	I/O
L32	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
L33	I/O
L34	I/O
M1	GND
M2	GND
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	I/O
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{DD}
M13	I/O
M14	V_{DDP}
M15	V_{DDP}
M16	V_{DDP}
M17	V_{DDP}
M18	V_{DDP}
M19	V_{DDP}
M20	V_{DDP}
M21	V_{DDP}
M22	I/O
M23	V_{DD}
M24	I/O
M25	I/O
M26	I/O
M27	I/O
M28	I/O
M29	I/O
M30	I/O
M31	I/O
M32	I/O
M33	GND
M34	GND
N1	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	I/O
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	I/O
N13	V_{DD}
N14	V_{DD}
N15	V_{DD}
N16	V_{DD}
N17	V_{DD}
N18	V_{DD}
N19	V_{DD}
N20	V_{DD}
N21	V_{DD}
N22	V_{DD}
N23	I/O
N24	I/O
N25	I/O
N26	I/O
N27	I/O
N28	I/O
N29	I/O
N30	I/O
N31	I/O
N32	I/O
N33	I/O
N34	I/O
P1	V_{DDP}
P2	V_{DDP}
P3	I/O
P4	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
P5	I/O
P6	I/O
P7	I/O
P8	I/O
P9	I/O
P10	I/O
P11	I/O
P12	V_{DDP}
P13	V_{DD}
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	GND
P21	GND
P22	V_{DD}
P23	V_{DDP}
P24	I/O
P25	I/O
P26	I/O
P27	I/O
P28	I/O
P29	I/O
P30	I/O
P31	I/O
P32	I/O
P33	V_{DDP}
P34	V_{DDP}
R1	V_{DDP}
R2	V_{DDP}
R3	I/O
R4	I/O
R5	I/O
R6	I/O
R7	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
R8	I/O
R9	I/O
R10	I/O
R11	I/O
R12	V_{DDP}
R13	V_{DD}
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	GND
R21	GND
R22	V_{DD}
R23	V_{DDP}
R24	I/O
R25	I/O
R26	I/O
R27	I/O
R28	I/O
R29	I/O
R30	I/O
R31	I/O
R32	I/O
R33	V_{DDP}
R34	V_{DDP}
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T5	I/O
T6	I/O
T7	I/O
T8	I/O
T9	I/O
T10	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
T11	I/O
T12	V_{DDP}
T13	V_{DD}
T14	GND
T15	GND
T16	GND
T17	GND
T18	GND
T19	GND
T20	GND
T21	GND
T22	V_{DD}
T23	V_{DDP}
T24	I/O
T25	I/O
T26	I/O
T27	I/O
T28	I/O
T29	I/O
T30	I/O
T31	I/O
T32	I/O
T33	I/O
T34	I/O
U1	GND
U2	GND
U3	I/O
U4	I/O / GLMX1
U5	AGND
U6	NPECL1
U7	I/O / GL1
U8	I/O
U9	I/O
U10	I/O
U11	I/O
U12	V_{DDP}
U13	V_{DD}

1152-Pin FBGA	
Pin Number	**APA1000 Function**
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	GND
U21	GND
U22	V_{DD}
U23	V_{DDP}
U24	I/O
U25	I/O
U26	I/O
U27	I/O
U28	I/O
U29	NPECL2
U30	AGND
U31	I/O / GLMX2
U32	I/O
U33	GND
U34	GND
V1	GND
V2	GND
V3	I/O
V4	AVDD
V5	I/O / GL2
V6	PPECL1 / Input
V7	I/O
V8	I/O
V9	I/O
V10	I/O
V11	I/O
V12	V_{DDP}
V13	V_{DD}
V14	GND
V15	GND

1152-Pin FBGA	
Pin Number	**APA1000 Function**
V16	GND
V17	GND
V18	GND
V19	GND
V20	GND
V21	GND
V22	V_{DD}
V23	V_{DDP}
V24	I/O
V25	I/O
V26	I/O
V27	I/O
V28	PPECL2 / Input
V29	I/O / GL4
V30	I/O / GL3
V31	AVDD
V32	I/O
V33	GND
V34	GND
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W5	I/O
W6	I/O
W7	I/O
W8	I/O
W9	I/O
W10	I/O
W11	I/O
W12	V_{DDP}
W13	V_{DD}
W14	GND
W15	GND
W16	GND
W17	GND

1152-Pin FBGA	
Pin Number	**APA1000 Function**
W18	GND
W19	GND
W20	GND
W21	GND
W22	V_{DD}
W23	V_{DDP}
W24	I/O
W25	I/O
W26	I/O
W27	I/O
W28	I/O
W29	I/O
W30	I/O
W31	I/O
W32	I/O
W33	I/O
W34	I/O
Y1	V_{DDP}
Y2	V_{DDP}
Y3	I/O
Y4	I/O
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V_{DDP}
Y13	V_{DD}
Y14	GND
Y15	GND
Y16	GND
Y17	GND
Y18	GND
Y19	GND
Y20	GND

1152-Pin FBGA	
Pin Number	**APA1000 Function**
Y21	GND
Y22	V_{DD}
Y23	V_{DDP}
Y24	I/O
Y25	I/O
Y26	I/O
Y27	I/O
Y28	I/O
Y29	I/O
Y30	I/O
Y31	I/O
Y32	I/O
Y33	V_{DDP}
Y34	V_{DDP}
AA1	V_{DDP}
AA2	V_{DDP}
AA3	I/O
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	V_{DDP}
AA13	V_{DD}
AA14	GND
AA15	GND
AA16	GND
AA17	GND
AA18	GND
AA19	GND
AA20	GND
AA21	GND
AA22	V_{DD}
AA23	V_{DDP}

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AA24	I/O
AA25	I/O
AA26	I/O
AA27	I/O
AA28	I/O
AA29	I/O
AA30	I/O
AA31	I/O
AA32	I/O
AA33	V_{DDP}
AA34	V_{DDP}
AB1	I/O
AB2	I/O
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	I/O
AB12	I/O
AB13	V_{DD}
AB14	V_{DD}
AB15	V_{DD}
AB16	V_{DD}
AB17	V_{DD}
AB18	V_{DD}
AB19	V_{DD}
AB20	V_{DD}
AB21	V_{DD}
AB22	V_{DD}
AB23	I/O
AB24	I/O
AB25	I/O
AB26	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AB27	I/O
AB28	I/O
AB29	I/O
AB30	I/O
AB31	I/O
AB32	I/O
AB33	I/O
AB34	I/O
AC1	GND
AC2	GND
AC3	I/O
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	I/O
AC10	I/O
AC11	I/O
AC12	V_{DD}
AC13	I/O
AC14	V_{DDP}
AC15	V_{DDP}
AC16	V_{DDP}
AC17	V_{DDP}
AC18	V_{DDP}
AC19	V_{DDP}
AC20	V_{DDP}
AC21	V_{DDP}
AC22	I/O
AC23	V_{DD}
AC24	I/O
AC25	I/O
AC26	I/O
AC27	I/O
AC28	I/O
AC29	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AC30	I/O
AC31	I/O
AC32	I/O
AC33	GND
AC34	GND
AD1	I/O
AD2	I/O
AD3	I/O
AD4	I/O
AD5	I/O
AD6	I/O
AD7	I/O
AD8	I/O
AD9	V_{DDP}
AD10	I/O
AD11	V_{DD}
AD12	I/O
AD13	I/O
AD14	I/O
AD15	I/O
AD16	I/O
AD17	I/O
AD18	I/O
AD19	I/O
AD20	I/O
AD21	I/O
AD22	I/O
AD23	I/O
AD24	V_{DD}
AD25	I/O
AD26	V_{DDP}
AD27	I/O
AD28	I/O
AD29	I/O
AD30	I/O
AD31	I/O
AD32	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AD33	I/O
AD34	I/O
AE1	V_{DD}
AE2	NC
AE3	I/O
AE4	I/O
AE5	I/O
AE6	I/O
AE7	I/O
AE8	I/O
AE9	I/O
AE10	GND
AE11	I/O
AE12	I/O
AE13	I/O
AE14	I/O
AE15	I/O
AE16	I/O
AE17	I/O
AE18	I/O
AE19	I/O
AE20	I/O
AE21	I/O
AE22	I/O
AE23	I/O
AE24	I/O
AE25	GND
AE26	I/O
AE27	I/O
AE28	I/O
AE29	I/O
AE30	I/O
AE31	I/O
AE32	I/O
AE33	NC
AE34	V_{DD}
AF1	V_{DD}

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AF2	I/O
AF3	GND
AF4	I/O
AF5	I/O
AF6	I/O
AF7	V_{DDP}
AF8	I/O
AF9	V_{DD}
AF10	I/O
AF11	V_{DDP}
AF12	I/O
AF13	I/O
AF14	I/O
AF15	I/O
AF16	I/O
AF17	I/O
AF18	I/O
AF19	I/O
AF20	I/O
AF21	I/O
AF22	I/O
AF23	I/O
AF24	V_{DDP}
AF25	TCK
AF26	V_{DD}
AF27	TRST
AF28	V_{DDP}
AF29	I/O
AF30	I/O
AF31	I/O
AF32	GND
AF33	I/O
AF34	V_{DD}
AG1	V_{DD}
AG2	NC
AG3	I/O
AG4	V_{DD}

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AG5	I/O
AG6	I/O
AG7	I/O
AG8	GND
AG9	I/O
AG10	I/O
AG11	I/O
AG12	I/O
AG13	I/O
AG14	I/O
AG15	I/O
AG16	I/O
AG17	I/O
AG18	I/O
AG19	I/O
AG20	I/O
AG21	I/O
AG22	I/O
AG23	I/O
AG24	I/O
AG25	I/O
AG26	I/O
AG27	GND
AG28	I/O
AG29	I/O
AG30	I/O
AG31	V_{DD}
AG32	I/O
AG33	NC
AG34	V_{DD}
AH1	V_{DD}
AH2	I/O
AH3	GND
AH4	I/O
AH5	V_{DDP}
AH6	I/O
AH7	V_{DD}

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AH8	I/O
AH9	V_{DDP}
AH10	I/O
AH11	I/O
AH12	I/O
AH13	I/O
AH14	I/O
AH15	I/O
AH16	I/O
AH17	I/O
AH18	I/O
AH19	I/O
AH20	I/O
AH21	I/O
AH22	I/O
AH23	I/O
AH24	I/O
AH25	I/O
AH26	V_{DDP}
AH27	I/O
AH28	V_{DD}
AH29	TDO
AH30	V_{DDP}
AH31	V_{PN}
AH32	GND
AH33	I/O
AH34	V_{DD}
AJ1	I/O
AJ2	NC
AJ3	I/O
AJ4	V_{DD}
AJ5	I/O
AJ6	GND
AJ7	I/O
AJ8	I/O
AJ9	I/O
AJ10	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AJ11	I/O
AJ12	I/O
AJ13	I/O
AJ14	I/O
AJ15	I/O
AJ16	I/O
AJ17	I/O
AJ18	I/O
AJ19	I/O
AJ20	I/O
AJ21	I/O
AJ22	I/O
AJ23	I/O
AJ24	I/O
AJ25	I/O
AJ26	I/O
AJ27	I/O
AJ28	I/O
AJ29	GND
AJ30	RCK
AJ31	V_{DD}
AJ32	I/O
AJ33	NC
AJ34	NC
AK1	GND
AK2	GND
AK3	GND
AK4	I/O
AK5	V_{DD}
AK6	I/O
AK7	V_{DDP}
AK8	I/O
AK9	I/O
AK10	I/O
AK11	I/O
AK12	I/O
AK13	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AK14	I/O
AK15	I/O
AK16	I/O
AK17	I/O
AK18	I/O
AK19	I/O
AK20	I/O
AK21	I/O
AK22	I/O
AK23	I/O
AK24	I/O
AK25	I/O
AK26	I/O
AK27	I/O
AK28	V_{DDP}
AK29	TDI
AK30	V_{DD}
AK31	V_{PP}
AK32	GND
AK33	GND
AK34	GND
AL1	GND
AL2	GND
AL3	GND
AL4	GND
AL5	I/O
AL6	V_{DD}
AL7	I/O
AL8	V_{DD}
AL9	I/O
AL10	I/O
AL11	I/O
AL12	I/O
AL13	I/O
AL14	I/O
AL15	I/O
AL16	I/O

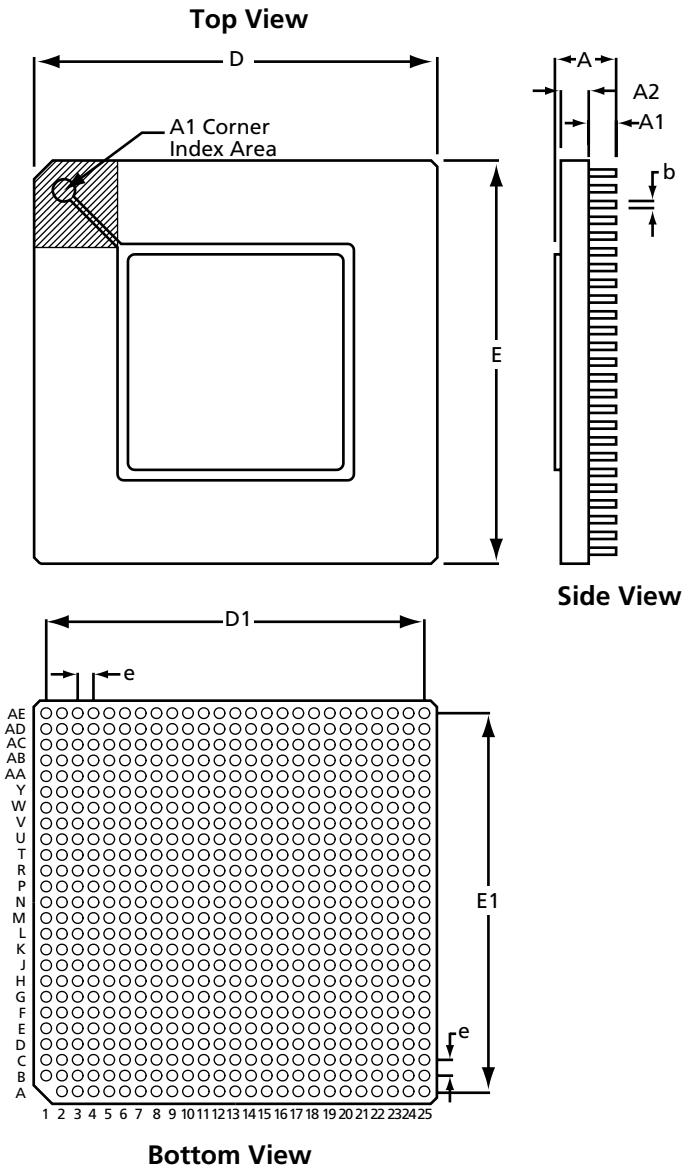
1152-Pin FBGA	
Pin Number	**APA1000 Function**
AL17	I/O
AL18	I/O
AL19	I/O
AL20	I/O
AL21	I/O
AL22	I/O
AL23	I/O
AL24	I/O
AL25	I/O
AL26	I/O
AL27	V_{DD}
AL28	I/O
AL29	V_{DD}
AL30	TMS
AL31	GND
AL32	GND
AL33	GND
AL34	GND
AM1	GND
AM2	GND
AM3	NC
AM4	GND
AM5	GND
AM6	I/O
AM7	GND
AM8	I/O
AM9	GND
AM10	I/O
AM11	I/O
AM12	I/O
AM13	I/O
AM14	I/O
AM15	I/O
AM16	I/O
AM17	I/O
AM18	I/O
AM19	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AM20	I/O
AM21	I/O
AM22	I/O
AM23	I/O
AM24	I/O
AM25	I/O
AM26	GND
AM27	I/O
AM28	GND
AM29	I/O
AM30	GND
AM31	GND
AM32	NC
AM33	GND
AM34	GND
AN1	NC
AN2	NC
AN3	GND
AN4	GND
AN5	GND
AN6	NC
AN7	I/O
AN8	NC
AN9	I/O
AN10	NC
AN11	I/O
AN12	GND
AN13	I/O
AN14	V_{DDP}
AN15	V_{DDP}
AN16	I/O
AN17	GND
AN18	GND
AN19	I/O
AN20	V_{DDP}
AN21	V_{DDP}
AN22	I/O

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AN23	GND
AN24	I/O
AN25	NC
AN26	I/O
AN27	NC
AN28	I/O
AN29	NC
AN30	GND
AN31	GND
AN32	GND
AN33	NC
AN34	NC
AP2	NC
AP3	GND
AP4	GND
AP5	GND
AP6	I/O
AP7	V_{DD}
AP8	V_{DD}
AP9	V_{DD}
AP10	V_{DD}
AP11	I/O
AP12	GND
AP13	I/O
AP14	V_{DDP}
AP15	V_{DDP}
AP16	I/O
AP17	GND
AP18	GND
AP19	I/O
AP20	V_{DDP}
AP21	V_{DDP}
AP22	I/O
AP23	GND
AP24	I/O
AP25	V_{DD}
AP26	V_{DD}

1152-Pin FBGA	
Pin Number	**APA1000 Function**
AP27	V_{DD}
AP28	V_{DD}
AP29	I/O
AP30	GND
AP31	GND
AP32	GND
AP33	NC

624-Pin CCGA/LGA



Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
A2	I/O	I/O
A3	I/O	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
A16	I/O	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	I/O	I/O
A22	I/O	I/O
A23	I/O	I/O
A24	V_{DDP}	V_{DDP}
A25	GND	GND
B1	I/O	I/O
B2	GND	GND
B3	V_{DDP}	V_{DDP}
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O	I/O
B20	I/O	I/O
B21	I/O	I/O
B22	I/O	I/O
B23	V_{DD}	V_{DD}
B24	GND	GND
B25	V_{DDP}	V_{DDP}
C1	I/O	I/O
C2	V_{DDP}	V_{DDP}
C3	GND	GND
C4	V_{DD}	V_{DD}
C5	I/O	I/O
C6	I/O	I/O
C7	GND	GND
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O
C19	GND	GND
C20	I/O	I/O
C21	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
C22	I/O	I/O
C23	GND	GND
C24	V_{DD}	V_{DD}
C25	I/O	I/O
D1	I/O	I/O
D2	I/O	I/O
D3	V_{DD}	V_{DD}
D4	GND	GND
D5	I/O	I/O
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	GND	GND
D12	I/O	I/O
D13	I/O	I/O
D14	I/O	I/O
D15	GND	GND
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	I/O	I/O
D22	I/O	I/O
D23	I/O	I/O
D24	I/O	I/O
D25	I/O	I/O
E1	I/O	I/O
E2	I/O	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	I/O	I/O
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	I/O	I/O
F6	I/O	I/O
F7	I/O	I/O
F8	GND	GND
F9	I/O	I/O
F10	I/O	I/O
F11	I/O	I/O
F12	I/O	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
F16	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
F17	I/O	I/O
F18	GND	GND
F19	I/O	I/O
F20	I/O	I/O
F21	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	I/O	I/O
G8	I/O	I/O
G9	I/O	I/O
G10	I/O	I/O
G11	I/O	I/O
G12	I/O	I/O
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
G16	I/O	I/O
G17	I/O	I/O
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
G21	I/O	I/O
G22	I/O	I/O
G23	I/O	I/O
G24	I/O	I/O
G25	I/O	I/O
H1	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
H2	I/O	I/O
H3	GND	GND
H4	I/O	I/O
H5	I/O	I/O
H6	I/O	I/O
H7	I/O	I/O
H8	V_{DDP}	V_{DDP}
H9	V_{DDP}	V_{DDP}
H10	V_{DDP}	V_{DDP}
H11	V_{DDP}	V_{DDP}
H12	V_{DDP}	V_{DDP}
H13	V_{DDP}	V_{DDP}
H14	V_{DDP}	V_{DDP}
H15	V_{DDP}	V_{DDP}
H16	V_{DDP}	V_{DDP}
H17	V_{DDP}	V_{DDP}
H18	V_{DDP}	V_{DDP}
H19	I/O	I/O
H20	I/O	I/O
H21	I/O	I/O
H22	I/O	I/O
H23	GND	GND
H24	I/O	I/O
H25	I/O	I/O
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J6	GND	GND
J7	I/O	I/O
J8	V_{DDP}	V_{DDP}
J9	GND	GND
J10	GND	GND
J11	GND	GND

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
J12	GND	GND
J13	GND	GND
J14	GND	GND
J15	GND	GND
J16	GND	GND
J17	GND	GND
J18	V_{DDP}	V_{DDP}
J19	I/O	I/O
J20	GND	GND
J21	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	I/O	I/O
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	V_{DDP}	V_{DDP}
K9	GND	GND
K10	V_{DD}	V_{DD}
K11	V_{DD}	V_{DD}
K12	V_{DD}	V_{DD}
K13	V_{DD}	V_{DD}
K14	V_{DD}	V_{DD}
K15	V_{DD}	V_{DD}
K16	V_{DD}	V_{DD}
K17	GND	GND
K18	V_{DDP}	V_{DDP}
K19	I/O	I/O
K20	I/O	I/O
K21	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
K22	I/O	I/O
K23	I/O	I/O
K24	I/O	I/O
K25	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	I/O	I/O
L7	I/O	I/O
L8	V_{DDP}	V_{DDP}
L9	GND	GND
L10	V_{DD}	V_{DD}
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GND	GND
L15	GND	GND
L16	V_{DD}	V_{DD}
L17	GND	GND
L18	V_{DDP}	V_{DDP}
L19	I/O	I/O
L20	I/O	I/O
L21	I/O	I/O
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	AGND	AGND
M5	NPECL1	NPECL1
M6	I/O / GL2	I/O / GL2

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
M7	I/O / GLMX1	I/O / GLMX1
M8	V_{DDP}	V_{DDP}
M9	GND	GND
M10	V_{DD}	V_{DD}
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	V_{DD}	V_{DD}
M17	GND	GND
M18	V_{DDP}	V_{DDP}
M19	I/O / GLMX2	I/O / GLMX2
M20	I/O / GL4	I/O / GL4
M21	NPECL2	NPECL2
M22	AGND	AGND
M23	I/O	I/O
M24	I/O	I/O
M25	I/O	I/O
N1	I/O	I/O
N2	I/O	I/O
N3	I/O	I/O
N4	AVDD	AVDD
N5	PPECL1 / Input	PPECL1 / Input
N6	I/O / GL1	I/O / GL1
N7	I/O	I/O
N8	V_{DDP}	V_{DDP}
N9	GND	GND
N10	V_{DD}	V_{DD}
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND

624-Pin CCGA/LGA		
Pin Number	**APA600 Function**	**APA1000 Function**
N16	V_{DD}	V_{DD}
N17	GND	GND
N18	V_{DDP}	V_{DDP}
N19	I/O	I/O
N20	I/O / GL3	I/O / GL3
N21	PPECL2 / Input	PPECL2 / Input
N22	AVDD	AVDD
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	GND	GND
P5	I/O	I/O
P6	I/O	I/O
P7	I/O	I/O
P8	V_{DDP}	V_{DDP}
P9	GND	GND
P10	V_{DD}	V_{DD}
P11	GND	GND
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	V_{DD}	V_{DD}
P17	GND	GND
P18	V_{DDP}	V_{DDP}
P19	I/O	I/O
P20	I/O	I/O
P21	I/O	I/O
P22	GND	GND
P23	I/O	I/O
P24	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	**APA600 Function**	**APA1000 Function**
P25	I/O	I/O
R1	I/O	I/O
R2	I/O	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	V_{DDP}	V_{DDP}
R9	GND	GND
R10	V_{DD}	V_{DD}
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	V_{DD}	V_{DD}
R17	GND	GND
R18	V_{DDP}	V_{DDP}
R19	I/O	I/O
R20	I/O	I/O
R21	I/O	I/O
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	I/O	I/O
T1	I/O	I/O
T2	I/O	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T6	I/O	I/O
T7	I/O	I/O
T8	V_{DDP}	V_{DDP}
T9	GND	GND

624-Pin CCGA/LGA		
Pin Number	**APA600 Function**	**APA1000 Function**
T10	V_{DD}	V_{DD}
T11	V_{DD}	V_{DD}
T12	V_{DD}	V_{DD}
T13	V_{DD}	V_{DD}
T14	V_{DD}	V_{DD}
T15	V_{DD}	V_{DD}
T16	V_{DD}	V_{DD}
T17	GND	GND
T18	V_{DDP}	V_{DDP}
T19	I/O	I/O
T20	I/O	I/O
T21	I/O	I/O
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U6	GND	GND
U7	I/O	I/O
U8	V_{DDP}	V_{DDP}
U9	GND	GND
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U18	V_{DDP}	V_{DDP}
U19	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
U20	GND	GND
U21	I/O	I/O
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O
V3	GND	GND
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	V_{DDP}	V_{DDP}
V9	V_{DDP}	V_{DDP}
V10	V_{DDP}	V_{DDP}
V11	V_{DDP}	V_{DDP}
V12	V_{DDP}	V_{DDP}
V13	V_{DDP}	V_{DDP}
V14	V_{DDP}	V_{DDP}
V15	V_{DDP}	V_{DDP}
V16	V_{DDP}	V_{DDP}
V17	V_{DDP}	V_{DDP}
V18	V_{DDP}	V_{DDP}
V19	RCK	RCK
V20	I/O	I/O
V21	I/O	I/O
V22	I/O	I/O
V23	GND	GND
V24	I/O	I/O
V25	I/O	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O
W8	I/O	I/O
W9	I/O	I/O
W10	I/O	I/O
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O
W15	I/O	I/O
W16	I/O	I/O
W17	I/O	I/O
W18	I/O	I/O
W19	TMS	TMS
W20	TDO	TDO
W21	I/O	I/O
W22	I/O	I/O
W23	I/O	I/O
W24	I/O	I/O
W25	I/O	I/O
Y1	I/O	I/O
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	I/O	I/O
Y6	I/O	I/O
Y7	I/O	I/O
Y8	GND	GND
Y9	I/O	I/O
Y10	I/O	I/O
Y11	I/O	I/O
Y12	I/O	I/O
Y13	I/O	I/O
Y14	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
Y15	I/O	I/O
Y16	I/O	I/O
Y17	GND	GND
Y18	I/O	I/O
Y19	TCK	TCK
Y20	VPP	VPP
Y21	VPN	VPN
Y22	I/O	I/O
Y23	I/O	I/O
Y24	I/O	I/O
Y25	I/O	I/O
AA1	I/O	I/O
AA2	I/O	I/O
AA3	I/O	I/O
AA4	I/O	I/O
AA5	I/O	I/O
AA6	I/O	I/O
AA7	I/O	I/O
AA8	I/O	I/O
AA9	I/O	I/O
AA10	I/O	I/O
AA11	I/O	I/O
AA12	I/O	I/O
AA13	I/O	I/O
AA14	I/O	I/O
AA15	I/O	I/O
AA16	I/O	I/O
AA17	I/O	I/O
AA18	I/O	I/O
AA19	I/O	I/O
AA20	TDI	TDI
AA21	TRST	TRST
AA22	I/O	I/O
AA23	I/O	I/O
AA24	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
AA25	I/O	I/O
AB1	I/O	I/O
AB2	I/O	I/O
AB3	I/O	I/O
AB4	I/O	I/O
AB5	I/O	I/O
AB6	I/O	I/O
AB7	I/O	I/O
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	GND	GND
AB12	I/O	I/O
AB13	I/O	I/O
AB14	I/O	I/O
AB15	GND	GND
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	I/O	I/O
AB21	I/O	I/O
AB22	I/O	I/O
AB23	I/O	I/O
AB24	I/O	I/O
AB25	I/O	I/O
AC1	I/O	I/O
AC2	V_{DD}	V_{DD}
AC3	GND	GND
AC4	I/O	I/O
AC5	I/O	I/O
AC6	I/O	I/O
AC7	GND	GND
AC8	I/O	I/O
AC9	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	I/O
AC13	I/O	I/O
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	GND	GND
AC20	I/O	I/O
AC21	I/O	I/O
AC22	I/O	I/O
AC23	I/O	I/O
AC24	V_{DD}	V_{DD}
AC25	I/O	I/O
AD1	V_{DDP}	V_{DDP}
AD2	GND	GND
AD3	V_{DD}	V_{DD}
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	I/O	I/O
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	I/O	I/O
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	I/O	I/O
AD18	I/O	I/O
AD19	I/O	I/O

624-Pin CCGA/LGA		
Pin Number	APA600 Function	APA1000 Function
AD20	I/O	I/O
AD21	I/O	I/O
AD22	I/O	I/O
AD23	V_{DD}	V_{DD}
AD24	GND	GND
AD25	V_{DDP}	V_{DDP}
AE1	GND	GND
AE2	V_{DDP}	V_{DDP}
AE3	I/O	I/O
AE4	I/O	I/O
AE5	I/O	I/O
AE6	I/O	I/O
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	I/O	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	I/O	I/O
AE16	I/O	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	I/O	I/O
AE22	I/O	I/O
AE23	I/O	I/O
AE24	V_{DDP}	V_{DDP}
AE25	GND	GND

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v5.9)	Page
v5.8 (June 2009)	The –F speed grade is no longer supported and was removed from the datasheet.	N/A
	A note regarding RoHS compliant packages was added to the "Device Resources" table.	iii
v5.7 (September 2008)	The "PLL Electrical Specifications" table was updated significantly. Changes were made to the Input, VCO (Voltage Controlled Oscillator), and Output frequencies, and the acquisition time.	2-18
	Table 2-10 • PLL I/O Constraints is new.	2-19
	Table 2-23 • DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Commercial and Industrial Temperature Only is the same table that was in v5.7, but it now only applies to commercial and industrial temperature ranges. Table 2-24 • DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only is based on Table 2-23 but Table 2-24 only applies to military temperature. The V_{OH} and V_{OL} specifications were updated in Table 2-24, and changes have been made to the drive currents at which 3.3 V V_{OH} and V_{OL} voltage levels are measured and are now split by slew rate. In addition in Table 2-24, the maximum V_{IL} specification has changed from 0.8 V to 0.7 V for 3.3 V Schmitt-trigger input operation.	2-38
v5.6 (August 2008)	V_{OH} and V_{OL} data in Table 2-24 • DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only was changed back to the data in v5.5.	2-38
v5.5 (February 2007)	V_{OH} and V_{OL} data was updated in Table 2-24 • DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only.	2-38
v5.4 (October 2006)	A statement about single cell and cascaded cell timing diagrams was added to the "Enclosed Timing Diagrams – FIFO Mode:" section.	2-65
	The following pins were updated in the "144-FBGA Pin" table: **Pin Number Updated Function** C2 I/O / GL1 F1 I/O / GL2	3-38
v5.3 (May 2006)	The heading, MIL-STD-883B, and note 4 were added to the "Device Resources" table.	iii
	The "Temperature Grade Offerings" table was updated to include the military (M) temperature grade in the following device/packages: APA300-FG144 APA300-FG256 APA600-FG256 APA600-FG484 APA600-FG676 APA1000-FG896	iv
v5.2 (December 2005)	90° and 270° phase shift support was removed from the datasheet.	N/A
	The "Ordering Information" section was updated to include RoHS information.	ii
	The last paragraph of the "Boundary Scan (JTAG)" section was updated.	2-8
	The Output Frequency Range in the "Timing Control and Characteristics" section.	2-10
	The title for Table 2-19 • Military Temperature Grade Product Performance Retention was updated.	2-32
	The caption was updated in Figure 2-45 • FIFO Reset.	2-72

Previous version	Changes in current version (v5.9)	Page
v5.1	MIL-STD-883 was added to the datasheet.	N/A
	V_{CC} and V_{CCI} were changed to V_{DDP}.	N/A
	Table 2-9 • Temperature and Voltage Derating Factors was updated to include 135°C.	2-17
v5.0	In the "208-Pin PQFP" table, the following pin numbers have been updated: **Pin Number** **Function** 24 I/O / GL2 30 I/O / GL1	3-6
	In the "208-Pin CQFP" table, the following pin numbers have been updated: **Pin Number** **Function** 23 I/O / GLMX1 24 I/O / GL2 28 PPECL1 / Input 30 I/O / GL1 128 I/O / GL3 129 PPECL2 / Input 134 I/O / GL4 135 I/O / GLMX2	3-13
v4.1	In the "624-Pin CCGA/LGA" table, the following pin numbers have been updated: **Pin Number** **Function** M6 I/O / GL2 M7 I/O / GLMX1 M19 I/O / GLMX2 M20 I/O / GL4 N5 PPECL1 / Input N6 I/O / GL1 N20 I/O / GL3 N21 PPECL2 / Input	3-79
	MIL-STD 883B data will be added into this datasheet after the MIL-STD 883B qualification is complete.	
	Green packaging information in the "Ordering Information" section was updated.	ii
	The "Temperature Grade Offerings" table was updated for the CG624.	iv
	The "Ordering Information" section was updated.	ii
	The "Live at Power-Up" section is new.	1-3
	Note 2 in Figure 2-1 • Ultra-Fast Local Resources was updated.	2-1
	The 3.3 V column in Table 2-3 was updated.	2-6
	The "Input/Output Blocks" section was updated.	2-6
	The note was removed from Table 2-4 • I/O Features.	2-6
	The "Power-Up Sequencing" section was updated.	2-7
	The first bullet in the "ProASIC PLUS Clock Management System" section was updated.	2-10
	The first paragraph in the "Performance Retention" section was updated.	2-31
	Mixed Voltage was removed from Table 2-20 • Recommended Maximum Operating Conditions Programming and PLL Supplies.	2-33
	Table 2-21 • Recommended Operating Conditions was updated.	2-33
	Mixed Mode Voltage was removed from Table 2-22 and the Military/MIL-STD-883B column was updated.	2-34
	All tables from Table 2-27 • Worst-Case Commercial Conditions to Table 2-47 • Worst-Case Military Conditions[1] were updated.	2-42 to 2-51
	Table 2-50 • JTAG Switching Characteristics is new.	2-53

Previous version	Changes in current version (v5.9)	Page
v4.1 (continued)	Figure 2-27 • JTAG Operation Timing is new.	2-53
	Note 1 in Table 2-52 • T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial was updated.	2-55
	The notes in Table 2-56 • T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial were updated.	2-59
	A note was added to Figure 2-45 • FIFO Reset.	2-72
	A note was added to Table 2-68 • T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/Industrial.	2-72
	The "TRST Test Reset Input" section was updated in the "Pin Description" section.	2-73
	The "624-Pin CCGA/LGA" section was updated for the APA600 and APA1000. Please review all pin data.	3-78
v4.0	Figure 2-17 • Using the PLL for Clock Deskewing was updated.	2-16
	Table 2-48 • Recommended Operating Conditions was updated.	2-52
	The "1152-Pin FBGA" figure was updated.	3-69
	Pin names were changed to more accurately reflect the multiple functions supported by each pin.	
v3.5	The ProASIC PLUS and ProASIC PLUS Military/Aerospace datasheets were combined. This document now supports Commercial, Industrial, and Military Temperature devices.	
	Table 1 • ProASICPLUS Product Profile was updated.	i
	The "Ordering Information" section was updated.	ii
	"Plastic Device Resources" table was updated.	ii
	The Long Term Jitter Peak-to-Peak Max. in the "PLL Electrical Specifications" table was updated.	2-18
	The "Calculating Typical Power Dissipation" section was updated.	2-28
	"Performance Retention" section	2-31
	Table 2-19 • Military Temperature Grade Product Performance Retention	2-32
	Table 2-21 • Recommended Operating Conditions was updated.	2-33
	Table 2-22 • DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V) was updated.	2-34
	Table 2-24 • DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only was updated.	2-38
	Table 2-48 • Recommended Operating Conditions was updated.	2-52
v3.4	The "Temperature Grade Offerings" table is new.	iv
	The "Speed Grade and Temperature Matrix" table is new.	iv
	The "ProASIC PLUS Clock Management System" section was updated.	2-10
	The "Lock Signal" section was updated.	2-13
	The "PLL Electrical Specifications" table was updated.	2-18
	The "User Security" section was updated.	2-20
	The "Design Environment" section was updated.	2-25
	Table 2-16 • Package Thermal Characteristics was updated.	2-27
	The "Asynchronous FIFO Full and Empty Transitions" section was updated.	2-65
	The "AVDD PLL Power Supply" section in the "Pin Description" section was updated.	2-73
v3.3	The "144-Pin TQFP" table was updated. The following pins changed: Pin 15 = GLMX1 Pin 16 = GL1 Pin 21 = GL2 Pin 88 = GL3 Pin93 = GL4 Pin 94 = GLMX2	3-4

Previous version	Changes in current version (v5.9)	Page
v3.2	The "ProASIC^PLUS Clock Management System" section was updated.	2-10
	Figure 2-11 • PLL Block – Top-Level View and Detailed PLL Block Diagram was updated.	2-11
	Table 2-7 • Clock-Conditioning Circuitry MUX Settings is new.	2-12
	Figure 2-17 • Using the PLL for Clock Deskewing was updated.	2-16
	The "PLL Electrical Specifications" section was updated.	2-18
	Figure 2-23 • Tristate Buffer Delays was updated.	2-42
	In the "Calculating Typical Power Dissipation" section, P9 was changed to 7.5 mW.	2-28
	The "Programming, Storage, and Operating Limits" section was updated.	2-31
	The "Recommended Design Practice for VPN/VPP" section was updated.	2-74
v3.1	The datasheet was updated to include references to guidelines concerning the use of certain ProASIC^PLUS I/O standards.	
v3.0	In Table 2-2 • Array Coordinates, the Memory Rows – Bottom coordinates were changed.	2-5
	Figure 2-5 • Core Cell Coordinates for the APA1000 was updated.	2-5
	The V_{IL} Minimum in the Table 2-24 • DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only was changed from 0.3 to –0.3.	2-38
	In the "Output Buffer Delays" section, the OB25LPLL t_{DHL} Standard changed to 5.3.	2-44
	In the "Sample Macrocell Library Listing" section, the AND2 Standard maximum changed to 0.7 and the –F maximum changed to 0.8.	2-51
v2.0	The Table 1 • ProASICPLUS Product Profile was updated.	i
	The "Ordering Information" section was updated.	ii
	The "Plastic Device Resources" section was updated.	ii
	The "ProASIC^PLUS Architecture" section was updated.	1-2
	Table 2-2 • Array Coordinates was updated.	2-5
	Figure 2-5 • Core Cell Coordinates for the APA1000 is new.	2-13
	Figure 2-8 • LVPECL High and Low Threshold Values is new.	2-7
	The Introduction section in the "ProASIC^PLUS Clock Management System" section was updated.	2-10
	The "Physical Implementation" section was updated.	2-10
	The "Functional Description" section was updated.	2-10
	Figure 2-11 • PLL Block – Top-Level View and Detailed PLL Block Diagram through Figure 2-17 • Using the PLL for Clock Deskewing were updated.	2-11 to 2-16
	The "PLL Electrical Specifications" section was updated.	2-18
	Figure 2-22 • Multi-Port Memory Usage was updated.	2-24
	The "Calculating Typical Power Dissipation" section was updated.	2-28
	The "Nominal Supply Voltages' section was updated.	1-34
	The Table 2-24 • DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only was updated.	2-38
	The "Tristate Buffer Delays" section was updated.	2-42
	The "Output Buffer Delays" section was updated.	2-44
	The"Input Buffer Delays" section was updated.	2-46
	"Global Routing Skew" section was updated.	2-50
	The"Sample Macrocell Library Listing" section was updated.	2-51
	The "Pin Description" section was updated.	2-73

Previous version	Changes in current version (v5.9)				Page
v2.0 (continued)	The following pins have been changed in the "100-Pin TQFP" table:				3-1
	Pin Number	**Function**	**Pin Number**	**Function**	
	10	I/O (GLMX1)	60	GL3	
	11	GL1	61	PPECL2 (I/P)	
	13	NPECL1	63	NPECL2	
	15	PPECL1(I/P)	65	GL4	
	16	GL2	66	I/O (GLMX2)	
	"144-Pin TQFP" section is new.				3-3
	The following pins have been changed in the "208-Pin PQFP" table:				3-5
	Pin Number	**Function**	**Pin Number**	**Function**	
	23	I/O (GLMX1)	128	GL3	
	24	GL1	129	PPECL2 (I/P)	
	26	NPECL1	132	NPECL2	
	28	PPECL1 (I/P)	134	GL4	
	30	GL2	135	I/O (GLMX2)	
	The following pins have been changed in the "456-Pin PBGA" table:				3-22
	Pin Number	**Function**	**Pin Number**	**Function**	
	M1	GL1	N22	NPECL2	
	M2	GL2	N23	GL3	
	M22	GL4	N25	I/O (GLMX2)	
	N2	I/O (GLMX1)	P5	NPECL1	
	N4	PPECL1 (I/P)	P26	PPECL2 (I/P)	
	The following pins have been changed in the "144-Pin FBGA" table:				3-37
	Pin Number	**Function**	**Pin Number**	**Function**	
	C2	GL2	F9	GL4	
	D12	I/O (GLMX2	)F11	PPECL2 (I/P	
	E11	NPECL2	F12	GL3	
	F1	GL1	G1	PPECL1 (I/P)	
	F3	I/O (GLMX1)	G4	NPECL1	
	The following pins have been changed in the "256-Pin FBGA" table:				3-40
	Pin Number	**Function**	**Pin Number**	**Function**	
	H1	GL1	H16	GL4	
	H2	NPECL1	J1	GL2	
	H3	I/O (GLMX1)	J2	PPECL1 (I/P)	
	H13	I/O (GLMX2)	J13	PPECL2 (I/P)	
	H14	NPECL2	J16	GL3	
	The following pins have been changed in the "484-Pin FBGA" table:				3-45
	Pin Number	**Function**	**Pin Number**	**Function**	
	L4	GL1	L19	GL4	
	L5	NPECL1	M4	GL2	
	L6	I/O (GLMX1)	M5	PPECL1 (I/P)	
	L16	I/O (GLMX2)	M16	PPECL2 (I/P)	
	L17	NPECL2	M19	GL3	
	The following pins have been changed in the "676-Pin FBGA" table:				3-51
	Pin Number	**Function**	**Pin Number**	**Function**	
	N1	GL1	N25	GL4	
	N3	I/O (GLMX1)	P1	GL2	
	N5	NPECL1	P5	PPECL1 (I/P)	
	N22	GL3	P22	I/O (GLMX2)	
	N24	NPECL2	P24	PPECL2 (I/P)	
	The following pins have been changed in the "896-Pin FBGA" table:				3-59
	Pin Number	**Function**	**Pin Number**	**Function**	
	R2	I/O (GLMX1)	T3	GL2	
	R4	NPECL1	T4	PPECL1 (I/P)	
	R5	GL1	T26	PPECL2 (I/P)	
	R27	NPECL2	T27	GL4	
	R29	I/O (GLMX2)	T28	GL3	

Previous version	Changes in current version (v5.9)	Page
v2.0 (continued)	The following pins have been changed in the "1152-Pin FBGA" table: **Pin Number** / **Function** / **Pin Number** / **Function** U4 / I/O (GLMX1) / U29 / NPECL2 U6 / NPECL1 / U31 / I/O (GLMX2) U7 / GL1 / V28 / PPECL2 (I/P) V5 / GL2 / V29 / GL4 V6 / PPECL1 (I/P) / V30 / GL3	3-69
Advance v0.7	The "ProASIC^PLUS Architecture" section was updated.	1-2
	The "Array Coordinates" section and Table 2-2 • Array Coordinates are new.	2-5
	The "Power-Up Sequencing" section is new.	2-7
	"I/O Features" section was updated.	2-6
	The "Timing Control and Characteristics" section was updated. "Physical Implementation" section, "Functional Description" section, "Lock Signal" section, and "PLL Configuration Options" section are new.	2-10 to 2-13
	"PLL Block – Top-Level View and Detailed PLL Block Diagram" section was updated.	2-11
	Figure 2-12 • Input Connectors to ProASICPLUS Clock Conditioning Circuitry was updated.	2-12
	"Sample Implementations" section, "Adjustable Clock Delay" section, and the "Clock Skew Minimization" section are new.	2-13
	Figure 2-13 • Using the PLL 33 MHz In, 133 MHz Outthrough and Figure 2-17 • Using the PLL for Clock Deskewing are new.	2-14 to 2-16
	The "PLL Electrical Specifications" section is new.	2-18
	The "Design Environment" section was updated.	2-25
	Figure 2-23 • Tristate Buffer Delays was updated.	2-42
	The "Calculating Typical Power Dissipation" section was updated.	2-28
	The "DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V)" section was updated.	2-34
	The Table 2-24 • DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only was updated.	2-38
	The "DC Specifications (3.3 V PCI Operation)1" section was updated.	2-40
	The "Tristate Buffer Delays" section (the figure and table) have been updated.	2-42
	The "Output Buffer Delays" section (the figure and table) have been updated.	2-44
	The "Input Buffer Delays" section was updated.	2-46
	The "Global Input Buffer Delays" section was updated.	2-48
	The "Predicted Global Routing Delay" section was updated.	2-50
	The "Global Routing Skew" section was updated.	2-50
	The "Sample Macrocell Library Listing" section was updated.	2-51
	The "Pin Description" section was updated. GLMX is new.	2-73
	The "Recommended Design Practice for VPN/VPP" section was updated.	2-74
	Pin AK31 of FG1152 for the APA1000 changed to V_{PP}	3-69
Advance v0.6	The "Features and Benefits" section were updated.	i
	The "ProASICPLUS Product Profile" section was updated.	i
	The "Ordering Information" section was updated.	ii
	The "Plastic Device Resources" was updated.	ii
	The "ProASIC^PLUS Architecture" section was updated.	1-2
	Table 2-1 • Clock Spines was updated.	2-4
	Figure 2-11 • PLL Block – Top-Level View and Detailed PLL Block Diagram was updated.	2-11
	The "Design Environment" section was updated.	2-25
	The "Package Thermal Characteristics" section was updated.	2-27

Previous version	Changes in current version (v5.9)	Page
Advance v0.6 (continued)	The "Calculating Typical Power Dissipation" section was updated.	2-28
	The "Absolute Maximum Ratings*" section was updated.	2-31
	The "Programming, Storage, and Operating Limits" section was updated.	2-31
	The "Nominal Supply Voltages' section was updated.	1-34
	The "Recommended Operating Conditions" section was updated.	2-33
	The "DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V)" section was updated.	2-34
	The "DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only" section was updated.	2-38
	The "Synchronous Write and Read to the Same Location" section was updated.	2-61
	The "Asynchronous Write and Synchronous Read to the Same Location" section was updated.	2-62
	The "Asynchronous FIFO Read" section was updated.	2-67
	The "Pin Description" section has been updated.	2-73
	The "Recommended Design Practice for VPN/VPP" section is new.	2-74
	The "100-Pin TQFP" section is new.	3-1
	The "484-Pin FBGA" section is new.	3-45
Advance v0.5	The description for the V_{PN} pin has changed.	2-74
Advance v0.4	The "Plastic Device Resources" section has been updated.	ii
	Figure 2-9 • ProASICPLUS JTAG Boundary Scan Test Logic Circuit and Figure 2-10 • TAP Controller State Diagram have been updated.	2-11
	The "Tristate Buffer Delays" section has been updated.	2-42
	The "Output Buffer Delays" section has been updated.	2-44
	The "Input Buffer Delays" section has been updated.	2-46
	The "Global Input Buffer Delays" section has been updated.	2-48
	The "456-Pin PBGA" section has been updated.	3-22
	The "676-Pin FBGA" section has been updated.	3-51
Advance v0.3	The "ProASICPLUS Product Profile" section has been changed.	i
	The "Plastic Device Resources" section has been updated.	ii
	The "ProASICPLUS I/O Power Supply Voltages" sectionhas been updated.	2-6
	WDATA has ben changed to DI, and RDATA has been changed to DO to make them consistent with the signal names found in the *Macro Library Guide*.	
	Figure 2-18 • Example SRAM Block Diagrams and Figure 2-19 • Basic FIFO Block Diagrams have been updated.	2-22 and 2-23
	The "Design Environment" section and Figure 2-23 • Tristate Buffer Delays have been updated.	2-25 and 2-42
	The table in the "Package Thermal Characteristics" section has been updated.	2-27
	The "Calculating Typical Power Dissipation" section is new.	2-28
	The "Programming, Storage, and Operating Limits" section is new.	2-31
	The "Nominal Supply Voltages' section has been updated.	1-34
	The "DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V)" section was updated.	2-34
	The "DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only" section was updated.	2-38
	The "Recommended Operating Conditions" section was updated.	2-33
	The "ProASIC PLUS Clock Management System" section was updated.	2-10
	Figure 2-11 • PLL Block – Top-Level View and Detailed PLL Block Diagram was updated.	2-11
	Figure 2-10 • TAP Controller State Diagram is new.	2-9
	Tables 5, 6, and 7 from Advanced v0.3 were removed.	

Previous version	Changes in current version (v5.9)	Page
Advance v0.3 (continued)	The "Memory Block SRAM Interface Signals" section was updated.	2-22
	The "Memory Block FIFO Interface Signals" section was updated.	2-23
	All pinout tables have been updated, and several packages are new: 208-Pin PQFP – APA150, APA300, APA450, APA600 456-Pin PBGA – APA150, APA300, APA450, APA600 144-Pin FBGA – APA150, APA300, APA450 256-Pin FBGA – APA150, APA300, APA450, APA600 676-Pin FBGA – APA600	
Advance v0.1	Figure 2-20 • APA1000 Memory Block Architecture has been updated.	2-24

Data Sheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advance

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

Export Administration Regulations (EAR)

The products described in this datasheet are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status datasheet may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.