APDS-9930

Digital Proximity and Ambient Light Sensor

Data Sheet

Description

The APDS-9930 provides digital ambient light sensing (ALS), IR LED and a complete proximity detection system in a single 8 pin package. The proximity function offers plug and play detection to 100 mm (without front glass) thus eliminating the need for factory calibration of the end equipment or sub-assembly. The proximity detection feature operates well from bright sunlight to dark rooms. The wide dynamic range also allows for operation in short distance detection behind dark glass such as a cell phone. In addition, an internal state machine provides the ability to put the device into a low power mode in between ALS and proximity measurements providing very low average power consumption. The ALS provides a *photopic* response to light intensity in very low light condition or behind a dark faceplate.

The APDS-9930 is particularly useful for display management with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Display panel and keyboard backlighting can account for up to 30 to 40 percent of total platform power. The ALS features are ideal for use in notebook PCs, LCD monitors, flat-panel televisions, and cell phones.

The proximity function is targeted specifically towards near field proximity applications. In cell phones, the proximity detection can detect when the user positions the phone close to their ear. The device is fast enough to provide proximity information at a high repetition rate needed when answering a phone call. This provides both improved "green" power saving capability and the added security to lock the computer when the user is not present. The addition of the micro-optics lenses within the module, provide highly efficient transmission and reception of infrared energy which lowers overall power dissipation.

Ordering Information

Part Number	Packaging	Quantity
APDS-9930	Tape & Reel	5000 per reel
APDS-9930-140	Tape & Reel	1000 per reel
APDS-9930-200	Tape & Reel	1000 per reel

Features

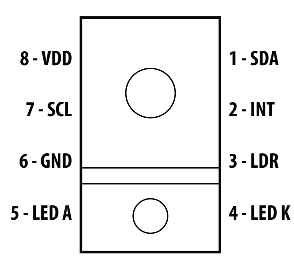
ALS, IR LED and Proximity Detector in an Optical Module

- Ambient Light Sensing (ALS)
  - Approximates Human Eye Response
  - Programmable Interrupt Function with Upper and Lower Threshold
  - Up to 16-Bit Resolution
  - High Sensitivity Operates Behind Darkened Glass
  - Low Lux Performance at 0.01 lux
- Proximity Detection
  - Fully Calibrated to 100 mm Detection
  - Integrated IR LED and Synchronous LED Driver
  - Eliminates "Factory Calibration" of Prox
- Programmable Wait Timer
  - Wait State Power – 90 µA Typical
  - Programmable from 2.7 ms to > 8 sec
- I^2C Interface Compatible
  - Up to 400 kHz (I^2C Fast-Mode)
  - Dedicated Interrupt Pin
- Sleep Mode Power - 2.2 µA Typical
- Small Package L3.94 x W2.36 x H1.35 mm

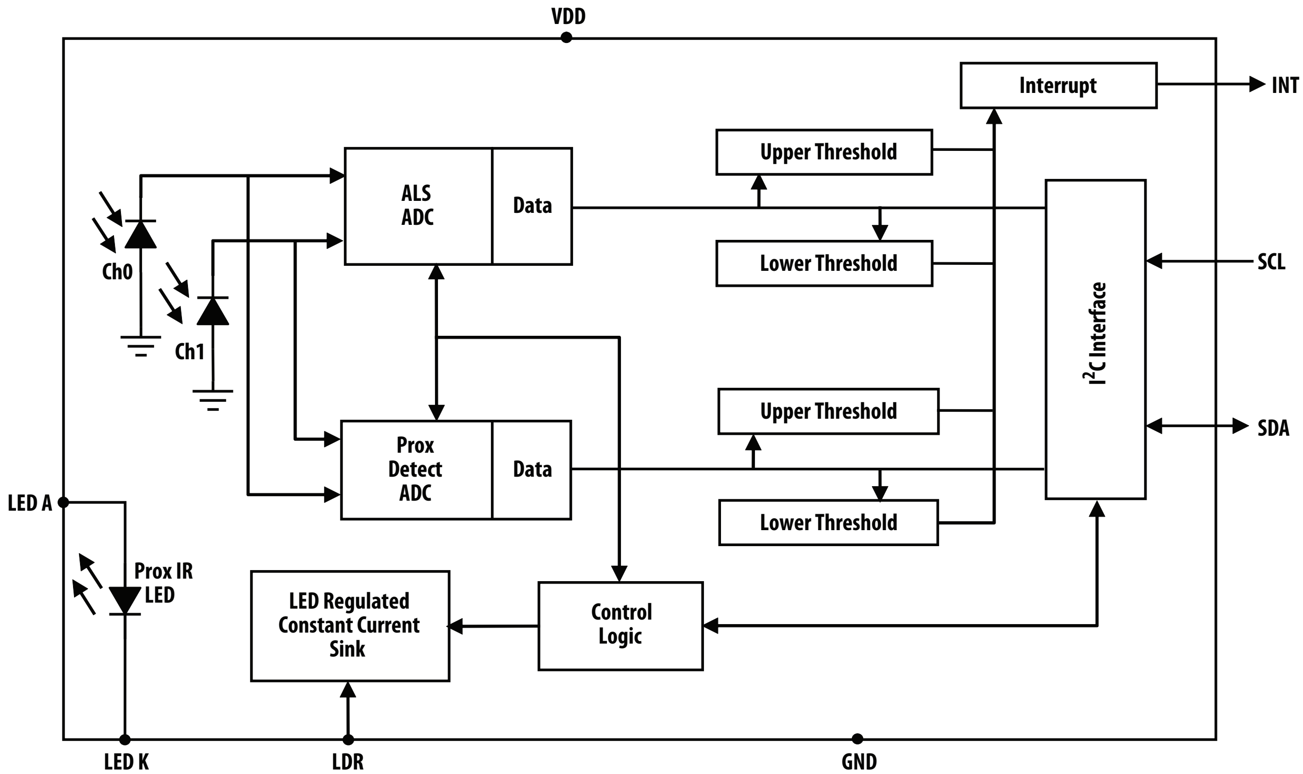
Applications

- Cell Phone Backlight Dimming
- Cell Phone Touch-screen Disable
- Notebook/Monitor Security
- Automatic Speakerphone Enable
- Automatic Menu Pop-up
- Digital Camera Eye Sensor

Package Diagram



Functional Block Diagram



Detailed Description

The APDS-9930 light-to-digital device provides on-chip Ch0 and Ch1 diodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine and an I^{2}C interface. Each device combines one Ch0 photodiode (visible plus infrared) and one Ch1 infrared-responding (IR) photodiode. Two integrating ADCs simultaneously convert the amplified photodiode currents to a digital value providing up to 16-bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the Ch0 and CH1 data registers. This digital output can be read by a microprocessor where the illuminance (ambient light level) in Lux is derived using an empirical formula to approximate the human eye response.

Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I^{2}C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the APDS-9930 device is inherently more immune to noise when compared to an analog interface.

The APDS-9930 provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of an ALS or proximity conversion exceeds either an upper or lower threshold. Additionally, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both ALS and proximity.

Proximity detection is fully provided with an 850 nm IR LED. An internal LED driver (LDR) pin, is jumper connected to the LED cathode (LED K) to provide a factory calibrated proximity of 100 +/- 20 mm. This is accomplished with a proprietary current calibration technique that accounts for all variances in silicon, optics, package and most importantly IR LED output power. This will eliminate or greatly reduce the need for factory calibration that is required for most discrete proximity sensor solutions. While the APDS-9930 is factory calibrated at a given pulse count, the number of proximity LED pulses can be programmed from 1 to 255 pulses, which will allow greater proximity distances to be achieved. Each pulse has a 16 μs period.

I/O Pins Configuration

PIN	NAME	TYPE	DESCRIPTION
1	SDA	I/O	I^2C serial data I/O terminal – serial data I/O for I^2C.
2	INT	O	Interrupt – open drain.
3	LDR	I	LED driver for proximity emitter – up to 100 mA, open drain.
4	LEDK	O	LED Cathode, connect to LDR pin in most systems to use internal LED driver circuit
5	LEDA	I	LED Anode, connect to V_{BATT} on PCB
6	GND		Power supply ground. All voltages are referenced to GND.
7	SCL	I	I^2C serial clock input terminal – clock signal for I^2C serial data.
8	V_{DD}		Power Supply voltage.

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Parameter	Symbol	Min	Max	Units	Test Conditions
Power Supply voltage	V_{DD}		3.8	V	[1]
Digital voltage range		-0.5	3.8	V	
Digital output current	I_O	-1	20	mA	
Storage temperature range	Tstg	-40	85	°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note:

1. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating Ambient Temperature	T_A	-30		85	°C
Supply voltage	V_{DD}	2.2	3.0	3.6	V
Supply Voltage Accuracy, V_{DD} total error including transients		-3		+3	%
LED Supply Voltage	V_{BATT}	2.5		4.5	V

Operating Characteristics, V_{DD} = 3 V, T_A = 25° C (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply current [1]	I_{DD}		195	250	µA	Active (ATIME=0xdb, 100ms)
			90			Wait Mode
			2.2	4.0		Sleep Mode
INT SDA output low voltage	V_{OL}	0		0.4	V	3 mA sink current
		0		0.6		6 mA sink current
Leakage current, SDA, SCL, INT Pins	I_{LEAK}	-5		5	µA	
Leakage current, LDR Pin	I_{LEAK}	-10		10	µA	
SCL, SDA input high voltage	V_{IH}	1.25		VDD	V	
SCL, SDA input low voltage	V_{IL}			0.54	V	

Note:
1. The power consumption is raised by the programmed amount of Proximity LED Drive during the 8 us the LED pulse is on. The nominal and maximum values are shown under Proximity Characteristics. There the I_{DD} supply current is I_{DD} Active + Proximity LED Drive programmed value.

ALS Characteristics, V_{DD} = 3 V, T_A = 25° C, Gain = 16, AEN = 1 , AGL = 0 (unless otherwise noted)

Parameter	Channel	Min	Typ	Max	Units	Test Conditions
Dark ALS ADC count value	Ch0	0	1	5	counts	Ee = 0, AGAIN = 120x, ATIME = 0xDB(100ms)
	Ch1	0	1	5		
ALS ADC Integration Time Step Size		2.58	2.73	2.90	ms	ATIME = 0xff
ALS ADC Number of Integration Steps		1		256	steps	
Full Scale ADC Counts per Step				1023	counts	
Full scale ADC count value				65535	counts	ATIME = 0xC0
ALS ADC count value	Ch0	4000	5000	6000	counts	λp = 625 nm, Ee = 46.8 µW/cm2, ATIME = 0xF6 (27 ms), Note 2
	Ch1		950			
	Ch0	4000	5000	6000		λp = 850 nm, Ee = 61.7 µW/cm2, ATIME = 0xF6 (27 ms), Note 3
	Ch1		2900			
ALS ADC count value ratio: Ch1/Ch0		15.2	19.0	22.8	%	λp = 625 nm, ATIME = 0xF6 (27 ms)
		43	58	73		λp = 850 nm, ATIME = 0xF6 (27 ms)
Gain scaling, relative to 1x gain setting		7.2	8.0	8.8		AGAIN = 8×
		14.4	16.0	17.6		AGAIN = 16×
		108	120	132		AGAIN = 120×

Notes:
1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Red 625 nm LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The 625 nm irradiance Ee is supplied by an AlInGaP light-emitting diode with the following characteristics: peak wavelength = 625 nm and spectral halfwidth ½ = 20 nm.
3. The 850 nm irradiance Ee is supplied by a GaAs light-emitting diode with the following characteristics: peak wavelength = 850 nm and spectral halfwidth ½ = 42 nm.

Proximity Characteristics, V_{DD} = 3 V, T_A = 25° C, PGAIN = 1, PEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
I_{DD} Supply current – LDR Pulse On		3		mA	
ADC Conversion Time Step Size	2.58	2.73	2.9	ms	PTIME = 0xff
ADC Number of Integration Steps		1		steps	PTIME = 0xff
Full Scale ADC Counts			1023	counts	PTIME = 0xff
Proximity IR LED Pulse Count	0		255	pulses	
Proximity Pulse Period		16.0		µs	
Proximity Pulse – LED On Time		7.3		µs	
Proximity LED Drive		100		mA	PDRIVE = 0; I_{SINK} Sink current @ 600 mV, LDR Pin
		50			PDRIVE = 1
		25			PDRIVE = 2
		12.5			PDRIVE = 3
Proximity ADC count value, no object		100	200	counts	Dedicated power supply VBatt = 3 V LED driving 8 pulses, PDRIVE = 00, PGAIN = 10, open view (no glass) and no reflective object above the module. [1]
Proximity ADC count value, 100 mm distance object	450	520	590	counts	Reflecting object – 73 mm x 83 mm Kodak 90% grey card, 100 mm distance, LED driving 8 pulses, PDRIVE = 00, PGAIN = 10, open view (no glass) above the module. Tested value is the average of 5 consecutive readings. [1]

Note:
1. 100 mA and 8 pulses are the recommended driving conditions. For other driving conditions, contact Avago Field Sales.

IR LED Characteristics, V_{DD} = 3 V, T_A = 25C

Parameter	Min	Typ	Max	Units	Test Conditions
Peak Wavelength, λ_P		850		nm	I_F = 20 mA
Spectrum Width, Half Power, $\Delta\lambda$		40		nm	I_F = 20 mA
Optical Rise Time, T_R		20		ns	I_{FP} = 100 mA
Optical Fall Time, T_F		20		ns	I_{FP} = 100 mA

Wait Characteristics, V_{DD} = 3 V, T_A = 25° C, Gain = 16, WEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Wait Step Size		2.73	2.9	ms	WTIME = 0xff
Wait Number of Step	1		256	steps	

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted) *

Parameter	Symbol	Min.	Max.	Unit
Clock frequency (I²C-bus only)	f_{SCL}	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t_{HDSTA}	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	µs
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	µs
Data hold time	$t_{HD;DAT}$	60	–	ns
Data set-up time	$t_{SU;DAT}$	100	–	ns
LOW period of the SCL clock	t_{LOW}	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	–	µs
Clock/data fall time	t_f	20	300	ns
Clock/data rise time	t_r	20	300	ns
Input pin capacitance	C_i	–	10	pF

* Specified by design and characterization; not production tested.

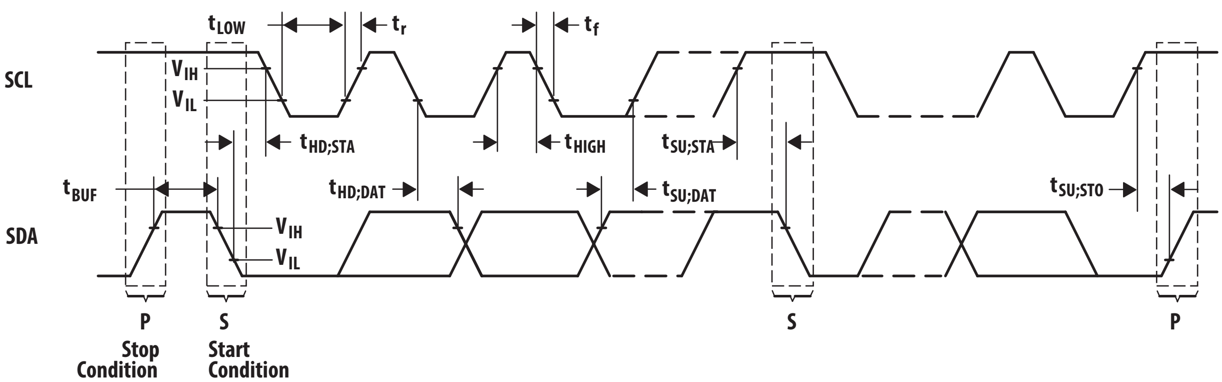


Figure 1. I²C Bus Timing Diagram

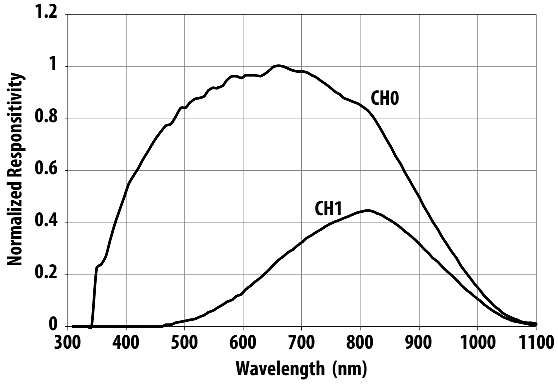


Figure 2. Spectral Response

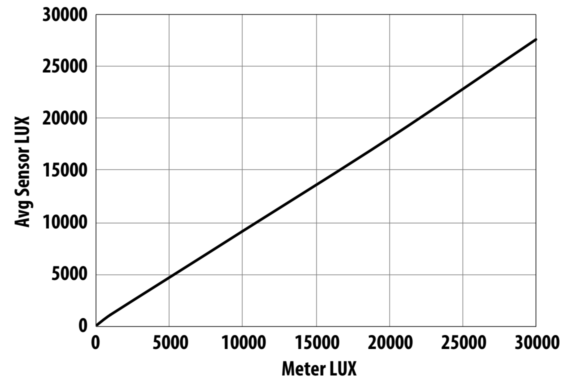


Figure 3a. ALS Sensor LUX vs. Meter LUX using White Light

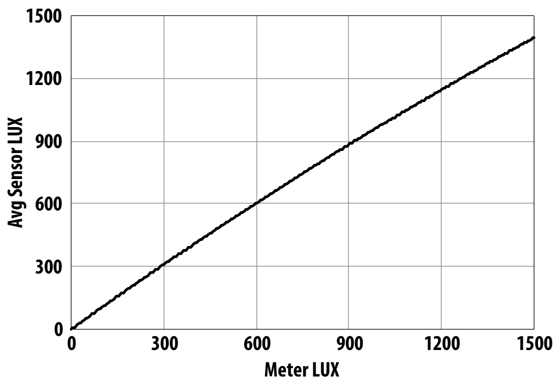


Figure 3b. ALS Sensor LUX vs. Meter LUX using Incandescent Light

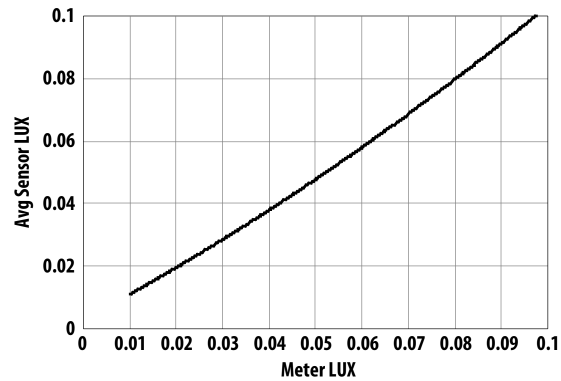


Figure 3c. ALS Sensor LUX vs. Meter LUX using Low Lux White Light

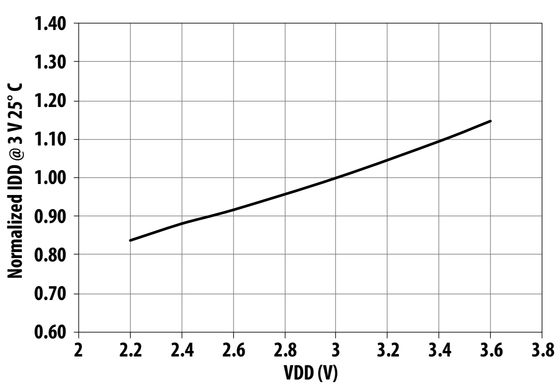


Figure 4a. Normalized IDD vs. VDD

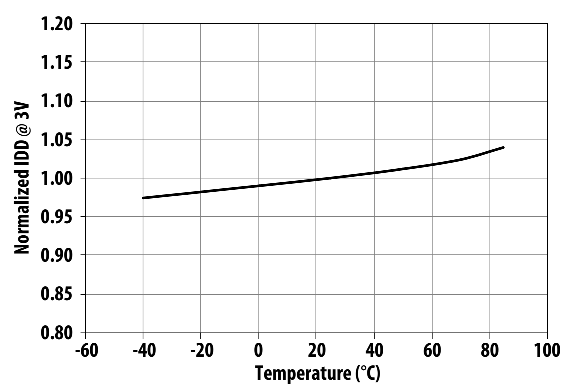


Figure 4b. Normalized IDD vs. Temperature

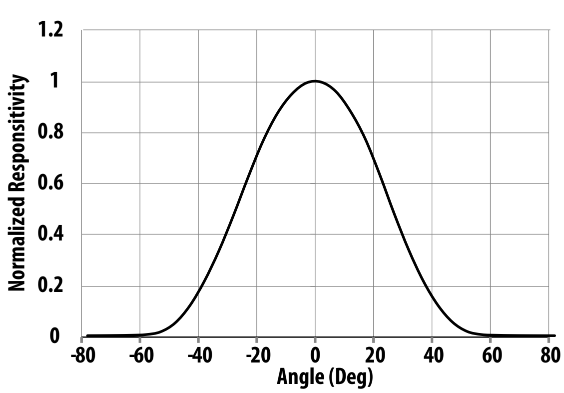


Figure 5a. Normalized PD Responsitivity vs. Angular Displacement

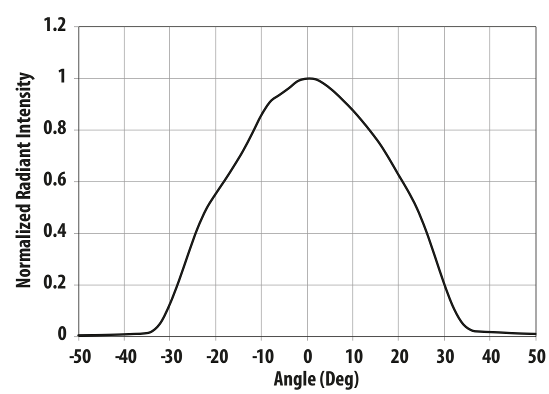


Figure 5b. Normalized LED Angular Emitting Profile

PRINCIPLES OF OPERATION

System State Machine

An internal state machine provides system control of the ALS, proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I2C bus, the device transitions to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a proximity or ALS function is enabled. Once enabled, the device will execute the Prox, Wait, and ALS states in sequence as indicated in Figure 6. Upon completion and return to Idle, the device will automatically begin a new prox–wait–ALS cycle as long as PON and either PEN or AEN remain enabled.

If the Prox or ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I2C command is received.

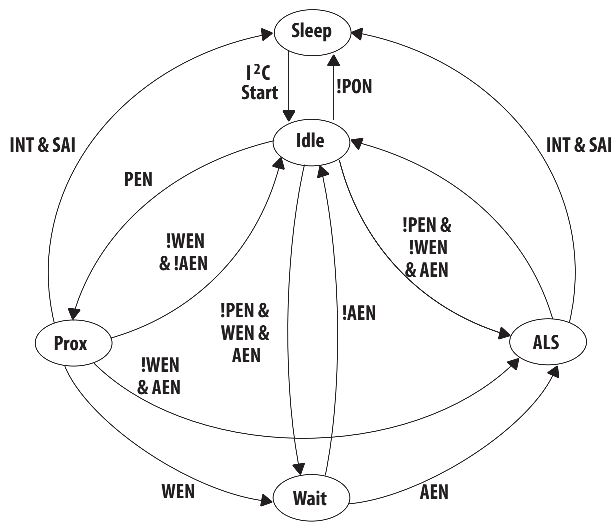


Figure 6. Simplified State Diagram

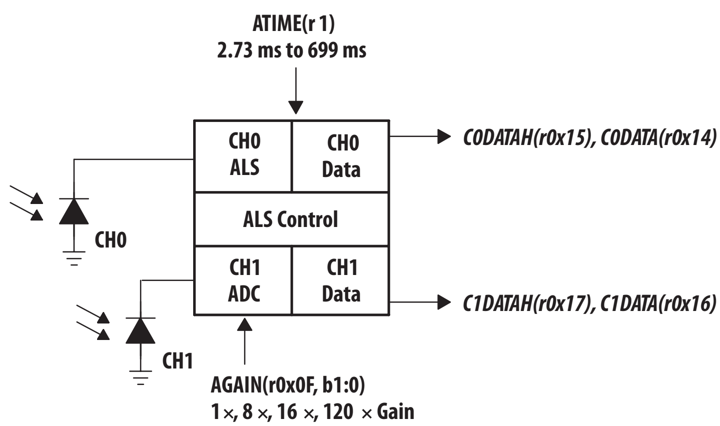


Figure 7. ALS Operation

Photodiodes

Conventional silicon detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high (such as with incandescent lighting) due to the difference between the silicon detector response and the brightness perceived by the human eye.

This problem is overcome in the APDS-9930 through the use of two photodiodes. One of the photodiodes, referred to as the Ch0 channel, is sensitive to both visible and infrared light while the second photodiode is sensitive primarily to infrared light. Two integrating ADCs convert the photodiode currents to digital outputs. The CH1DATA digital value is used to compensate for the effect of the infrared component of light on the CH0DATA digital value. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in units of Lux.

ALS Operation

The ALS engine contains ALS gain control (AGAIN) and two integrating analog-to-digital converters (ADC) for the Ch0 and Ch1 photodiodes. The ALS integration time (ALSIT) impacts both the resolution and the sensitivity of the ALS reading. Integration of both channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the Ch0 and CH1 data registers (Ch0DATAx and Ch1DATAx). This data is also referred to as channel "count". The transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically moves to the next state in accordance with the configured state machine.

The ALS Timing register value (ATIME) for programming the integration time (ALSIT) is a 2's complement values. The ALS Timing register value can be calculated as follows:

ATIME = 256 – ALSIT / 2.73 ms

Inversely, the integration time can be calculated from the register value as follows:

ALSIT = 2.73 ms * (256 – ATIME)

In order to reject 50/60-Hz ripple strongly present in fluorescent lighting, the integration time needs to be programmed in multiples of 10 / 8.3 ms or the half cycle time. Both frequencies can be rejected with a programmed value of 50 ms (ATIME = 0xED) or multiples of 50 ms (i.e. 100, 150, 200, 400, 600).

The registers for programming the AGAIN hold a two-bit value representing a gain of 1×, 8×, 16×, or 120×. The gain, in terms of amount of gain, will be represented by the value AGAINx, i.e. AGAINx = 1, 8, 16, or 120. With the AGL bit set, the gains will be lowered to 1/6, 8/6, 16/6, and 20×, allowing for up to 30k lux.

Calculating ALS Lux

Definition:

CH0DATA = 256 * Ch0DATAH (r0x15) + Ch0DATAL (r0x14)
CH1DATA = 256 * Ch1DATAH (r0x17) + Ch1DATAL (r0x16)
IAC = IR Adjusted Count
LPC = Lux per Count
ALSIT = ALS Integration Time (ms)
AGAIN = ALS Gain
DF = Device Factor, DF = 52 for APDS-9930
GA = Glass (or Lens) Attenuation Factor
B, C, D – Coefficients

Lux Equation:

IAC1 = CH0DATA – B x CH1DATA
IAC2 = C x CH0DATA – D x CH1DATA
IAC = Max (IAC1, IAC2, 0)
LPC = GA x DF / (ALSIT × AGAIN)
Lux = IAC x LPC

Coefficients in open air:

GA = 0.49
B = 1.862
C = 0.746
D = 1.291

Sample Lux Calculation in Open Air

Assume the following constants:

ALSIT = 400
AGAIN = 1
LPC = GA x DF / (ALSIT × AGAIN)
LPC = 0.49 x 52 / (400 x 1)
LPC = 0.06

Assume the following measurements:

CH0DATA = 5000
CH1DATA = 525
Then:
IAC1 = 5000 – 1.862 x 525 = 4022
IAC2 = 0.746 x 5000 – 1.291 x 525 = 3052
IAC = Max (4022, 3052, 0) = 4022

Lux:

Lux = IAC X LPC
Lux = 4022 X 0.06
Lux = 256

Note: please refer to application note for coefficient GA, B, C and D calculation with window.

Proximity Detection

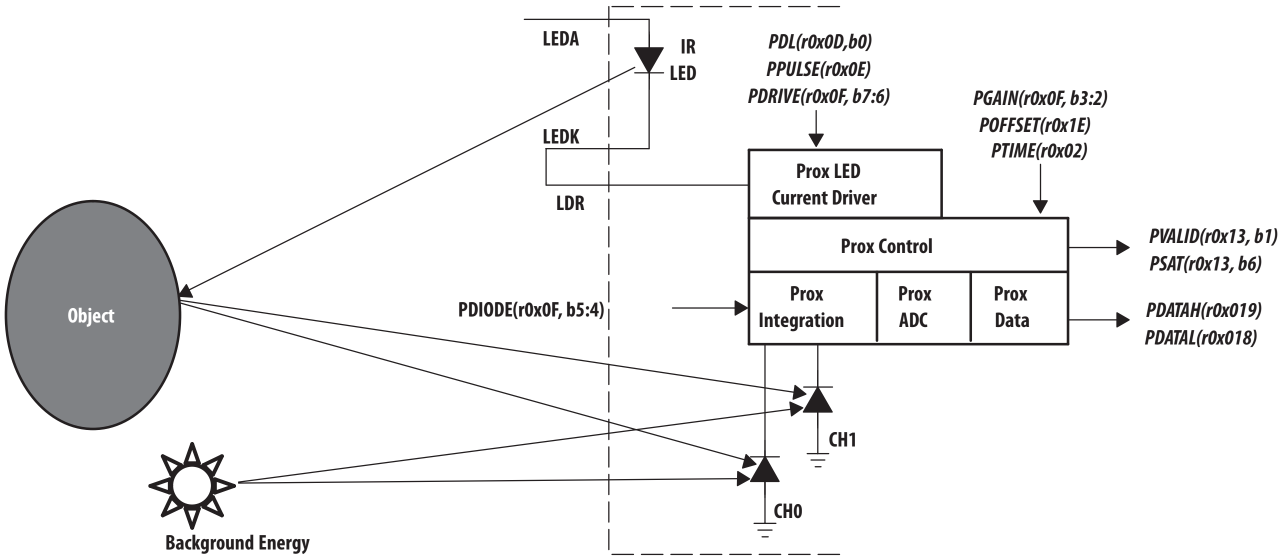


Figure 8. Proximity Detection

Proximity detection is accomplished by measuring the amount of IR energy, from the internal IR LED, reflected off an object to determine its distance. The internal proximity IR LED is driven by the integrated proximity LED current driver as shown in Figure 8.

The LED current driver, output on the LDR terminal, provides a regulated current sink that eliminates the need for an external current limiting resistor. The combination of proximity LED drive strength (PDRIVE) and proximity drive level (PDL) determine the drive current. PDRIVE sets the drive current to 100 mA, 50 mA, 25 mA, or 12.5 mA when PDL is not asserted. However, when PDL is asserted, the drive current is reduced by a factor of 9.

Referring to the Detailed State Machine figure, the LED current driver pulses the IR LED as shown in Figure 9 during the Prox Accum state. Figure 9 also illustrates that the LED On pulse has a fixed width of 7.3 µs and period of 16.0 µs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

Figure 8 illustrates light rays emitting from the internal IR LED, reflecting off an object, and being absorbed by the CH1 photodiodes. The proximity diode selector (PDIODE) selects Ch1 diode for a given proximity measurement. Note that PDIODE must be set for proximity detection to work.

Referring again to Figure 9, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the IR LED energy to accumulate from pulse to pulse. The proximity gain (PGAIN) determines the integration rate, which can be programmed to 1×, 2×, 4×, or 8× gain. At power up, PGAIN defaults to 1× gain, which is recommended for most applications. For reference, PGAIN equal to 4× is comparable to the APDS-9900's 1× gain setting. During LED On time integration, the proximity saturation bit in the Status register (0x13) will be set if the integrator saturates. This condition can occur if the proximity gain is set too high for the lighting conditions, such as in the presence of bright sunlight. Once asserted, PSAT will remain set until a special function proximity interrupt clear command is received from the host (see command register).

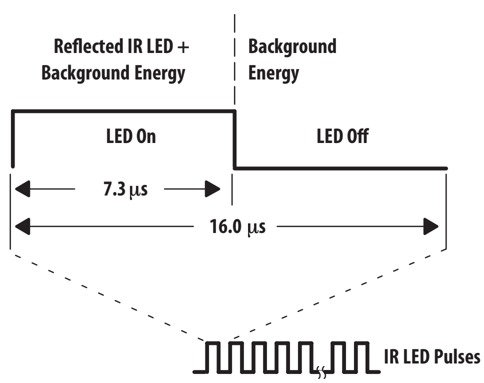


Figure 9. Proximity LED Current Driver Waveform

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which is programmable from 1 to 256 2.73-ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.73 ms ADC conversion time (0xFF).

In many practical proximity applications, a number of optical system and environmental conditions can produce an offset in the proximity measurement result. To counter these effects, a proximity offset (POFFSET) is provided which allows the proximity data to be shifted positive or negative.

Once the first proximity cycle has completed, the proximity valid (PVALID) bit in the Status register will be set and remain set until the proximity detection function is disabled (PEN).

Optical Design Considerations

The APDS-9930 simplifies the optical system design by eliminating the need for light pipes and improves system optical efficiency by providing apertures and package shielding which will reduce crosstalk when placed in the final system. By reducing the IR LED to glass surface crosstalk, proximity performance is greatly improved and enables a wide range of cell phone applications utilizing the APDS-9930. The module package design has been optimized for minimum package foot print and short distance proximity of 100 mm typical. The spacing between the glass surface and package top surface is critical to controlling the crosstalk. If the package to top surface spacing gap, window thickness and transmittance are met, there should be no need to add additional components (such as a barrier) between the LED and photodiode. Thus with some simple mechanical design implementations, the APDS-9930 will perform well in the end equipment system.

APDS-9930 Module Optimized design parameters:

- Window thickness, t ≤ 1.0 mm
- Air gap, g ≤ 1.0 mm [1]
- Assuming window IR transmittance 90%

Note:

1. Applications with an air gap from 0.5 mm to 1.0 mm are recommended to use Poffset Register (0x1E) in their factory calibration.

The APDS-9930 is available in a low profile package that contains optics that provide optical gain on both the LED and the sensor side of the package. The device has a package Z height of 1.35 mm and will support an air gap of ≤ 1.0 mm between the glass and the package. The assumption of the optical system level design is that glass surface above the module is ≤ 1.0 mm.

By integrating the micro-optics in the package, the IR energy emitted can be reduced thus conserving the precious battery life in the application.

The system designer can optimize his designs for slim form factor Z height as well as improve the proximity sensing, save battery power, and disable the touch screen in a cellular phone.

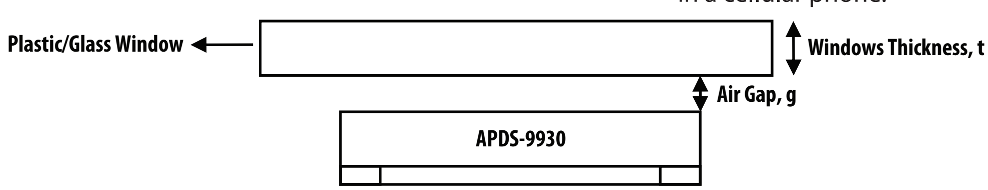


Figure 10. Proximity Detection

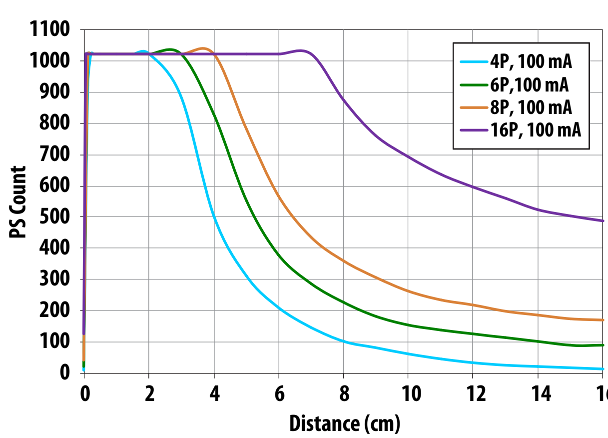


Figure 11a. PS Output vs. Distance at 100 mA, PGAIN = 10, at various Pulse Count. No glass in front of the module, 18% Kodak Grey Card.

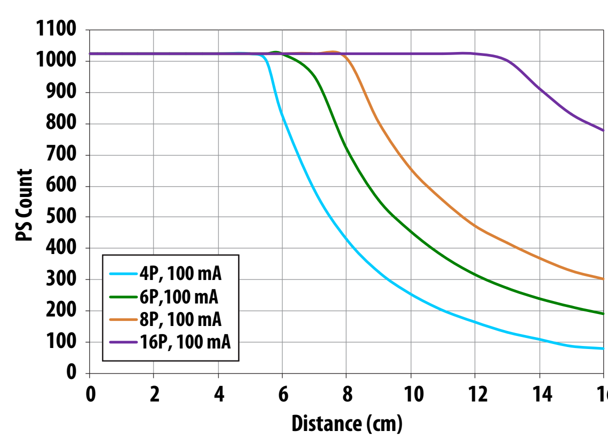


Figure 11b. PS Output vs. Distance at 100 mA, PGAIN = 10, at various Pulse Count. No glass in front of the module, 90% Kodak Grey Card.

Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity or proximity values outside of a user-defined range. While the interrupt function is always enabled and its status is available in the status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) or ALS interrupt enable (AIEN) fields in the enable register (0x00).

Four 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level and proximity range. An interrupt can be generated when the ALS CH0 data (Ch0DATA) falls outside of the desired light level range, as determined by the values in the ALS interrupt low threshold registers (AILTx) and ALS interrupt high threshold registers (AIHTx). Likewise, an out-of-range proximity interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range ALS or proximity occurrences before an interrupt is generated. The persistence filter register (0x0C) allows the user to set the ALS persistence filter (APERS) and the proximity persistence filter (PPERS) values. See the persistence filter register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see command register).

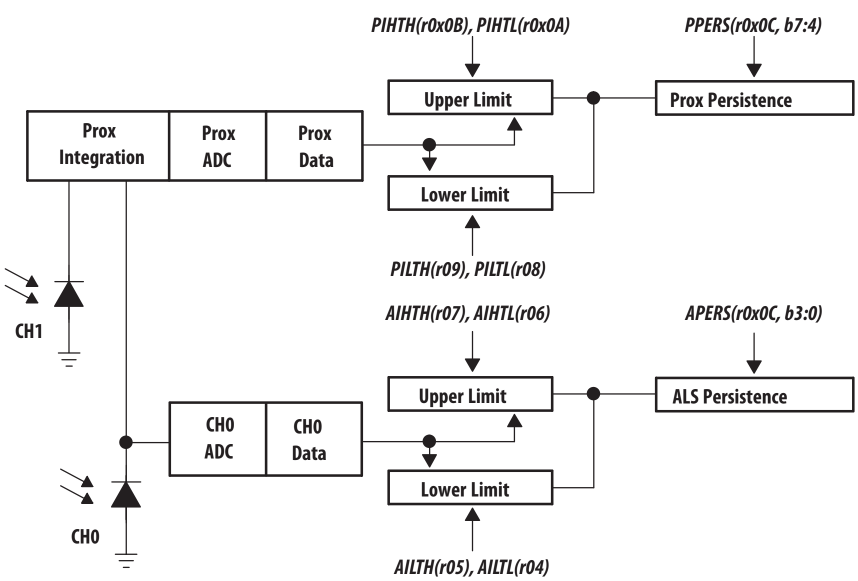


Figure 12. Programmable Interrupt

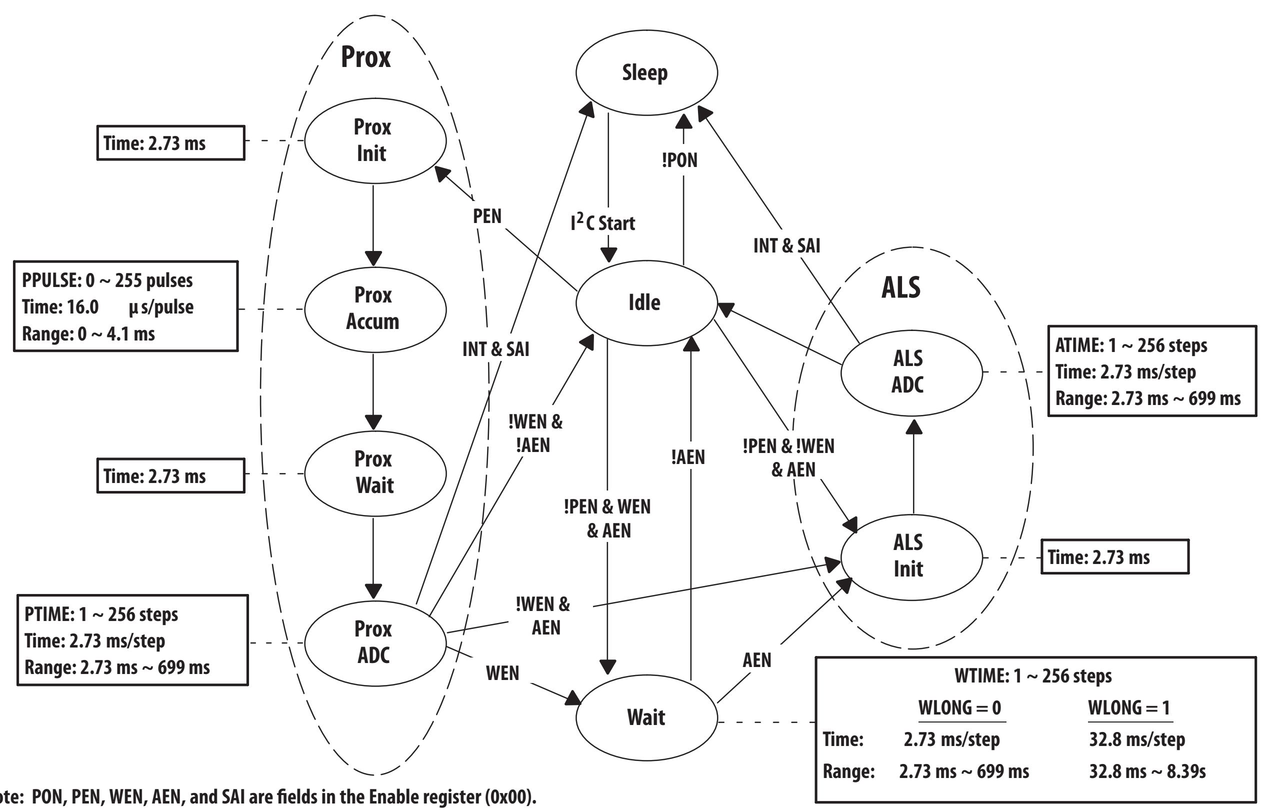
State Diagram

The system state machine shown in Figure 6 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing. Upon VDD power on, it is recommended to wait at least 4.5ms before issuing the I2C command.

When the proximity detection feature is enabled (PEN), the state machine transitions through the Prox Init, Prox Accum, Prox Wait, and Prox ADC states. The Prox Init and Prox Wait times are a fixed 2.73 ms, whereas the Prox Accum time is determined by the number of proximity LED pulses (PPULSE) and the Prox ADC time is determined by the integration time (PTIME). The formulas to determine the Prox Accum and Prox ADC times are given in the associated boxes in Figure 13. If an interrupt is generated as a result of the proximity cycle, it will be asserted at the end of the Prox ADC state and transition to the Sleep state if SAI is enabled.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 13.

When the ALS feature is enabled (AEN), the state machine will transition through the ALS Init and ALS ADC states. The ALS Init state takes 2.73 ms, while the ALS ADC time is dependent on the integration time (ATIME). The formula to determine ALS ADC time is given in the associated box in Figure 13. If an interrupt is generated as a result of the ALS cycle, it will be asserted at the end of the ALS ADC state and transition to the Sleep state if SAI is enabled.



Note: PON, PEN, WEN, AEN, and SAI are fields in the Enable register (0x00).

Figure 13. Extended State Diagram

Power Management

Power consumption can be managed with the Wait state, because the Wait state typically consumes only 90 µA of IDD current. An example of the power management feature is given below. With the assumptions provided in the example, average IDD is estimated to be 176 µA.

Power Management

SYSTEM STATE MACHINE STATE	PROGRAMMABLE PARAMETER	PROGRAMMED VALUE	DURATION	TYPICAL CURRENT
Prox Init			2.73 ms	0.195 mA
Prox Accum	PPULSE	0x04	0.064 ms	
Prox Accum – LED On			0.029 ms (Note 1)	103 mA
Prox Accum – LED OFF			0.035 ms (Note 2)	0.195 mA
Prox Wait			2.73 ms	0.195 mA
Prox ADC	PTIME	0xFF	2.73 ms	0.195 mA
Wait	WTIME WLONG	0xEE 0	49.2 ms	0.090 mA
ALS Init			2.73 ms	0.195 mA
ALS ADC	ATIME	0xEE	49.2 ms	0.195 mA

Notes:
1. Prox Accum – LED On time = 7.3 µs per pulse × 4 pulses = 29.3µs = 0.029 ms
2. Prox Accum – LED Off time = 8.7 µs per pulse × 4 pulses = 34.7µs = 0.035 ms

Average IDD Current = ((0.029 × 103) + (0.035 x 0.195) + (2.73 × 0.195) + (49.2 × 0.090) + (49.2 × 0.195) + (2.73 × 0.195 × 3)) / 109 = 176 µA

Keeping with the same programmed values as per the example, the table below shows how the average IDD current is affected by the Wait state time, which is determined by WEN, WTIME, and WLONG. Note that the worst-case current occurs when the Wait state is not enabled.

Average IDD Current

WEN	WTIME	WLONG	WAIT STATE	AVERAGE IDD CURRENT
0	n/a	n/a	0 ms	245 µA
1	0xFF	0	2.73 ms	238 µA
1	0xEE	0	49.2 ms	176 µA
1	0x00	0	699 ms	103 µA
1	0x00	1	8389 ms	92 µA

Basic Software Operation

The following pseudo-code shows how to do basic initialization of the APDS-9930.

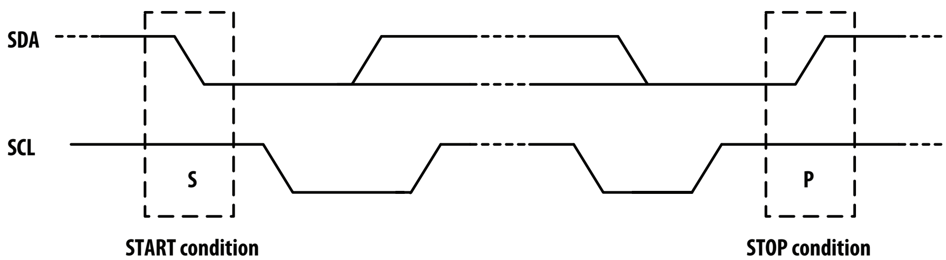
```
uint8 ATIME, PIME, WTIME, PPULSE;
ATIME = 0xff; // 2.7 ms – minimum ALS integration time
WTIME = 0xff; // 2.7 ms – minimum Wait time
PTIME = 0xff; // 2.7 ms – minimum Prox integration time
PPULSE = 1; // Minimum prox pulse count

WriteRegData(0, 0); //Disable and Powerdown
WriteRegData (1, ATIME);
WriteRegData (2, PTIME);
WriteRegData (3, WTIME);
WriteRegData (0xe, PPULSE);

uint8 PDRIVE, PDIODE, PGAIN, AGAIN;
PDRIVE = 0; //100mA of LED Power
PDIODE = 0x20; // CH1 Diode
PGAIN = 0; //1x Prox gain
AGAIN = 0; //1x ALS gain

WriteRegData (0xf, PDRIVE | PDIODE | PGAIN | AGAIN);

uint8 WEN, PEN, AEN, PON;
WEN = 8; // Enable Wait
PEN = 4; // Enable Prox
AEN = 2; // Enable ALS
PON = 1; // Enable Power On
WriteRegData (0, WEN | PEN | AEN | PON); // WriteRegData(0,0x0f);

Wait(12); //Wait for 12 ms

int CH0_data, CH1_data, Prox_data;

CH0_data = Read_Word(0x14);
CH1_data = Read_Word(0x16);
Prox_data = Read_Word(0x18);

WriteRegData(uint8 reg, uint8 data)
{
    m_I2CBus.WriteI2C(0x39, 0x80 | reg, 1, &data);
}

uint16 Read_Word(uint8 reg);
{
    uint8 barr[2];
    m_I2CBus.ReadI2C(0x39, 0xA0 | reg, 2, ref barr);
    return (uint16)(barr[0] + 256 * barr[1]);
}
```

I^{2}C Protocol

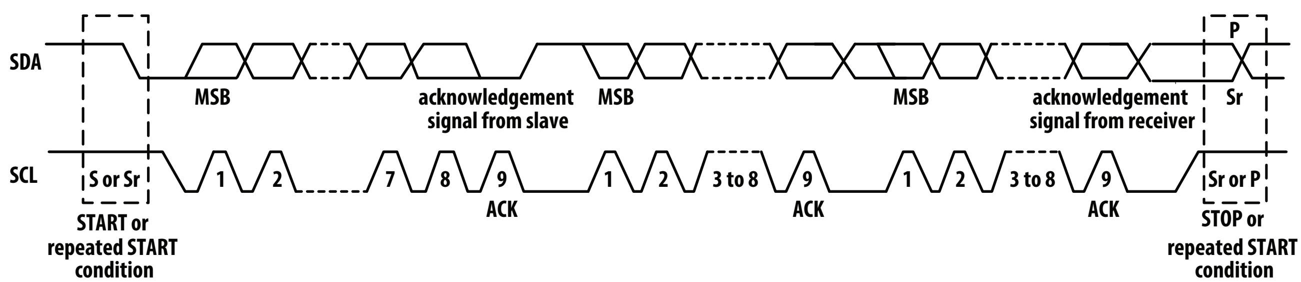
Interface and control of the APDS-9930 is accomplished through an I^{2}C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x39 hex using 7 bit addressing protocol. (Contact factory for other addressing options.)

The I^{2}C standard provides for three types of bus transaction: read, write and a combined protocol. During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5 bit register address. The control commands can also be used to clear interrupts. For a complete description of I^{2}C protocols, please review the I^{2}C Specification at: http://www.NXP.com

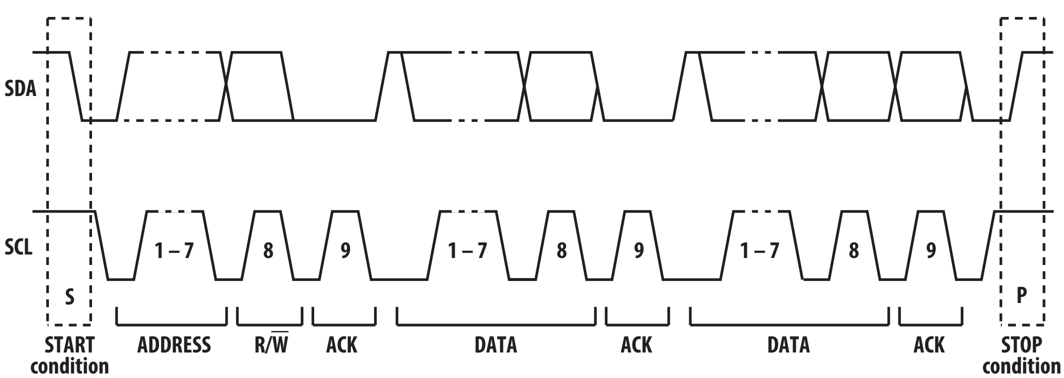
Start and Stop conditions



Data transfer on I^{2}C-bus



A complete data transfer



A	Acknowledge (0)
N	Not Acknowledged (1)
P	Stop Condition
R	Read (1)
S	Start Condition
Sr	Repeated Start Condition
W	Write (0)
…	Continuation of protocol
(white box)	Master-to-Slave
(grey box)	Slave-to-Master

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data	A	P

I^2C Write Protocol

1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	P

I^2C Write Protocol (Clear Interrupt)

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Low	A	Data High	A	P

I^2C Write Word Protocol

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	Sr	Slave Address	R	A	Data	N	P

I^2C Read Protocol – Combined Format

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	W	A	Command Code	A	Sr	Slave Address	R	A	Data Low	A

8	1	1
Data High	N	P

I^2C Read Word Protocol

Register Set

The APDS-9930 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

ADDRESS	RESISTER NAME	R/W	REGISTER FUNCTION	Reset Value
–	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enable of states and interrupts	0x00
0x01	ATIME	R/W	ALS ADC time	0xFF
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x05	AILTH	R/W	ALS interrupt low threshold hi byte	0x00
0x06	AIHTL	R/W	ALS interrupt hi threshold low byte	0x00
0x07	AIHTL	R/W	ALS interrupt hi threshold hi byte	0x00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold hi byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt hi threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt hi threshold hi byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Gain control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	Ch0DATAL	R	Ch0 ADC low data register	0x00
0x15	Ch0DATAH	R	Ch0 ADC high data register	0x00
0x16	Ch1DATAL	R	Ch1 ADC low data register	0x00
0x17	Ch1DATAH	R	Ch1 ADC high data register	0x00
0x18	PDATAL	R	Proximity ADC low data register	0x00
0x19	PDATAH	R	Proximity ADC high data register	0x00
0x1E	POFFSET	R/W	Proximity offset register	--

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

	7	6	5	4	3	2	1	0	
COMMAND	CMD	TYPE		ADD					–

FIELD	BITS	DESCRIPTION
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:

FIELD VALUE	INTEGRATION TIME
00	Repeated Byte protocol transaction
01	Auto-Increment protocol transaction
10	Reserved – Do not use
11	Special function – See description below

Byte protocol will repeatedly read the same register with each data access.
Block protocol will provide auto-increment function to read successive bytes.

FIELD	BITS	DESCRIPTION
ADD	4:0	Address register/special function register. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write or read transactions:

FIELD VALUE	READ VALUE
00000	Normal – no action
00101	Proximity interrupt clear
00110	ALS interrupt clear
00111	Proximity and ALS interrupt clear
other	Reserved – Do not write

ALS/Proximity Interrupt Clear. Clears any pending ALS/Proximity interrupt. This special function is self clearing.

Enable Register (0x00)

The ENABLE register is used primarily to power the APDS-9930 device on/off, enable functions, and interrupts.

	7	6	5	4	3	2	1	0	Address
ENABLE	Reserved	SAI	PIEN	AIEN	WEN	PEN	AEN	PON	0x00

FIELD	BITS	DESCRIPTION
Reserved	7	Reserved. Write as 0.
SAI	6	Sleep after interrupt. When asserted, the device will power down at the end of a proximity or ALS cycle if an interrupt has been generated.
PIEN	5	Proximity Interrupt Mask. When asserted, permits proximity interrupts to be generated.
AIEN	4	ALS Interrupt Mask. When asserted, permits ALS interrupt to be generated.
WEN	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity Enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	ALS Enable. This bit actives the two channel ADC. Writing a 1 activates the ALS. Writing a 0 disables the ALS.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

ALS Timing Register (0x01)

The ALS timing register controls the integration time of the ALS Ch0 and Ch1 channel ADCs in 2.73 ms increments.

FIELD	BITS	DESCRIPTION			
ATIME	7:0	VALUE	CYCLES	TIME (ALSIT)	Max Count
		0xff	1	2.73 ms	1023
		0xf6	10	27.3 ms	10239
		0xdb	37	101 ms	37887
		0xc0	64	175 ms	65535
		0x00	256	699 ms	65535

Proximity Time Control Register (0x02)

The proximity timing register controls the integration time of the proximity ADC in 2.73 ms increments. It is recommended that this register be programmed to a value of 0xff (1 cycle, 1023 bits).

FIELD	BITS	DESCRIPTION			
PTIME	7:0	VALUE	CYCLES	TIME	Max Count
		0xff	1	2.73 ms	1023

Wait Time Register (0x03)

Wait time is set 2.73 ms increments unless the WLONG bit is asserted in which case the wait times are 12x longer. WTIME is programmed as a 2's complement number.

FIELD	BITS	DESCRIPTION			
WTIME	7:0	REGISTER VALUE	WALL TIME	TIME (WLONG = 0)	TIME (WLONG = 1)
		0xff	1	2.73 ms	0.033 sec
		0xb6	74	202 ms	2.4 sec
		0x00	256	699 ms	8.4 sec

Note. The Proximity Wait Time Register should be configured before PEN and/or AEN is/are asserted.

ALS Interrupt Threshold Register (0x04 – 0x07)

The ALS interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If Ch0 channel data crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

REGISTER	ADDRESS	BITS	DESCRIPTION
AILTL	0x04	7:0	ALS Ch0 channel low threshold lower byte
AILTH	0x05	7:0	ALS Ch0 channel low threshold upper byte
AIHTL	0x06	7:0	ALS Ch0 channel high threshold lower byte
AIHTH	0x07	7:0	ALS Ch0 channel high threshold upper byte

Proximity Interrupt Threshold Register (0x08 – 0x0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity ADC channel low threshold lower byte
PILTH	0x09	7:0	Proximity ADC channel low threshold upper byte
PIHTL	0x0A	7:0	Proximity ADC channel high threshold lower byte
PIHTH	0x0B	7:0	Proximity ADC channel high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time. Separate filtering is provided for proximity and ALS functions.

ALS interrupts are generated by looking only at the ADC integration results of channel 0.

	7	6	5	4	3	2	1	0	
PERS	PPERS				APERS				0x0c

FIELD	BITS	DESCRIPTION		
PPERS	7:4	Proximity interrupt persistence. Controls rate of proximity interrupt to the host processor.		
		FIELD VALUE	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every	Every proximity cycle generates an interrupt
		0001	1	1 consecutive proximity values out of range
		…	…	…
		1111	15	15 consecutive proximity values out of range
APERS	3:0	Interrupt persistence. Controls rate of interrupt to the host processor.		
		FIELD VALUE	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every	Every ALS cycle generates an interrupt
		0001	1	1 consecutive Ch0 channel values out of range
		0010	2	2 consecutive Ch0 channel values out of range
		0011	3	3 consecutive Ch0 channel values out of range
		0100	5	5 consecutive Ch0 channel values out of range
		0101	10	10 consecutive Ch0 channel values out of range
		0110	15	15 consecutive Ch0 channel values out of range
		0111	20	20 consecutive Ch0 channel values out of range
		1000	25	25 consecutive Ch0 channel values out of range
		1001	30	30 consecutive Ch0 channel values out of range
		1010	35	35 consecutive Ch0 channel values out of range
		1011	40	40 consecutive Ch0 channel values out of range
		1100	45	45 consecutive Ch0 channel values out of range
		1101	50	50 consecutive Ch0 channel values out of range
		1110	55	55 consecutive Ch0 channel values out of range
		1111	60	60 consecutive Ch0 channel values out of range

Configuration Register (0x0D)

The configuration register sets the proximity LED drive level, wait long time, and ALS gain level.

	7	6	5	4	3	2	1	0	
CONFIG	Reserved					AGL	WLONG	PDL	0x0D

FIELD	BITS	DESCRIPTION
Reserved	7:3	Reserved. Write as 0.
AGL	2	ALS gain level. When asserted, the 1× and 8× ALS gain (AGAIN) modes are scaled by 0.16. Otherwise,AGAIN is scaled by 1. Do not use with AGAIN greater than 8×.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12x from that programmed in the WTIME register.
PDL	0	Proximity drive level. When asserted, the proximity LDR drive current is reduced by 9.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that the LDR pin will generate during the Prox Accum state. The pulses are generated at a 62.5 kHz rate. 100 mA and 8 pulses are the recommended driving conditions. For other driving conditions, contact Avago Field Sales.

	7	6	5	4	3	2	1	0	
PPULSE	PPULSE								0x0E

FIELD	BITS	DESCRIPTION
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		PDIODE		PGAIN		AGAIN		0x0F

FIELD	BITS	DESCRIPTION		
PDRIVE	7:6	LED Drive Strength.		
		FIELD VALUE	**LED STRENGTH — PDL = 0**	**LED STRENGTH — PDL = 1**
		00	100 mA	11.1 mA
		01	50 mA	5.6 mA
		10	25 mA	2.8 mA
		11	12.5 mA	1.4 mA
PDIODE	5:4	Proximity Diode Select.		
		FIELD VALUE	**DIODE SELECTION**	
		00	Reserved	
		01	Reserved	
		10	Proximity uses the Ch1 diode	
		11	Reserved	
PGAIN	3:2	Proximity Gain Control.		
		FIELD VALUE	**Proximity GAIN VALUE**	
		00	1X Gain	
		01	2X Gain	
		10	4X Gain	
		11	8X Gain	
AGAIN	1:0	ALS Gain Control.		
		FIELD VALUE	**ALS GAIN VALUE**	
		00	1X Gain	
		01	8X Gain	
		10	16X Gain	
		11	120X Gain	

Device ID Register (0x12)

The ID register provides the value for the part number. The ID register is a read-only register.

	7	6	5	4	3	2	1	0	
ID	Device ID								0x12

FIELD	BITS	DESCRIPTION
ID	7:0	Part number identification
		0x39 = APDS-9930

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

	7	6	5	4	3	2	1	0	
STATUS	Reserved	PSAT	PINT	AINT	Reserved	Reserved	PVALID	AVALID	0x13

FIELD	BITS	DESCRIPTION
Reserved	7	Reserved.
PSAT	6	Proximity Saturation. Indicates that the proximity measurement is saturated
PINT	5	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
AINT	4	ALS Interrupt. Indicates that the device is asserting an ALS interrupt.
Reserved	3:2	Reserved.
PVALID	1	PS Valid. Indicates that the PS has completed an integration cycle.
AVALID	0	ALS Valid. Indicates that the ALS Ch0/Ch1 channels have completed an integration cycle.

ALS Data Registers (0x14 – 0x17)

ALS Ch0 and CH1 data are stored as two 16-bit values. To ensure the data is read correctly, a two byte read I^2C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

REGISTER	ADDRESS	BITS	DESCRIPTION
Ch0DATAL	0x14	7:0	ALS Ch0 channel data low byte
Ch0DATAH	0x15	7:0	ALS Ch0 channel data high byte
Ch1DATAL	0x16	7:0	ALS Ch1 channel data low byte
Ch1DATAH	0x17	7:0	ALS Ch1 channel data high byte

Proximity DATA Register (0x18 – 0x19)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two byte read I^2C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

Proximity Offset Register (0x1E)

The 8-bit proximity offset register provides compensation for proximity offsets caused by device variations, optical crosstalk, and other environmental factors. Proximity offset is a sign-magnitude value where the sign bit, bit 7, determines if the offset is negative (bit 7 = 0) or positive (bit 7 = 1). The magnitude of the offset compensation depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE). Because a number of environmental factors contribute to proximity offset, this register is best suited for use in an adaptive closed-loop control system.

	7	6	5	4	3	2	1	0	Address
POFFSET	SIGN	MAGINITUDE							0x1E

FIELD	BITS	DESCRIPTION
SIGN	7	Proximity Offset Sign. The offset sign shifts the proximity data negative when equal to 0 and positive when equal to 1.
MAGNITUDE	6:0	Proximity Offset Magnitude. The offset magnitude shifts the proximity data positive or negative, depending on the proximity offset sign. The actual amount of the shift depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE).

Application Information: Hardware

In a proximity sensing system, the included IR LED can be pulsed with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LEDA pin, the key goal can be met. Place a 1 µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LEDA pin, and at least 10 µF of bulk capacitance to supply the 100 mA current surge. This may be distributed as two 4.7 µF capacitors.

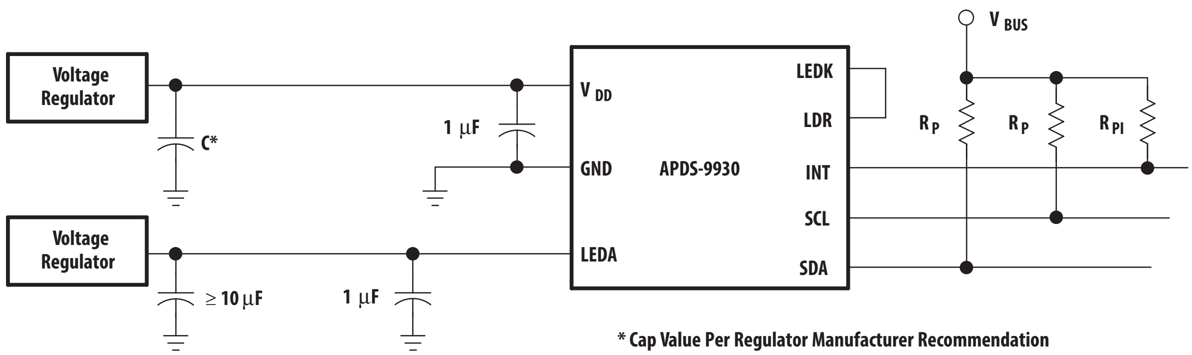


Figure 14a. Proximity Sensing Using Separate Power Supplies

If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22 Ω resistor in series with the V_{DD} supply line and a 1 µF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

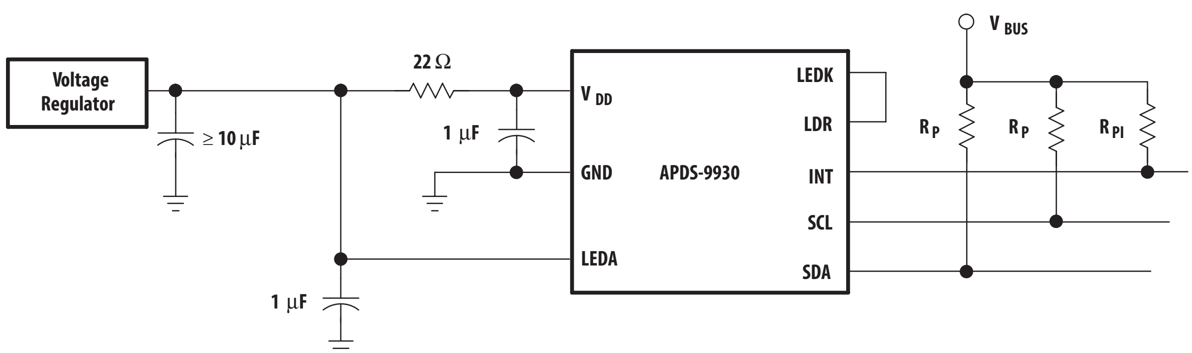
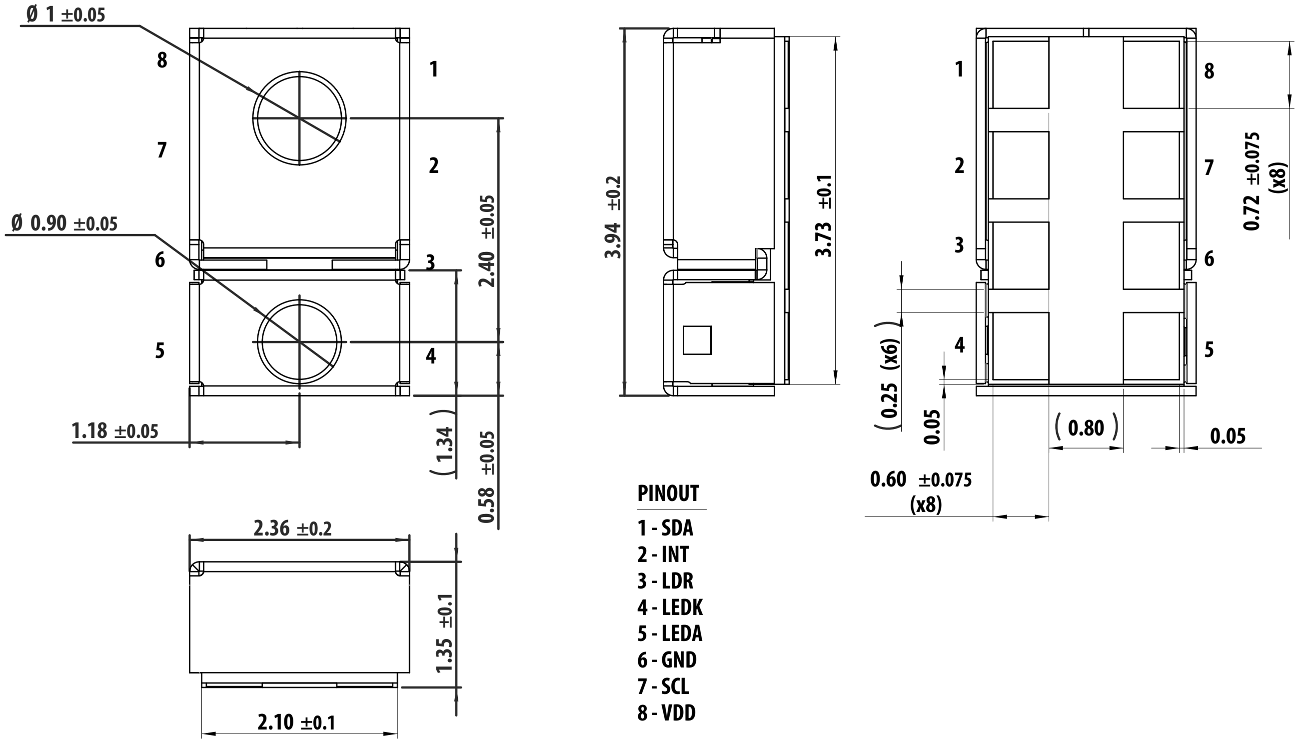


Figure 14b. Proximity Sensing Using Single Power Supply

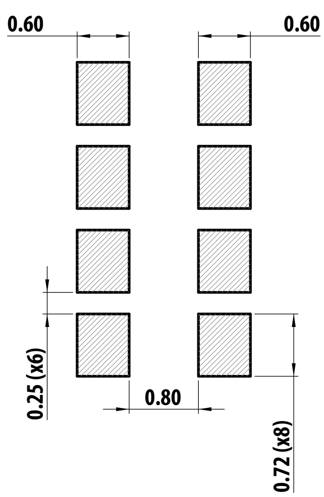
V_{BUS} in the preceding figures refers to the I²C-bus voltage. The I²C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_P) value is a function of the I²C bus speed, the I²C-bus voltage, and the capacitive load. A 10 kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

Package Outline Dimensions



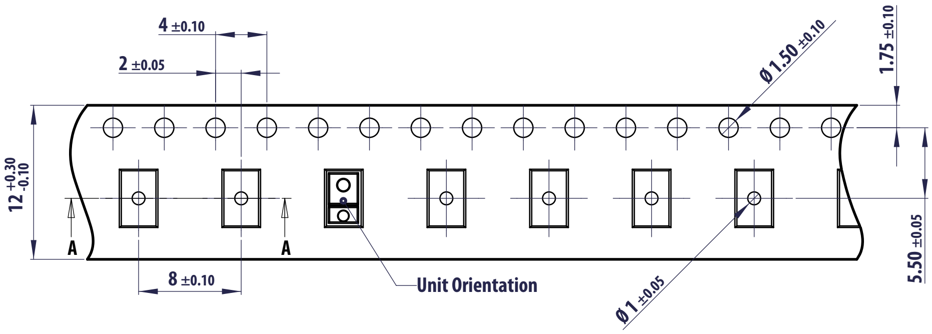
PCB Pad Layout

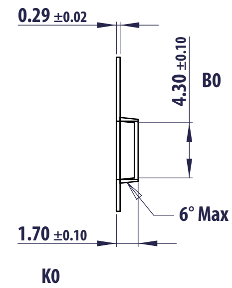
Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are as follows:

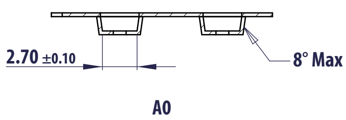


Note: All linear dimensions are in mm.

Tape Dimensions

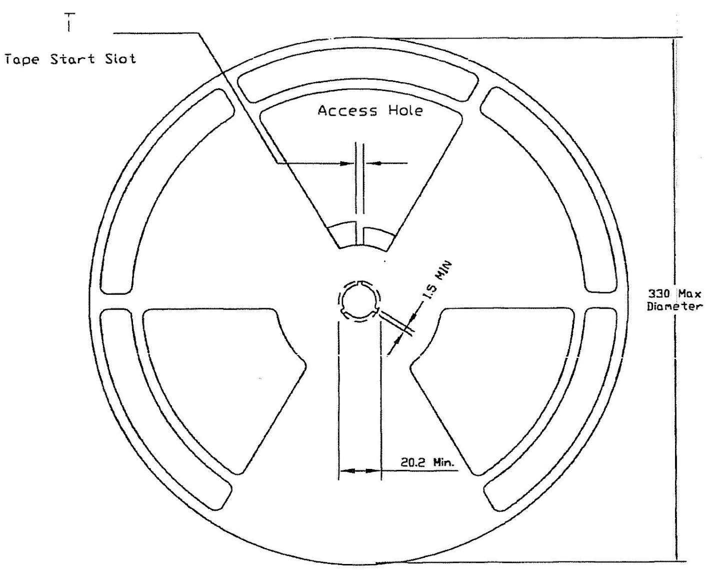


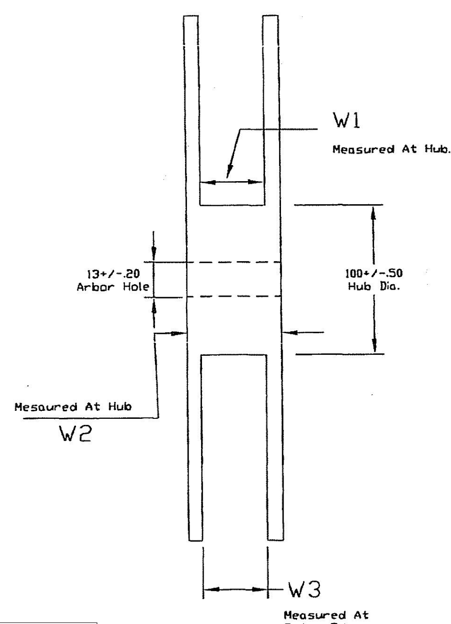




All dimensions unit: mm

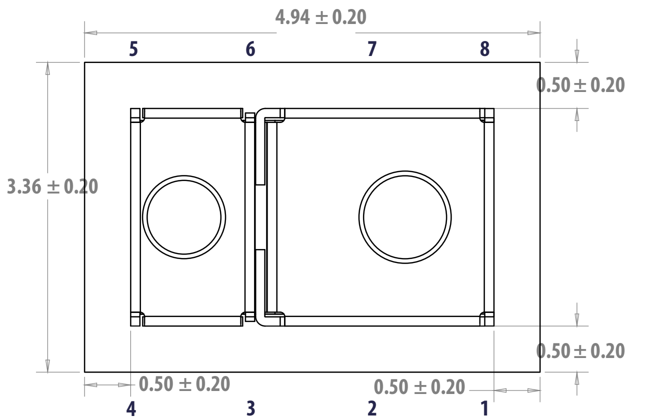
Reel Dimensions



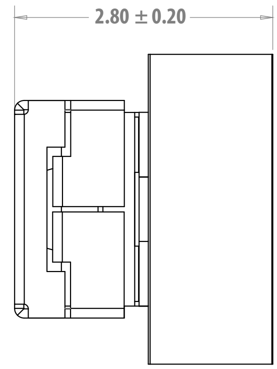


TAPE WIDTH	T	W1	W2	W3
12MM	4+/- .50	12.4 + 2.0 - 0.0	18.4 MAX	11.9 MIN 15.4 MAX

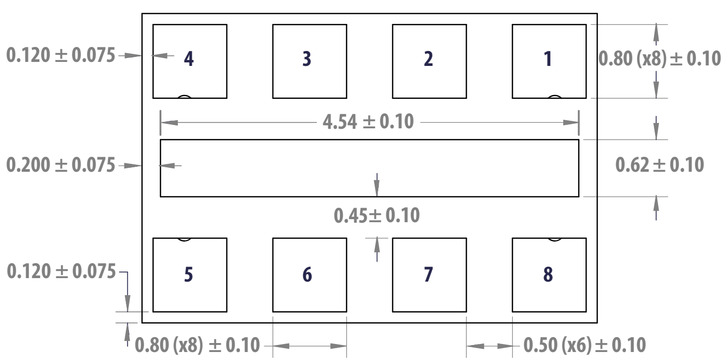
Package Outline Dimensions for Option -140



Top View

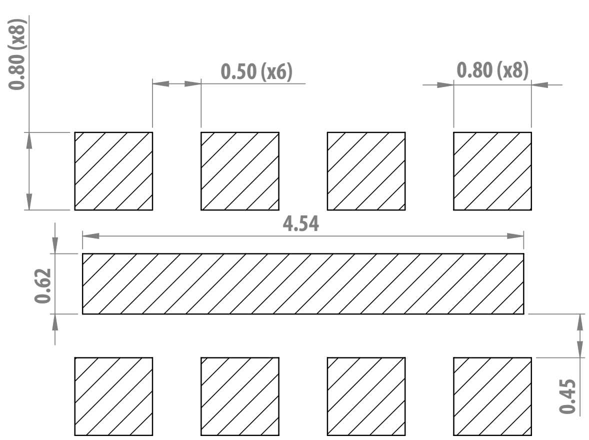


Side View

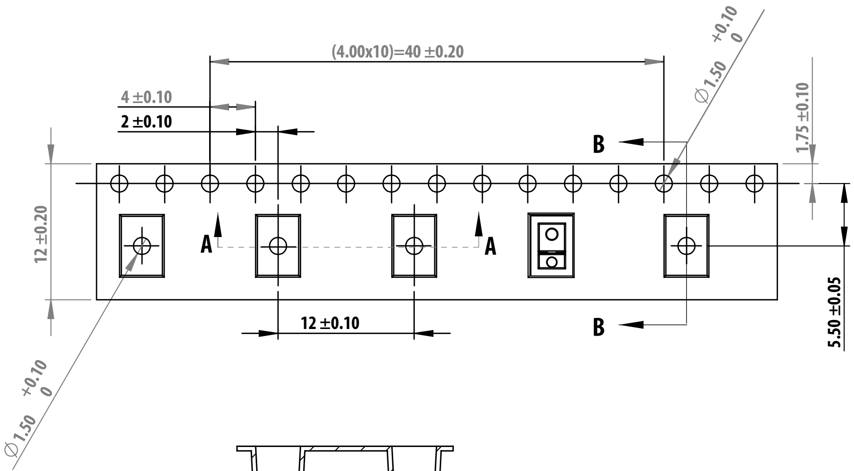


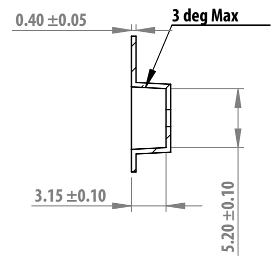
Bottom View

PCB Pad Layout for Option -140

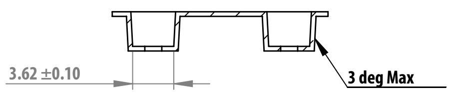


Tape Dimensions for Option -140

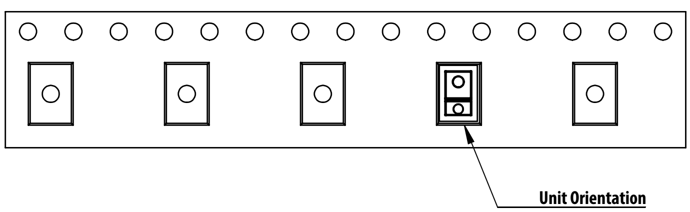




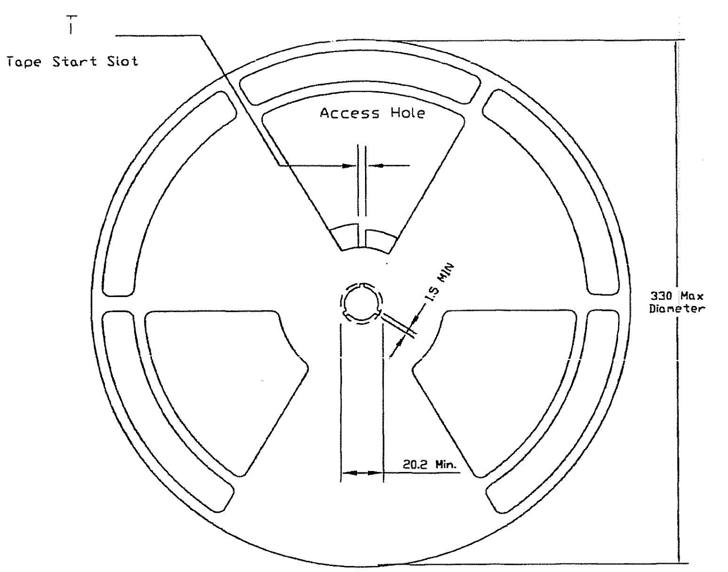
SECTION B-B

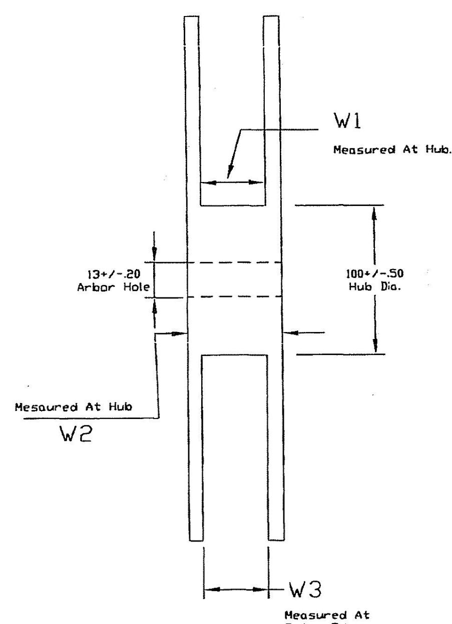


SECTION A-A



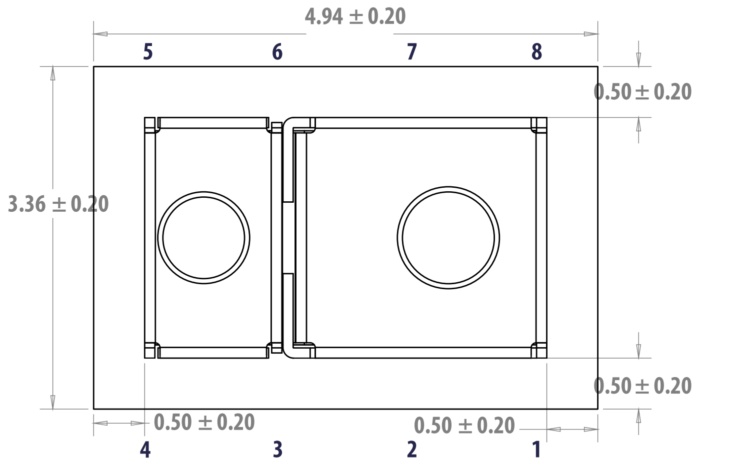
Reel Dimensions for Option -140



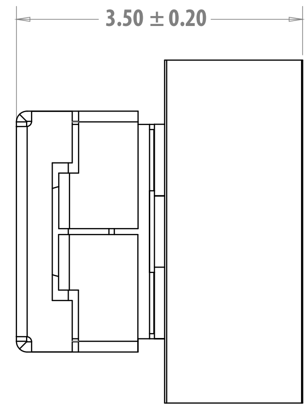


TAPE WIDTH	T	W1	W2	W3
12MM	4+/- .50	12.4 + 2.0 - 0.0	18.4 MAX	11.9 MIN 15.4 MAX

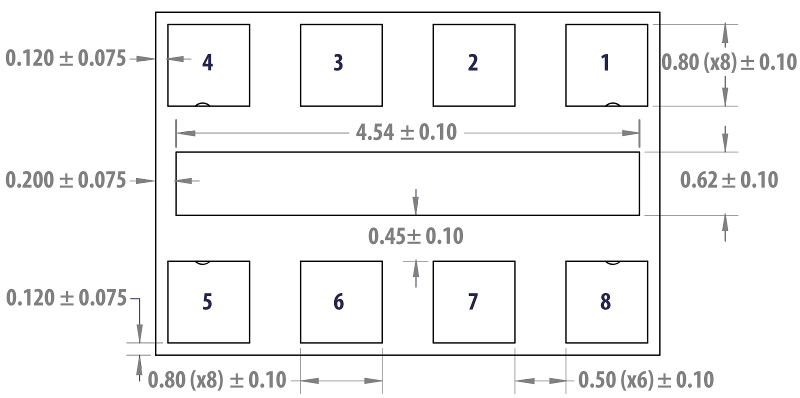
Package Outline Dimensions for Option -200



Top View

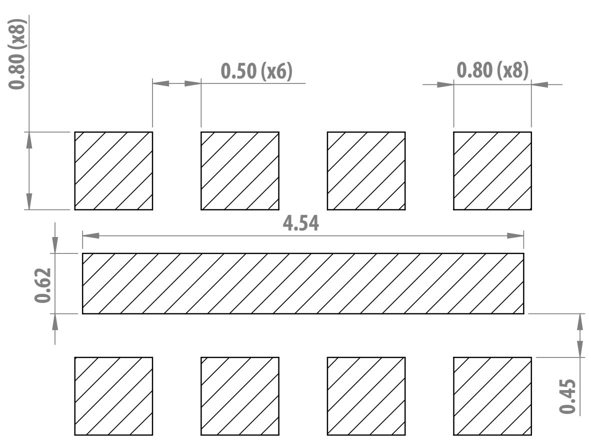


Side View

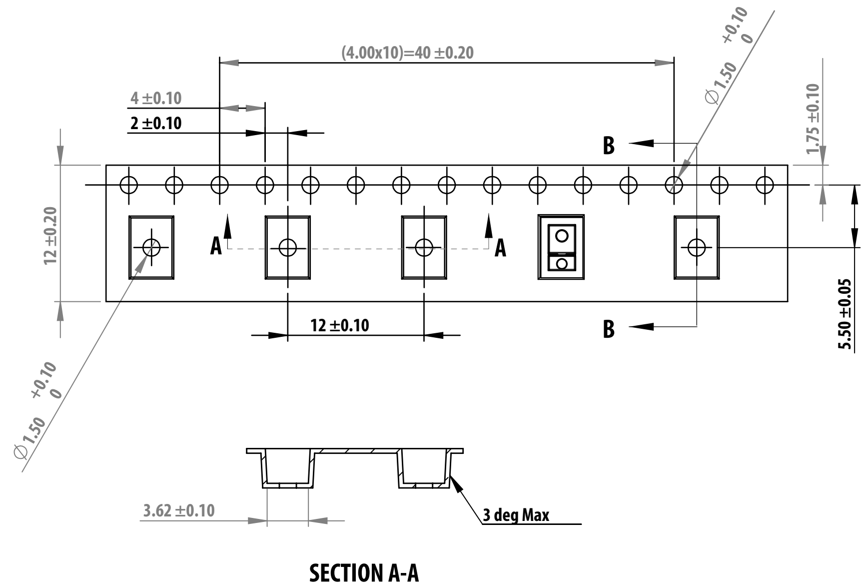


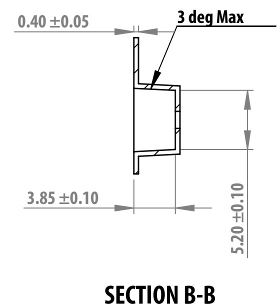
Bottom View

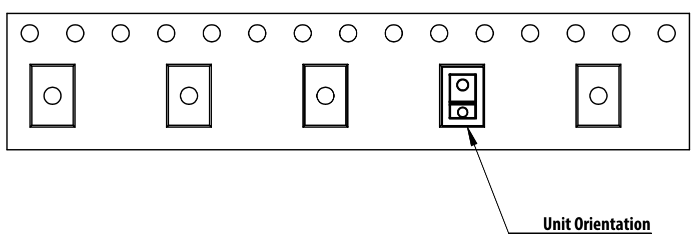
PCB Pad Layout for Option -200



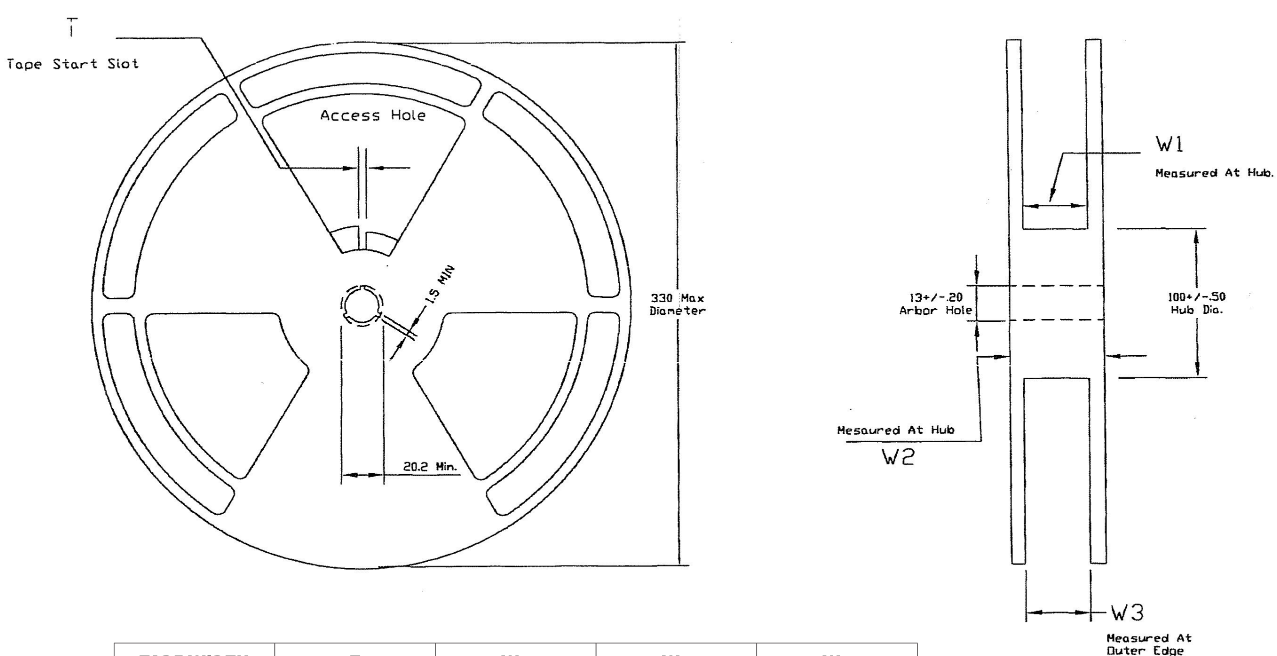
Tape Dimensions for Option -200







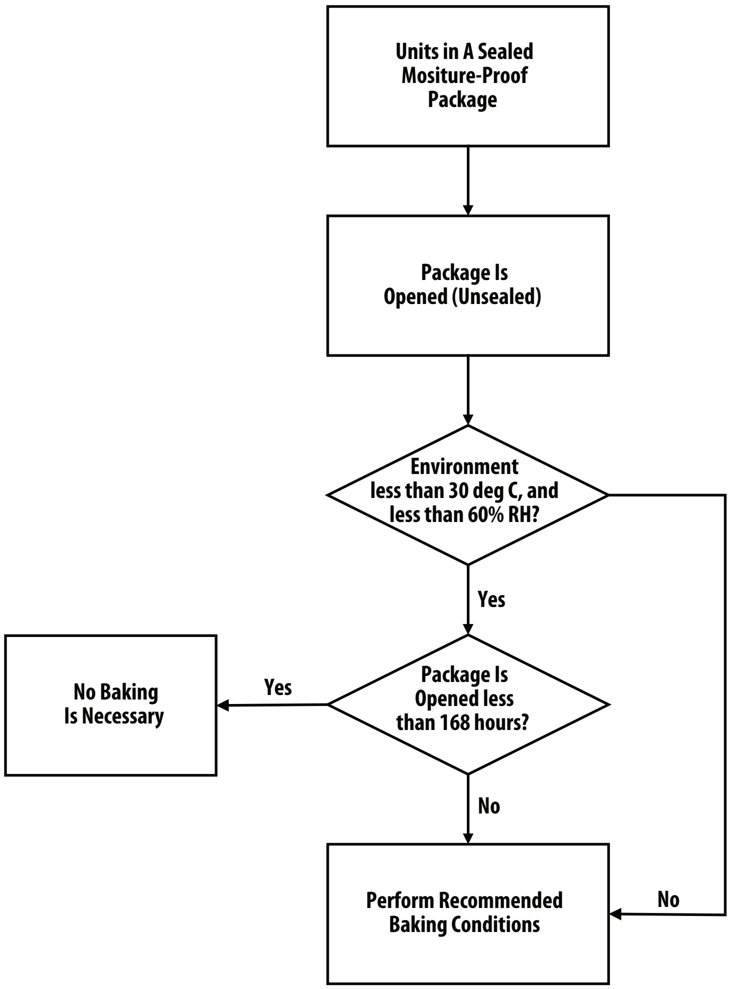
Reel Dimensions for Option -200



TAPE WIDTH	T	W1	W2	W3
12MM	4+/- .50	12.4 + 2.0 - 0.0	18.4 MAX	11.9 MIN 15.4 MAX

Moisture-Proof Packaging

All APDS-9930 options are shipped in a moisture-proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions:

Package	Temperature	Time
In Reel	60 °C	48 hours
In Bulk	100 °C	4 hours

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

Recommended Storage Conditions:

Storage Temperature	10 °C to 30 °C
Relative Humidity	below 60% RH

Time from unsealing to soldering:

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box