SECONDARY SIDE SYNCHRONOUS RECTIFICATION SWITCHER

Description

The APR34509 is a secondary side Combo IC, which combines an N-Channel MOSFET and a driver circuit designed for Synchronous Rectification (SR), supports CCM, DCM and Quasi-Resonant Flyback Topologies.

The N-Channel MOSFET is optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and body diode reverse recovery performance.

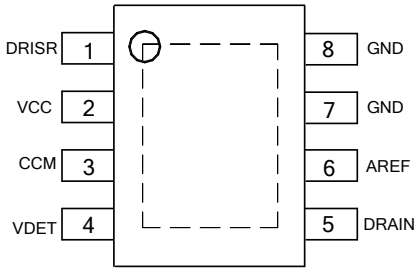
The synchronous rectification can effectively reduce the secondary side rectifier power dissipation and provide high performance solution. By sensing MOSFET drain-to-source voltage, the APR34509 can output ideal drive signal with less external components.

It can provide high performance solution for 5V to 12V output voltage application.

The APR34509 is available in SO-8EP package.

Pin Assignments

(Top View)



Note: The DRAIN pin of internal MOSFET is exposed PAD, which is at the bottom of IC (the dashed box). The secondary current should flow from GND (pins 7 and 8) to this exposed PAD.

SO-8EP

Features

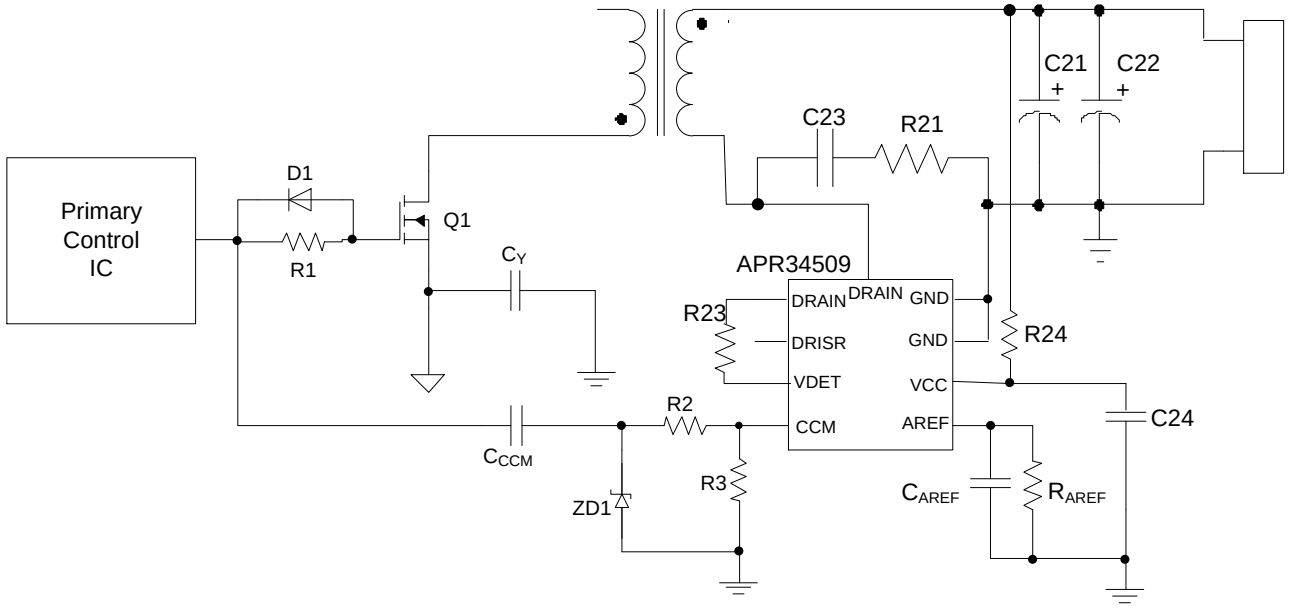
- Synchronous Rectification for DCM Operation Flyback
- Eliminate Resonant Ring Interference
- Fast Detector of Supply Voltages
- Fewest External Components
- Moisture Sensitivity: MSL Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per M2003 JESD22-B102 (e3)
- Weight: 0.081 grams (Approximate)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Adapters/Chargers for Cell/Cordless Phones, ADSL Modems, MP3 and Other Portable Apparatus
- Standby and Auxiliary Power Supplies

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

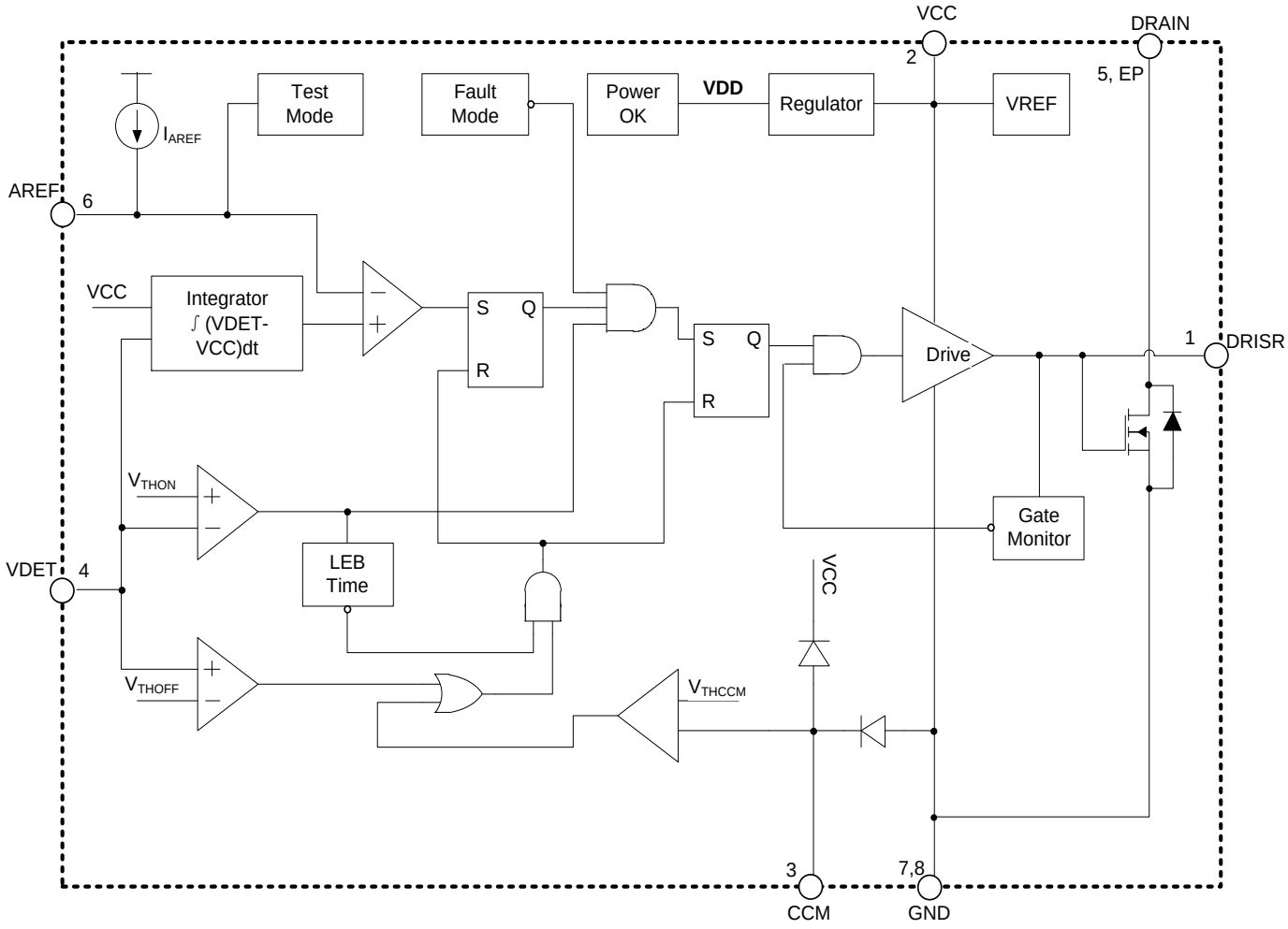
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1	DRISR	Synchronous rectification MOSFET drive.
2	VCC	Power supply, connected with system output.
3	CCM	Primary trigger signal sense input.
4	VDET	Synchronous rectification sense input and dynamic function output, connected to DRAIN through a resistor.
5	DRAIN	Drain pin of internal MOSFET. The Drain voltage signal can obtain from this pin.
6	AREF	Program a voltage reference with a resistor from AREF to GND, to enable synchronous rectification MOSFET drive signal.
7, 8	GND	Source pin of internal MOSFET, connected to Ground.
Exposed PAD	DRAIN	Drain pin of internal MOSFET. The secondary current should flow from GND (Pins 7 and 8) to this DRAIN pad.

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to 16	V
V_{DET}, V_{DRAIN}	Voltage at VDET, DRAIN Pin	-2 to 62	V
V_{AREF}, V_{DRISR}	Voltage at AREF, DRISR Pin	-0.3 to 16	V
I_D	Continuous Drain Current	20	A
I_{DM}	Pulsed Drain Current	80	A
P_D	Power Dissipation at T_A = +25°C	2.2	W
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	56	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	12	°C/W
T_J	Operating Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
ESD	Human Body Model	4000	V

Notes: 4. Stresses greater than those listed under "*Absolute Maximum Ratings*" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods can affect device reliability.

5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch^2 cooling area.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	3.3	13	V
T_A	Ambient Temperature	-40	+85	°C

Electrical Characteristics (@T_A = +25°C, V_{CC} = 5V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
$I_{STARTUP}$	Startup Current	V_{CC} = $V_{STARTUP}$-0.1V	—	100	150	μA
I_{OP}	Operating Current	VDET Pin Floating V_{CC} = 5V	—	100	150	μA
$V_{STARTUP}$	Startup Voltage	—	2.75	3.1	3.55	V
—	UVLO	—	2.45	2.8	3.25	V
Gate Driver						
V_{THON}	Gate Turn-On Threshold	—	0	—	1	V
V_{THOFF}	Gate Turn-Off Threshold	—	-14	-7.5	-1	mV
t_{DON}	Turn-On Delay Time	From V_{THON} to V_{DRISR} = 1V	—	70	130	ns
t_{DOFF}	Turn-Off Propagation Delay Time	From V_{THOFF} to V_{DRISR} = 4V	—	100	150	ns
t_{RG}	Turn-On Rising Time	From 1V to 4V, V_{CC} = 5V, C_L = 4.7nF	—	50	100	ns
t_{FG}	Turn-Off Falling Time	From 4V to 1V, V_{CC} = 5V, C_L = 4.7nF	—	20	35	ns
t_{ON_MIN}	Minimum On Time	—	1.2	1.6	2	μs
V_{DRISR} V_{DRI_HIGH}	Drive Maximum Voltage	—	—	—	V_{CC}	V
V_{DRISR} V_{DRI_HOLD}	SR Drive Hold Voltage	V_{CC} < 5V	—	—	V_{CC}	V
		V_{CC} >= 5V	—	5	—	
Kqs	(Note 6)	—	0.44	0.52	0.6	mA*μs
V_{S_MIN}	Synchronous Rectification (SR) Minimum Operating Voltage (Note 7)	—	—	—	4.5	V
Synchronous Rectification Detection						
V_{TH_CCM}	V_{DRISR} Rising Threshold	V_{DRISR} Output Transitions From High to Low	0.43	0.53	0.71	V
t_{DCCM}	CCM Propagation Delay	From CCM Rising to V_{DRISR} Falling 10%	—	20	35	ns

Notes: 6. This item is used to specify the value of R_{AREF}.
7. This item specifies the minimum SR operating voltage of V_{IN_DC}, $V_{IN\_DC} \geq N_{PS} * V_{S\_MIN}$.

Electrical Characteristics (@T_A =+25°C, unless otherwise specified. continued)

MOSFET Static Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DSS(BR)}$	Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 0.25mA	62	—	—	V
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.25mA	0.7	1.3	2	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50V, V_{GS} = 0V	—	—	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 4.5V, V_{DS} = 0V	—	—	±100	nA
$R_{DS(ON)}$	Drain to Source On-State Resistance	V_{GS} = 4.5V, I_D = 3A	—	8	—	mΩ

MOSFET Dynamic Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f =1MHz	—	1872	—	pF
C_{oss}	Output Capacitance		—	506	—	
C_{rss}	Reverse Transfer Capacitance		—	43	—	
Q_{gs}	Gate to Source Charge	V_{GS} = 0V to 10V, V_{DD} = 25V, I_D=15A	—	3.1	—	nC
Q_{gd}	Gate to Drain Charge (Miller Charger)		—	4.8	—	
Q_g	Total Gate Charge	V_{GS} = 4.5V	—	15	—	
R_g	Gate Resistance	—	—	1.8	—	Ω

Synchronous Rectification Principle Description

SR MOSFET Turn-On

The APR34509 determines the synchronous rectification MOSFET turn-on time by monitoring the MOSFET drain-to-source voltage. For both of DCM and CCM operation, the turn-on principle is same. When the drain voltage is lower than the turn-on threshold voltage V_{THON}, the IC outputs a positive drive voltage after a turn-on delay time (t_{DON}). The MOSFET will turn on and the current will transfer from the body diode into the MOSFET's channel. Since of parasitic parameter, the voltage on MOSFET drain pin has moderate voltage ringing at this moment, which maybe impact on SR controller VDET voltage sense and bring about turn-off fault. To avoid fault situation happening, a Minimum On Time (t_{ONMIN}) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.

In Figure 1, the turn-on blanking time t_{ONMIN} is to prevent the MOSFET drain-to-source voltage ringing affect. During this time, the V_{DRISR} is pulled up to V_{CC}; after t_{ONMIN}, the drive voltage stops being pulled up by the driver, and begins to drop; when V_{DRISR} drops to V_{DRI_HOLD}, it will be held at this voltage until being pulled down.

DCM Turn-Off Operation

The DCM operation of the SR is described with timing diagram shown in Figure 1.

In the process of drain current decreasing linearly toward zero, the drain-source voltage rises synchronically. When it rises over the turn off threshold voltage V_{THOFF}, the APR34509 pulls the drive signal down after a turn-off delay (t_{DOFF}).

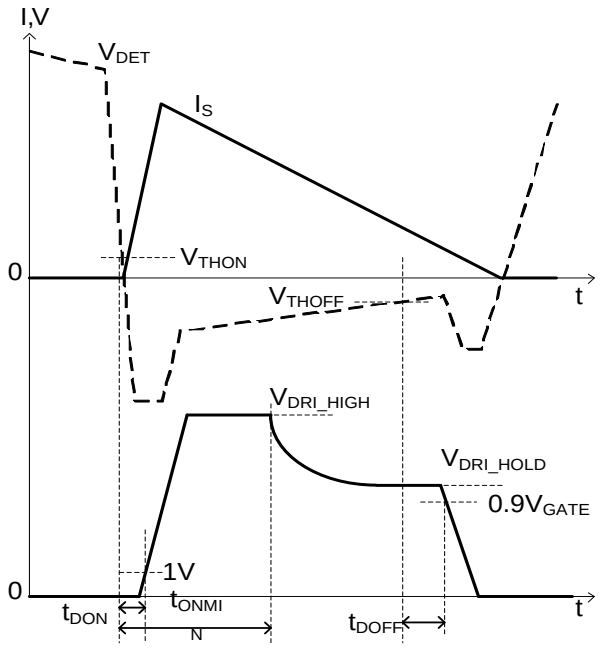


Figure 1. Typical Waveforms of APR34509 in DCM

CCM Turn-Off Operation

The CCM pin is used to sense trigger signal for turn-off the SR MOSFET before primary switch turn-on in Continuous Conduction Mode (CCM) system. After t_{ONMIN}, if the CCM pin voltage rises over the threshold voltage V_{THCCM}, the drive voltage will be pulled down after a short delay time t_{DCCM} to turn off SR MOSFET. The CCM pin senses trigger signal coming from primary switch turn-on signal through a RC networks circuit, a Y–type isolating capacitor C_{CCM}, two resistors R2 and R3. Note variations of these resistors, of C_{CCM}, and of the dV/dt across C_{CCM} require that worst-case tolerances be taken into account when determining the minimum value of C_{CCM}. For example, the value of this resistor will impact the rise time of CCM voltage. The bigger resistor, the slower the CCM voltage rises.

The zener diode ZD1 is used for ESD test.

The value of C_Y should be much higher than that of C_{CCM}. If necessary, increase the value of C_Y to ensure that $C_Y >> C_{CCM}$; do not decrease C_{CCM}.

C_Y is the main common-mode capacitance between the primary and the secondary sides of the system. This is usually a discrete component, whose value ranges from 47pF to 2200pF. Aside from any EMI-control purposes, it also serves as the return path for the CCM signal charging and discharging current pulses.

Synchronous Rectification Principle Description (continued)

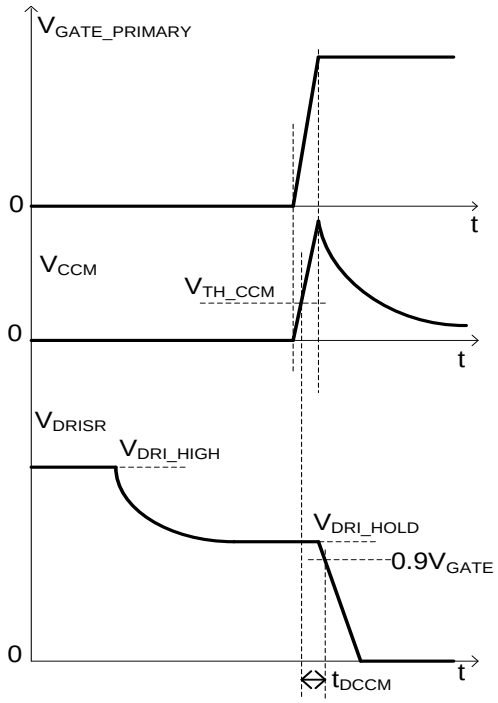


Figure 2. Typical Turn-Off Waveforms of APR34509 in CCM

Minimum On Time

When the controlled MOSFET gate is turned on, some ringing noise is generated. The minimum on-time timer blanks the V_{THOFF} comparator and CCM comparator, keeping the controlled MOSFET on for at least the minimum on time. During the minimum on time, the turn off threshold (DCM and CCM) is totally blanked.

The Value and Meaning of AREF Resistor

As to DCM operation Flyback converter, after secondary rectifier stops conduction, the primary MOSFET Drain-to-source ringing waveform is resulted from the resonant of primary inductance and equivalent switch device output capacitance. This ringing waveform probably leads to Synchronous Rectifier error conduction. To avoid this fault happening, the APR34509 has a special function design by means of volt-second product detecting. From the sensed voltage of VDET pin to see, the volt-second product of voltage above VCC at primary switch on time is much higher than the volt-second product of each cycle ringing voltage above V_{CC}. Therefore, before every time Synchronous Rectifier turns on, the APR34509 judges if the detected volt-second product of VDET voltage above V_{CC} is higher than a threshold and then turns on synchronous Rectifier. The purpose of AREF resistor is to determine the volt-second product threshold. The APR34509 has a parameter, Kqs, which converts R_{AREF} value to volt-second product,

$$\mathrm{Area2} = \mathrm{R}_{\mathrm{AREF}} * \mathrm{Kqs}$$

In general, Area1 and Area3 values depend on system design and are always fixed after system design frozen. As to Diodes Incorporated's PSR design, the Area1 value changes with primary peak current value and Area3 value generally keeps constant at all conditions. So the AREF resistor design should consider the worst case, the minimum primary peak current condition. Since of system design parameter distribution, Area1 and Area3 have moderate tolerance. So Area2 should be designed between the middle of Area1 and Area3 to keep enough design margin.

Note: To keep the volt-second product threshold stable, a capacitor is suggested to parallel with AREF resistor. And the recommended value of this capacitor is 20nF.

$$\mathrm{Area3} < \mathrm{R}_{\mathrm{AREF}} * \mathrm{Kqs} < \mathrm{Area1}$$

Synchronous Rectification Principle Description (continued)

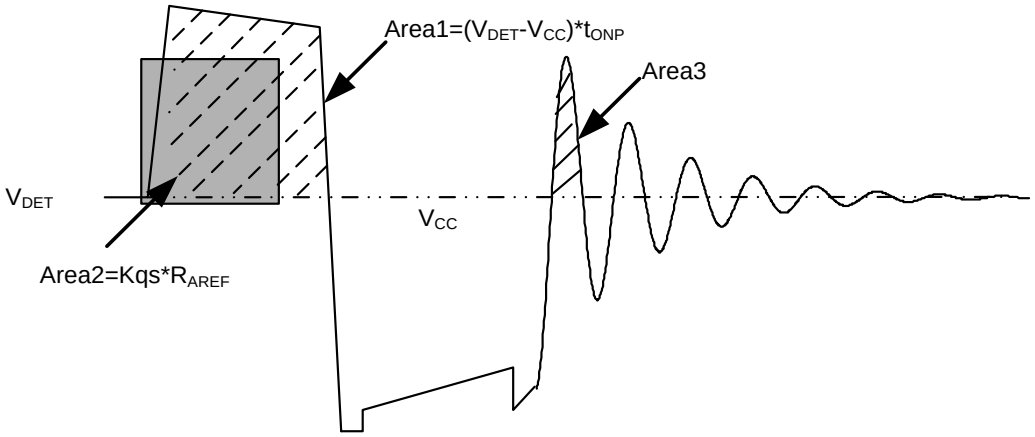


Figure 3. AREF Function

SR Minimum Operating Voltage

The APR34509 sets a minimum SR operating voltage by comparing the difference between V_{DET} and output voltage (V_{CC}). The value of V_{DET}–V_{CC} must be higher than its internal reference, then the APR34509 will begin to integrate the area of (V_{DET}–V_{CC})*t_{ONP}. If not, the area integrating will not begin and the SR driver will be disabled.

SR Turn-Off Timing Impact on PSR CV Sampling

As for the synchronous rectification on Flyback power system, SR MOSFET must turn off before the secondary side current decreases to zero in order to avoid reverse-current flow. When SR turns off in advance, the secondary current will flow through the body diode. The SR turn-off time is determined by the V_{THOFF} at a fixed system. When V_{THOFF} is more close to zero, the SR turn-on time gets longer and body diode conduction time gets shorter. Since of the different voltage drop between SR MOSFET and body diode, the PSR feedback signal V_{FB} appears a voltage jump at the time of SR MOSFET turn-off. If the PSR CV sampling time t_{SAMPLE} is close to even behind this voltage jump time, there will be system unstable operation issue or the lower output voltage issue.

To ensure stable operating of system, it must be met:

$t_{BODYDIODE} < t_{ONS} - t_{SAMPLE}$

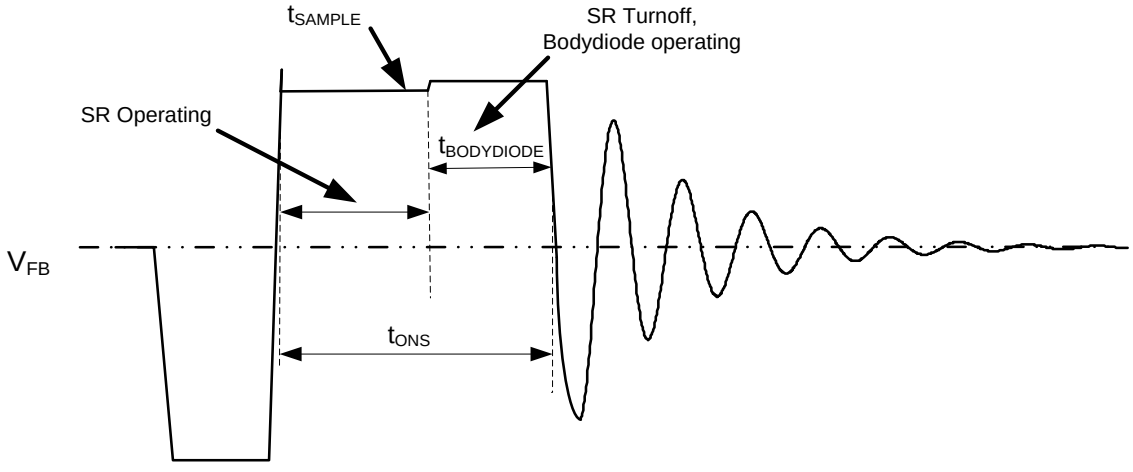


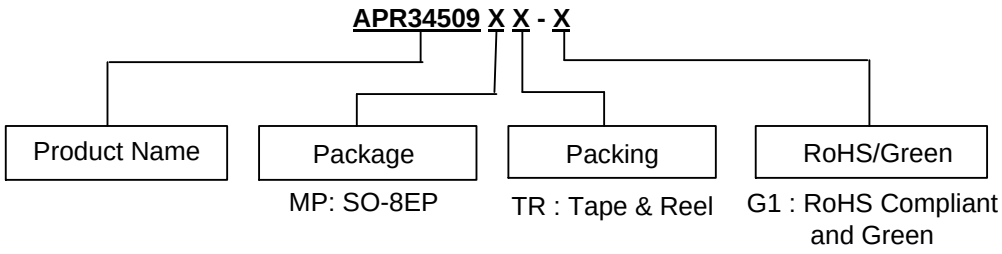
Figure 4. SR Turn-Off Timing Impact on PSR CV Sampling

Recommended Application Circuit Parameters

The two resistors R23 and R24 are used to pass ESD test. The values of R23 and R24 should be over 20Ω and below 47Ω respectively because of the undershoot performance. The package of R23 and R24 must be at least 0805 and there isn't any trace under these two resistors.

C_{AREF} is recommended to parallel with AREF resistor to keep the volt-second product threshold stable.
A 20nF C_{AREF} and a 100nF C24 are recommended.

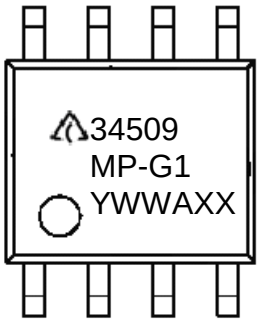
Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing
SO-8EP	-40 to +85°C	APR34509MPTR-G1	34509MP-G1	4000/Tape & Reel

Marking Information

(Top View)

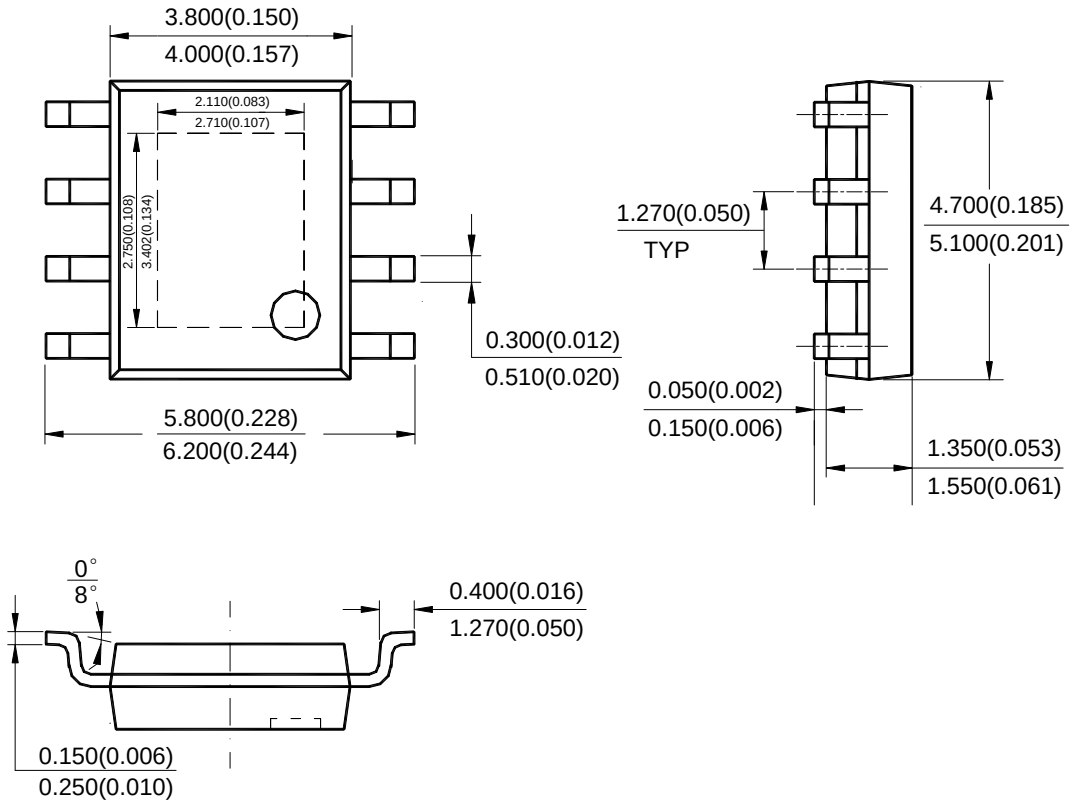


First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch No.

Package Outline Dimensions (All dimensions in mm(inch).)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SO-8EP

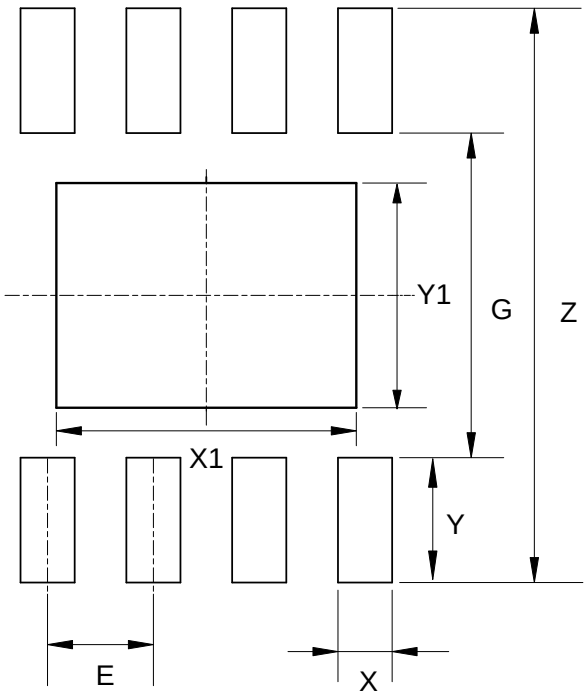


Note: Eject hole, oriented hole and mold mark is optional.

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SO-8EP



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	X1 (mm)/(inch)	Y1 (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	3.600/0.142	2.700/0.106	1.270/0.050