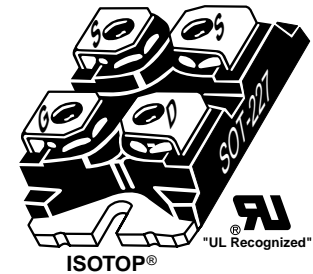


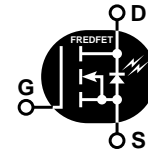
POWER MOS V[®]

FREDFET

Power MOS V[®] is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V[®] also achieves faster switching speeds through optimized gate layout.



- Fast Recovery Body Diode
- 100% Avalanche Tested
- Lower Leakage
- Popular SOT-227 Package
- Faster Switching



Unless stated otherwise, Microsemi discrete FREDFETs contain a single FREDFET die. This device is made with two parallel FREDFET die. It is intended for switch-mode operation. It is not suitable for linear mode operation.


MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT50M85JVFR	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	50	Amps
I_{DM}	Pulsed Drain Current ^①	200	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	500	Watts
	Linear Derating Factor	4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	30	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	500			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	50			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D(Cont.)}$)			0.085	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			500	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			2000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1\text{mA}$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

Microsemi Website - <http://www.microsemi.com>

DYNAMIC CHARACTERISTICS

APT50M85JVFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V		9000	10800	pF
C _{oss}	Output Capacitance	V _{DS} = 25V		1240	1740	
C _{rss}	Reverse Transfer Capacitance	f = 1 MHz		500	750	
Q _g	Total Gate Charge ^③	V _{GS} = 10V		390	535	nC
Q _{gs}	Gate-Source Charge	V _{DD} = 0.5 V _{DSS}		42	65	
Q _{gd}	Gate-Drain ("Miller") Charge	I _D = I _D [Cont.] @ 25°C		170	255	
t _{d(on)}	Turn-on Delay Time	V _{GS} = 15V		15	30	ns
t _r	Rise Time	V _{DD} = 0.5 V _{DSS}		17	34	
t _{d(off)}	Turn-off Delay Time	I _D = I _D [Cont.] @ 25°C		52	80	
t _f	Fall Time	R _G = 0.6Ω		7	14	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			50	Amps
I _{SM}	Pulsed Source Current ^① (Body Diode)			200	
V _{SD}	Diode Forward Voltage ^② (V _{GS} = 0V, I _S = -I _D [Cont.])			1.3	Volts
dv/dt	Peak Diode Recovery ^{dv/dt} ^⑤			5	V/ns
t _{rr}	Reverse Recovery Time (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C		300	ns
		T _j = 125°C		600	
Q _{rr}	Reverse Recovery Charge (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C	2.5		μC
		T _j = 125°C	8		
I _{RRM}	Peak Recovery Current (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C	16		Amps
		T _j = 125°C	28		

THERMAL/PACKAGE CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.25	°C/W
R _{θJA}	Junction to Ambient			40	
V _{Isolation}	RMS Voltage (50-60 Hz Sinusoidal Waveform From Terminals to Mounting Base for 1 Min.)	2500			Volts
Torque	Maximum Torque for Device Mounting Screws and Electrical Terminations.			13	lb•in

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T_j = +25°C, L = 2.89mH, R_G = 25Ω, Peak I_L = 30A

⑤ I_S = -I_D [Cont.], di/dt = 100A/μs, V_{DD} - V_{DSS}, T_j = 150°C, R_G = 2.0Ω, V_R = 200V

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

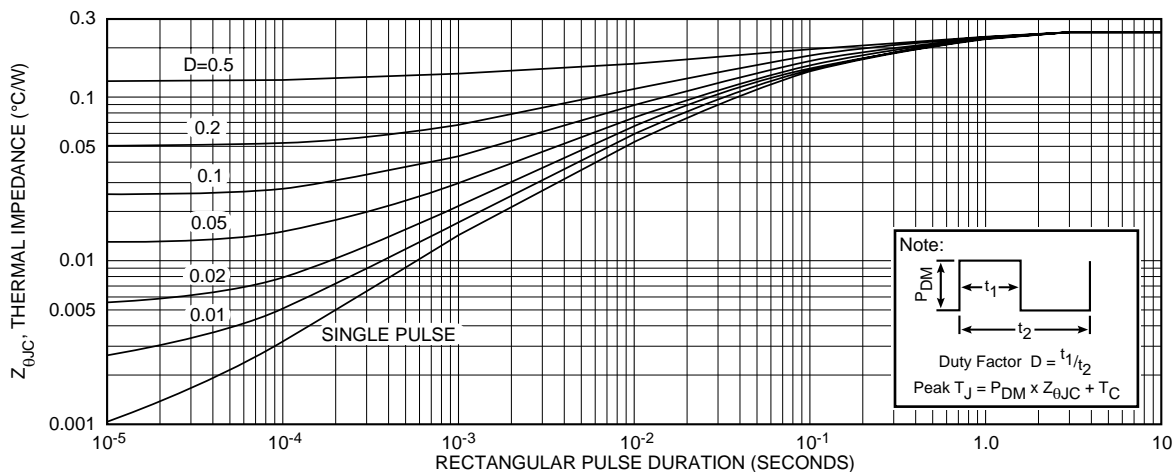


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

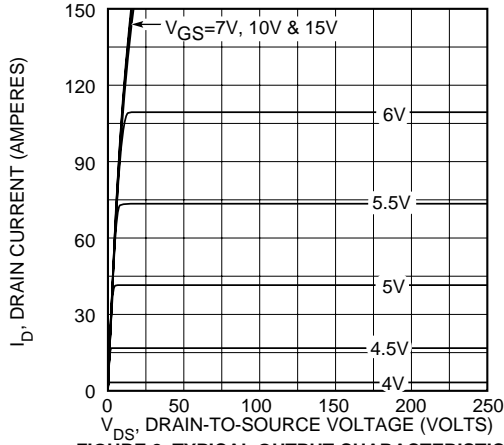


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

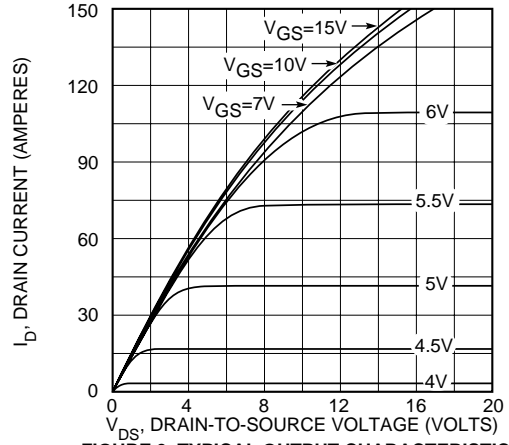


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

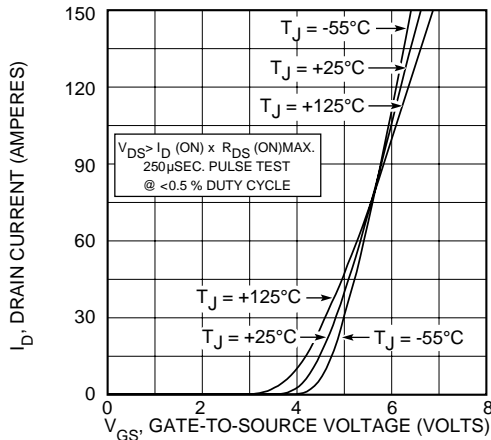


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

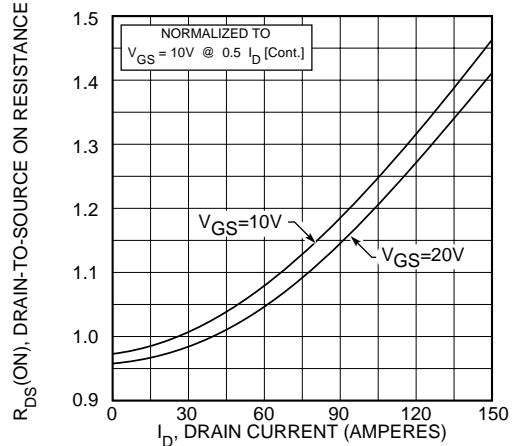


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

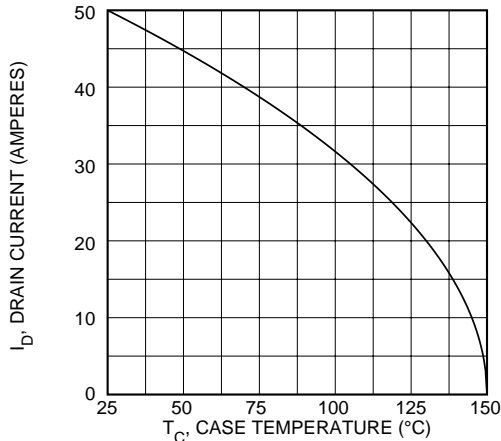


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

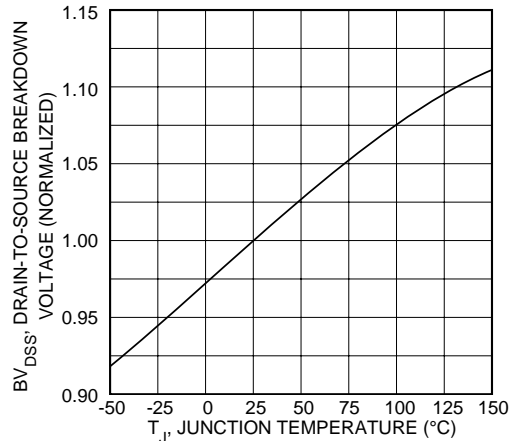


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

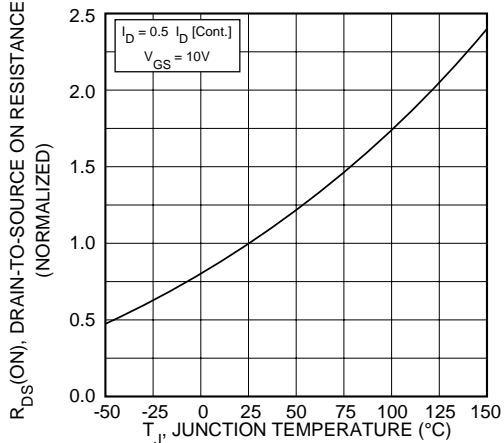


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

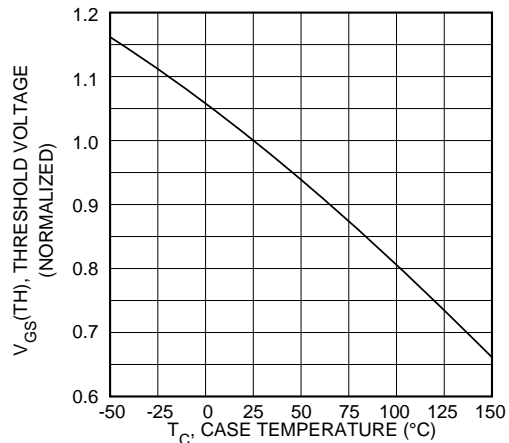


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE