AS1382

1A, High Efficiency, DC-DC Step Down Converter

General Description

The AS1382 is a high-efficiency, constant-frequency synchronous buck converter available in adjustabe- and fixed-voltage versions. The wide input voltage range (2.7V to 5.5V), automatic powersave mode and minimal external component requirements make the AS1382 perfect for any single Li-Ion battery-powered application.

Typical supply current with no load is 95µA and decreases to 0.04µA in shutdown mode.

An internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The internally fixed switching frequency (2MHz, 3MHz or 4MHz) allows the usage of small surface mount external components.

Very low output voltages can be delivered with the internal 0.58V feedback reference voltage.

The AS1382 is available in a 6-pin WL-CSP package.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of this device are listed below:

Figure 1:
Added Value of Using AS1382

| Benefits	Features
• Ideal for single Li-Ion battery powered applications	• Wide input voltage range (2.7V to 5.5V)
• Extended battery life	• High efficiency up to 96%
• Supports a variety of end applications	• Output voltage range (0.58V to 3.35V) • Output current of 1A • Switching frequency: 2MHz, 3MHz, 4MHz • High efficiency/low noise operation
• Over – temperature protection and shutdown	• Integrated temperature monitoring
• Cost effective, small package	• WL-CSP6 with 0.4mm pitch

Applications

The device is ideal for mobile communication devices, laptops and PDAs, ultra-low-power systems, medical instruments, or any other space-limited application with low power-consumption requirements.

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS1382
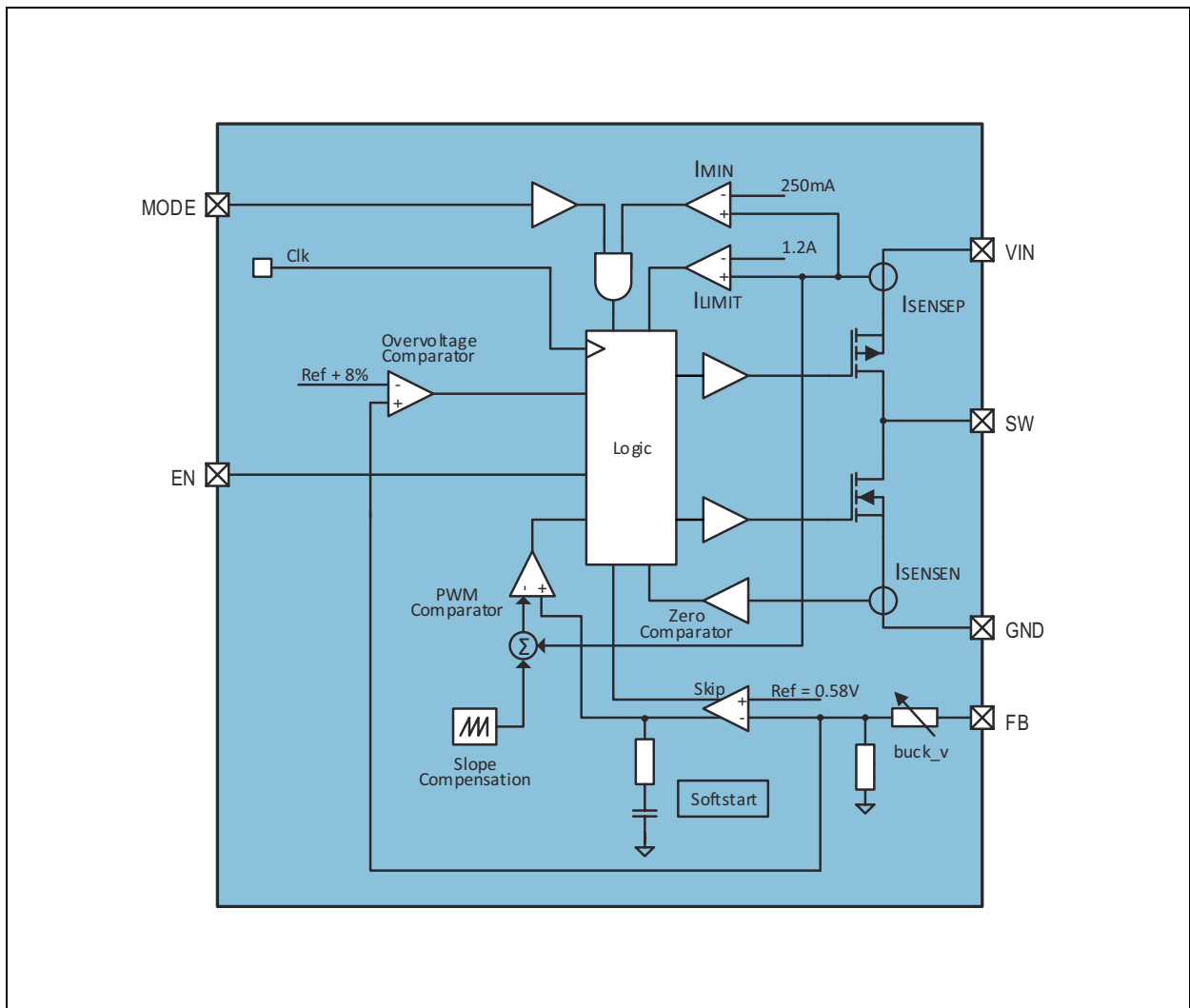
Block Diagram: Shows the detailed Block Diagram of the AS1382 Step Down DCDC Converter

Pin Assignments

Ball Assignments: Shows the TOP view ball assignment of the AS1382.

Pin A1 indicator

A1 MODE	A2 VIN
B1 SW	B2 EN
C1 FB	C2 GND
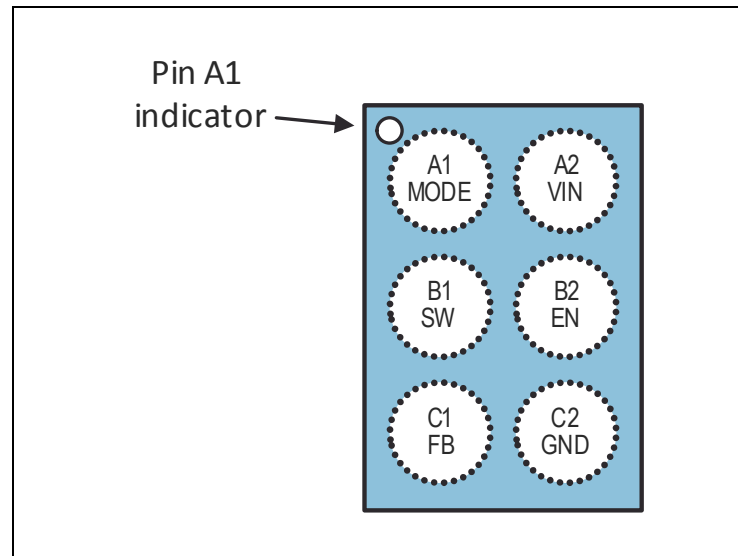
Figure 4:
Pin Description

Pin #	Pin Name	Pin Type	Description
A1	MODE	DIG IN	Mode Selection
B1	SW	DIG OUT	**Switch Node Connection to Coil.** This pin connects to the drains of the internal synchronous power MOSFET switches.
C1	FB	ANA IN	**Feedback Pin.** This pin receives the feedback voltage from the external resistor divider across the output. (Adjustable variant only)
			Output Voltage Feedback Pin. An internal resistor divider steps the output voltage down for comparison to the internal reference voltage. (Fixed voltage variants only)
A2	VIN	SUP IN	**Input Supply Voltage.** This pin must be closely de-coupled to GND with a ≥ 4.7µF ceramic capacitor. Connect to any supply voltage between 2.7V to 5.5V. [1]
B2	EN	DIG IN	**Enable Input.** Driving this pin above 1.2V enables the device. Driving this pin below 0.4V puts the device in shutdown mode. In shutdown mode all functions are disabled while SW goes high impedance, drawing < 1µA supply current. [1]
C2	GND	GND	**Ground**

Pin Description: Shows the pin number, type, name and description of every pin.

Note(s):

1. This pin should not be left floating.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{GND}	Supply Voltage to Ground 5V pins	-0.5	7.0	V	Applicable for pins VIN, EN, MODE, FB, SW
	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous power dissipation		0.55	W	P_T [1] for WL-CSP6 package (R_{THJA} ~95K/W)
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±2		kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_A	Operating Temperature	-40	85	°C	
R_{THJA}	Junction to Ambient Thermal Resistance		95	°C/W	
T_J	Junction Temperature		125	°C	
T_{STRG}	Storage Temperature Range	-55	125	°C	
T_{BODY}	Package Body Temperature		260	°C	Norm: IPC/JEDEC J-STD-020 [2]
RH_{NC}	Relative Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	1			Represents an unlimited floor life time

Note(s):

1. Depending on actual PCB layout and PCB used

2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices"

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input Voltage	Pin VIN	2.7		5.5	V
I_{SUP_DCDC}	Current Consumption	Operating Current without Load		95		μA
		Shutdown Current		0.04		
I_{FB}	Feedback Current	T_{AMB} = 25°C		1	30	nA
V_{FB}	Feedback Voltage	ADJ variant	0.56	0.58	0.60	V
V_{OUT}	Regulated Output Voltage	Fixed V_{OUT} variant	0.6125		3.35	V
		ADJ variant	0.58		3.35	V
V_{OUT_TOL}	Output Voltage Tolerance	Fixed output variants, min. 40mV	-3		3	%
η_{EFF}	Efficiency	see figures below			96	%
LNR	Output Voltage Line Regulation	Vin = 2.7V to 5.5V		0.1		%/V
LDR	Output Voltage Load Regulation	I_{OUT} = 0 to 100mA		0.02		%/mA
I_{LIMIT}	Peak Coil Current	I_{OUT} = 1A		1.5		A
I_{LOAD}	Load Current	$V_{OUT} \leq$ 1.8V	0		1	A
		V_{OUT} > 1.8V	0		0.7	A
I_{T_COMP}	Min load to guarantee correct output voltage in high temp			20		μA
R_{PMOS}	P-Channel FET $R_{DS(ON)}$ [1]	I_{LSW} = 100mA		0.25	0.55	Ω
R_{NMOS}	N-Channel FET $R_{DS(ON)}$ [1]	I_{LSW} = -100mA		0.25	0.55	Ω
V_{IH}	Logic in threshold	pin EN, MODE	1.2			V
V_{IL}					0.4	V
f_{SW}	Switching Frequency	Variant A		4		MHz
		Variant B		3		MHz
		Variant C		2		MHz

Symbol	Parameter	Note	Min	Typ	Max	Unit
T$_{SHDN}$	Thermal Shutdown			160		°C
ΔT$_{SHDN}$	Thermal Shutdown Hysteresis			25		°C

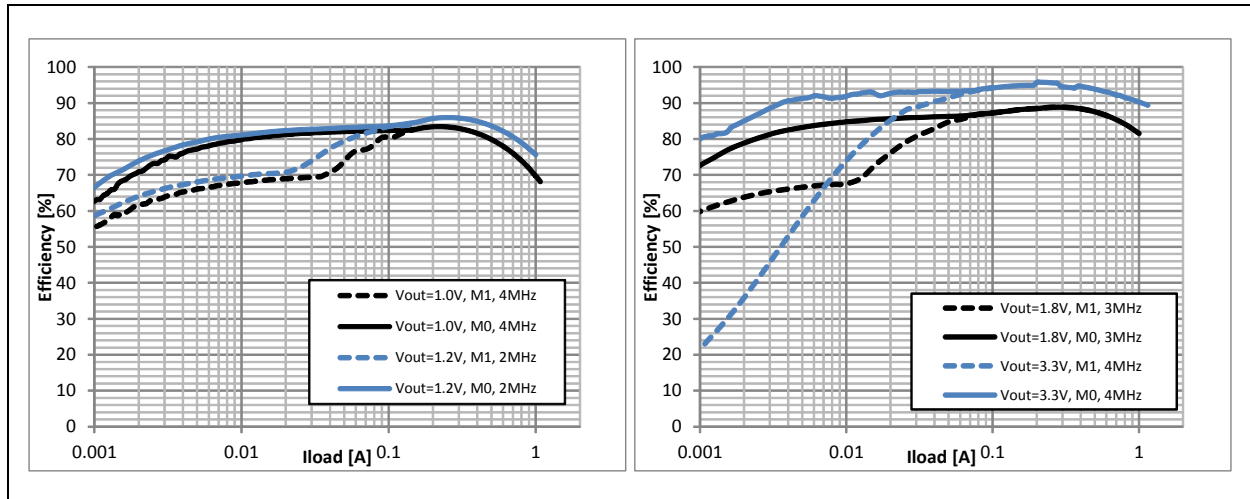**Electrical Characteristics:** Shows the Electrical Characteristics of the DCDC Converter. V_{IN} = EN = 3.7V, V_{OUT} < V_{IN} − 0.5V, T_{AMB} = −40 to 85°C (unless otherwise specified)

Note(s):

1. Guaranteed per design

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Typical Operating Characteristics

Figure 7:
Efficiency vs. Output Current for Various Output Voltages

Efficiency vs. Output Current: These figures show the Efficiency vs. Output Current for various Output Voltages. V_{IN} = 3.6V, T_{AMB} = 25°C. Murata LQM2HPN1R0MG0 coil (1uH, DCR 55mΩ).

Figure 8:
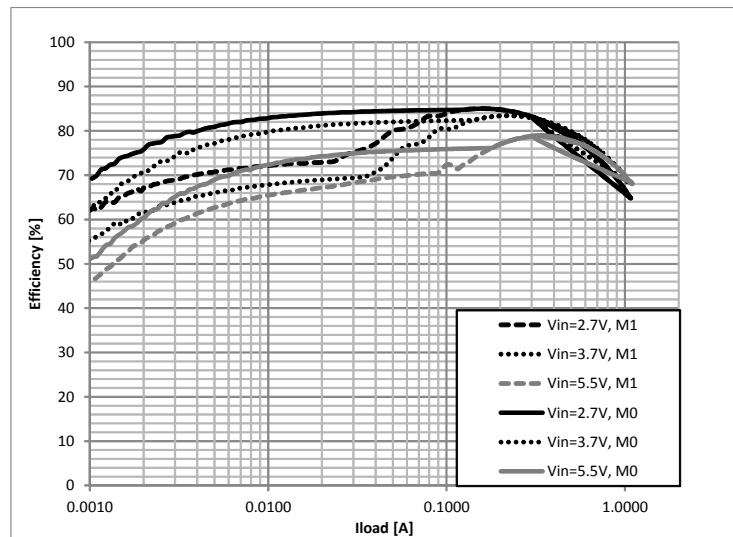**Efficiency vs. Output Current for Various Input Voltages**

Efficiency vs. Output Current: These figures show the Efficiency vs. Output Current for various Input Voltages. V_{OUT} = 1.0V, T_{AMB} = 25°C, 4MHz. Murata LQM2HPN1R0MG0 coil (1uH, DCR 55mΩ).

Efficiency vs. Input Voltage: These figures show the Efficiency vs. Input Voltage for various Load Currents. V_{OUT} = 1.2V, T_{AMB} = 25°C, 2MHz. Murata LQM2HPN1R0MG0 coil (1uH, DCR 55mΩ).

Figure 9:
Efficiency vs. Input Voltage for Various Load Currents

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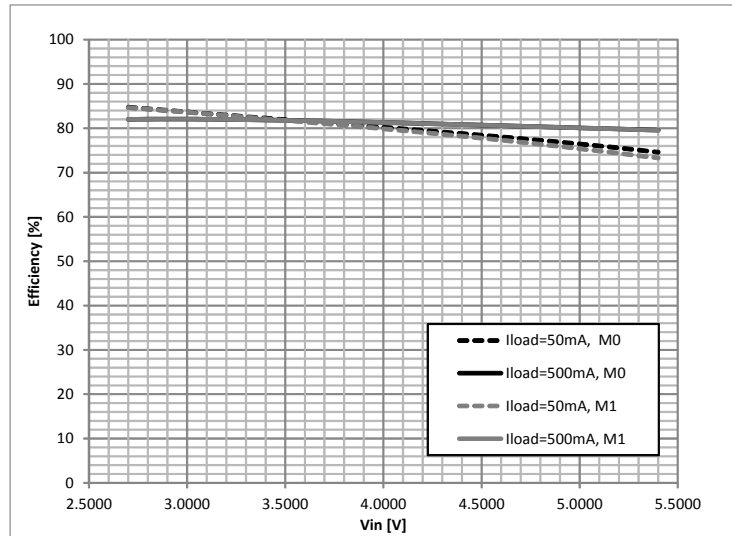
Detailed Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 96% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1A with an output capacitor of only 10μF. The implemented current limitation protects the DCDC and the coil during overload condition.

Mode Settings

Low-Ripple, Low-Noise Operation

MODE pin = high

In this mode there is no minimum coil current necessary before switching OFF the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences. Because of the inverted coil current in that case the regulator will not operate in pulse skip mode.

Figure 10:
AS1382 Low Noise Mode

coil current (200mA/div)

LX (2V/div)

VOUT (50mV/div)

time (5us/div)
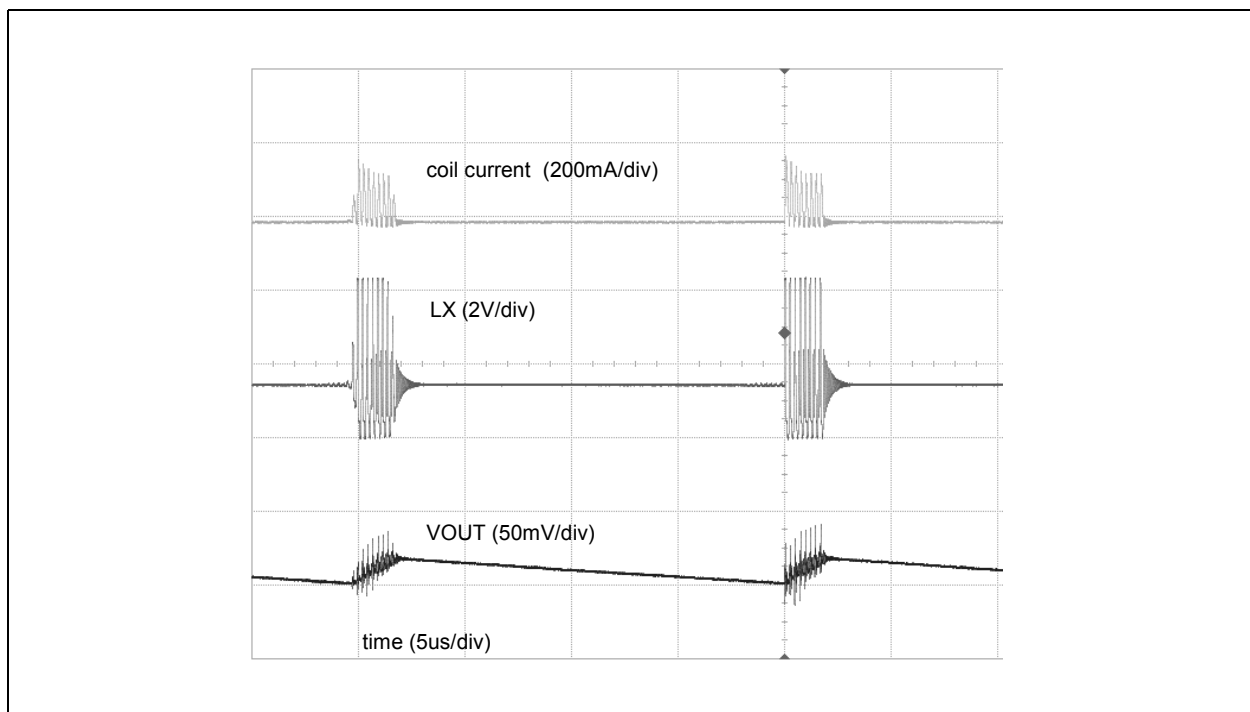
DC/DC Buck Burst Mode: Shows the DC/DC switching waveforms for low noise operation

High-Efficiency Operation

MODE pin = low

In this mode there is a minimum coil current necessary before switching OFF the PMOS. As result there are less pulses at low output load necessary, and therefore the efficiency at low output load is increased. This results in higher ripple, and noisy pulse skip operation up to a higher output current.

Figure 11:
AS1382 High Efficiency Mode

coil current (200mA/div)

LX (2V/div)

VOUT (50mV/div)

time (20us/div)
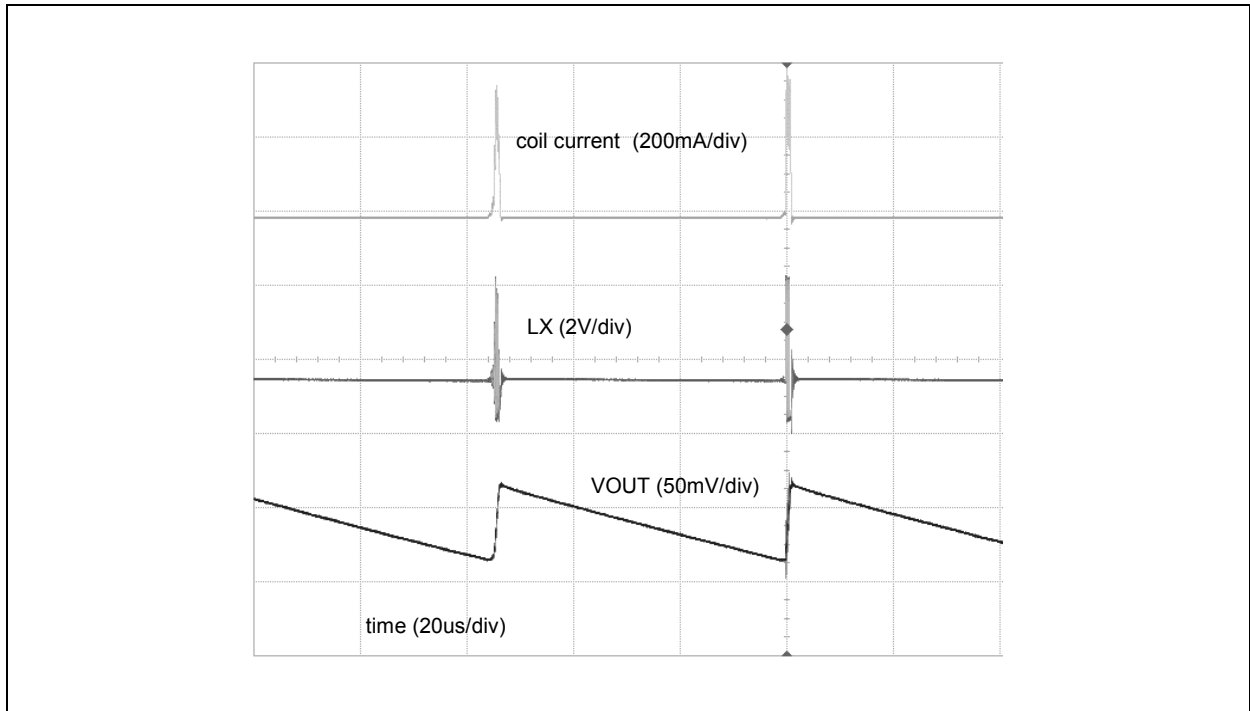
DC/DC Buck Burst Mode: Shows the DC/DC switching waveforms for high efficiency operation

It is also possible to switch between these two modes during operation.

For Example:

MODE pin = low: System is in idle state. No audio, RF signal. Decreased supply current preferred. Increased ripple doesn't affect system performance.

MODE pin = high: System is operating. Audio signal on and/or RF signal used. Decreased ripple and noise preferred. Increased power supply current can be tolerated.

Application Information

The AS1382 is perfect for mobile communications equipment like cell phones and smart phones, digital cameras and camcorders, portable MP3 and DVD players, PDA's and palmtop computers and any other handheld instruments.

Figure 12:
Typical Application Circuit
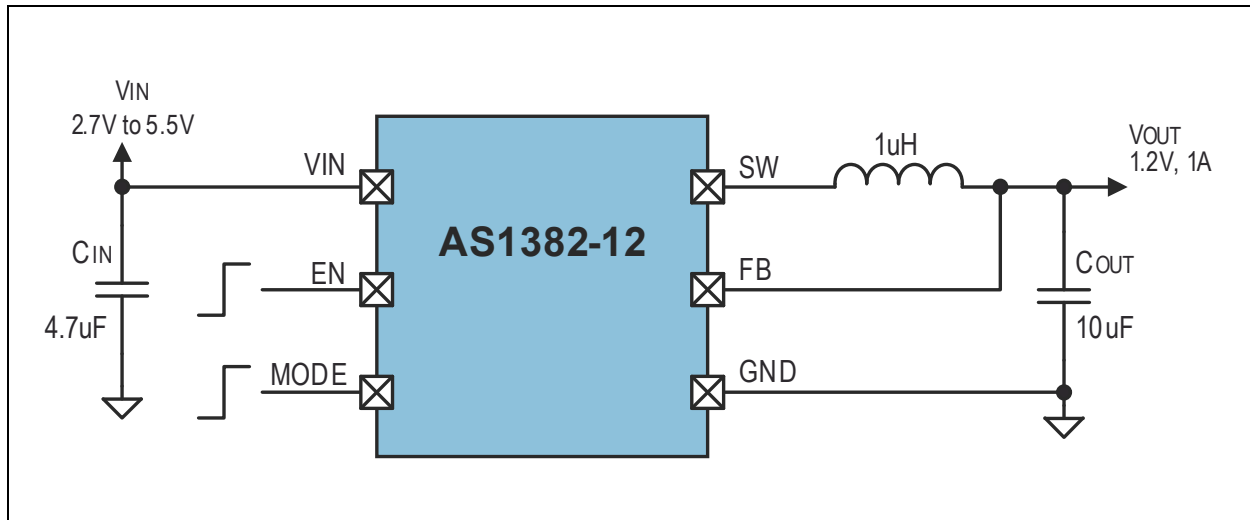
Typical Application: This figure shows the typical application of the DCDC Step Down Converter.

External Components

Inductors

Figure 13:
Recommended Inductors

Part Number	L	DCR	Current Rating	Dimensions (L/W/H)	Manufacturer
XFL4020-102	1uH	12mΩ	4.5A	4.3/4.3/2.1	www.coilcraft.com
LQM2HPN1R0MG0	1uH	55mΩ	1.6A	2.5/2.0/0.9	www.murata.com

Ceramic Input and Output Capacitors

When choosing ceramic capacitors for C_{IN} and C_{OUT}, the X5R or X7R dielectric formulations are recommended. These dielectrics have the best temperature and voltage characteristics for a given value and size. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and therefore should not be used.

Figure 14:
Recommended Input and Output Capacitors

Part Number	C	TC Code	Voltage Rating	Dimensions (L/W/H)	Manufacturer
GRM21BR61E475KA12L	4.7µF	X5R	25V	0805	www.murata.com
GRM219R60J106KE19D	10µF	X5R	6.3V	0805	www.murata.com

Because ceramic capacitors lose a lot of their initial capacitance at their maximum rated voltage, it is recommended that either a higher input capacity or a capacitance with a higher rated voltage is used.

Feedback Resistor Selection

In the AS1382-AD, the output voltage is set by an external resistor divider connected to FB. This circuitry allows for remote voltage sensing and adjustment.

Figure 15:
Adjustable Variant
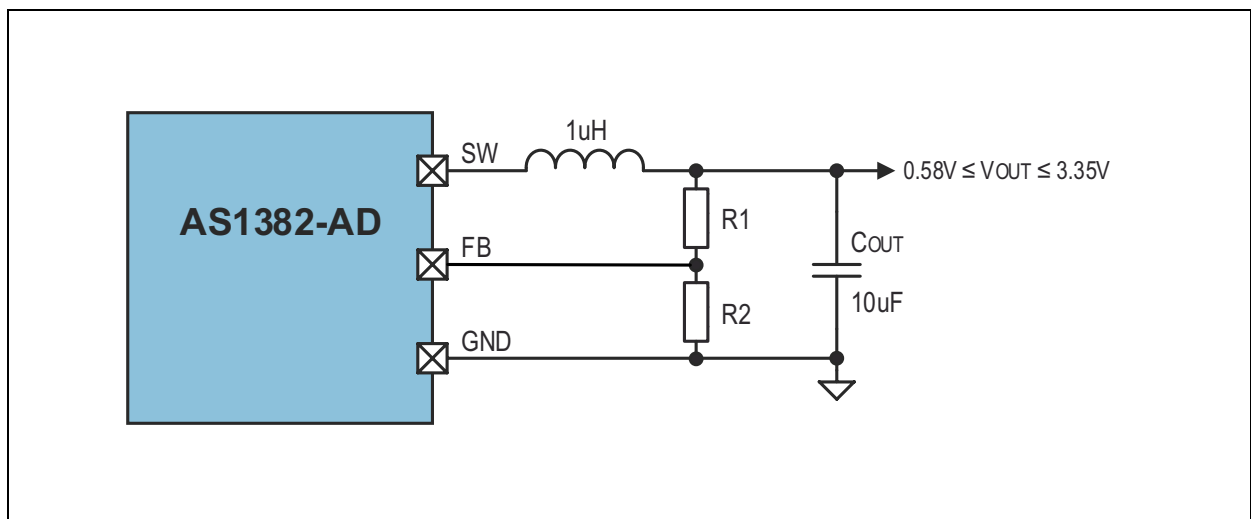
AS1382-AD: Shows the application diagram for the adjustable output version with the external resistor divider

The Resistor values for the circuit shown above can be calculated with the following equation:

**(EQ1)** $$V_{OUT} = V_{FB} \times \left[1 + \frac{R_1}{R_2} \right]$$

The output voltage can be adjusted by selecting different values for R1 and R2. For R2 a value between 10kΩ and 50kΩ is recommended. To minimize current to FB pin it is recommended to keep sum of R_1 and R_2 below 100 kΩ. It is also recommended to keep V_{IN} 500mV higher than V_{OUT}.

An optional feedback capacitor (C_{FB}) can be added in parallel with R_1 to reduce output ripple. Typical value for the C_{FB} is below 300pF

PCB Layout

Long printed circuit tracks can generate additional ripple and noise that mask correct operation and prove difficult to "de-bug" during production testing. Thus the input loop formed by C_{IN}, V_{IN} and GND pins should be minimized. Similarly, the output loop formed by C_{OUT}, VOUT and GND should also be minimized. Figure 16 shows a PCB layout example for the AS1382.

Figure 16:
PCB Layout Example For The Adjustable Variant
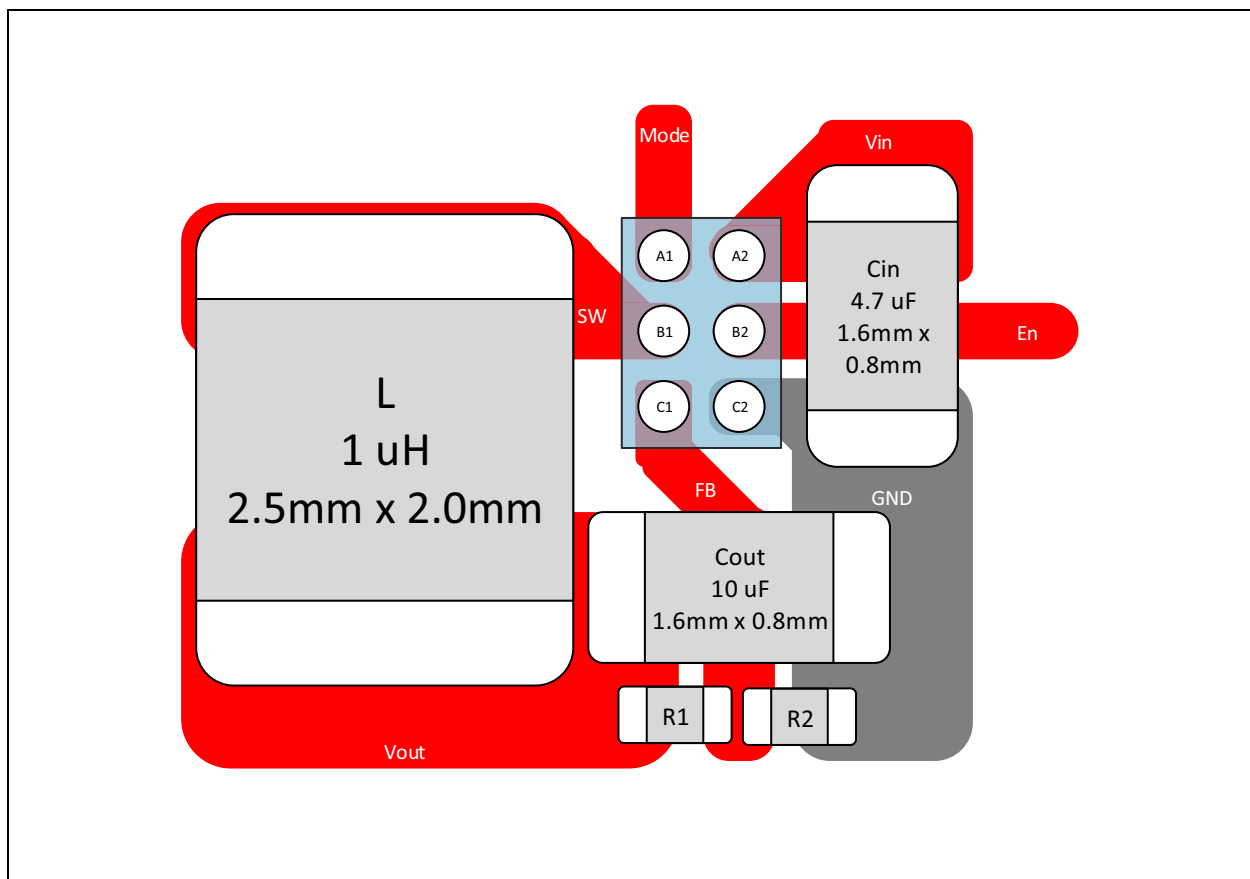
Package Drawings & Markings

Figure 17:
6 Balls WL-CSP With 0.4mm Pitch
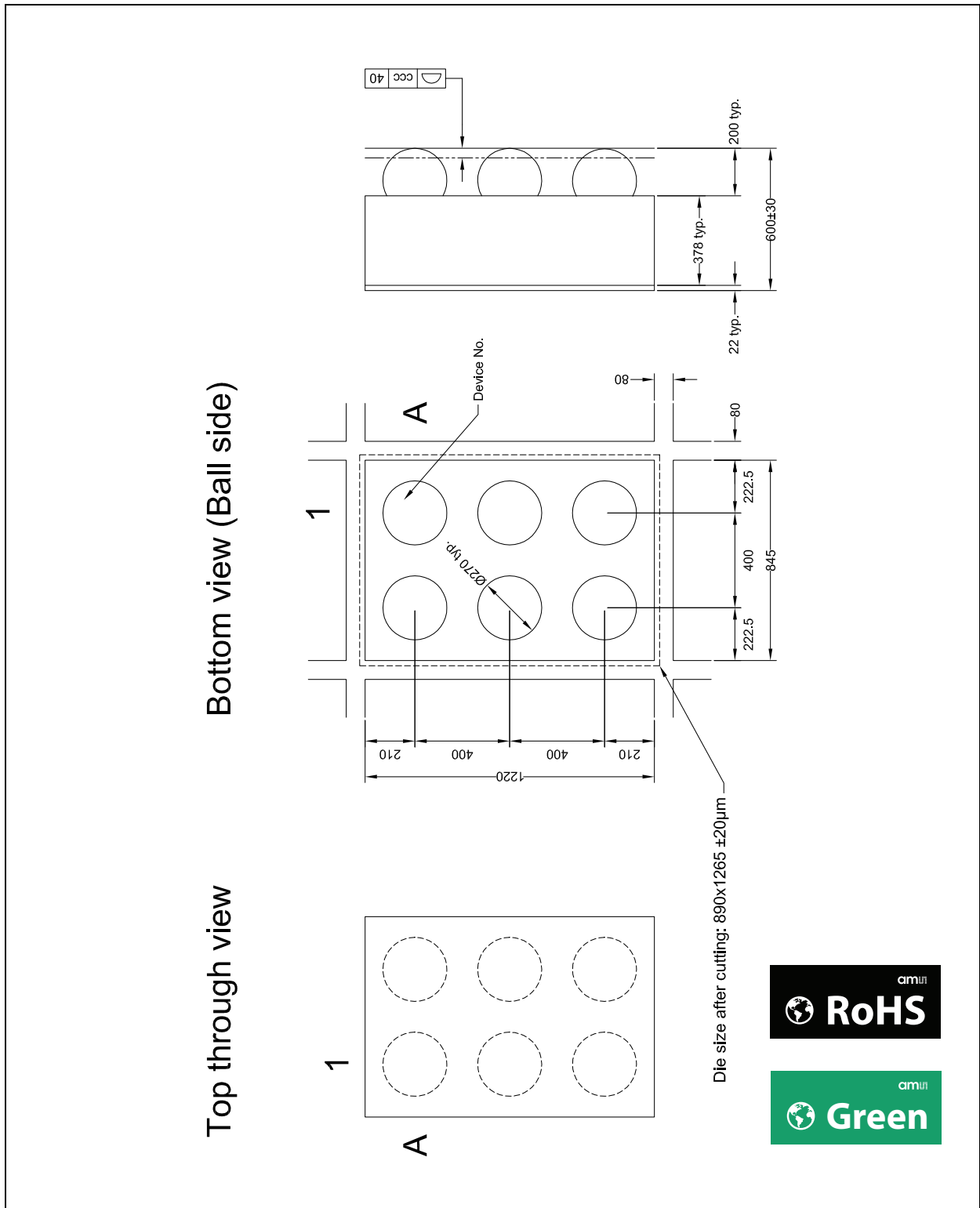
Note(s):

1. Pin 1 = A1

2. ccc Coplanarity

3. All dimensions are in µm

Figure 18:
WL-CSP Marking

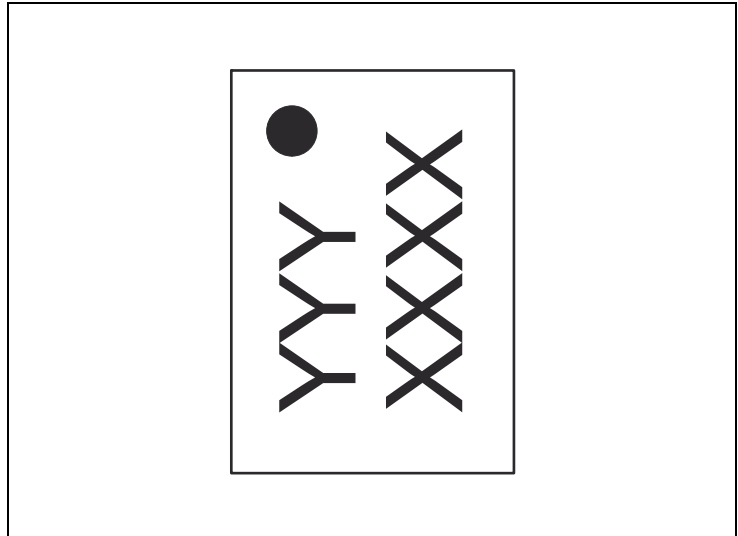**AS1382 Marking:** Shows the package marking of the WL-CSP product version

Figure 19:
Package Code

YYY	XXXX
Marking code	Tracecode

AS1382 Package Code: Shows the package code of the WL-CSP product version

Ordering & Contact Information

Figure 20:
Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1382-BWLT-ES	ABZ		Manually programmed engineering sample	T & R	6-pin WL-CSP
AS1382C-BWLT-AD	AA6	Adjustable	2MHz, 1A Synchronous DCDC Converter	T & R	6-pin WL-CSP
AS1382A-BWLT-AD	ACD	Adjustable	4MHz, 1A Synchronous DCDC Converter	T & R	6-pin WL-CSP
AS1382A-BWLT-10 [1]	AA7	1.0V	4MHz, 1A Synchronous DCDC Converter	T & R	6-pin WL-CSP
AS1382A-BWLT-12 [1]	ABW	1.2V	4MHz, 1A Synchronous DCDC Converter	T & R	6-pin WL-CSP
AS1382A-BWLT-15 [1]	ABX	1.5V	4MHz, 1A Synchronous DCDC Converter	T & R	6-pin WL-CSP
AS1382C-BWLT-18	ABY	1.8V	2MHz, 1A Synchronous DCDC Converter	T & R	6-pin WL-CSP

Ordering Information: Specifies the available variants of the AS1382

Note(s):

1. Available upon request

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Revision Information

Changes from 1-04 (2015-Jun-19) to current revision 1-05 (2016-Oct-25)	Page
Updated Figure 6 and added note below	5
Updated Equation 1	13

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.

2. Correction of typographical errors is not explicitly mentioned.