SPI Serial Persistent SRAM Memory

(AS3001401, AS3004401, AS3008401, AS3016401)

Features

- Interface
  - Serial Peripheral Interface SPI, up to 50MHz clock rate
- Technology
  - 40nm pMTJ STT-MRAM
    - Virtually unlimited Data Endurance and Data Retention (see ***Endurance & Retention*** on page *20)*
- Density
  - 1Mb, 4Mb, 8Mb, 16Mb
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
- Operating Temperature Range
  - Industrial: -40°C to 85°C
  - Industrial Plus: -40°C to 105°C
- Packages
  - 8-pad WSON (5.0mm x 6.0mm)
  - 8-pin SOIC (5.2mm x 5.2mm)
- Data Protection
  - Hardware Based
    - Write Protect Pin (WP#)
  - Software Based
    - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect [2:0])
- Supports JEDEC Reset
- RoHS & REACH Compliant

Performance

Device Operation	Typical Values	Units
Frequency of Operation	50 (maximum)	MHz
Standby Current	160 (typical)	µA
Deep Power Down Current	5 (typical)	µA
Active Read Current – (1-1-1) @ 50MHz	8 (typical)	mA
Active Write Current – (1-1-1) @ 50MHz	14 (typical)	mA

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General Description

ASxxxx401 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 1Mbit to 16Mbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile.

Figure 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance and scalable non-volatile memory technology.

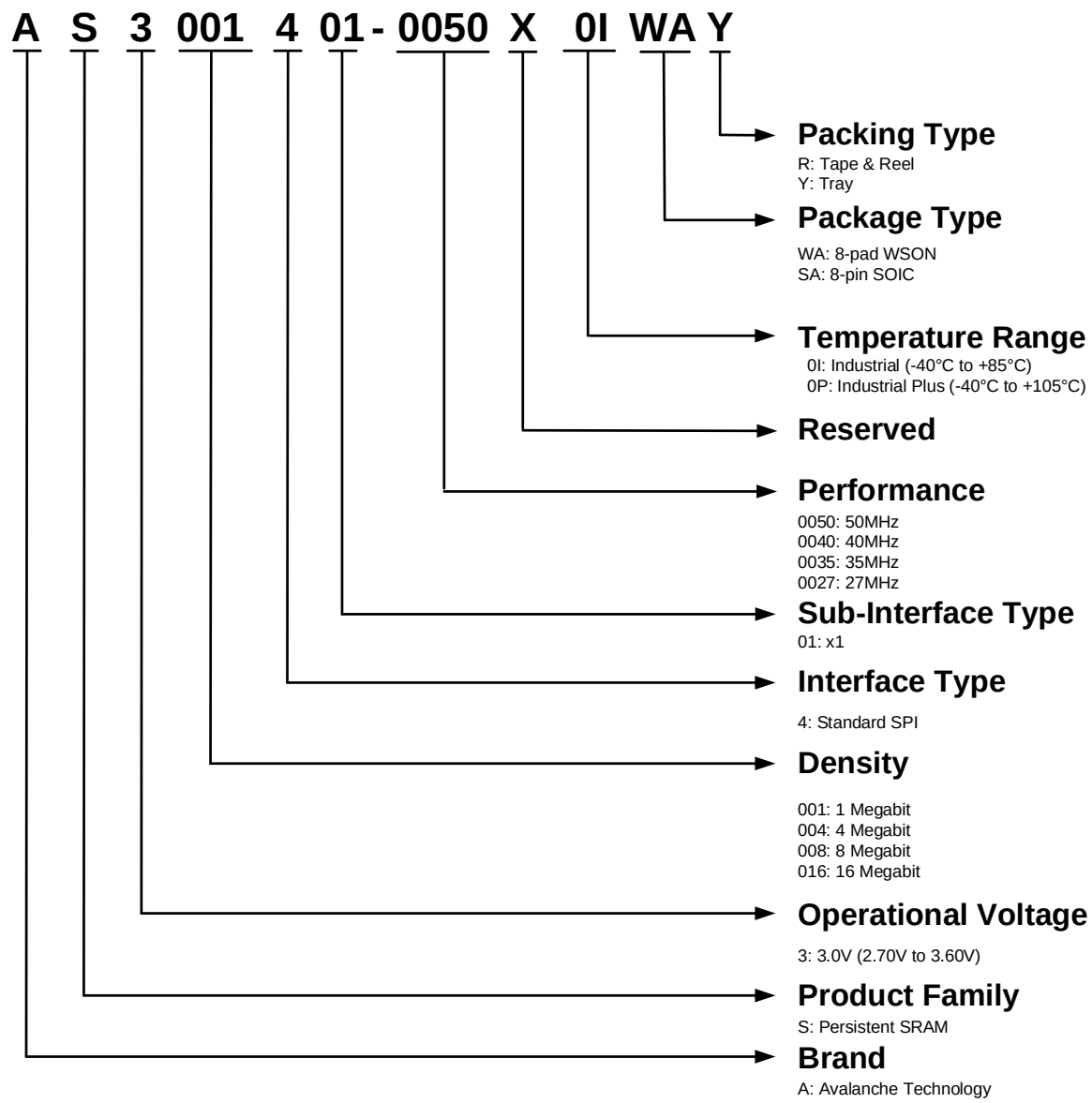
ASxxxx401 has a Serial Peripheral Interface (SPI). SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (low to high) or falling (high to low) or both edges of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

ASxxxx401 is available in small footprint 8-pad WSON and 8-pin SOIC packages. These packages are compatible with similar low-power volatile and non-volatile products.

ASxxxx401 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1: Valid Combinations List

Valid Combinations – 50MHz				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS3001401-0050X	0I, 0P	WA, SA	R, Y	AS3001401-0050X0IWAR
				AS3001401-0050X0IWAY
				AS3001401-0050X0ISAR
				AS3001401-0050X0ISAY
				AS3001401-0050X0PWAR
				AS3001401-0050X0PWAY
				AS3001401-0050X0PSAR
				AS3001401-0050X0PSAY
AS3004401-0050X	0I, 0P	WA, SA	R, Y	AS3004401-0050X0IWAR
				AS3004401-0050X0IWAY
				AS3004401-0050X0ISAR
				AS3004401-0050X0ISAY
				AS3004401-0050X0PWAR
				AS3004401-0050X0PWAY
				AS3004401-0050X0PSAR
				AS3004401-0050X0PSAY
AS3008401-0050X	0I, 0P	WA, SA	R, Y	AS3008401-0050X0IWAR
				AS3008401-0050X0IWAY
				AS3008401-0050X0ISAR
				AS3008401-0050X0ISAY
				AS3008401-0050X0PWAR
				AS3008401-0050X0PWAY
				AS3008401-0050X0PSAR
				AS3008401-0050X0PSAY
AS3016401-0050X	0I, 0P	WA, SA	R, Y	AS3016401-0050X0IWAR
				AS3016401-0050X0IWAY
				AS3016401-0050X0ISAR
				AS3016401-0050X0ISAY
				AS3016401-0050X0PWAR
				AS3016401-0050X0PWAY
				AS3016401-0050X0PSAR
				AS3016401-0050X0PSAY

Signal Description and Assignment

Figure 2: Device Pinout

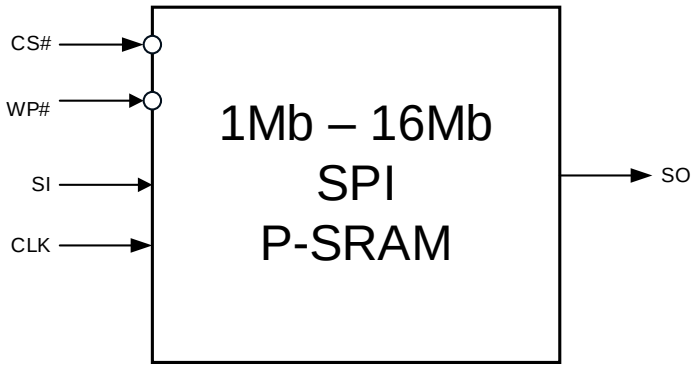


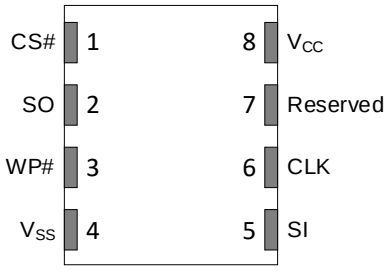
Table 2: Signal Description

Signal	Type	Description
CS#	Input	**Chip Select:** When CS# is driven High, the device will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS# Low enables the device, placing it in the active mode. After power-up, a falling edge on CS# is required prior to the start of any instructions.
WP#	Input	**Write Protect (SPI):** Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven.
CLK	Input	**Clock:** Provides the timing for the serial interface. address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock.
SI	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into the device on the rising edge of the clock in Single SPI mode.
SO	Output	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of the device on the falling edge of the clock in Single SPI mode.
V_{CC}	Supply	**V_{CC}:** Core and I/O power supply.
V_{SS}	Supply	**V_{SS}:** Core and I/O ground supply.

Package Options

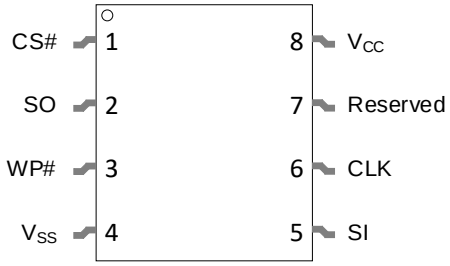
8-Pad WSON (Top View)

Figure 3: 8-Pad WSON



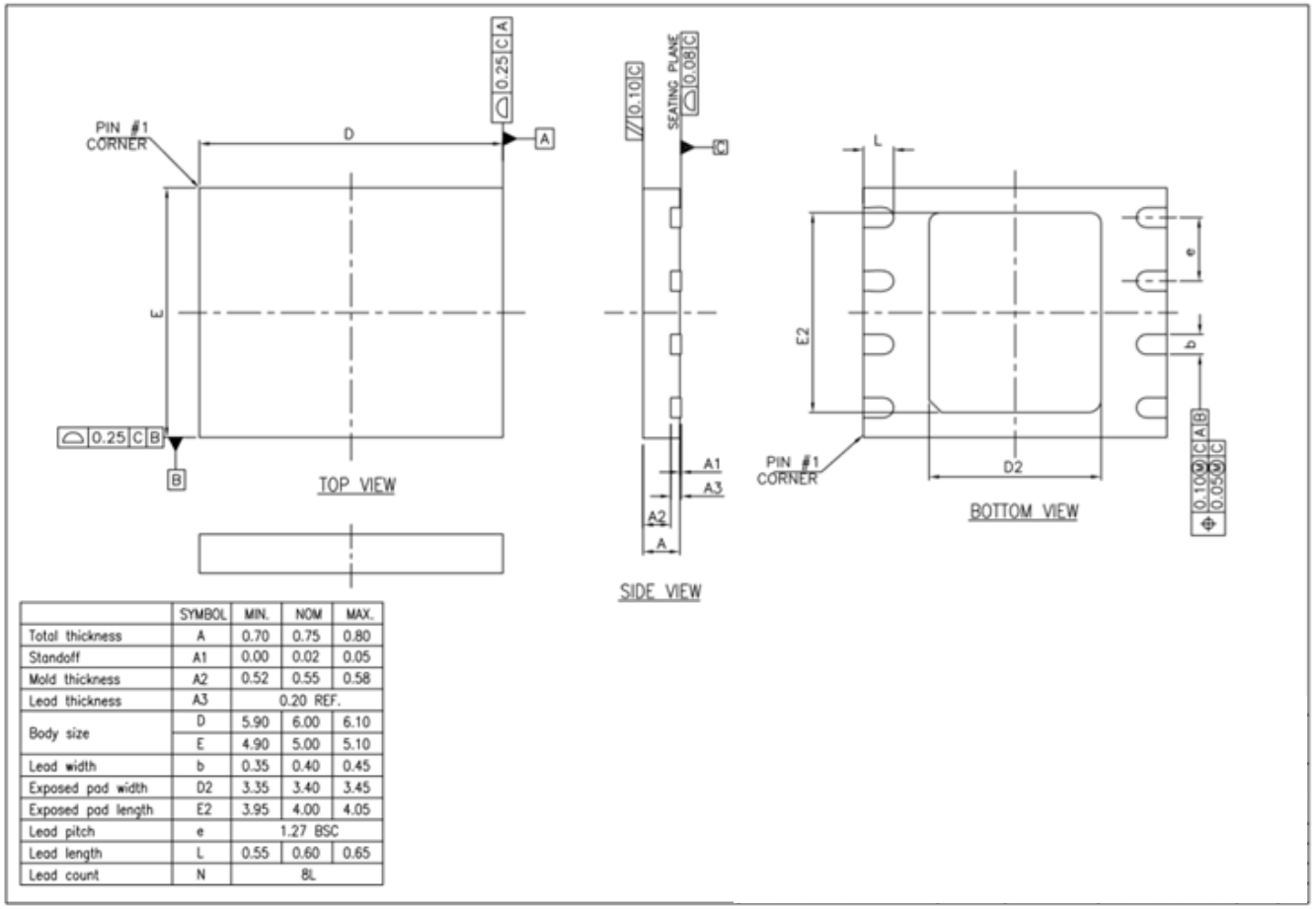
8-Pin SOIC (Top View)

Figure 4: 8-Pin SOIC



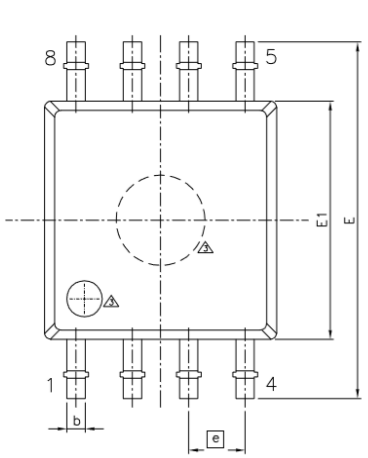
Package Drawings

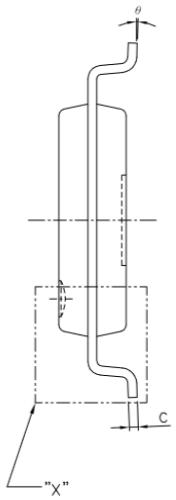
8-Pad WSON



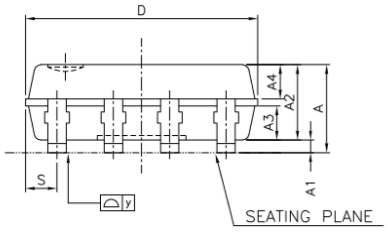
	SYMBOL	MIN.	NOM	MAX.
Total thickness	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Mold thickness	A2	0.52	0.55	0.58
Lead thickness	A3		0.20 REF.	
Body size	D	5.90	6.00	6.10
	E	4.90	5.00	5.10
Lead width	b	0.35	0.40	0.45
Exposed pad width	D2	3.35	3.40	3.45
Exposed pad length	E2	3.95	4.00	4.05
Lead pitch	e		1.27 BSC	
Lead length	L	0.55	0.60	0.65
Lead count	N		8L	

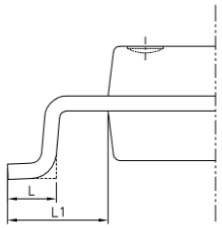
8-Pin SOIC





SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	———	———	2.16	———	———	85.04
A1	0.05	0.15	0.25	1.97	5.91	9.84
A2	1.70	1.80	1.91	66.93	70.87	75.20
A3	0.773	0.798	0.823	30.43	31.42	32.40
A4	0.773	0.798	0.823	30.43	31.42	32.40
b	0.36	0.41	0.51	14.17	16.14	20.08
C	0.19	0.20	0.25	7.48	7.87	9.84
D	5.13	5.23	5.33	201.97	205.91	209.84
E	7.70	7.90	8.10	303.15	311.02	318.90
E1	5.18	5.28	5.38	203.94	207.87	211.81
e	1.27 BSC			50 BSC		
L	0.50	0.65	0.80	19.69	25.59	31.50
L1	1.27	1.37	1.47	50.00	53.94	57.87
S	0.62	0.74	0.88	24.41	29.13	34.65
φ	0°	5°	8°	0°	5°	8°
y	———	———	0.075	———	———	2.95





DETAIL "X"

NOTE:

1. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0,15mm (6mil) PER SIDE.
2. DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUS SHALL NOT EXCEED 0,25mm (10 mil) PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER

Architecture

ASxxxx401 is a high performance serial STT-MRAM device. It features a SPI-compatible bus interface running at 50MHz, and hardware/software based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB}.

ASxxxx401 contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. The device is accessed via the SPI pins. ***Table 3*** summarizes all the different interface modes supported and their respective I/O usage. ***Table 4*** shows the clock edge used for each instruction component.

Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. 1-1-1 means command, address and data are transmitted on a single I/O.

Table 3: Interface Modes of Operations

Instruction Component	SPI (1-1-1)
Command	SI
Address	SI
Data Input	SI
Data Output	SO

Table 4: Clock Edge Used for instructions

Instruction Type	Command	Address	Data Input	Data Output
(1-1-1)	↑R	↑R	↑R	↓F

Notes:
R: Rising Clock Edge
F: Falling Clock Edge

ASxxxx401 offers both hardware and software based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array.

One lower power state is available in ASxxxx401, namely Deep Power Down. Data is not lost while the device is in either of this low power state. Moreover, the device maintains all its configurations.

Figure 5: Functional Block Diagram

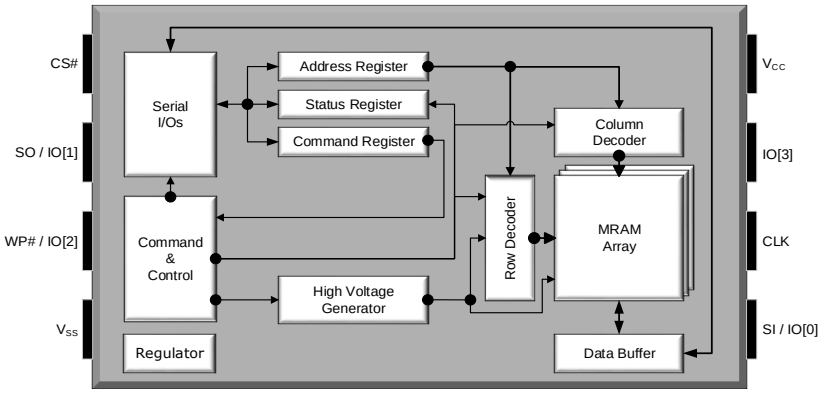


Table 5: Modes of Operation

Mode	Current	CS#	CLK	SI	SO
Standby	I_{SB}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	I_{READ}	L	Toggle	Command, Address	Data Output
Active - Write	I_{WRITE}	L	Toggle	Command, Address, Data Input	Hi-Z
Deep Power Down	I_{DPD}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z

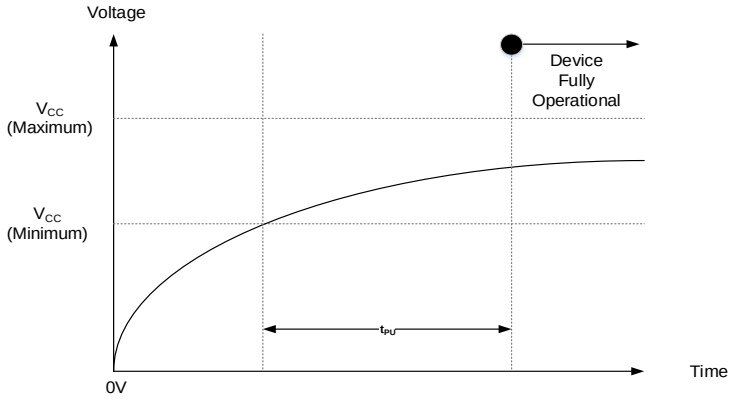
Notes:
H: High (Logic '1')
L: Low (Logic '0')
Hi-Z: High Impedance

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- Ramp up V_{CC} (R_{VR})
- CS# must follow V_{CC} during power-up (a 10KΩ pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- During initial Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences
- Upon Power-up, the device is in Standby mode

Figure 6: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- Ramp down V_{CC} (R_{VF})
- CS# must follow V_{CC} during power-down (a 10KΩ pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- The Power-up timing needs to be observed after V_{CC} goes above V_{CC} (minimum)

Figure 7: Power-Down Behavior

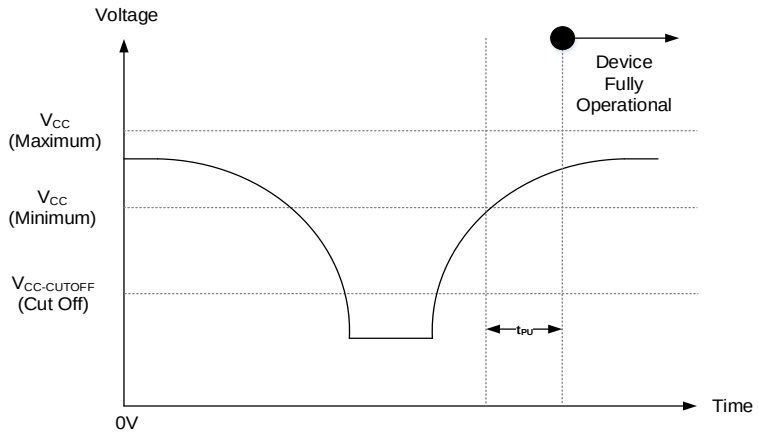


Table 6: Power Up/Down Timing – 3.0V

Parameter	Symbol	Test Conditions	3.0V			
			Minimum	Typical	Maximum	Units
V_{CC} Range	V_{CC}	All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}		250	-	-	µs
V_{CC} Cutoff – Must Initialize Device	$V_{CC-CUTOFF}$		1.6	-	-	V
Time to Enter Deep Power Down	t_{EDPD}		-	-	3	µs
Time to Exit Deep Power Down	t_{EXDPD}		-	-	400	µs
CS# Pulse Width	t_{CSDPD}		50	-	-	ns

Memory Map

Table 7: Memory Map

Density	Address Range	24-bit Address [23:0]	
1Mb	000000h – 01FFFFh	[23:17] – Logic ‘0’	[16:0] - Addressable
4Mb	000000h – 07FFFFh	[23:19] – Logic ‘0’	[18:0] - Addressable
8Mb	000000h – 0FFFFFh	[23:20] – Logic ‘0’	[19:0] - Addressable
16Mb	000000h – 1FFFFFh	[23:21] – Logic ‘0’	[20:0] - Addressable

Register Map

Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection. The register bits are initialized to their default state on device initialization. Any modifications of the bits is volatile, if power is removed then on next boot up the default state is restored.

Table 8: Status Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
SR[7]	WP#EN	Hardware Based WP# Protection Enable/Disable	R/W	0	1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	Reserved	Reserved	-	-	-
SR[5]	TBPSEL	Software Top/Bottom Memory Array Protection Selection	R/W	0	1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BPSEL[2]	Block Protect Selection Bit 2	R/W	0	Block Protection Bits (Table 9, Table ***10***)
SR[3]	BPSEL[1]	Block Protect Selection Bit 1	R/W	0	
SR[2]	BPSEL[0]	Block Protect Selection Bit 0	R/W	0	
SR[1]	WREN	Write Operation Protection Enable/Disable	R	0	1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	Reserved	R	0	Reserved for future use

Table 9: Top Block Protection Address Range Selection (TBPSEL=0)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb
0	**0**	**0**	None	None	None	None	None
0	**0**	**1**	Upper 1/64	01F800h – 01FFFFh	07E000h – 07FFFFh	0FC000h – 0FFFFFh	1F8000h – 1FFFFFh
0	**1**	**0**	Upper 1/32	01F000h – 01FFFFh	07C000h – 07FFFFh	0F8000h – 0FFFFFh	1F0000h – 1FFFFFh
0	**1**	**1**	Upper 1/16	01E000h – 01FFFFh	078000h – 07FFFFh	0F0000h – 0FFFFFh	1E0000h – 1FFFFFh
1	**0**	**0**	Upper 1/8	01C000h – 01FFFFh	070000h – 07FFFFh	0E0000h – 0FFFFFh	1C0000h – 1FFFFFh
1	**0**	**1**	Upper 1/4	018000h – 01FFFFh	060000h – 07FFFFh	0C0000h – 0FFFFFh	180000h – 1FFFFFh
1	**1**	**0**	Upper 1/2	010000h – 01FFFFh	040000h – 07FFFFh	080000h – 0FFFFFh	1F0000h – 1FFFFFh
1	**1**	**1**	All	000000h – 01FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh	000000h – 1FFFFFh

Table 10: Bottom Block Protection Address Range Selection (TBPSEL=1)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb
0	**0**	**0**	None	None	None	None	None
0	**0**	**1**	Lower 1/64	000000h – 0007FFh	000000h – 001FFFh	000000h – 003FFFh	000000h – 007FFFh
0	**1**	**0**	Lower 1/32	000000h – 00FFFh	000000h – 003FFFh	000000h – 007FFFh	000000h – 00FFFFh
0	**1**	**1**	Lower 1/16	000000h – 001FFFh	000000h – 007FFFh	000000h – 00FFFFh	000000h – 01FFFFh
1	**0**	**0**	Lower 1/8	000000h – 003FFFh	000000h – 00FFFFh	000000h – 01FFFFh	000000h – 03FFFFh
1	**0**	**1**	Lower 1/4	000000h – 007FFFh	000000h – 01FFFFh	000000h – 03FFFFh	000000h – 07FFFFh
1	**1**	**0**	Lower 1/2	000000h – 00FFFFh	000000h – 03FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh
1	**1**	**1**	All	000000h – 01FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh	000000h – 1FFFFFh

Table 11: Write Protection Modes

WREN (Status Register)	WP#EN (Status Register)	WP# (Pin)	Status Register	Memory[1] Array Protected Area	Memory[1] Array Unprotected Area
0	**X**	**X**	Protected	Protected	Protected
1	**0**	**X**	Unprotected	Protected	Unprotected
1	**1**	**Low**	Protected	Protected	Unprotected
1	**1**	**High**	Unprotected	Protected	Unprotected

Notes:
High: Logic '1'
Low: Logic '0'
X: Don't Care – Can be Logic '0' or '1'
Protected: Write protected
Unprotected: Writable
1: Memory address range protection based on Block Protection Bits

Device Identification Register (Read Only)

Device identification register contains Avalanche's Manufacturing ID along with device configuration information.

Table 12: Device Identification Register – Read Only

Bits	Avalanche Manufacturer's ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temp	Density	Freq
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Frequency
31-24	23-20	19-16	15-12	11-8	7-0
1110 0110	0001-SPI (111)	0001 - 3V	0000 - -40ºC- 85ºC	0001 - 1Mb	00000110 – 50Mhz 00000011 – 40Mhz 00000100 – 35Mhz 00000101 – 27Mhz
			0001 - -40ºC-105ºC	0010 - 4Mb	
				0011 - 8Mb	
				0100 - 16Mb	

Table 13: Memory Read Latency Cycles vs. Maximum Clock Frequency

Read Type	Latency	Max Frequency
		ASxxxx2x050xx
1-1-1	0	50MHz

Instruction Set

Table 14: Instruction Set

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	Data Bytes	Max. Frequency	Prerequisite
1	**No Operation**	NOOP 00h	•				50 MHz	
2	**Write Enable**	WREN 06h	•				50MHz	
3	**Write Disable**	WRDI 04h	•				50 MHz	
4	**Enter Deep Power Down**	DPDE B9h	•				50 MHz	
5	**Software Reset Enable**	SRTE 66h	•				50 MHz	
6	**Software Reset**	SRST 99h	•				50 MHz	SRTE
7	**Exit Deep Power Down**	DPDX ABh	•				50[7] MHz	
8	**Read Status Register**	RDSR 05h		•		1	50 MHz	
9	**Read Device ID**	RDID 9Fh		•		4	50 MHz	
10	**Write Status Register**	WRSR 01h		•		1	50 MHz	WREN
11	**Read Memory Array**	READ 03h			•	1 to ∞	50 MHz	
12	**Write Memory Array**	WRTE 02h			•	1 to ∞	50 MHz	WREN

Notes:
1: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI).
2: Registers do not wrap data during reads. Reading beyond the specified number of bytes will yield indeterminate data.

Instruction Description and Structures

All communication between a host and ASxxxx401 is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from ASxxxx401. All command, address and data information is transferred sequentially. Instructions are structured as follows:

- Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic'1').
- CLK marks the transfer of each bit.
- Each instruction starts out with an 8-bit command. The command selects the type of operation ASxxxx401 must perform. The command is transferred on the rising edges of CLK.
- The command can be stand alone or followed by address to select a memory location or register. The address is always 24-bits wide.
  - The address is transferred on the rising edges of CLK.
- The address bits are followed by data bits. For Write instructions:
  - Write data bits to ASxxxx401 are transferred on the rising edges of CLK.
- Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction. WREN bit can also be reset by executing the WRDI instruction.
- Similar to write instructions, In read instructions, the address bits are followed by data bits for read instructions:
  - Read data bits from ASxxxx401 are transferred on the falling edges of CLK.
- The entire memory array can be read from or written to using a single read or write instruction. After the staring address is entered, subsequent address are internally incremented as long as CS# is Low and CLK continues to cycle.
- All commands, address and data are shifted with the most significant bit first.

Figure 8 to **Figure 10** show the description of instruction types supported.

Figure 8: Description of (1-0-0) Instruction Type

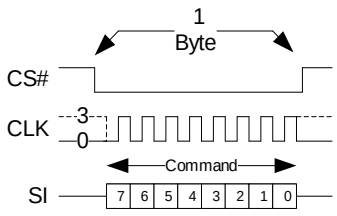


Figure 9: Description of (1-0-1) Instruction Type

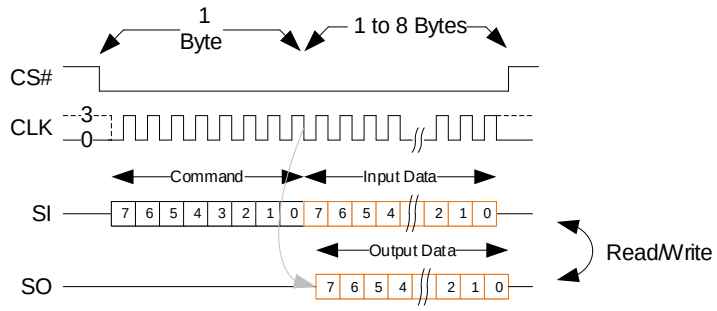
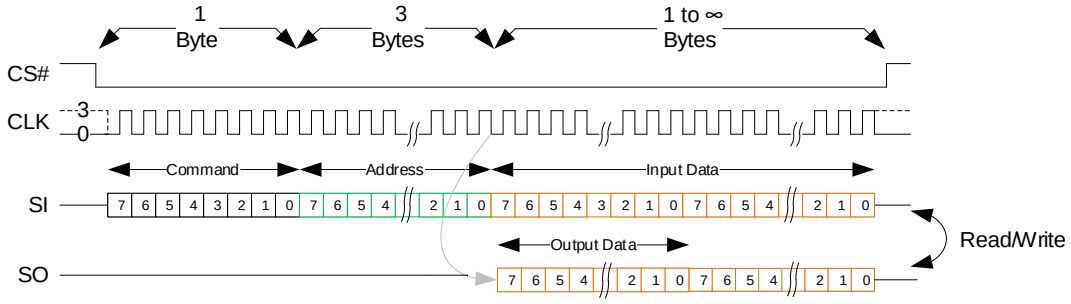


Figure 10: Description of (1-1-1) Instruction Type



Electrical Specifications

Table 15: Recommended Operating Conditions

Parameter / Condition		Minimum	Typical	Maximum	Units
Operating Temperature	Industrial	-40.0	-	85.0	°C
	Industrial Plus	-40.0	-	105.0	°C
V_{CC} Supply Voltage (3.0V)	3.0V	2.7	3.0	3.6	V
V_{SS} Supply Voltage		0.0	0.0	0.0	V

Table 16: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{IN}	5.0	pF
Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{INOUT}	6.0	pF

Table 17: Endurance & Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{14}	cycles
Data Retention	RET	105°C	10	years
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

Table 18: 3.0V DC Characteristics

Parameter	Symbol	Test Conditions		3.0V Device (2.7V-3.6V)			Units
				Minimum	Typical	Maximum	
Read Current (1-1-1)	I_{READ1}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=50MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	8	9	mA
Write Current (1-1-1)	I_{WRITE1}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=50MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	14	16	mA
Standby Current	I_{SB}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	Ta = 25ºC	-	160	-	µA
			Ta = 85ºC	-	-	500	µA
			Ta =105ºC	-	-	700	µA
Deep Power Down Current	I_{DPD}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	5	25	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-	±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-	±1.0	µA
Input High Voltage	V_{IH}			0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.3	-	0.3xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100µA		V_{CC}-0.2	-	-	V
		I_{OH} = -1mA		2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 150µA		-	-	0.2	V
		I_{OL} = 2mA		-	-	0.4	V

Absolute Maximum Ratings

Stresses greater that those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 19: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Junction Temperature	---	125	°C
Storage Temperature	-55 to 150		°C
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ |2000 V|		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ |500 V|		V
Latch-Up (I-test) JESD78	≥ |100 mA|		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

Table 20: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CC}
Input rise and fall times	3.0ns
Input and output measurement timing levels	$V_{CC}/2$
Output Load	CL = 30.0pF

CS# Operation & Timing

Figure 11: CS# Operation & Timing

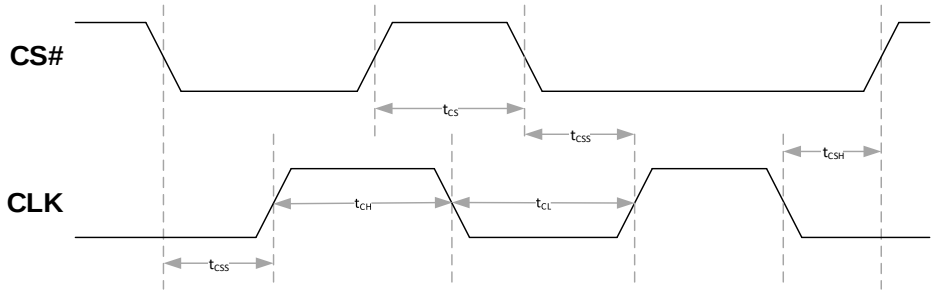


Table 21: CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1	50	MHz
Clock Low Time	t_{CL}	0.45 * 1/ f_{CLK}	-	ns
Clock High Time	t_{CH}	0.45 * 1/ f_{CLK}	-	ns
Chip Deselect Time after Read Cycle	t_{CS1}	20	-	ns
Chip Deselect Time after Register Write Cycle[1]	t_{CS2}	5	-	µs
Chip Deselect Time after Write Cycle	t_{CS3}	280	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4	-	ns

Notes:
Power supplies must be stable

Command, Address and Data Input Operation & Timing

Figure 12: Command, Address and Data Input Operation & Timing

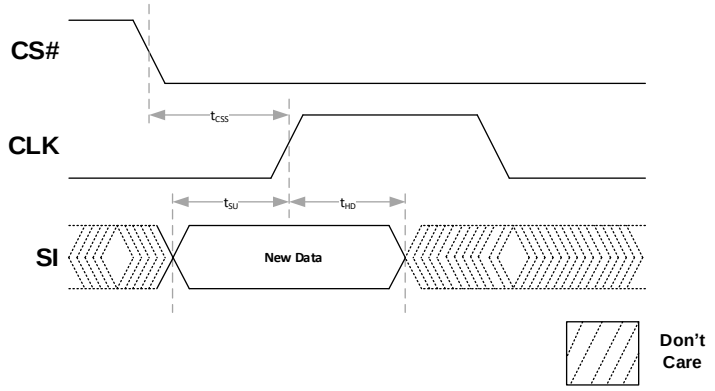


Table 22: Command, Address and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	2.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	3.0	-	ns

Notes:
Power supplies must be stable

Data Output Operation & Timing

Figure 13: Data Output Operation & Timing

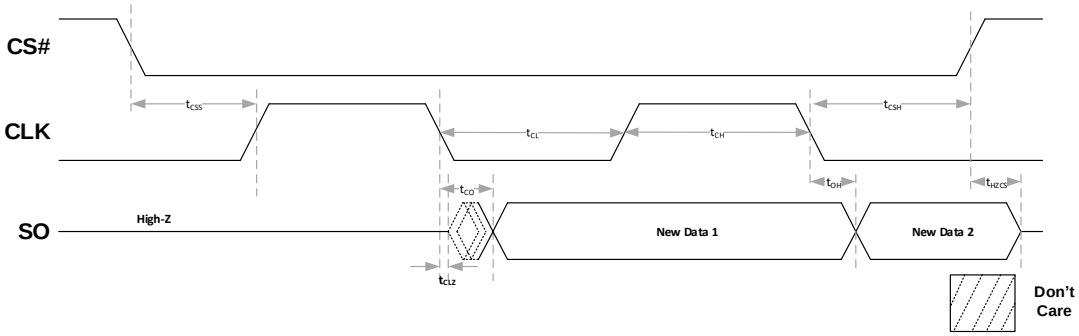


Table 23: Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	7.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	7.0	ns

Notes:
Power supplies must be stable

WP# Operation & Timing

Figure 14: WP# Operation & Timing

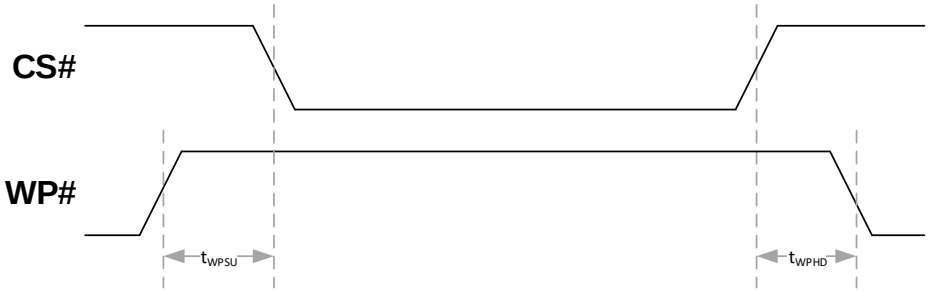


Table 24: WP# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
WP# Setup Time (w.r.t CS#)	t_{WPSU}	20	-	ns
WP# Hold Time (w.r.t CS#)	t_{WPHD}	20	-	ns

Notes:
Power supplies must be stable

JEDEC Reset Operation & Timing

Figure 15: JEDEC Reset Operation & Timing

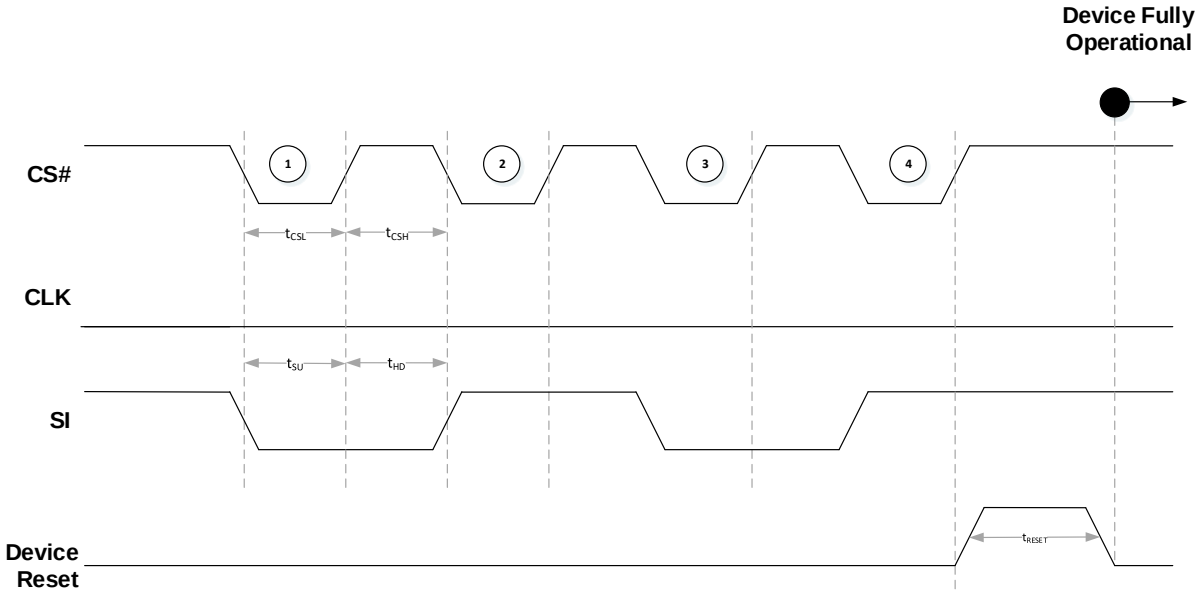


Table 25: JEDEC Reset and Software Reset Timing

Parameter	Symbol	Minimum	Maximum	Units
CS# Low Time	t_{CL}	1.0	-	µs
CS# High Time	t_{CH}	1.0	-	µs
SI Setup Time (w.r.t CS#)	t_{SU}	5.0	-	ns
SI Hold Time (w.r.t CS#)	t_{HD}	5.0	-	ns
JEDEC Hardware Reset	t_{RESET}	-	450.0	µs
Software Reset[1]	t_{SRST}	-	50.0	µs

Notes:
Power supplies must be stable
1: Software Reset timing is for Instruction based Reset (SRST)

Enter Deep Power Down Command (DPDE – B9h)

The command sequences are shown below. Executing the Enter Deep Power down (DPDE) command is the only way to put the device in the deep power down mode. The device consumption drops to I_{DP}.

The deep power down mode subsequently reduces the standby current from I_{SB} to I_{DP}. No other command must be issued while the device is in deep power down mode.

To enter the deep power down mode, CS# is driven low, following the enter deep power down (DPDE) command, CS# must be driven high after the eighth bit of the command code has been latched in or the DPDE command will not be executed. After CS# is driven high, it requires a delay of t_{EDPD} (Table 6 and 7) before the supply current is reduced to I_{DP} and the Deep Power Down mode is entered.

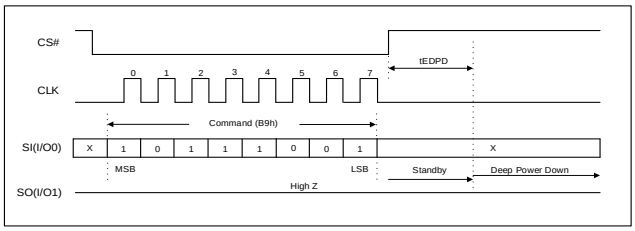


Figure 16: Enter Deep Power Down in SPI Command Sequence

Exit Deep Power Down Command (DPDX - ABh)

The command sequences are shown below. There are two ways to exit deep power down mode:

1. Toggling CS# with a CS# pulse width of tCSDPD while CLK and I/Os are Don't Care. During waking up from deep power down, I/Os remain to be in high Z.

2. Driving CS# low follows with the Exit Deep Power Down (DPDX) command. CS# must be driven high after the eight bit of the command code has been latched in or the DPDX command will not executed.

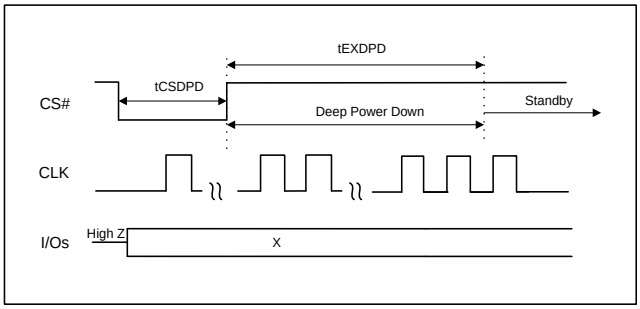


Figure 17: Exit Deep Power Down by Toggling CS#

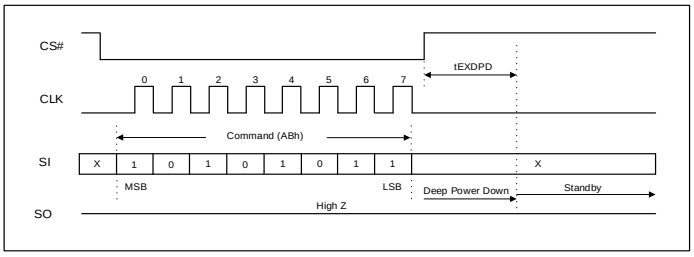


Figure 18: Exit Deep Power Down in SPI Command Sequence

It requires a delay of t_{EXDPD} (Table 6 and 7) before the device can fully exit the deep power down mode and enter standby mode. Status of all volatile bits in registers remains unchanged when the device enters or exits the deep power down mode.

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