

**Revision History****4Gb DDR4 AS4C256M16D4 - 96 ball FBGA PACKAGE**

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Aug 2019

## 256M x 16 bit DDR4 Synchronous DRAM (SDRAM)

Advance (Rev. 1.0, Aug. /2019)

### Features

- JEDEC Standard Compliant
- Fast clock rate: 1200/1333MHz
- Power supplies:
  - $V_{DD}$  &  $V_{DDQ} = +1.2V \pm 0.06V$
  - $V_{PP} = +2.5V -0.125V / +0.25V$
- Operating temperature range:
  - Commercial :  $T_C = 0\sim 95^\circ C$
  - Industrial:  $T_C = -40\sim 95^\circ C$
- Supports JEDEC clock jitter specification
- Bidirectional differential data strobe, DQS & DQS#
- Differential Clock, CK & CK#
- 8 internal banks: 2 groups of 4 banks each
- Separated IO gating structures by Bank Group
- 8n-bit prefetch architecture
- Precharge & Active power down
- Auto Refresh and Self Refresh
- Low-power auto self refresh (LPASR)
- Self Refresh Abort
- Fine Granularity Refresh
- Dynamic ODT ( $R_{TT\_PARK}$  &  $R_{TT\_Nom}$  &  $R_{TT\_WR}$ )
- Write Leveling
- DQ Training via MPR
- Programmable preamble is supported both of  $1t_{CK}$  and  $2t_{CK}$  mode
- Command/Address (CA) Parity
- Data bus write cyclic redundancy check (CRC)
- Boundary Scan Mode
- Internal  $V_{REFDQ}$  Training
- Read Preamble Training
- Control Gear Down Mode
- Per DRAM Addressability (PDA)
- Output Driver Impedance Control
- Dynamic on-die termination (ODT)
- Input Data Mask (DM) and Data Bus Inversion (DBI)
- ZQ Calibration
- Command/Address latency (CAL)
- Asynchronous Reset
- DLL enable/disable
- Burst Length (BL8/BC4/BC4 or 8 on the fly)
- Burst type: Sequential / Interleave
- CAS Latency (CL)
- CAS Write Latency (CWL)
- Additive Latency (AL): 0, CL-1, CL-2
- Average refresh period
  - 8192 cycles/64ms (7.8us at  $-40^\circ C \leq T_C \leq +85^\circ C$ )
  - 8192 cycles/32ms (3.9us at  $+85^\circ C \leq T_C \leq +95^\circ C$ )
- Data Interface: Pseudo Open Drain (POD)
- RoHS compliant
- Hard post package repair (hPPR)
- Soft post package repair (sPPR)
- Package: Pb Free and Halogen Free
  - 96-ball 7.5 x 13.5 x 1.2mm FBGA

**Table 1. Ordering Information**

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C256M16D4-83BCN	256M x 16	Commercial (Extended) 0°C to 95°C	1200	96-ball FBGA
AS4C256M16D4-83BIN	256M x 16	Industrial -40°C to 95°C	1200	96-ball FBGA
AS4C256M16D4-75BCN	256M x 16	Commercial (Extended) 0°C to 95°C	1333	96-ball FBGA
AS4C256M16D4-75BIN	256M x 16	Industrial -40°C to 95°C	1333	96-ball FBGA

**Table 2. Speed Grade Information**

Speed Grade	Clock Frequency	CAS Latency	tRCD(ns)	tRP(ns)
DDR4-2400	1200 MHz	17	14.16	14.16
DDR4-2666	1333 MHz	19	14.25	14.25

## Ball Assignment

	1	2	3	...	7	8	9
A	VDDQ	VSSQ	DQ8		UDQS#	VSSQ	VDDQ
B	VPP	VSS	VDD		UDQS	DQ9	VDD
C	VDDQ	DQ12	DQ10		DQ11	DQ13	VSSQ
D	VDD	VSSQ	DQ14		DQ15	VSSQ	VDDQ
E	VSS	UDM#/ UDBI#	VSSQ		LDM#/ LDBI#	VSSQ	VSS
F	VSSQ	VDDQ	LDQS#		DQ1	VDDQ	ZQ
G	VDDQ	DQ0	LDQS		VDD	VSS	VDDQ
H	VSSQ	DQ4	DQ2		DQ3	DQ5	VSSQ
J	VDD	VDDQ	DQ6		DQ7	VDDQ	VDD
K	VSS	CKE	ODT		CK	CK#	VSS
L	VDD	WE#/ A14	ACT#		CS#	RAS#/ A16	VDD
M	VREFCA	BG0	A10/AP		A12/ BC#	CAS#/ A15	VSS
N	VSS	BA0	A4		A3	BA1	TEN
P	Reset#	A6	A0		A1	A5	Alert#
R	VDD	A8	A2		A9	A7	VPP
T	VSS	A11	PAR		NC	A13	VDD

Figure 1. 96-Ball (FBGA Top View)

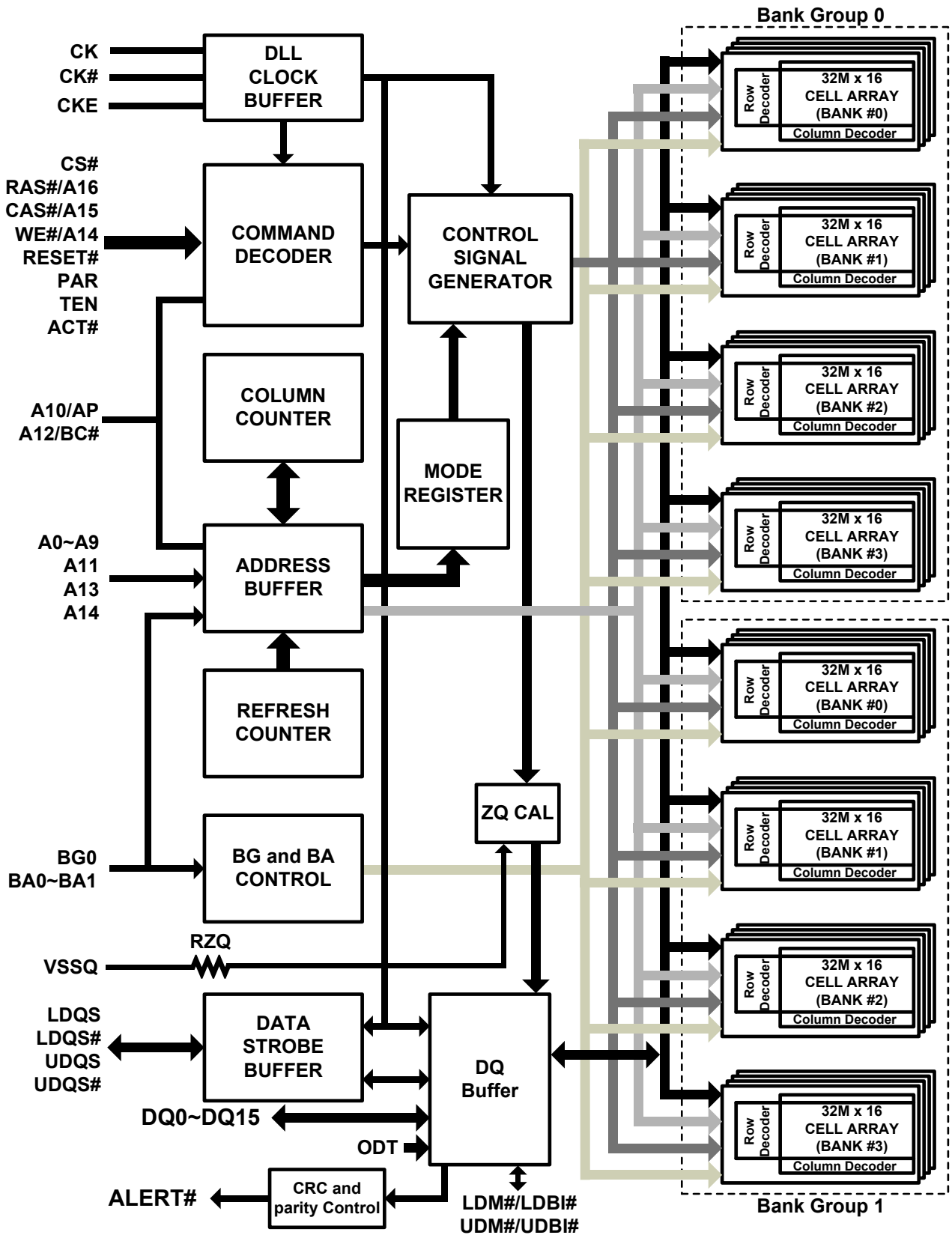
**Functional Block Diagram**


Figure 2. Block Diagram



## Ball Descriptions

Table 3. Ball Details

Symbol	Type	Description
CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE	Input	<b>Clock Enable:</b> CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power Down and Self-Refresh operation (all banks idle), or Active Power Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After $V_{REFCA}$ and Internal DQ $V_{REF}$ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#	Input	<b>Chip Select:</b> All commands are masked when CS# is registered high. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT	Input	<b>On Die Termination:</b> ODT (registered high) enables $R_{TT\_NOM}$ termination resistance internal to the DDR4 SDRAM. When enabled, ODT is applied to each DQ, LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM signal. The ODT pin will be ignored if MR1 is programmed to disable $R_{TT\_NOM}$ .
ACT#	Input	<b>Activation Command Input:</b> ACT# defines the Activation command being entered along with CS#. The input into RAS#/A16, CAS#/A15 and WE#/A14 will be considered as Row Address A16, A15 and A14.
RAS#/A16 CAS#/A15 WE#/A14	Input	<b>Command Inputs:</b> RAS#/A16, CAS#/A15 and WE#/A14 (along with CS#) define the command being entered. Those pins have multi function. For example, for activation with ACT# low, those are Addressing like A16, A15 and A14 but for non-activation command with ACT# high, those are Command pins for Read, Write and other command defined in command truth table.
LDM#/LDBI# UDM#/UDBI#	Input / Output	<b>Input Data Mask and Data Bus Inversion:</b> DM# is an input mask signal for write data. Input data is masked when DM# is sampled low coincident with that input data during a Write access. DM# is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. DBI# is an input/output identifying whether to store/output the true or inverted data. If DBI# is low the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI# is high.
BG0	Input	<b>Bank Group Inputs:</b> BG0 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0-BA1	Input	<b>Bank Address:</b> BA0-BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0-A16	Input	<b>Address Inputs:</b> Provide the row address for Activate Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC#, RAS#/A16, CAS#/A15 and WE#/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A15 and A16 are used on some higher densities.
A10/AP	Input	<b>Auto-precharge:</b> A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (high: Autoprecharge; low: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 low) or all banks (A10 high). If only one bank is to be precharged, the bank is selected by bank addresses.

A12/BC#	Input	<b>Burst Chop:</b> A12/BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (high, no burst chop; low: burst chopped). See command truth table for details.
Reset#	Input	<b>Active Low Asynchronous Reset:</b> Reset is active when Reset# is low, and inactive when Reset# is high. Reset# must be high during normal operation. Reset# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of $V_{DD}$ .
DQ0-DQ15	Input / Output	<b>Data Input/ Output:</b> Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal $V_{REF}$ level during test via Mode Register Setting MR4 A4=high. During this mode, $R_{TT}$ should be set Hi-Z.
LDQS, LDQS#, UDQS, UDQS#	Input / Output	<b>Data Strobe:</b> output with read data, input with write data. Edge-aligned with read data, centered in write data. LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. The data strobe LDQS and UDQS are paired with differential signals LDQS#, and UDQS#, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	<b>Command and Address Parity Input:</b> DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT#, RAS#/A16, CAS#/A15, WE#/A14, BG0, BA0-BA1, and A16-A0. Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK and when CS# is low.
Alert#	Input / Output	<b>Alert:</b> It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert# goes low for the period time interval and goes back high. If there is error in Command Address Parity Check, then Alert# goes low for relatively long period until ongoing DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, Alert# Pin must be bounded to $V_{DD}$ on board.
TEN	Input	<b>Connectivity Test Mode Enable:</b> Connectivity Test Mode is active when TEN is high, and inactive when TEN is low. TEN must be low during normal operation. TEN is a CMOS rail-to-rail signal with AC high and low at 80% and 20% of $V_{DD}$ (960mV for DC high and 240mV for DC low). Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to $V_{SS}$ .
NC	-	<b>No Connect:</b> These pins should be left unconnected.
$V_{DD}$	Supply	<b>Power Supply:</b> +1.2V $\pm$ 0.06V.
$V_{SS}$	Supply	<b>Ground</b>
$V_{DDQ}$	Supply	<b>DQ Power Supply:</b> +1.2V $\pm$ 0.06V.
$V_{SSQ}$	Supply	<b>DQ Ground</b>
$V_{PP}$	Supply	<b>DRAM Activating Power Supply:</b> 2.5V ( 2.375V min , 2.75V max)
$V_{REFCA}$	Supply	<b>Reference voltage for CA</b>
ZQ	Supply	<b>Reference pin for ZQ calibration.</b>
NOTE: Input only pins (BG0, BA0-BA1, A0-A16, ACT#, RAS#/A16, CAS#/A15, WE#/A14, CS#, CKE, ODT, and RESET#) do not supply termination.		



## Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally organized with eight-banks (2 bank groups each with 4 banks). The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Activate Command, which is then followed by a Read or Write command. The address bits registered coincident with the Activate Command are used to select the bank and row to be activated (BG0 select the bank group; BA0-BA1 select the bank; A0-A14 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

## Reset and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings need to be defined:

Gear down mode (MR3 A[3]) : 0 = 1/2 Rate  
Per DRAM Addressability (MR3 A[4]) : 0 = Disable  
CS# to Command/Address Latency (MR4 A[8:6]) : 000 = Disable  
CA Parity Latency Mode (MR5 A[2:0]) : 000 = Disable  
Hard Post Package Repair mode (MR4 A[13]) : 0 = Disable  
Soft Post Package Repair mode (MR4 A[5]) : 0 = Disable

## Power-up Initialization Sequence

The following sequence is required for Power up and Initialization:

1. Apply power (Reset# and TEN are recommended to be maintained below  $0.2 \times V_{DD}$ ; all other inputs may be undefined). Reset# needs to be maintained below  $0.2 \times V_{DD}$  for minimum 200us with stable power and TEN needs to be maintained below  $0.2 \times V_{DD}$  for minimum 700us with stable power. CKE is pulled "Low" anytime before Reset# being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to  $V_{DD,min}$  must be no greater than 200ms; and during the ramp,  $V_{DD} \geq V_{DDQ}$  and  $(V_{DD}-V_{DDQ}) < 0.3 V$ .  $V_{PP}$  must ramp at the same time or earlier than  $V_{DD}$  and  $V_{PP}$  must be equal to or higher than  $V_{DD}$  at all times.

During power-up, either of the following conditions may exist and must be met:

Condition A:

- $V_{DD}$  and  $V_{DDQ}$  are driven from a single power converter output, AND
- The voltage levels on all pins other than  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  must be less than or equal to  $V_{DDQ}$  and  $V_{DD}$  on one side and must be larger than or equal to  $V_{SSQ}$  and  $V_{SS}$  on the other side. In addition,  $V_{TT}$  is limited to 0.76 V max once power ramp is finished, AND
- $V_{REFCA}$  tracks  $V_{DD}/2$ .

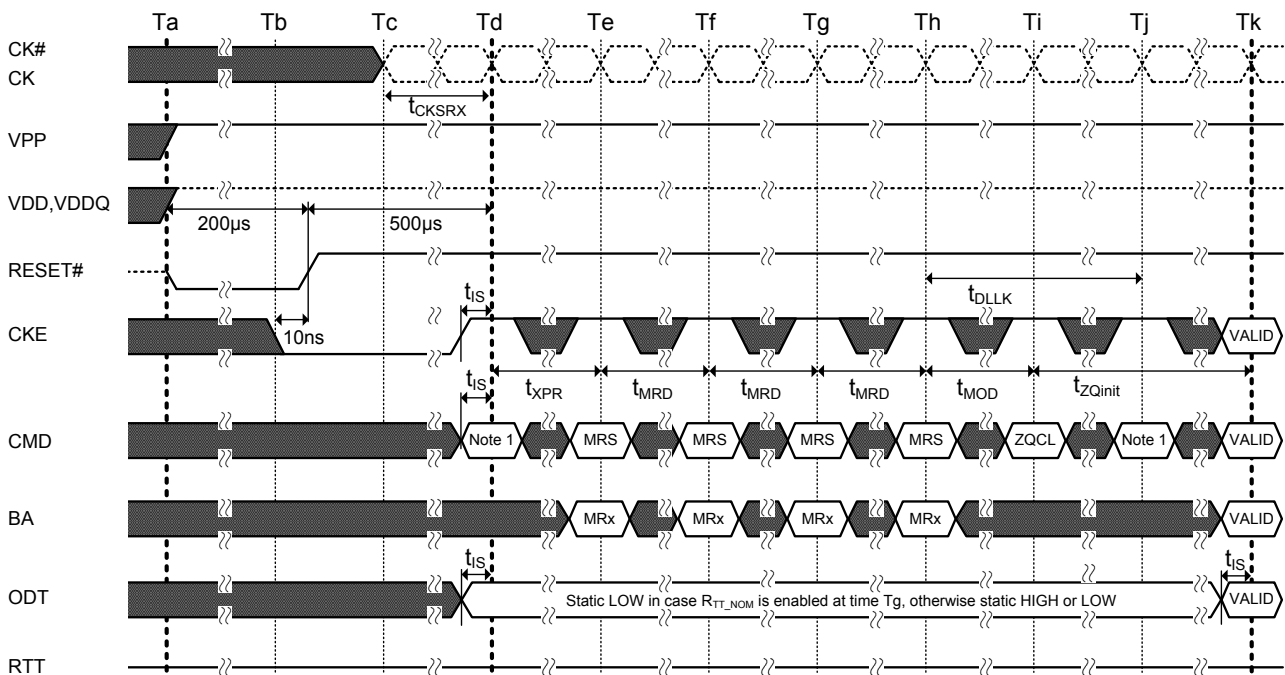
Condition B:

- Apply  $V_{DD}$  without any slope reversal before or at the same time as  $V_{DDQ}$
- Apply  $V_{DDQ}$  without any slope reversal before or at the same time as  $V_{TT}$  &  $V_{REFCA}$ .
- Apply  $V_{PP}$  without any slope reversal before or at the same time as  $V_{DD}$ .
- The voltage levels on all pins other than  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  must be less than or equal to  $V_{DDQ}$  and  $V_{DD}$  on one side and must be larger than or equal to  $V_{SSQ}$  and  $V_{SS}$  on the other side.

2. After Reset# is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.



3. Clocks (CK, CK#) need to be started and stabilized for at least 10ns or  $5t_{CK}$  (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock ( $t_{IS}$ ) must be met. Also a Deselect command must be registered (with  $t_{IS}$  set up time to clock) at clock edge Td. Once the CKE registered "high" after Reset, CKE needs to be continuously registered "high" until the initialization sequence is finished, including expiration of  $t_{DLLK}$  and  $t_{ZQinit}$ .
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as Reset# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after Reset# deassertion until CKE is registered high. The ODT input signal may be in undefined state until  $t_{IS}$  before CKE is registered high. When CKE is registered high, the ODT input signal may be statically held at either low or high. If  $R_{TT\_NOM}$  is to be enabled in MR1 the ODT input signal must be statically held low. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of  $t_{DLLK}$  and  $t_{ZQinit}$ .
5. After CKE is being registered high, wait minimum of Reset CKE Exit time,  $t_{XPR}$ , before issuing the first MRS command to load mode register. ( $t_{XPR} = \text{Max}(t_{XS}, 5nCK)$ )
6. Issue MRS Command to load MR3 with all application settings (To issue MRS command to MR3, provide "low" to BG0, "high" to BA1, BA0)
7. Issue MRS command to load MR6 with all application settings (To issue MRS command to MR6, provide "low" to BA0, "high" to BG0, BA1)
8. Issue MRS command to load MR5 with all application settings (To issue MRS command to MR5, provide "low" to BA1, "high" to BG0, BA0)
9. Issue MRS command to load MR4 with all application settings (To issue MRS command to MR4, provide "Low" to BA1, BA0, "High" to BG0)
10. Issue MRS command to load MR2 with all application settings (To issue MRS command to MR2, provide "Low" to BG0, BA0, "High" to BA1)
11. Issue MRS command to load MR1 with all application settings (To issue MRS command to MR1, provide "Low" to BG0, BA1, "High" to BA0)
12. Issue MRS command to load MR0 with all application settings (To issue MRS command to MR0, provide "Low" to BG0, BA1, BA0)
13. Issue ZQCL command to starting ZQ calibration.
14. Wait for both  $t_{DLLK}$  and  $t_{ZQinit}$  completed.
15. The DDR4 SDRAM is now ready for Read/Write training (include  $V_{REF}$  training and Write leveling).



NOTE 1. From time point "Td" until "Tk" DES commands must be applied between MRS and ZQCL commands.

NOTE 2. MRS Commands must be issued to all Mode Registers that have defined settings.

?? TIME BREAK    ■ DON'T CARE

**Figure 4. RESET# and Initialization Sequence at Power-on Ramping**

## V<sub>DD</sub> Slew rate at Power-up Initialization Sequence

**Table 4. V<sub>DD</sub> Slew Rate**

Symbol	Min.	Max.	Units	Notes
V <sub>DD_sl</sub>	0.004	600	V/ms	1,2
V <sub>DD_ona</sub>	-	200	ms	3

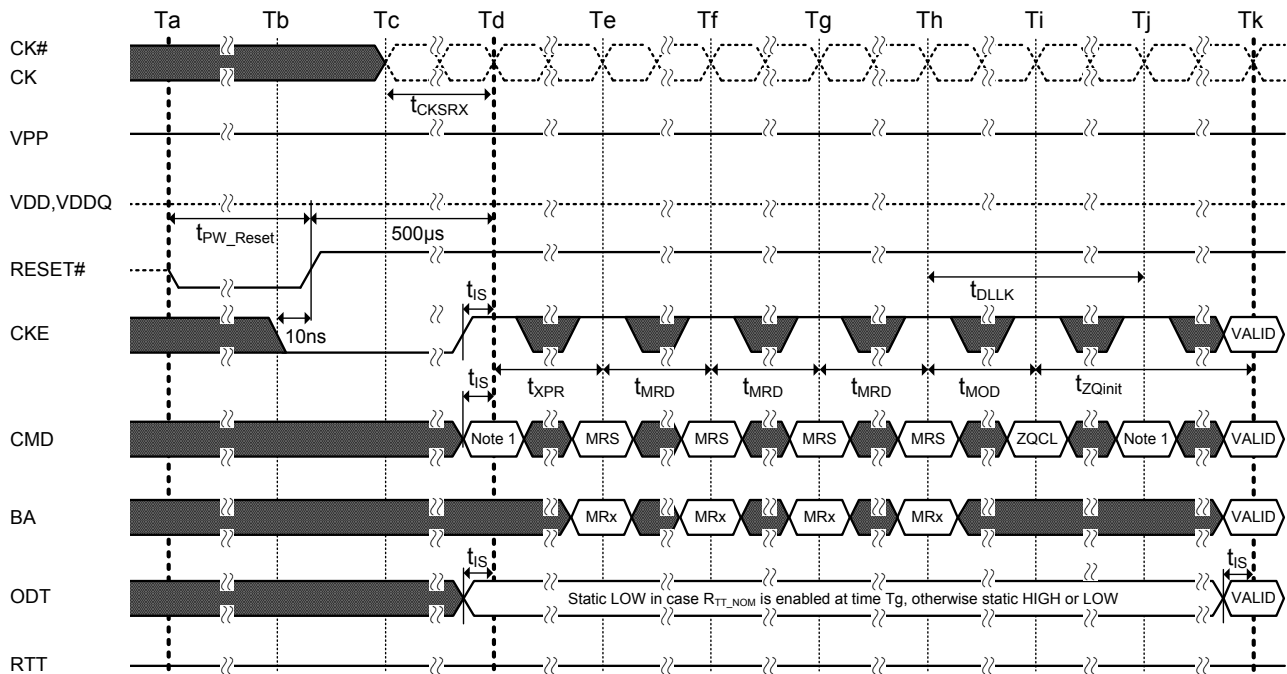
Notes:

1. Measurement made between 300mv and 80% V<sub>DD</sub> minimum.
2. 20 MHz bandlimited measurement.
3. Maximum time to ramp V<sub>DD</sub> from 300 mv to V<sub>DD</sub> minimum.

## Reset Initialization with Stable Power

The following sequence is required for Reset at no power interruption initialization:

1. Asserted Reset# below 0.2 x V<sub>DD</sub> anytime when reset is needed (all other inputs may be undefined). Reset# needs to be maintained for minimum t<sub>PW\_Reset</sub>. CKE is pulled "low" before Reset# being de-asserted (min. time 10 ns).
2. Follow steps 2 to 10 in "Power-up Initialization Sequence".
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include V<sub>REF</sub> training and Write leveling)



**NOTE 1.** From time point "Td" until "Tk" DES commands must be applied between MRS and ZQCL commands.

**NOTE 2.** MRS Commands must be issued to all Mode Registers that have defined settings.

⌘ TIME BREAK    ■ DON'T CARE

**Figure 5. Reset Procedure at Power Stable**

## Operation Mode Truth Table

Notes 1, 2, 3 and 4 apply to the entire Command Truth Table.

Note 5 Applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid].

**Table 5. Command Truth Table**

Function	Symbol	CKE <sub>n-1</sub>	CKE <sub>n</sub>	CS#	ACT#	RAS# /A16	CAS# /A15	WE# /A14	BG0	BA0-1	BC#/ A12	A13, A11	A10/ AP	A0-A9
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	OP Code			
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V
Self Refresh Entry <sup>7,9</sup>	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V
Self Refresh Exit <sup>7-10</sup>	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X
				L	H	H	H	H	H	V	V	V	V	V
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	L	V
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	H	V
RFU	RFU	H	H	L	H	L	H	H	RFU	RFU	RFU	RFU	RFU	RFU
Bank Activate	ACT	H	H	L	L	RA	RA	RA	BG	BA	RA	RA	RA	RA
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	L	CA
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	L	V	L	CA
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	H	V	L	CA
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	H	CA
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	L	V	H	CA
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	H	V	H	CA
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	L	CA
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	L	V	L	CA
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	H	V	L	CA
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	H	CA
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	L	V	H	CA
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	H	V	H	CA
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X
Power Down Entry <sup>6</sup>	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X
Power Down Exit <sup>6</sup>	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	H	V
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	L	V

Note 1. All DDR4 SDRAM commands are defined by states of CS#, ACT#, RAS#/A16, CAS#/A15, WE#/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When ACT# = H; pins RAS#/A16, CAS#/A15, and WE#/A14 are used as command pins RAS#, CAS#, and WE# respectively. When ACT# = L; pins RAS#/A16, CAS#/A15, and WE#/A14 are used as address pins A16, A15, and A14 respectively.

Note 2. Reset# is low enable command which will be used only for asynchronous reset so must be maintained high during any function.

Note 3. Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.

Note 4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

Note 5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

Note 6. The Power Down Mode does not perform any refresh operation.

Note 7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

Note 8. Controller guarantees self refresh exit to be synchronous.

Note 9. V<sub>PP</sub> and V<sub>REF</sub>(V<sub>REFCA</sub>) must be maintained during Self Refresh operation.

Note 10. The No Operation (NOP) command may be used only when entering gear-down mode.

Note 11. Refer to the CKE Truth Table for more detail with CKE transition.

**Table 6. CKE Truth Table**

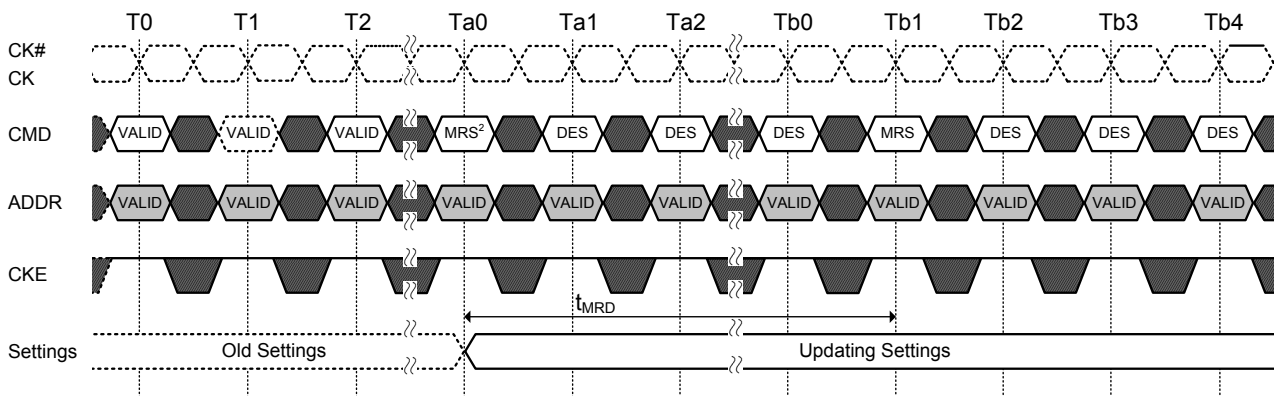
Current State <sup>(2)</sup>	CKEn-1 <sup>(1)</sup>	CKEn <sup>(1)</sup>	Command n <sup>(3)</sup> RAS#, CAS#, WE#, CS#	Action n <sup>(3)</sup>	Notes
Power-Down	L	L	X	Maintain Power-Down	14,15
	L	H	Deselect	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	Deselect	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	Deselect	Active Power-Down Entry	11,13,14
Reading	H	L	Deselect	Power-Down Entry	11,13,14,17
Writing	H	L	Deselect	Power-Down Entry	11,13,14,17
Precharging	H	L	Deselect	Power-Down Entry	11,13,14,17
Refreshing	H	L	Deselect	Precharge Power-Down Entry	11
All Banks Idle	H	L	Deselect	Precharge Power-Down Entry	11,13,14,18
	H	L	Refresh	Self-Refresh	9,13,18
See Command Truth Table for additional command details					10

**Notes:**

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge n.
3. Command n is the command registered at clock edge n, and Action n is a result of command n, ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. During any CKE transition (registration of CKE H → L or CKE L → H) the CKE level must be maintained until 1nCK prior to t<sub>CKEmin</sub> being satisfied (at which time CKE may transition again).
7. Deselect and NOP are defined in the Command Truth Table.
8. On Self Refresh Exit Deselect commands must be issued on every clock edge occurring during the t<sub>XS</sub> period. Read or ODT commands may be issued only after t<sub>XSDLL</sub> is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are Deselect only.
12. Valid commands for Self Refresh Exit are Deselect only. except for Gear Down mode. NOP is allowed for the mode.
13. Self Refresh cannot be entered during Read or Write operations. For a detailed list of restrictions see section "Self-Refresh Operation" and see section "Power-Down Modes".
14. The Power Down does not perform any refresh operations.
15. "X" means "don't care" (including floating around V<sub>REF</sub>) in Self Refresh and Power Down. It also applies to Address pins.
16. V<sub>PP</sub> and V<sub>REF</sub> (V<sub>REFCA</sub>) must be maintained during Self Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered.
18. 'Idle state' is defined as all banks are closed (t<sub>RP</sub>, t<sub>DAL</sub>, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t<sub>MRD</sub>, t<sub>MOD</sub>, t<sub>RFC</sub>, t<sub>ZQinit</sub>, t<sub>ZQoper</sub>, t<sub>ZQCS</sub>, etc.) as well as all Self Refresh exit and Power Down Exit parameters are satisfied (t<sub>XS</sub>, t<sub>XP</sub>, etc).

## Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR<sub>n</sub>) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. MRS Commands can be issued only when DRAM is at idle state. The mode register set command cycle time,  $t_{MRD}$  is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in the  $t_{MRD}$  timing figure.



NOTE 1. This timing diagram shows C/A Parity Latency mode is "Disable" case.

NOTE 2. List of MRS commands exception that do not apply to  $t_{MRD}$

- Gear down mode
- C/A Parity Latency mode
- CS to Command/Address Latency mode
- Per DRAM Addressability mode
- $V_{REFDQ}$  training Value,  $V_{REFDQ}$  Training mode and  $V_{REFDQ}$  training Range.

?? TIME BREAK ■ DON'T CARE

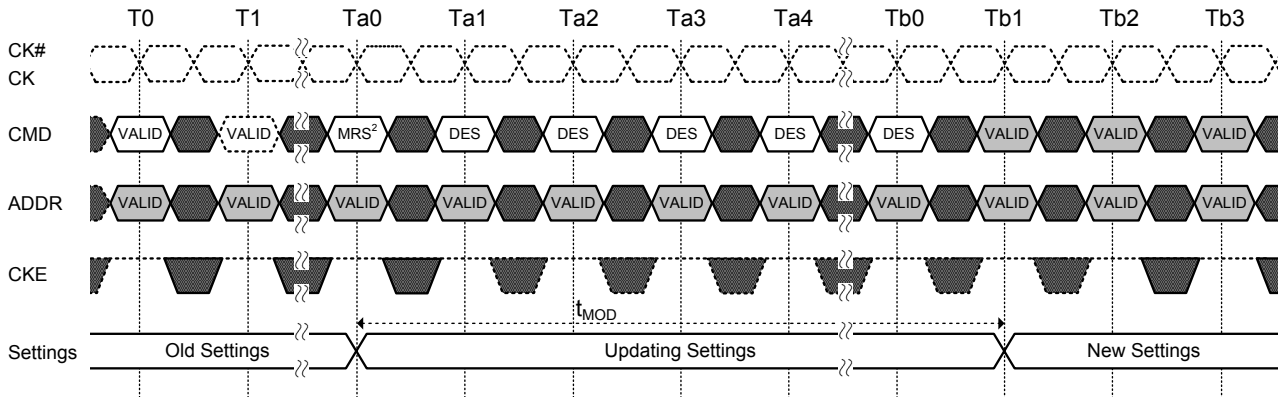
**Figure 6.  $t_{MRD}$  timing**

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

The MRS commands that do not apply  $t_{MRD}$  timing to next MRS command. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

The most MRS command to Non-MRS command delay,  $t_{MOD}$ , is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES, as shown in the  $t_{MOD}$  timing figure.

Some of the mode register setting cases, function updating takes longer than  $t_{MOD}$ . The MRS commands that do not apply  $t_{MOD}$  timing to next valid command excluding DES is listed in Note 2 of  $t_{MOD}$  timing figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



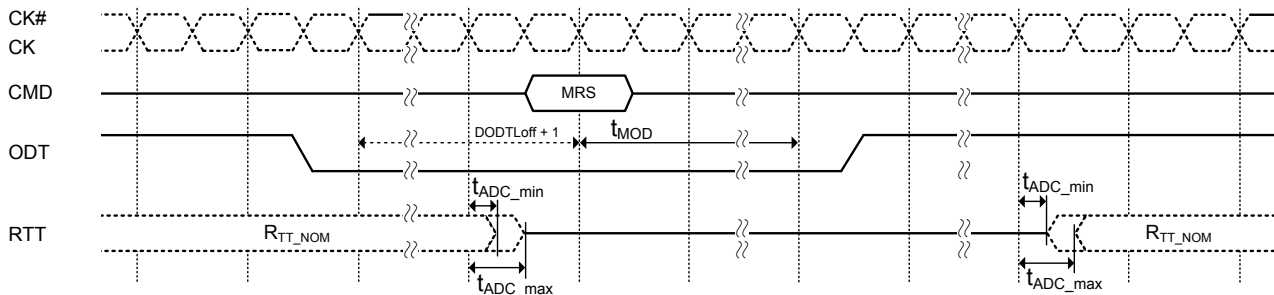
NOTE 1. This timing diagram shows C/A Parity Latency mode is "Disable" case.

NOTE 2. List of MRS commands exception that do not apply to  $t_{MOD}$

- DLL Enable, DLL Reset
- $V_{REFDQ}$  training Value, internal  $V_{REF}$  Monitor,  $V_{REFDQ}$  Training mode and  $V_{REFDQ}$  training Range
- Gear down mode
- Per DRAM addressability mode
- CA Parity mode

?? TIME BREAK ■ DON'T CARE

**Figure 7.  $t_{MOD}$  timing**



NOTE 1. This timing diagram shows C/A Parity Latency mode is "Disable" case.

NOTE 2. When an MRS command mentioned in this note affects  $R_{TT\_NOM}$  turn on timings,  $R_{TT\_NOM}$  turn off timings and  $R_{TT\_NOM}$  value, this means the MR register value changes. The ODT signal should set to be low for at least  $DODTLoFF + 1$  clock before their affecting MRS command is issued and remain low until  $t_{MOD}$  expires. The following MR registers affects  $R_{TT\_NOM}$  turn on timings,  $R_{TT\_NOM}$  turn off timings and  $R_{TT\_NOM}$  value and it requires ODT to be low when an MRS command change the MR register value. If there are no change the MR register value that correspond to commands mentioned in this note, then ODT signal is not require to be low.

- DLL control for precharge power down
- Additive latency and CAS read latency
- DLL enable and disable
- CAS write latency
- CA Parity mode
- Gear down mode
- $R_{TT\_NOM}$

**Figure 8. ODT Status at MRS affecting ODT turn-on/off timing**

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state, i.e., all banks are in the precharged state with  $t_{RP}$  satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If  $R_{TT\_NOM}$  function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring  $R_{TT\_NOM}$  is in an off state prior to MRS command affecting  $R_{TT\_NOM}$  turn-on and off timing. The ODT signal may be registered high after  $t_{MOD}$  has expired. ODT signal is a don't care during MRS command if DRAM  $R_{TT\_NOM}$  function is disabled in the mode register prior and after an MRS command.

## Mode Register MR0

**Table 7. MR0 Definition**

BG0	BA1	BA0	RAS# /A16	CAS# /A15	WE# A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0 <sup>1</sup>	0 <sup>1</sup>	WR & RTP <sup>2,3</sup>			DLL Rst	TM	CL			BT	CL	BL	

A8	DLL Reset
0	No
1	Yes

A7	Test Mode
0	Normal

A3	Read Burst Type
0	Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A11	A10	A9	WR	RTP
0	0	0	10	5
0	0	1	12	6
0	1	0	14	7
0	1	1	16	8
1	0	0	18	9
1	0	1	20	10

A6	A5	A4	A2	CAS Latency
0	0	0	0	9
0	0	0	1	10
0	0	1	0	11
0	0	1	1	12
0	1	0	0	13
0	1	0	1	14
0	1	1	0	15
0	1	1	1	16
1	1	0	1	17

Write Recovery and Read to Precharge for auto precharge

Note 1. Reserved for future use and must be programmed to 0 during MR.

Note 2. WR (write recovery for autoprecharge)min in clock cycles is calculated following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with  $t_{RP}$  to determine  $t_{DAL}$ .

Note 3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.

## CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal read command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL):  $RL = AL + CL$ .

## Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1 places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7] = 1.

## DLL Reset

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL reset function has been issued. After the DLL is enabled, a subsequent DLL reset should be applied. Any time the DLL reset function is used,  $t_{DLLK}$  must be met before functions requiring the DLL can be used. (For example, Read commands or ODT synchronous operations).



## Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 of Mode Register MR0. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. The burst length is defined by bits A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

**Table 8. Burst Type and Burst Order**

Burst Length	Read/Write	Starting Column Address			Burst type = Sequential (decimal) A3=0	burst type = Interleaved (decimal) A3=1	Note
		A2	A1	A0			
4 Chop	Read	0	0	0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	1, 2, 3
		0	0	1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	
		0	1	0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	
		0	1	1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	
		1	0	0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	
		1	0	1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	
		1	1	0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	
	1	1	1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T		
	Write	0	V	V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 2, 4, 5
		1	V	V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	
8	Read	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2
		0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
	Write	1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
		V	V	V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2, 4

**Notes:**

- In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for  $t_{WR}$  and  $t_{WTR}$  will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for  $t_{WR}$  and  $t_{WTR}$  will not be pulled in by two clocks.
- 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
- T: Output driver for data and strobes are in high impedance.
- V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
- X: Don't Care.

## Write Recovery (WR)/Read-to-Precharge (RTP)

The programmed write recovery (WR) value is used for the auto precharge feature along with  $t_{RP}$  to determine  $t_{DAL}$ . WR for auto precharge (MIN) in clock cycles is calculated by dividing  $t_{WR}$  (in ns) by  $t_{CK}$  (in ns) and rounding to the next integer:

The WR value must be programmed to be equal to or larger than  $t_{WR}$  (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array;  $t_{WR}$  values will change when enabled. If there is a CRC error, the device blocks the Write operation and discards the data.

Internal Read-to-Precharge (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing  $t_{RTP}$  (in ns) by  $t_{CK}$  (in ns) and rounding to the next integer:

The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with  $t_{RP}$  to determine the ACT timing to the same bank.

## Mode Register MR1

**Table 9. MR1 Definition**

BG0	BA1	BA0	RAS# /A16	CAS# /A15	WE# A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0 <sup>1</sup>	Qoff <sup>2</sup>	0 <sup>1</sup>	R <sub>TT_NOM</sub>			WL	0 <sup>1</sup>	0 <sup>1</sup>	AL <sup>4</sup>		ODI		DLL

A12	Qoff	A7	Write Leveling Enable	A0	DLL Enable	A2	A1	Output Driver Impedance Control
0	Output buffer enabled	0	Disable	0	Disable <sup>3</sup>	0	0	RZQ/7
1	Output buffer disabled	1	Enable	1	Enable	0	1	RZQ/5
						1	0	Reserved
						1	1	Reserved

A10	A9	A8	R <sub>TT_NOM</sub>
0	0	0	R <sub>TT_NOM</sub> Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

A4	A3	Additive Latency
0	0	0(AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

Note 1. Reserved for future use and must be programmed to 0 during MRS.

Note 2. Outputs disabled - DQs, DQSs, DQS#s.

Note 3. States reversed to "0 as Disable" with respect to DDR4.

Note 4. Additive Latency is not supported for x16 device.

## DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the Self Refresh operation and is automatically re-enabled upon exit of the Self Refresh operation. Any time the DLL is enabled and subsequently reset,  $t_{DLLK}$  clock cycles must occur before a Read or Synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the  $t_{DQSCK}$ ,  $t_{AON}$ , or  $t_{AOF}$  parameters.

During  $t_{DLLK}$ , CKE must continuously be registered High. The device does not require DLL for any Write operation, except when  $R_{TT\_WR}$  is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin Low and/or by programming the  $R_{TT\_NOM}$  bits MR1[10:8] = 000 via an MRS command during DLL off mode.

The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set  $R_{TT\_WR}$ , MR2[11:9] = 00.

## Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2:1].

## ODT $R_{TT\_NOM}$ Values

The device is capable of providing three different termination values:  $R_{TT\_PARK}$ ,  $R_{TT\_NOM}$ , and  $R_{TT\_WR}$ . The nominal termination value,  $R_{TT\_NOM}$ , is programmed in MR1. A separate value,  $R_{TT\_WR}$ , may be programmed in MR2 to enable a unique  $R_{TT}$  value when ODT is enabled during Write operations. The  $R_{TT\_WR}$  value can be applied during Write commands even when  $R_{TT\_NOM}$  is disabled. A third  $R_{TT}$  value,  $R_{TT\_PARK}$ , is programmed in MR5.  $R_{TT\_PARK}$  provides a termination value when the ODT signal is Low.

## Additive Latency

The Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in the device. In this operation, the device allows a Read or Write command (either with or without auto precharge) to be issued immediately after the Activate command. The command is held for the time of AL before it is issued inside the device. Read latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. Write latency (WL) is controlled by the sum of the AL and CAS Write latency (CWL) register settings. Additive Latency is not supported for x16 device.

## Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

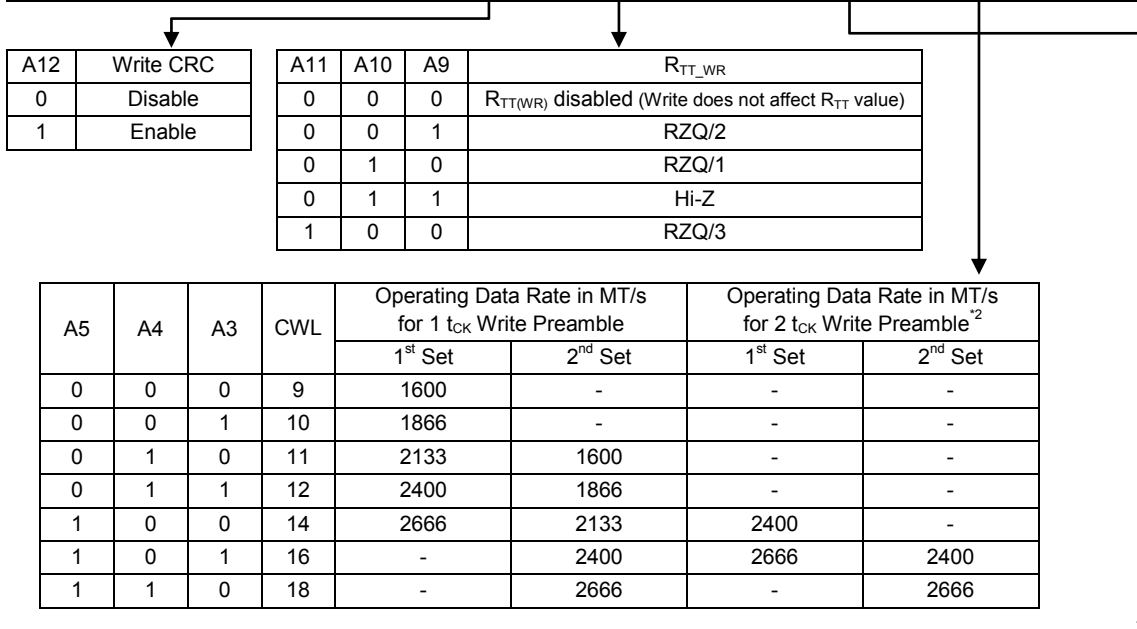
## Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring module power. For normal operation, set MR1[12] to 0.

## Mode Register MR2

**Table 10. MR2 Definition**

BG0	BA1	BA0	RAS# /A16	CAS# /A15	WE# A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0 <sup>*1</sup>	Write CRC	R <sub>TT_WR</sub>			0 <sup>*1</sup>	LPASR	CWL			0 <sup>*1</sup>	0 <sup>*1</sup>	0 <sup>*1</sup>	



A12	Write CRC
0	Disable
1	Enable

A11	A10	A9	R <sub>TT_WR</sub>
0	0	0	R <sub>TT(WR)</sub> disabled (Write does not affect R <sub>TT</sub> value)
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3

A5	A4	A3	CWL	Operating Data Rate in MT/s for 1 t <sub>CK</sub> Write Preamble		Operating Data Rate in MT/s for 2 t <sub>CK</sub> Write Preamble <sup>*2</sup>	
				1 <sup>st</sup> Set	2 <sup>nd</sup> Set	1 <sup>st</sup> Set	2 <sup>nd</sup> Set
0	0	0	9	1600	-	-	-
0	0	1	10	1866	-	-	-
0	1	0	11	2133	1600	-	-
0	1	1	12	2400	1866	-	-
1	0	0	14	2666	2133	2400	-
1	0	1	16	-	2400	2666	2400
1	1	0	18	-	2666	-	2666

A7	A6	Low Power Auto Self Refresh (LPASR)
0	0	Manual Mode - Normal Operating Temperature Range (T <sub>C</sub> : -40°C ~ 85°C)
0	1	Manual Mode - Reduced Operating Temperature Range (T <sub>C</sub> : -40°C ~ 45°C)
1	0	Manual Mode - Extended Operating Temperature Range (T <sub>C</sub> : -40°C ~ 95°C)
1	1	ASR Mode (Auto Self Refresh)

Note 1. Reserved for future use and must be programmed to 0 during MRS.

Note 2. The 2 t<sub>CK</sub> Write Preamble is valid for DDR4-2400/2666 Speed Grade. For the 2<sup>nd</sup> Set of t<sub>CK</sub> Write Preamble, no additional CWL is needed.

## CAS Write Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall Write latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS write latency (CWL): WL = AL + PL + CWL.

## Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring Self Refresh operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

## Dynamic ODT

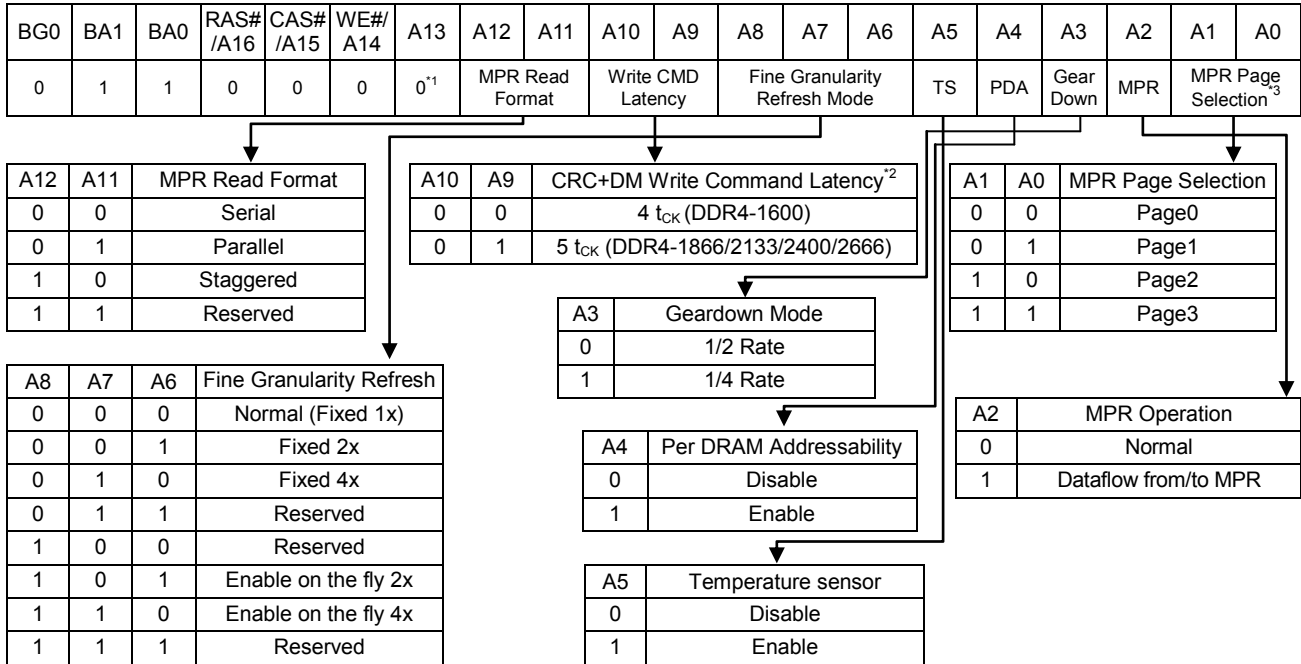
In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT (R<sub>TT\_WR</sub>) settings in MR2[11:9]. In write leveling mode, only R<sub>TT\_NOM</sub> is available.

## Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

## Mode Register MR3

**Table 11. MR3 Definition**



Note 1. Reserved for future use and must be programmed to 0 during MRS.

Note 2. Write Command latency when CRC and DM are both enabled:

- At less than or equal to 1600 then 4t<sub>CK</sub>; neither 5t<sub>CK</sub> nor 6t<sub>CK</sub>
- At greater than 1600 and less than or equal to 2666 then 5t<sub>CK</sub>; neither 4t<sub>CK</sub> nor 6t<sub>CK</sub>

Note 3. Refer to MPR Data Format table.

### **Write Command Latency When CRC/DM is Enabled**

The Write command latency (WCL) must be set when both Write CRC and DM are enabled for Write CRC persistent mode. This provides the extra time required when completing a Write burst when Write CRC and DM are enabled.

### **Fine Granularity Refresh Mode**

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening  $t_{RFC}$  and decreasing cycle time allows more accesses to the chip and allows for increased scheduling flexibility.

### **Temperature Sensor Status**

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

### **Per-DRAM Addressability**

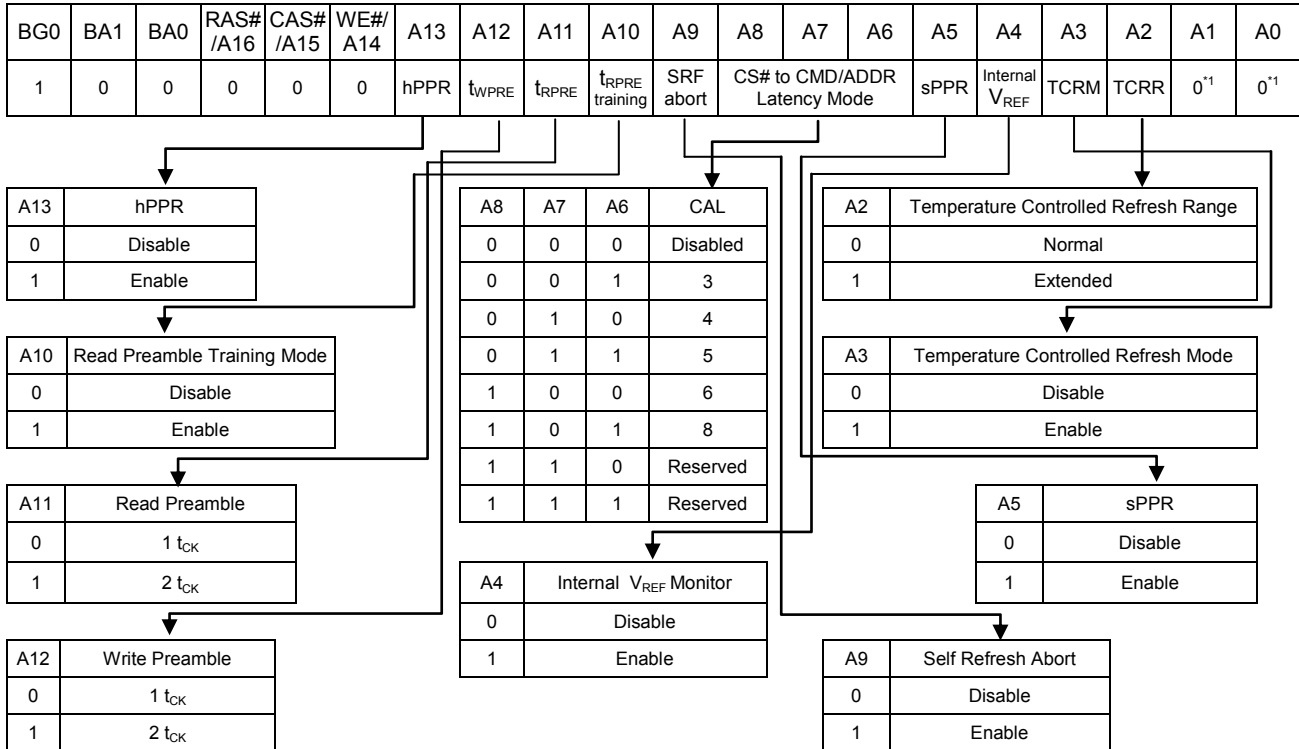
The MRS command mask allows programmability of a given device that may be in the same rank (devices sharing the same command and address signals). As an example, this feature can be used to program different ODT or  $V_{REF}$  values on DRAM devices within a given rank.

### **Gear-Down Mode**

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS#, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

## Mode Register MR4

**Table 12. MR4 Definition**



Note 1. Reserved for future use and must be programmed to 0 during MRS.

### Write Preamble

Programmable Write preamble, t<sub>WPRE</sub>, can be set to 1t<sub>CK</sub> or 2t<sub>CK</sub> via the MR4 register. The 1t<sub>CK</sub> setting is similar to DDR3. However, when operating in 2t<sub>CK</sub> Write preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable t<sub>CK</sub> range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

### Read Preamble

Programmable Read preamble t<sub>RPRE</sub> can be set to 1t<sub>CK</sub> or 2t<sub>CK</sub> via the MR4 register. Both the 1t<sub>CK</sub> and 2t<sub>CK</sub> DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 Read preamble settings may require the memory controller to train (or read level) its data strobe receivers using the Read preamble training.

### Read Preamble Training

Programmable Read preamble training can be set to 1t<sub>CK</sub> or 2t<sub>CK</sub>. This mode can be used by the memory controller to train or Read level its data strobe receivers.

### Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than t<sub>REFI</sub> of the normal temperature range by skipping external Refresh commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of -40°C to 85°C, while the extended temperature range covers -40°C to 95°C.



### Command Address Latency

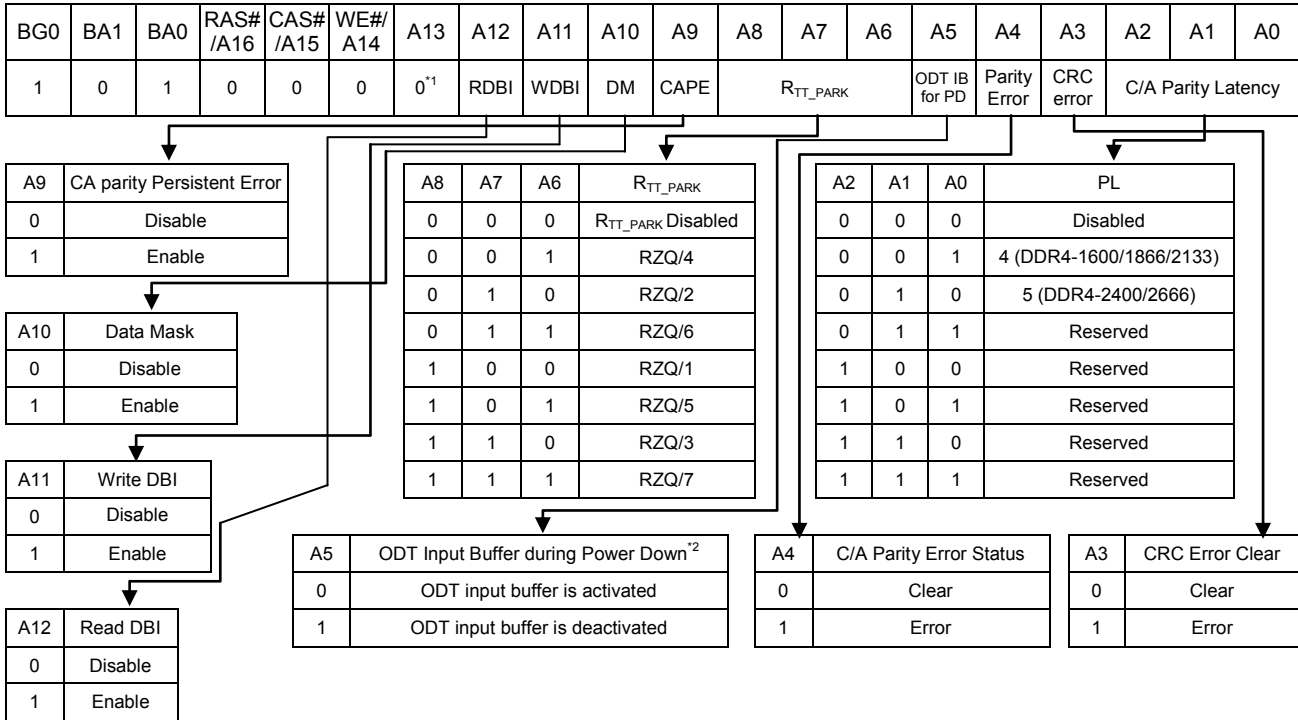
Command Address Latency (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles ( $t_{CAL}$ ) between a CS# registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of  $[t_{CK}(ns)/t_{CAL}(ns)]$ .

### Internal VREF Monitor

The device generates its own internal  $V_{REFDQ}$ . This mode may be enabled during  $V_{REFDQ}$  training, and when enabled,  $V_{REF, time-short}$  and  $V_{REF, time-long}$  need to be increased by 10ns if DQ0, DQ1, DQ2, or DQ3 have 0pF loading. An additional 15ns per pF of loading is also needed.

## Mode Register MR5

Table 13. MR5 Definition



Note 1. Reserved for future use and must be programmed to 0 during MRS.

Note 2. When R<sub>TT\_NOM</sub> Disable is set in MR1, A5 of MR5 will be ignored.

## Data Bus Inversion

The Data Bus Inversion (DBI) function has been added to the device and is supported for x16 configurations. The DBI function shares a common pin with the DM functions. The DBI function applies to both Read and Write operations; Write DBI cannot be enabled at the same time the DM function is enabled. DBI is not allowed during MPR Read operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12.

## Data Mask

The Data Mask (DM) function, also described as a partial write, has been added to the device and is supported for x16 configurations. The DM function shares a common pin with the DBI functions. The DM function applies only to Write operations and cannot be enabled at the same time the write DBI function is enabled.

## CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

## ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide R<sub>TT\_NOM</sub> termination. However, the device may provide R<sub>TT\_PARK</sub> termination depending on the MR settings. This is primarily for additional power savings.

### **CA Parity Error Status**

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

### **CRC Error Clear**

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

### **CA Parity Latency Mode**

CA parity is enabled when a latency value, dependent on  $t_{CK}$ , is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT#, RAS#/A16, CAS#/A15, WE#/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS# are not included in the parity calculation.

## Mode Register MR6

**Table 14. MR6 Definition**

BG0	BA1	BA0	RAS# /A16	CAS# /A15	WE# /A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	0	0 <sup>*1</sup>	t <sub>CCD_L</sub>			0 <sup>*1</sup>	0 <sup>*1</sup>	V <sub>REFDQ</sub> Training	V <sub>REFDQ</sub> Range	V <sub>REFDQ</sub> Training Value					

A12	A11	A10	t <sub>CCD_L.min</sub> (t <sub>CK</sub> )	t <sub>DLLK.min</sub> (t <sub>CK</sub> )	Note
0	0	0	4	597	Data rate ≤1333Mbps
0	0	1	5	597	1333Mbps < Data rate ≤1866Mbps
0	1	0	6	768	1866Mbps < Data rate ≤2400Mbps
0	1	1	7	1024	2400Mbps < Data rate ≤2666Mbps
1	0	0	Reserved	Reserved	Reserved
1	0	1	Reserved	-	Reserved
1	1	0	Reserved	-	Reserved
1	1	1	Reserved	-	Reserved

A6	V <sub>REFDQ</sub> Range
0	Range 1
1	Range 2

A7	V <sub>REFDQ</sub> Training
0	Disable
1	Enable

A5:A0	Range1	Range2	A5:A0	Range1	Range2	A5:A0	Range1	Range2	A5:A0	Range1	Range2
000000	60.00%	45.00%	001101	68.45%	53.45%	01 1010	76.90%	61.90%	10 0111	85.35%	70.35%
000001	60.65%	45.65%	001110	69.10%	54.10%	01 1011	77.55%	62.55%	10 1000	86.00%	71.00%
000010	61.30%	46.30%	001111	69.75%	54.75%	01 1100	78.20%	63.20%	10 1001	86.65%	71.65%
000011	61.95%	46.95%	010000	70.40%	55.40%	01 1101	78.85%	63.85%	10 1010	87.30%	72.30%
000100	62.60%	47.60%	010001	71.05%	56.05%	01 1110	79.50%	64.50%	10 1011	87.95%	72.95%
000101	63.25%	48.25%	010010	71.70%	56.70%	01 1111	80.15%	65.15%	10 1100	88.60%	73.60%
000110	63.90%	48.90%	010011	72.35%	57.35%	10 0000	80.80%	65.80%	10 1101	89.25%	74.25%
000111	64.55%	49.55%	010100	73.00%	58.00%	10 0001	81.45%	66.45%	10 1110	89.90%	74.90%
001000	65.20%	50.20%	010101	73.65%	58.65%	10 0010	82.10%	67.10%	10 1111	90.55%	75.55%
001001	65.85%	50.85%	010110	74.30%	59.30%	10 0011	82.75%	67.75%	11 0000	91.20%	76.20%
001010	66.50%	51.50%	010111	74.95%	59.95%	10 0100	83.40%	68.40%	11 0001	91.85%	76.85%
001011	67.15%	52.15%	011000	75.60%	60.60%	10 0101	84.05%	69.05%	11 0010	92.50%	77.50%
001100	67.80%	52.80%	011001	76.25%	61.25%	10 0110	84.70%	69.70%	11 0011 to 111111 : Reserved		

Note 1. Reserved for future use and must be programmed to 0 during MRS.

### t<sub>CCD\_L</sub> Programming

The device controller must program the correct t<sub>CCD\_L</sub> value. t<sub>CCD\_L</sub> will be programmed according to the value defined per operating frequency in the AC parameter table.

### V<sub>REFDQ</sub> Training Enable

V<sub>REFDQ</sub> Training is where the device internally generates its own V<sub>REFDQ</sub> to be used by the DQ input receivers. The device controller is responsible for setting and calibrating the internal V<sub>REFDQ</sub> level using an MRS protocol (adjust up, adjust down, etc.). The procedure is a series of Writes and Reads in conduction with V<sub>REFDQ</sub> adjustments to optimize and verify the data eye. Enabling V<sub>REFDQ</sub> Training must be used whenever values are being written to the MR6[6:0] register.

### V<sub>REFDQ</sub> Training Range

The device defines two V<sub>REFDQ</sub> calibration ranges: Range 1 and Range 2. Range 1 supports V<sub>REFDQ</sub> between 60% and 92% of V<sub>DDQ</sub> while Range 2 supports V<sub>REFDQ</sub> between 45% and 77% of V<sub>DDQ</sub>, Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

### V<sub>REFDQ</sub> Training Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of V<sub>REFDQ</sub>.

**Mode Register MR7: Ignore**

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM. Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

## DLL-off Mode and DLL on/off Switching Procedure

### DLL on/off switching procedure

The DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”.

### DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

- Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors,  $R_{TT\_NOM}$ , must be in high impedance state before MRS to MR1 to disable the DLL.)
- Set MR1 bit A0 to “0” to disable the DLL.
- Wait  $t_{MOD}$ .
- Enter Self Refresh Mode; wait until ( $t_{CKSRE}$ ) is satisfied.
- Change frequency, following the guidelines in the Input Clock Frequency Change section.
- Wait until a stable clock is available for at least ( $t_{CKSRX}$ ) at device inputs.
- Starting with the Self Refresh Exit command, CKE must continuously be registered high until all  $t_{MOD}$  timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all  $t_{MOD}$  timings from any MRS command are satisfied. If  $R_{TT\_NOM}$  features were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don't Care.
- Wait  $t_{XS\_Fast}$  or  $t_{XS\_Abort}$  or  $t_{XS}$ , then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary; a ZQCL command may also be issued after  $t_{XS\_Fast}$ ).
  - $t_{XS\_Fast}$ : ZQCL, ZQCS, MRS commands. For MRS command, only CL and WR/RTP register in MR0, CWL register in MR2 and gear-down mode in MR3 are allowed to be accessed provided the device is not in per DRAM addressability mode. Access to other device mode registers must satisfy  $t_{XS}$  timing.
  - $t_{XS\_Abort}$ : If the MR4 bit A9 is enabled then the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of  $t_{XS\_Abort}$ . Upon exit from Self-Refresh, the device requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.
  - $t_{XS}$ : ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8
- Wait for  $t_{MOD}$ , then device is ready for next command.

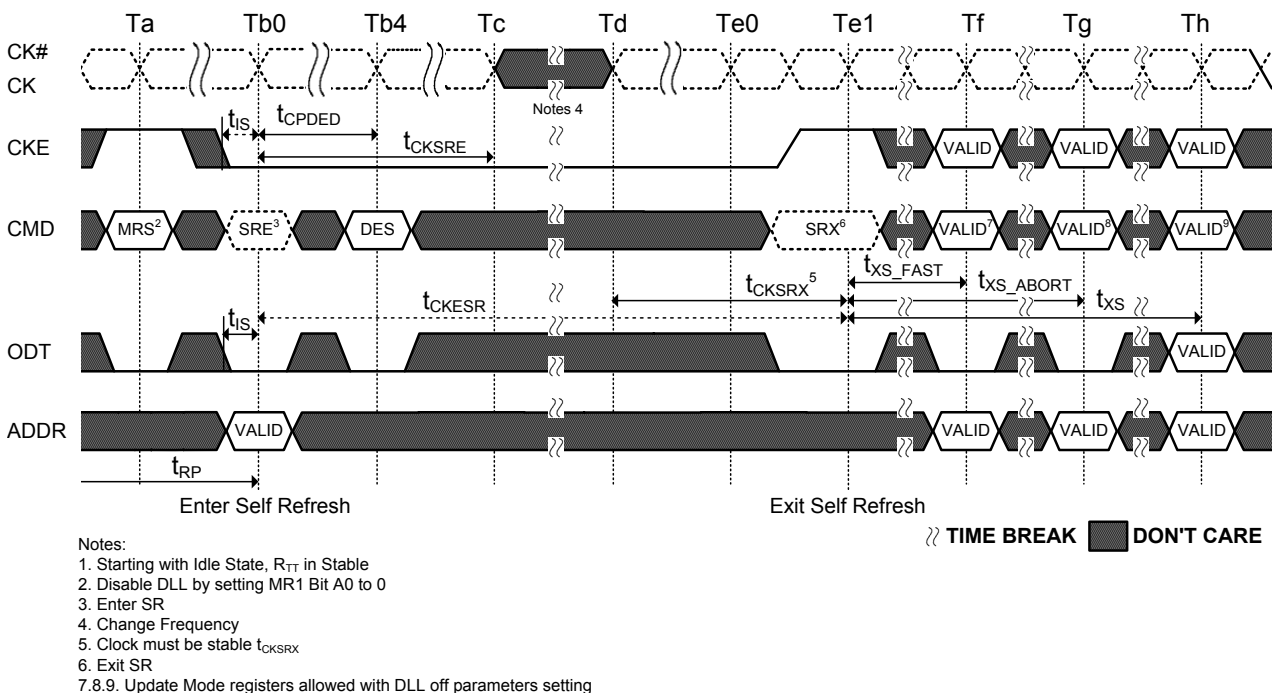
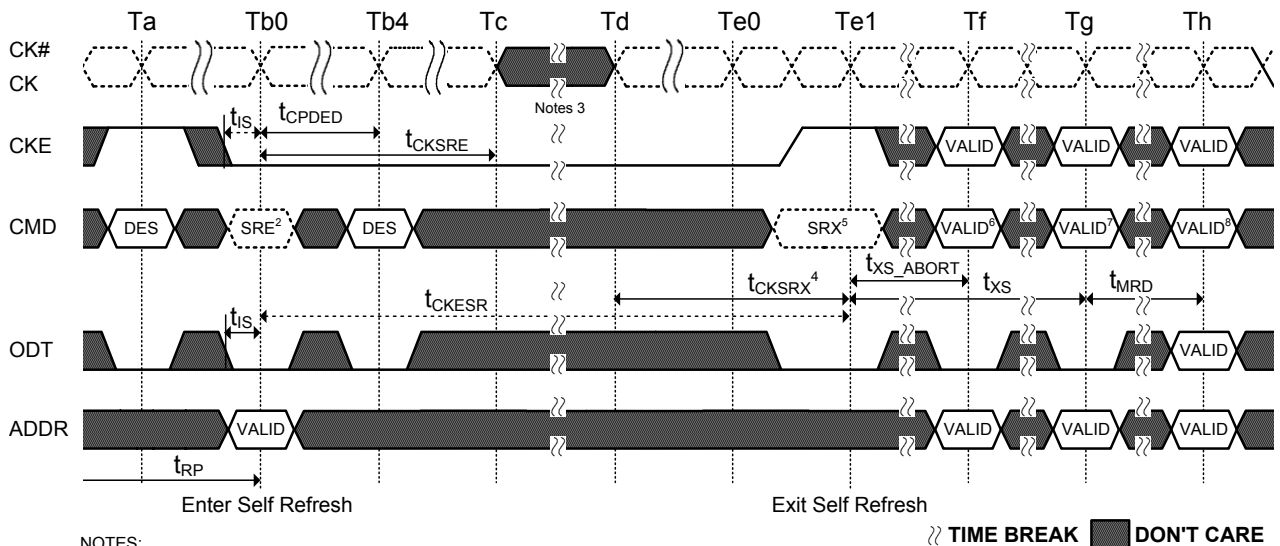


Figure 9. DLL Switch Sequence from DLL ON to DLL OFF

## DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors ( $R_{TT\_NOM}$ ) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until  $t_{CKSRE}$  satisfied.
3. Change frequency, following the guidelines in the Input Clock Frequency Change section.
4. Wait until a stable clock is available for at least ( $t_{CKSRX}$ ) at device inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered high until  $t_{DLLK}$  timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered low until  $t_{DLLK}$  timings from subsequent DLL Reset command is satisfied. If  $R_{TT\_NOM}$  were disabled in the mode registers when Self Refresh mode was entered, ODT signal is don't care.
6. Wait  $t_{XS}$  or  $t_{XS\_ABORT}$  depending on Bit A9 in MR4, then set MR1 bit A0 to “1” to enable the DLL.
7. Wait  $t_{MRD}$ , then set MR0 bit A8 to “1” to start DLL Reset.
8. Wait  $t_{MRD}$ , then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After  $t_{MOD}$  satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after  $t_{DLLK}$ .)
9. Wait for  $t_{MOD}$ , then device is ready for next command. (Remember to wait  $t_{DLLK}$  after DLL Reset before applying command requiring a locked DLL). In addition, wait also for  $t_{ZQoper}$  in case a ZQCL command was issued.



**NOTES:**

1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable  $t_{CKSRX}$
5. Exit SR
- 6.7. Set DLL-on by MR1 A0='1'
8. Start DLLReset
9. Update rest MR register values after  $t_{DLLK}$  (not shown in the diagram)

**Figure 10. DLL Switch Sequence from DLL OFF to DLL ON**



## DLL-off Mode

DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”. The MR1 A0 bit for DLL control can be switched either during initialization or during self refresh mode. Refer to the Input Clock Frequency Change section for more details.

The maximum clock frequency for DLL-off Mode is specified by the parameter  $t_{CKDLL\_OFF}$ . There is no minimum frequency limit besides the need to satisfy the refresh interval,  $t_{REFI}$ .

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9.

DLL-off mode will affect the Read data Clock to Data Strobe relationship ( $t_{DQSCk}$ ), but not the Data Strobe to Data relationship ( $t_{DQSQ}$ ,  $t_{QH}$ ). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where  $t_{DQSCk}$  starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode  $t_{DQSCk}$  starts (AL+CL - 1) cycles after the read command. Another difference is that  $t_{DQSCk}$  may not be small compared to  $t_{CK}$  (it might even be larger than  $t_{CK}$ ) and the difference between  $t_{DQSCkmin}$  and  $t_{DQSCkmax}$  is significantly larger than in DLL-on mode.  $t_{DQSCk(DLL\_off)}$  values are undefined.

The timing relations on DLL-off mode Read operation are shown in the following diagram, where CL = 10, AL = 0, and BL = 8.

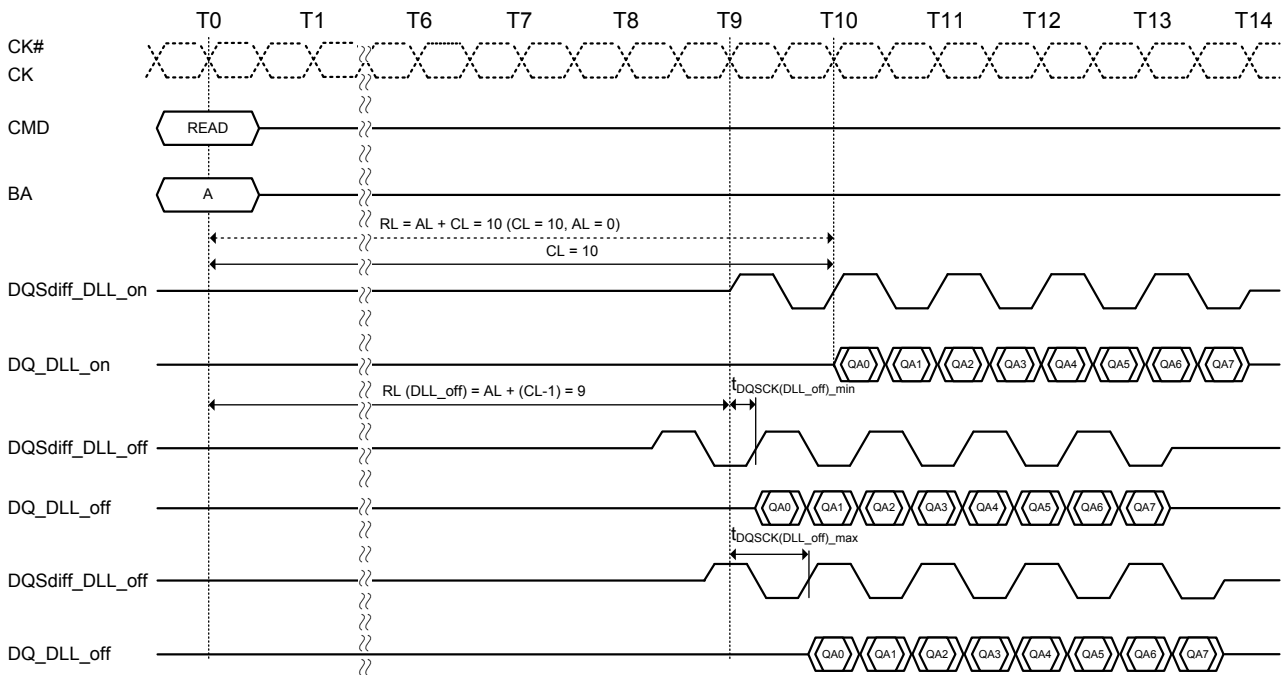


Figure 11. Read operation at DLL-off mode

## Input Clock Frequency Change

After the device is initialized, the DDR4 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that after the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only when in Self- Refresh mode. Outside Self-Refresh mode, it is illegal to change the clock frequency.

After the device has been successfully placed into Self-Refresh mode and  $t_{CKSRE}$  has been satisfied, the state of the clock becomes a "Don't Care". Following a "Don't Care", changing the clock frequency is permissible, provided the new clock frequency is stable prior to  $t_{CKSRX}$ . When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in Self-Refresh Operation.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, Gear-down mode, Read & Write Preamble, Command Address Latency (CAL Mode), Command Address Parity (CA Parity Mode), and  $t_{CCD\_L}/t_{DLLK}$  value.

In particular, the Command Address Parity Latency (PL) must be disabled when the clock rate changes, i.e. while in Self Refresh Mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2666 with CA Parity Mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 5. The correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter Self Refresh Mode, (3) change clock rate from DDR4-2133 to DDR4-2666, (4) exit Self Refresh Mode, (5) Enable CA Parity Mode setting PL = 5 via MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, i.e. after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the idle state, unless the DRAM is reset. If the DRAM leaves the idle state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to after the next time the DRAM enters the idle state.

If MR6 is issued prior to Self Refresh Entry for new  $t_{DLLK}$  value, then DLL will relock automatically at Self Refresh Exit. However, if MR6 is issued after Self Refresh Entry, then MR0 must be issued to reset the DLL.

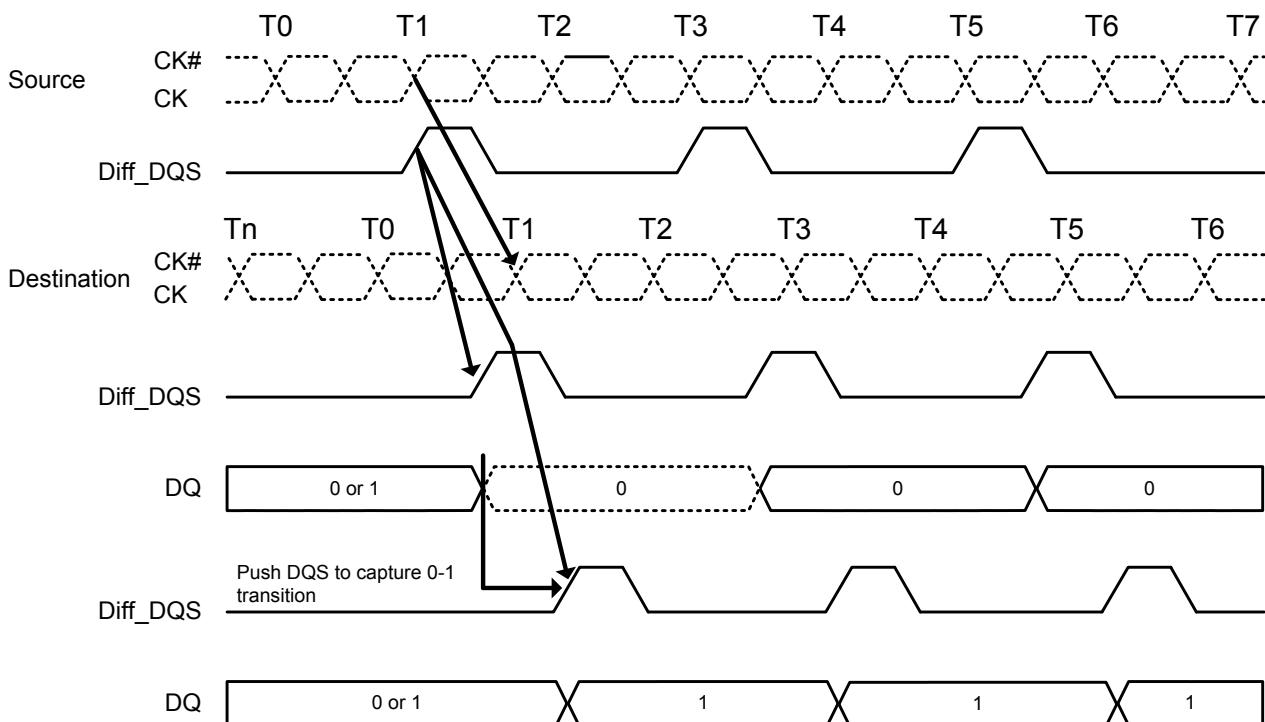
The device input clock frequency can change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL-on mode to DLL-off mode transition sequence. (See DLL on/off switching procedure)

## Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain  $t_{DQSS}$ ,  $t_{DSS}$ , and  $t_{DSH}$  specification. Therefore, the device supports a write leveling feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the  $t_{DQSS}$ ,  $t_{DSS}$  and  $t_{DSH}$  specifications.

The memory controller can use the write leveling feature and feedback from the device to adjust the DQS, DQS# to CK, CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS, DQS# to align the rising edge of DQS, DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK, CK#, sampled with the rising edge of DQS, DQS#, through the DQ bus. The controller repeatedly delays DQS, DQS# until a transition from 0 to 1 is detected. The DQS, DQS# delay established through this exercise would ensure  $t_{DQSS}$  specification.

Besides  $t_{DQSS}$ ,  $t_{DSS}$  and  $t_{DSH}$  specification also needs to be fulfilled. One way to achieve this is to combine the actual  $t_{DQSS}$  in the application with an appropriate duty cycle and jitter on the DQS, DQS# signals. Depending on the actual  $t_{DQSS}$  in the application, the actual values for  $t_{DQSL}$  and  $t_{DQSH}$  may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy  $t_{DSS}$  and  $t_{DSH}$  specification. A conceptual timing of this scheme is shown below.



**Figure 12. Write Leveling Concept**

DQS, DQS# driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits should carry the leveling feedback to the controller across the DRAM configurations x16. On a x16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper  $\text{diff\_DQS}(\text{diff\_UDQS})$  to clock relationship whereas the lower data bits would indicate the lower  $\text{diff\_DQS}(\text{diff\_LDQS})$  to clock relationship.

## DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (see the MR setting involved in the leveling procedure table). Note that in write leveling mode, only DQS terminations are activated and deactivated via ODT pin, unlike normal operation (see the DRAM termination function in the leveling mode table).

**Table 15. MR setting involved in the leveling procedure**

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

**Table 16. DRAM termination function in the leveling mode**

ODT pin @DRAM if R <sub>TT_NOM/PARK</sub> Value is set via MRS	DQS/DQS# termination	DQs termination
R <sub>TT_NOM</sub> with ODT High	on	off
R <sub>TT_PARK</sub> with ODT Low	on	off

Notes:

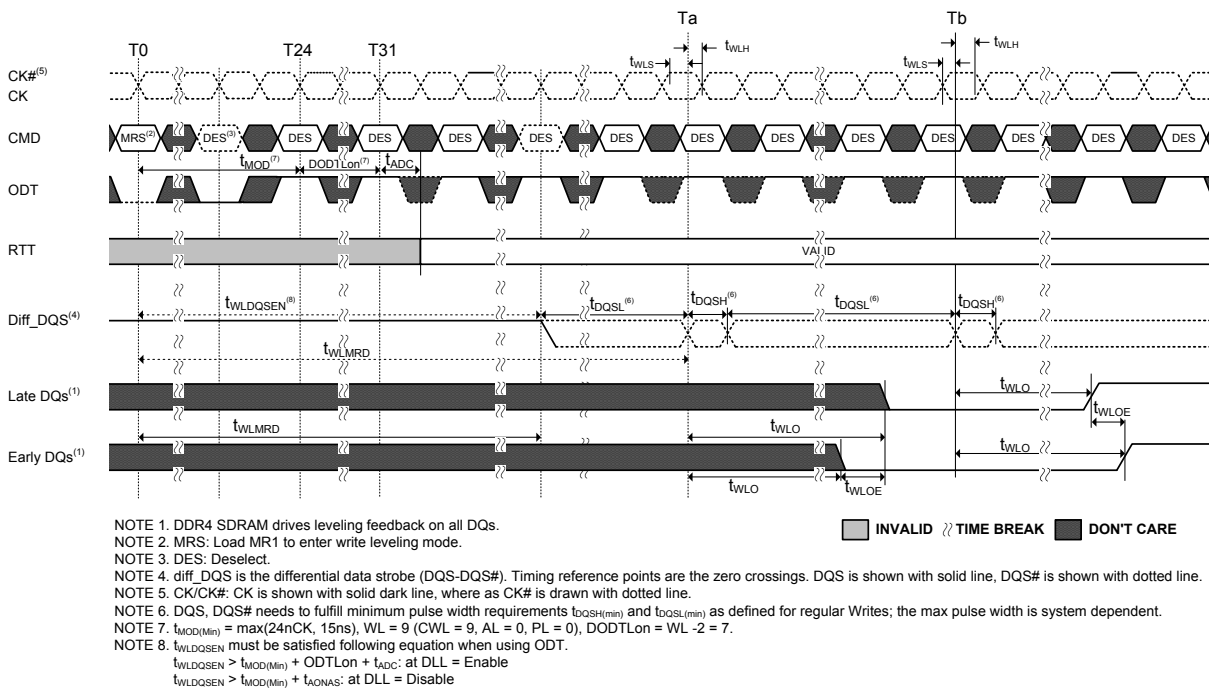
1. In Write Leveling Mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] = 1) all R<sub>TT\_NOM</sub> and R<sub>TT\_PARK</sub> settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit A7] = 1 with MR1[bit A12] = 0) all R<sub>TT\_NOM</sub> and R<sub>TT\_PARK</sub> settings are allowed.
2. Dynamic ODT function is not available in Write Leveling Mode. DRAM MR2 bits A[11:9] must be '000' prior to entering Write Leveling Mode.

## Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only Deselect commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change the other MR1 bits. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after  $t_{MOD}$ , at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and DQS# high after a delay of  $t_{WLDQSEN}$ , at which time the DRAM has applied on-die termination on these signals. After  $t_{DQSL}$  and  $t_{WLMRD}$ , the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller.  $t_{WLMRD(max)}$  timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after  $t_{WLO}$  timing. There is a DQ output uncertainty of  $t_{WLOE}$  defined to allow mismatch on DQ bits. The  $t_{WLOE}$  period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS - DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall Write Leveling procedure.



**Figure 13. Write Leveling Sequence (DQS capturing CK low at Ta and CK high at Tb)**

## Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see  $\sim T0$ ), stop driving the strobe signals (see  $\sim Tc0$ ). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until  $t_{MOD}$  after the respective MRS command ( $Te1$ ).
2. Drive ODT pin low ( $t_{IS}$  must be satisfied) and continue registering low (see  $Tb0$ ).
3. After the  $R_{TT}$  is switched off, disable Write Level Mode via MRS command (see  $Tc2$ ).
4. After  $t_{MOD}$  is satisfied ( $Te1$ ), any valid command may be registered. (MRS commands may be issued after  $t_{MRD}$  ( $Td1$ ).

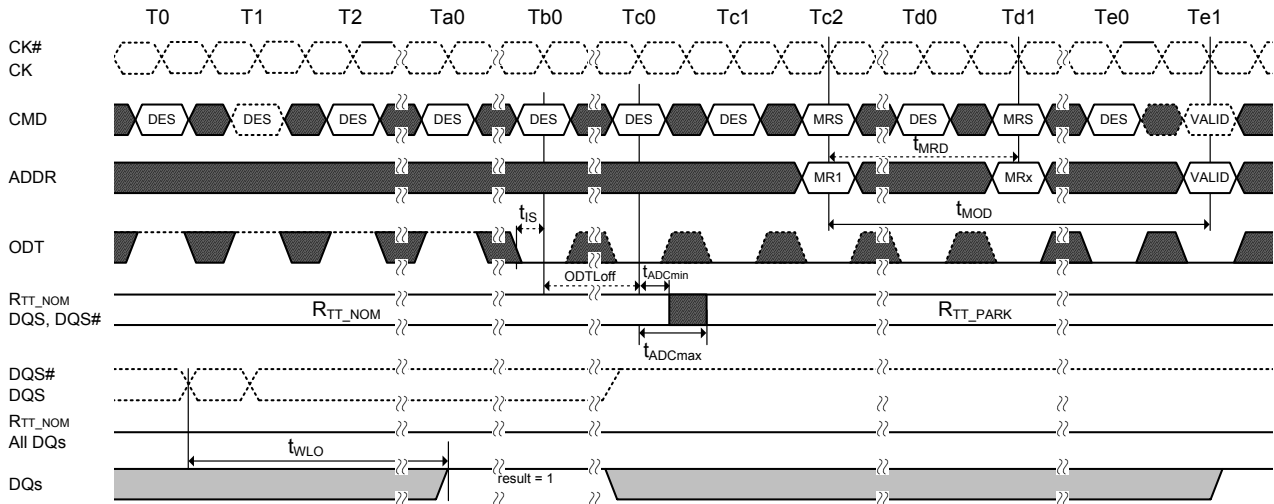


Figure 14. Write Leveling Exit

## CAL Mode (CS# to Command Address Latency)

DDR4 supports Command Address Latency (CAL) function as a power savings feature. CAL is the delay in clock cycles between CS# and CMD/ADDR defined by MR4[A8:A6].

CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched, the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence.

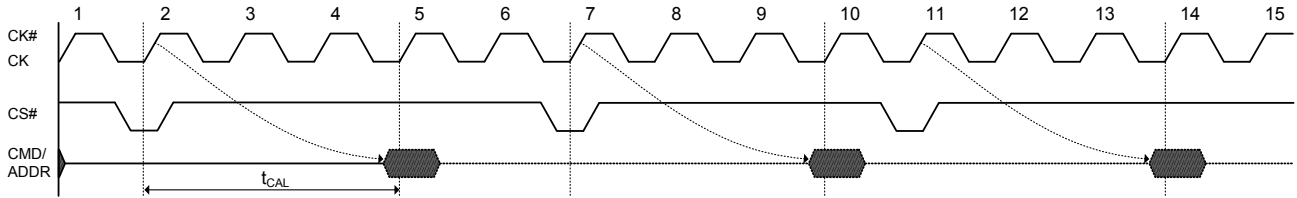


Figure 15. Definition of CAL

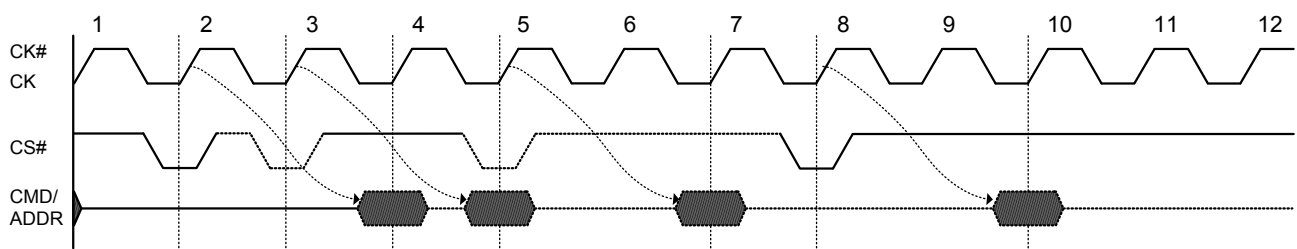
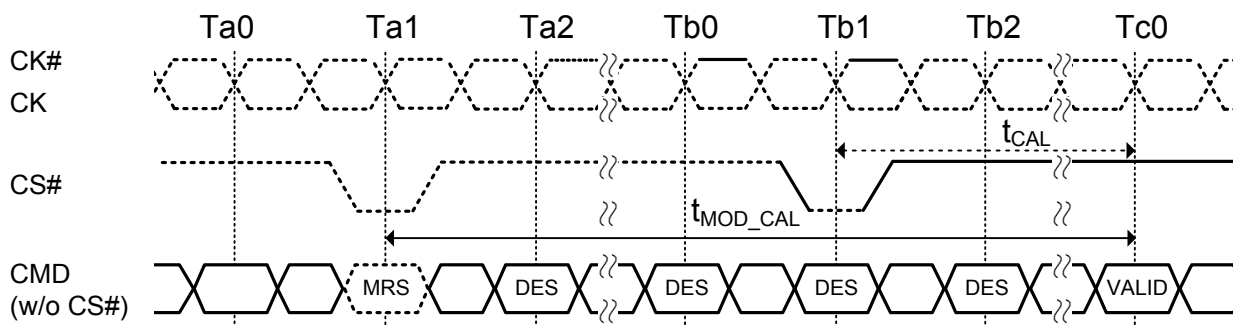


Figure 16. CAL operational timing for consecutive command issues

## MRS Timings with Command/Address Latency enabled

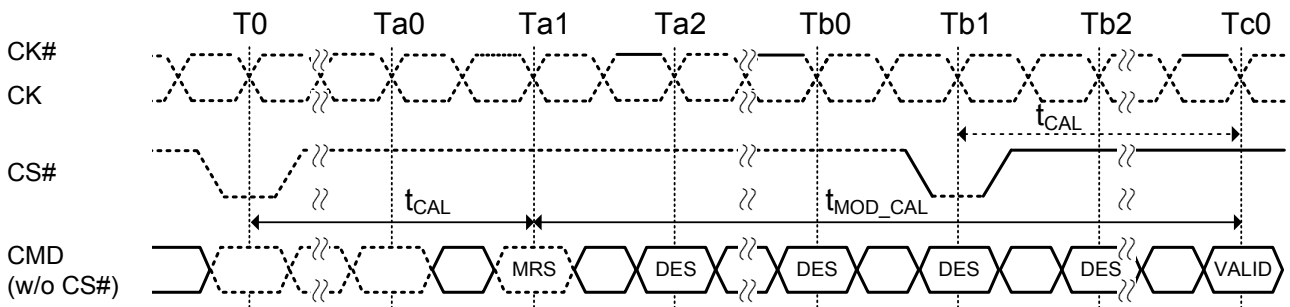
When Command/Address latency mode is enabled, users must allow more time for MRS commands to take effect. When CAL mode is enabled, or being enabled by an MRS command, the earliest the next valid command can be issued is  $t_{MOD\_CAL}$ , where  $t_{MOD\_CAL} = t_{MOD} + t_{CAL}$ .



NOTE1: MRS command at Ta1 enables CAL mode.

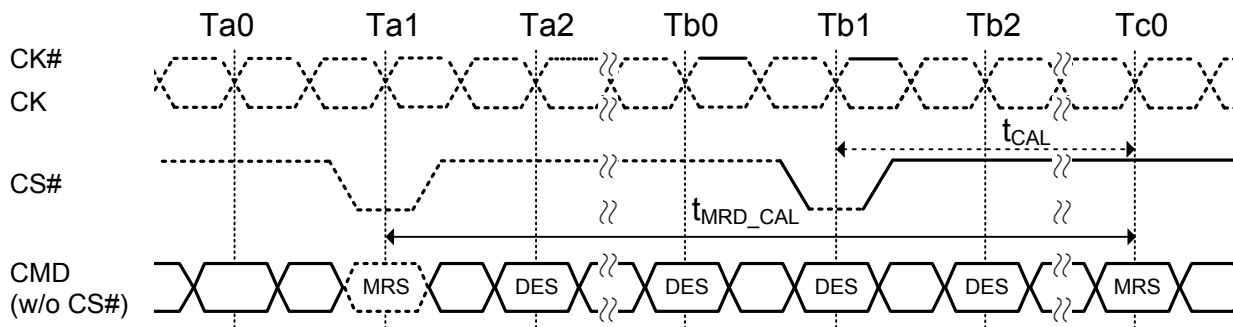
NOTE2:  $t_{MOD\_CAL} = t_{MOD} + t_{CAL}$ .

Figure 17. CAL enable timing -  $t_{MOD\_CAL}$



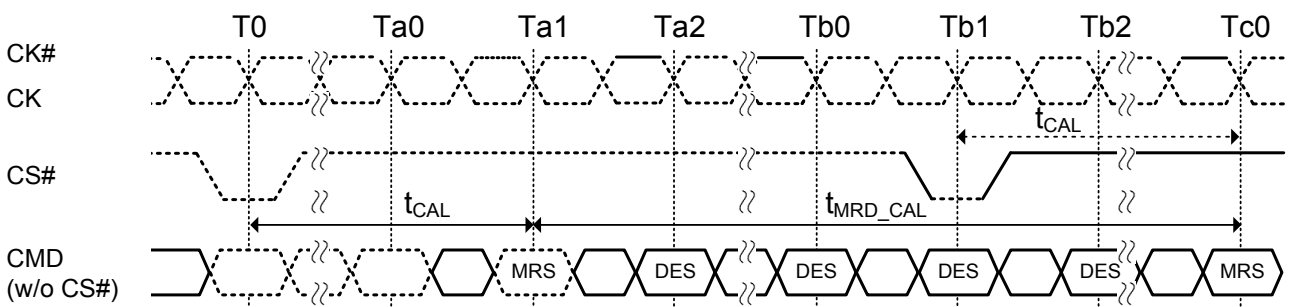
NOTE1: MRS at Ta1 may or may not modify CAL,  $t_{MOD\_CAL}$  is computed based on new  $t_{CAL}$  setting.  
 NOTE2:  $t_{MOD\_CAL} = t_{MOD} + t_{CAL}$

**Figure 18.  $t_{MOD\_CAL}$ , MRS to valid command timing with CAL enabled**



NOTE1: MRS command at Ta1 enables CAL mode.  
 NOTE2:  $t_{MRD\_CAL} = t_{MOD} + t_{CAL}$

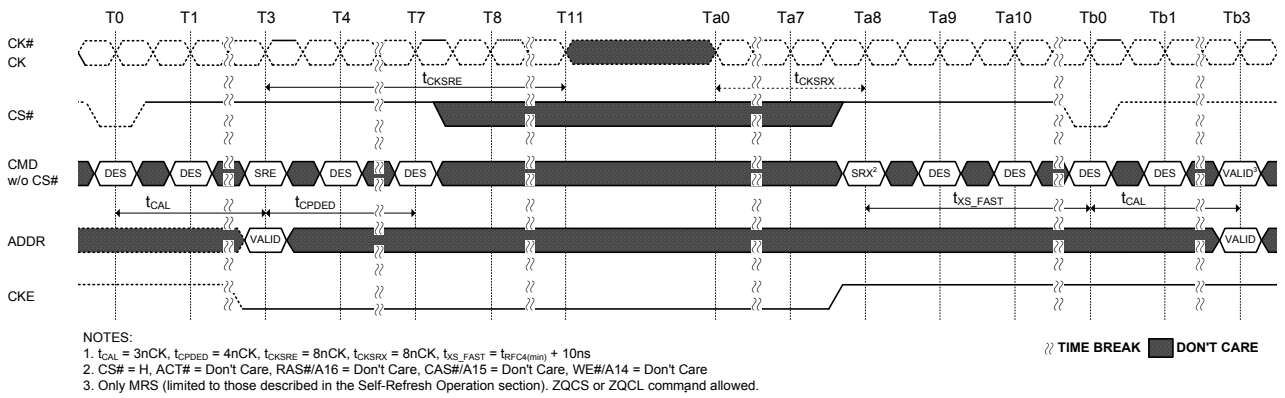
**Figure 19. CAL enabling MRS to next MRS command,  $t_{MRD\_CAL}$**



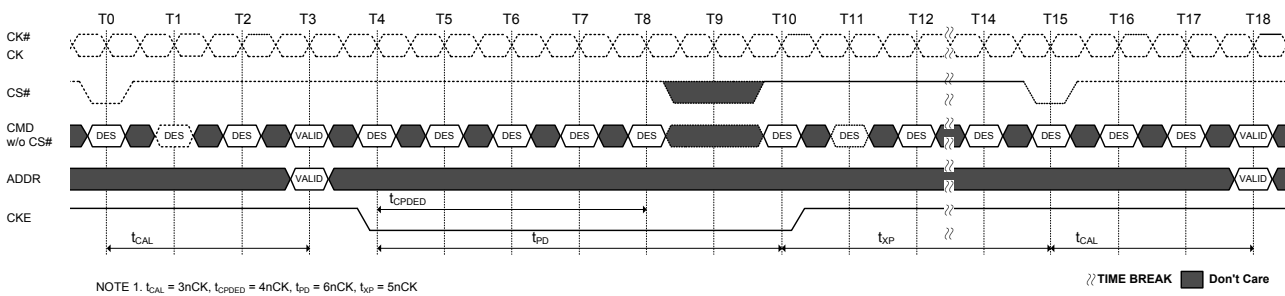
NOTE1: MRS at Ta1 may or may not modify CAL,  $t_{MRD\_CAL}$  is computed based on new  $t_{CAL}$  setting.  
 NOTE2:  $t_{MRD\_CAL} = t_{MOD} + t_{CAL}$

**Figure 20.  $t_{MRD\_CAL}$ , mode register cycle time with CAL enabled**

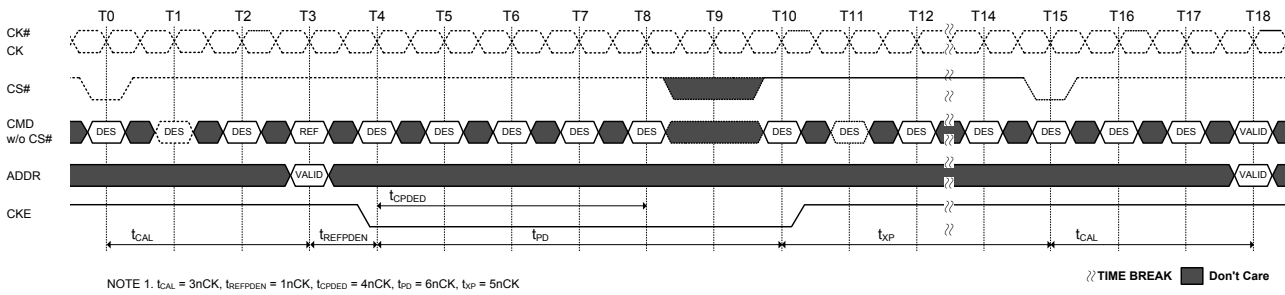




**Figure 21. Self Refresh Entry/Exit Timing with CAL**



**Figure 22. Active Power Down Entry and Exit Timing with CAL**



**Figure 23. Refresh Command to Power Down Entry with CAL**

## Fine Granularity Refresh Mode

DDR4 supports Command Address Latency (CAL) function as a power savings feature. CAL is the delay in clock cycles between CS# and CMD/ADDR defined by MR4[A8:A6].

CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched, the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence.

### Mode Register and Command Truth Table

The Refresh cycle time ( $t_{RFC}$ ) and the average Refresh interval ( $t_{REFI}$ ) can be programmed by the MRS command. The appropriate setting in the mode register will set a single set of Refresh cycle time and average Refresh interval for the device (fixed mode), or allow the dynamic selection of one of two sets of Refresh cycle time and average Refresh interval for the device (on-the-fly mode). The on-the-fly (OTF) mode must be enabled by MRS before any on-the-fly Refresh command can be issued.

**Table 17. MR3 definition for Fine Granularity Refresh Mode**

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal Mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

There are two types of on-the-fly modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two on-the-fly modes is selected ('A8=1'), the device evaluates BG0 bit when a Refresh command is issued, and depending on the status of BG0, it dynamically switches its internal Refresh configuration between 1x and 2x (or 1x and 4x) modes, and executes the corresponding Refresh operation.

**Table 18. Refresh command truth table**

Function	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	BG0	BA0-1	A10/AP	A[9:0], A[13:11]	MR3 [8:6]
Refresh (Fixed rate)	L	H	L	L	H	V	V	V	V	0VV
Refresh (on-the-fly 1x)	L	H	L	L	H	L	V	V	V	1VV
Refresh (on-the-fly 2x)	L	H	L	L	H	H	V	V	V	101
Refresh (on-the-fly 4x)	L	H	L	L	H	H	V	V	V	110

## t<sub>REFI</sub> and t<sub>RFC</sub> parameters

The default Refresh rate mode is fixed 1x mode where Refresh commands should be issued with the normal rate, i.e.,  $t_{REFI1} = t_{REFI(base)}$  (for  $T_{CASE} \leq 85^{\circ}C$ ), and the duration of each refresh command is the normal refresh cycle time ( $t_{RFC1}$ ). In 2x mode (either fixed 2x or on-the-fly 2x mode), Refresh commands should be issued to the device at the double frequency ( $t_{REFI2} = t_{REFI(base)}/2$ ) of the normal Refresh rate. In 4x mode, Refresh command rate should be quadrupled ( $t_{REFI4} = t_{REFI(base)}/4$ ). Per each mode and command type, t<sub>RFC</sub> parameter has different values as defined in the following table.

The refresh command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency ( $t_{REFI2} = t_{REFI(base)}/2$ ) may be referred to as a REF2x command. Finally, the refresh command that should be issued at the quadruple rate ( $t_{REFI4} = t_{REFI(base)}/4$ ) may be referred to as a REF4x command.

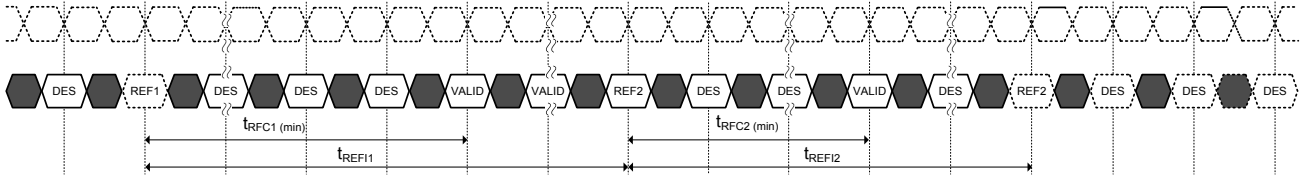
In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

**Table 19. Refresh command truth table**

Refresh Mode	Parameter		4Gb	Unit
	t <sub>REFI(base)</sub>		7.8	μS
1x mode	t <sub>REFI1</sub>	-40°C ≤ T <sub>CASE</sub> ≤ 85°C	t <sub>REFI(base)</sub>	μS
		85°C ≤ T <sub>CASE</sub> ≤ 95°C	t <sub>REFI(base)}/2</sub>	μS
	t <sub>RFC1(min)</sub>		260	ns
2x mode	t <sub>REFI2</sub>	-40°C ≤ T <sub>CASE</sub> ≤ 85°C	t <sub>REFI(base)}/2</sub>	μS
		85°C ≤ T <sub>CASE</sub> ≤ 95°C	t <sub>REFI(base)}/4</sub>	μS
	t <sub>RFC2(min)</sub>		160	ns
4X mode	t <sub>REFI4</sub>	-40°C ≤ T <sub>CASE</sub> ≤ 85°C	t <sub>REFI(base)}/4</sub>	μS
		85°C ≤ T <sub>CASE</sub> ≤ 95°C	t <sub>REFI(base)}/8</sub>	μS
	t <sub>RFC4(min)</sub>		110	ns

## Changing Refresh Rate

If Refresh rate is changed by either MRS or on the fly, new  $t_{REF1}$  and  $t_{RFC}$  parameters would be applied from the moment of the rate change. When REF1x command is issued to the DRAM, then  $t_{REF1}$  and  $t_{RFC1}$  are applied from the time that the command was issued. when REF2x command is issued, then  $t_{REF2}$  and  $t_{RFC2}$  should be satisfied.



**Figure 24. On-the-fly Refresh Command Timing**

The following conditions must be satisfied before the Refresh rate can be changed. Otherwise, data retention cannot be guaranteed.

- In the fixed 2x Refresh rate mode or the on-the-fly 1x/2x Refresh mode, an even number of REF2x commands must be issued because the last change of the Refresh rate mode with an MRS command before the Refresh rate can be changed by another MRS command.
- In the on-the-fly 1x/2x Refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
- In the fixed 4x Refresh rate mode or the on-the-fly 1x/4x Refresh mode, a multiple-of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate with an MRS command before the Refresh rate can be changed by another MRS command.
- In the on-the-fly 1x/4x Refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x Refresh rate mode. Switching between fixed and on-the-fly modes keeping the same rate is not regarded as a Refresh rate change.

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### Usage with Temperature Controlled Refresh mode

If the Temperature Controlled Refresh mode is enabled, then only the normal mode (Fixed 1x mode; MR3 [8:6] = 000) is allowed. If any other Refresh mode than the normal mode is selected, then the temperature controlled Refresh mode must be disabled.

### Self Refresh entry and exit

The device can enter Self Refresh mode anytime in 1x, 2x and 4x mode without any restriction on the number of Refresh commands that has been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows:

1. There are no special restrictions on the fixed 1x Refresh rate mode.
2. In the fixed 2x Refresh rate mode or the enable-on-the-fly 1x/2x Refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval ( $t_{REFI}$ ).
3. In the fixed 4x Refresh rate mode or the enable-on-the-fly 1x/4x Refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval ( $t_{REFI}$ ).

## Self Refresh Operation

The Self-Refresh command can be used to retain data in the device, even if the rest of the system is powered down. When in the Self-Refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS#, RAS#/A16, CAS#/A15, and CKE held low with WE#/A14 and ACT# high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the device must be idle with all bank precharge state with  $t_{RP}$  satisfied. Idle state is defined as all banks are closed ( $t_{RP}$ ,  $t_{DAL}$ , etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied ( $t_{MRD}$ ,  $t_{MOD}$ ,  $t_{RFC}$ ,  $t_{ZQinit}$ ,  $t_{ZQoper}$ ,  $t_{ZQCS}$ , etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of ODT pin and  $R_{TT\_PARK}$  set when it enters in Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set  $R_{TT\_PARK}$  asynchronously during  $t_{XSDLL}$  when  $R_{TT\_PARK}$  is enabled. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the device has entered Self-Refresh mode, all of the external control signals, except CKE and RESET#, are "don't care." For proper Self-Refresh operation, all power supply and reference pins ( $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$ ,  $V_{PP}$ , and  $V_{REFCA}$ ) must be at valid levels. DRAM internal  $V_{REFDQ}$  generator circuitry may remain on or turned off depending on the MR6 bit 7 setting. If DRAM internal  $V_{REFDQ}$  circuitry is turned off in self refresh, when DRAM exits from self refresh state, it ensures that  $V_{REFDQ}$  generator circuitry is powered up and stable within  $t_{XS}$  period. First Write operation or first Write Leveling Activity may not occur earlier than  $t_{XS}$  after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within  $t_{CKE}$  period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR4 SDRAM must remain in Self-Refresh mode is  $t_{CKESR}$ . The user may change the external clock frequency or halt the external clock  $t_{CKSRE}$  after Self-Refresh entry is registered, however, the clock must be restarted and stable  $t_{CKSRX}$  before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back high. Once a Self-Refresh Exit command (SRX, combination of CKE going high and Deselect on command bus) is registered, following timing delay must be satisfied:

Commands that do not require locked DLL:

- $t_{XS}$  = ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8
- $t_{XSFast}$  = ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register and DLL Reset in MR0,  $R_{TT\_NOM}$  register in MR1, CWL and  $R_{TT\_WR}$  register in MR2 and gear-down mode in MR3, Write and Read Preamble register in MR4,  $R_{TT\_PARK}$  register in MR5,  $t_{CCD\_L}/t_{DLLK}$  and  $V_{REFDQ}$  Training Value in MR6 are allowed to be accessed provided DRAM is not in per DRAM addressability mode. Access to other DRAM mode registers must satisfy  $t_{XS}$  timing. Note that synchronous ODT for write commands (WR, WRS4, WRS8, WRA, WRAS4 and WRAS8) and dynamic ODT controlled by write command require locked DLL.

Commands that require locked DLL:

- $t_{XSDLL}$  - RD, RDS4, RDS8, RDA, RDAS4, RDAS8

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in the ZQ Calibration Commands section. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain high for the entire Self-Refresh exit period  $t_{XSDLL}$  for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the device can be put back into Self-Refresh mode or Power down mode after waiting at least  $t_{XS}$  period and issuing one refresh command (refresh period of  $t_{RFC}$ ). Deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval  $t_{XS}$ . Low level of ODT pin must be registered on each positive clock edge during  $t_{XSDLL}$  when normal mode (DLL-on) is set. Under DLL-off mode, asynchronous ODT function might be allowed.

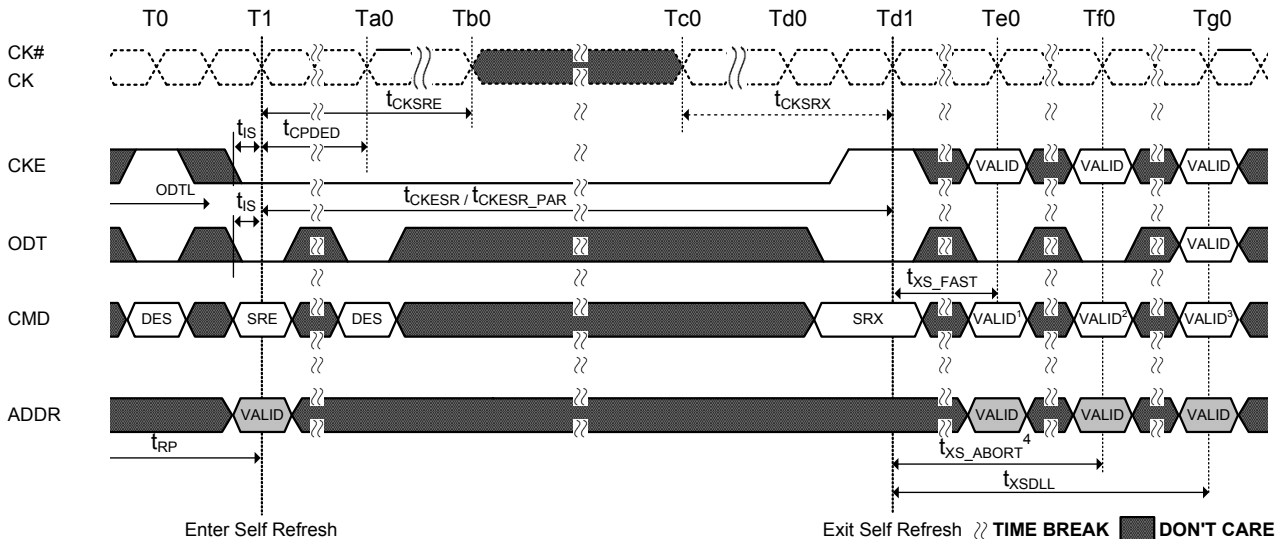
The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the device requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

## Self Refresh Abort

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is  $t_{XS}$ . The value of  $t_{XS}$  is  $(t_{RFC}+10ns)$ . This delay is to allow for any refreshes started by the DRAM to complete.  $t_{RFC}$  continues to grow with higher density devices so  $t_{XS}$  will grow as well.

A Bit A9 in MR4 is defined to enable the self refresh abort mode. If the bit is disabled then the controller uses  $t_{XS}$  timings. If the bit is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of  $t_{XS\_abort}$ .

Upon exit from Self-Refresh, the device requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.



- NOTE 1. Only MRS (limited to those described in the Self-Refresh Operation section), ZQCS or ZQCL command allowed.
- NOTE 2. Valid commands not requiring a locked DLL.
- NOTE 3. Valid commands requiring a locked DLL.
- NOTE 4. Only DES is allowed during  $t_{XS\_ABORT}$ .

**Figure 25. Self-Refresh Entry/Exit Timing**

## Low Power Auto Self Refresh (LPASR)

DDR4 devices support Low Power Auto Self-Refresh (LPASR) operation at multiple temperatures ranges (See temperature table below)

## **Auto Self Refresh (ASR)**

DDR4 DRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting the above MR2 bits A6=1 and A7=1. The device will manage Self Refresh entry through the supported temperature range of the DRAM. In this mode, the device will change self-refresh rate as the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

## **Manual Modes**

If ASR mode is not enabled, the LPASR Mode Register must be manually programmed to one of the three self-refresh operating modes. In this mode, the user has the flexibility to select a fixed self-refresh operating mode at the entry of the selfrefresh according to their system memory temperature conditions. The user is responsible to maintain the required memory temperature condition for the mode selected during the self-refresh operation. The user may change the selected mode after exiting from self refresh and before the next self-refresh entry. If the temperature condition is exceeded for the mode selected, there is risk to data retention resulting in loss of data.

**Table 20. Self Refresh Function table**

MR2 [A7]	MR2 [A6]	LPASR Mode	Self Refresh Operation	Allowed Operating Temperature Range for Self Refresh Mode (all reference to DRAM T <sub>CASE</sub> )
0	0	Normal	Fixed normal self-Refresh rate to maintain data retention for the normal operating temperature. User is required to ensure 85°C DRAM T <sub>CASE(max)</sub> is not exceeded to avoid any risk of data loss	(-40°C ~ 85°C)
0	1	Reduced Temperature range	Variable or fixed self-Refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM T <sub>CASE(max)</sub> is not exceeded to avoid any risk of data loss	(-40°C ~ 45°C)
1	0	Extended Temperature range	Fixed high self-Refresh rate to optimize data retention to support the extended temperature range	(-40°C ~ 95°C)
1	1	Auto Self Refresh	ASR Mode Enabled. Self-Refresh power consumption and data retention are optimized for any given operating temperature conditions	All of the above

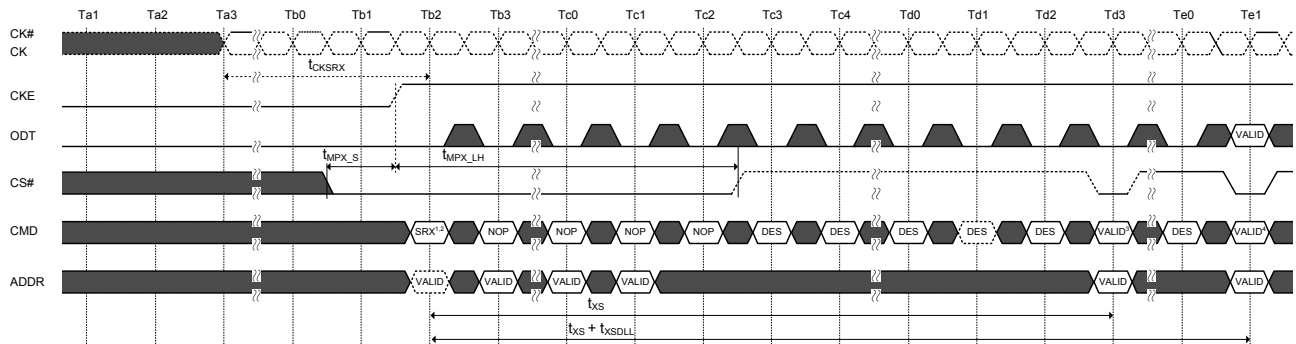


## Self Refresh Exit with No Operation command

Self Refresh Exit with No Operation command (NOP) allows for a common command/address bus between active DRAM and DRAM in Max Power Saving Mode. Self Refresh Mode may exit with No Operation commands (NOP) provided:

- The DRAM entered Self Refresh Mode with CA Parity and CAL disabled.
- $t_{MPX\_S}$  and  $t_{MPX\_LH}$  are satisfied.
- NOP commands are only issued during  $t_{MPX\_LH}$  window.

No other command is allowed during  $t_{MPX\_LH}$  window after SRX command is issued.



- NOTE 1. CS# = L, ACT# = H, RAS#/A16 = H, CAS#/A15 = H, WE#/A14 = H at Tb2 ( No Operation command )  
 NOTE 2. SRX at Tb2 is only allowed when DRAM shared Command/Address bus is under exiting Max Power Saving Mode.  
 NOTE 3. Valid commands not requiring a locked DLL  
 NOTE 4. Valid commands requiring a locked DLL  
 NOTE 5.  $t_{CS\_FAST}$  and  $t_{CS\_ABORT}$  are *not* allowed this case.  
 NOTE 6. Duration of CS# Low around CKE rising edge must satisfy  $t_{MPX\_S}$  and  $t_{MPX\_LH}$  as defined by Max Power Saving Mode AC parameters.

Figure 26. Self Refresh Exit with No Operation command

## Power down Mode

Power-down is synchronously entered when CKE is registered low (along with Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or Read / Write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams below illustrate entry and exit of power-down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

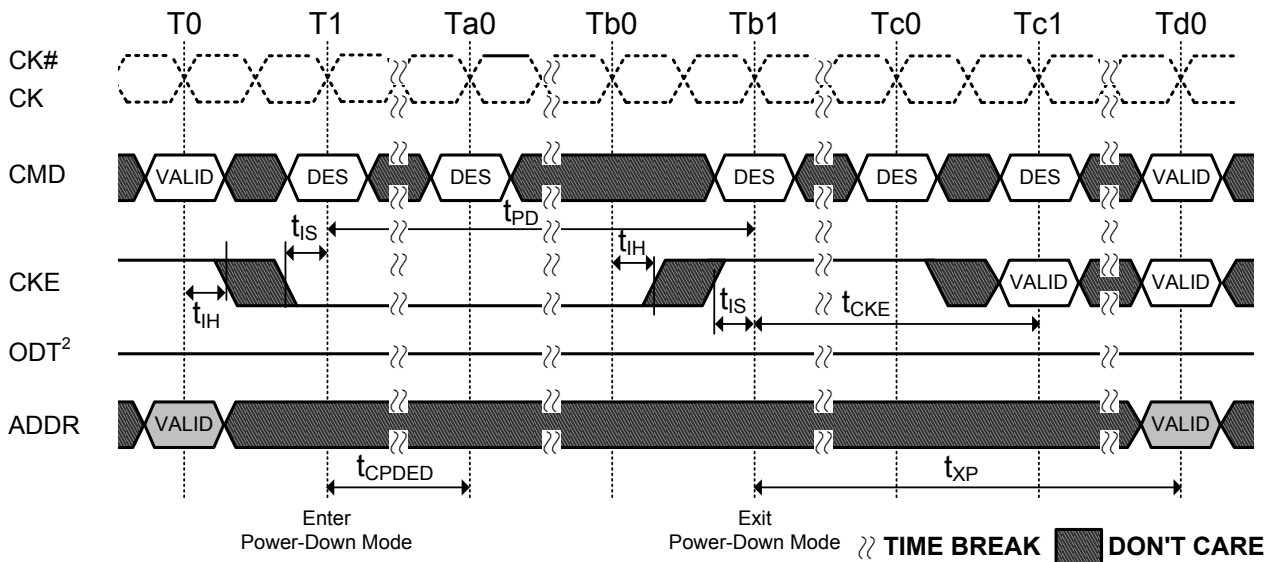
Entering power-down deactivates the input and output buffers, excluding CK, CK#, CKE and RESET#. In power-down mode, DRAM ODT input buffer deactivation is based on MR5 bit A5. If it is configured to 0b, ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide  $R_{TT\_NOM}$  termination. Note that DRAM continues to provide  $R_{TT\_PARK}$  termination if it is enabled in DRAM mode register MR5 A[8:6]. To protect DRAM internal delay on CKE line to block the input signals, multiple Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as  $t_{CPDED}$ . CKE low will result in deactivation of command and address receivers after  $t_{CPDED}$  has expired.

**Table 21. Power-Down Entry Definitions**

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	$t_{XP}$ to any valid command
Precharged (All banks precharged)	On	Fast	$t_{XP}$ to any valid command

Also, the DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE low, RESET# high, and a stable clock signal must be maintained at the inputs of the device, and ODT should be in a valid state, but all other input signals are "Don't Care." (If RESET# goes low during Power-Down, the device will be out of power-down mode and into reset state.) CKE low must be maintained until  $t_{CKE}$  has been satisfied. Power-down duration is limited by 9 times  $t_{REFI}$ .

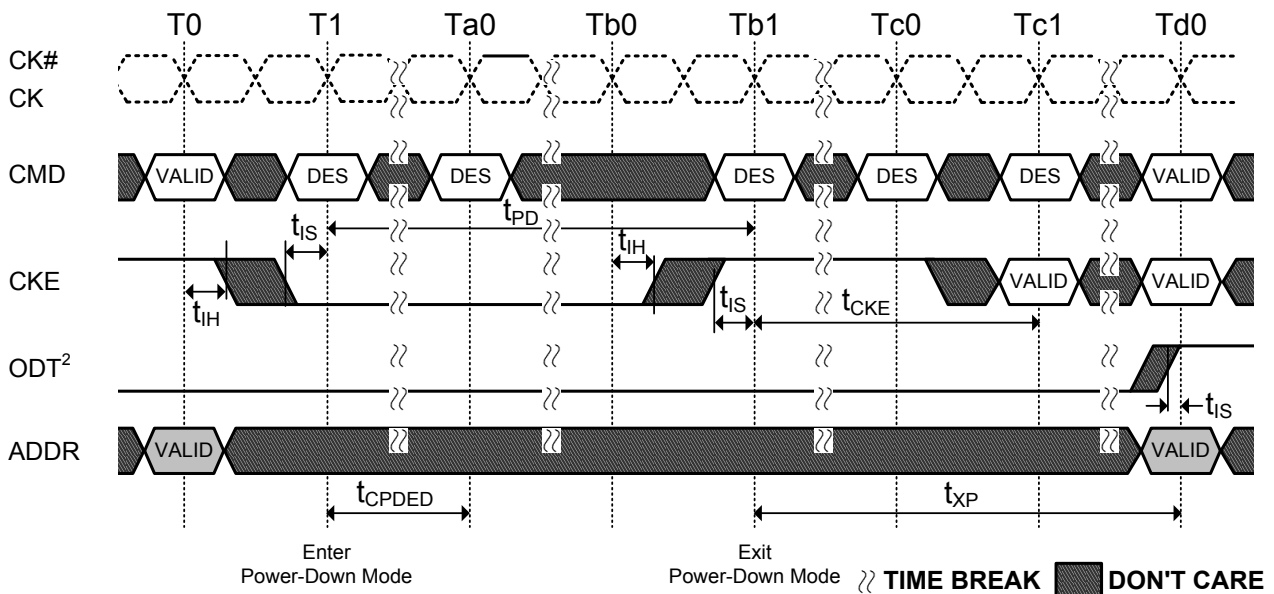
The power-down state is synchronously exited when CKE is registered high (along with a Deselect command). CKE high must be maintained until  $t_{CKE}$  has been satisfied. The ODT input signal must be at valid level when device exits from power-down mode independent of MR5 bit A5 if  $R_{TT\_NOM}$  is enabled in DRAM mode register. If  $R_{TT\_NOM}$  is disabled then ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency,  $t_{XP}$  after CKE goes high. Power-down exit latency is defined in the AC specifications table.



NOTE 1. Valid command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.

NOTE 2. ODT pin driven to a valid state. MR5 bit A5=0 (default setting) is shown.

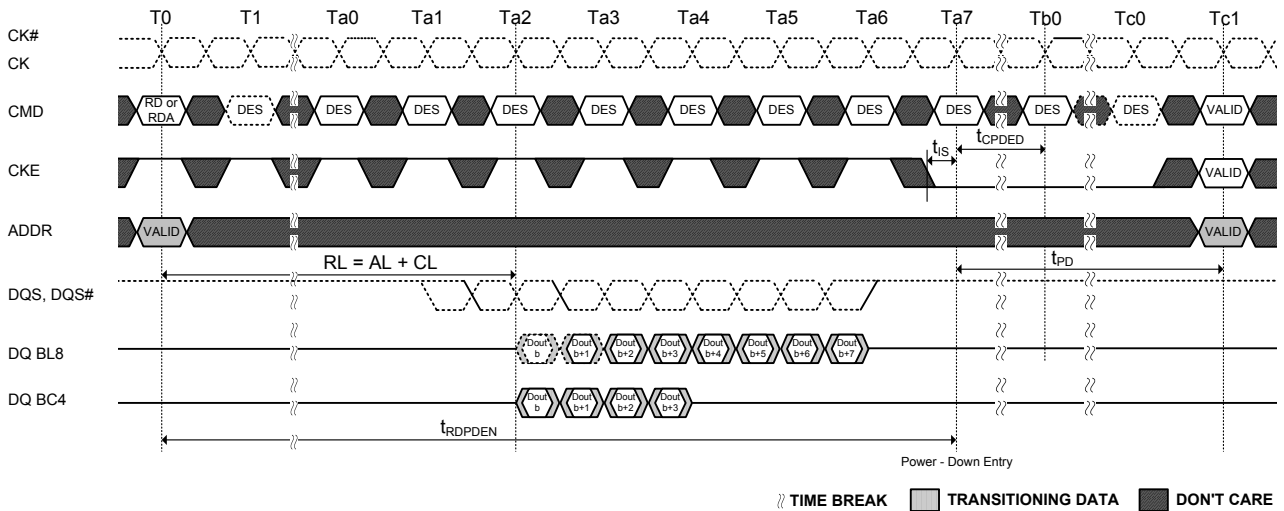
**Figure 27. Active Power-Down Entry and Exit Timing Diagram MR5 bit A5=0**



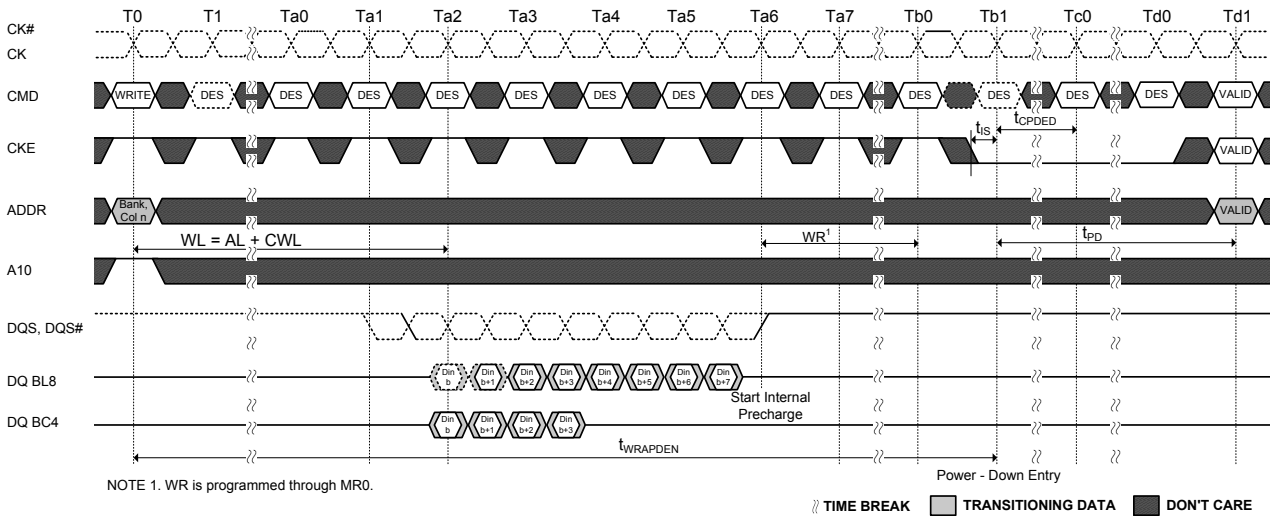
NOTE 1. Valid command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.

NOTE 2. ODT pin driven to a valid state. MR5 bit A5=1 is shown.

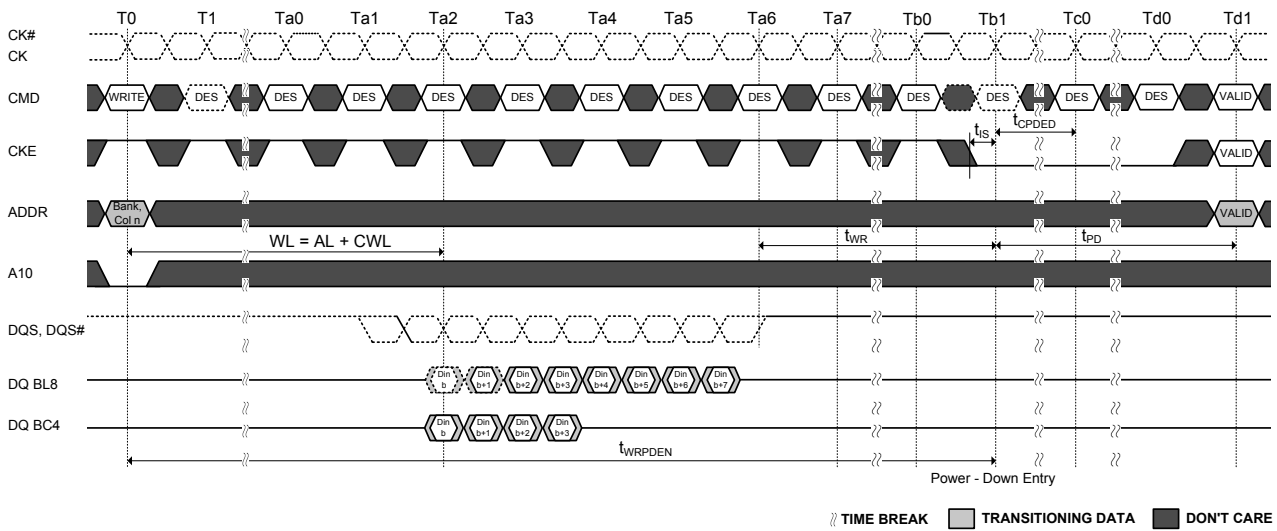
**Figure 28. Active Power-Down Entry and Exit Timing Diagram MR5 bit A5=1**



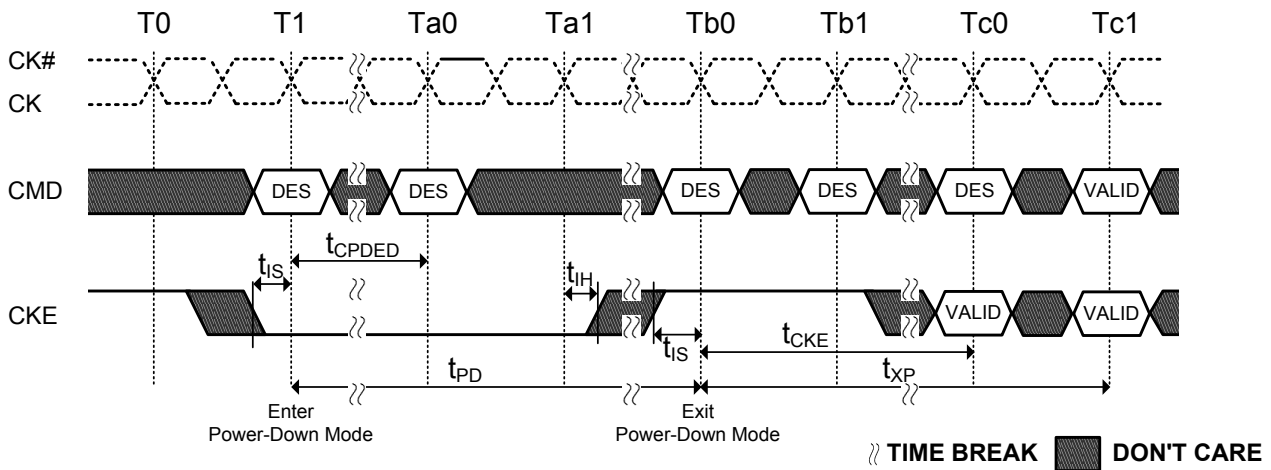
**Figure 29. Power-Down Entry after Read and Read with Auto Precharge**



**Figure 30. Power-Down Entry After Write with Auto Precharge**



**Figure 31. Power-Down Entry After Write**



**Figure 32. Precharge Power-Down Entry and Exit**

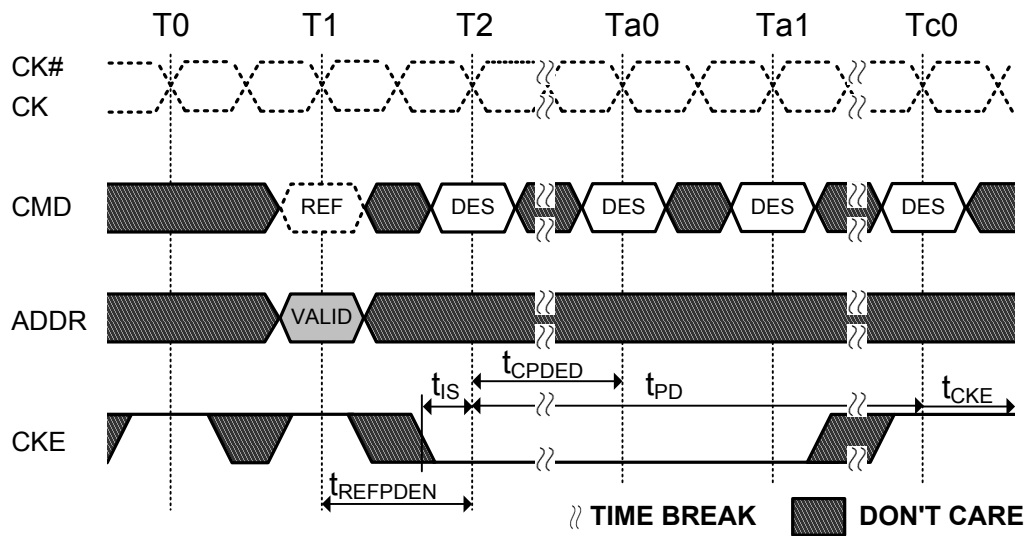


Figure 33. Refresh Command Power-Down Entry

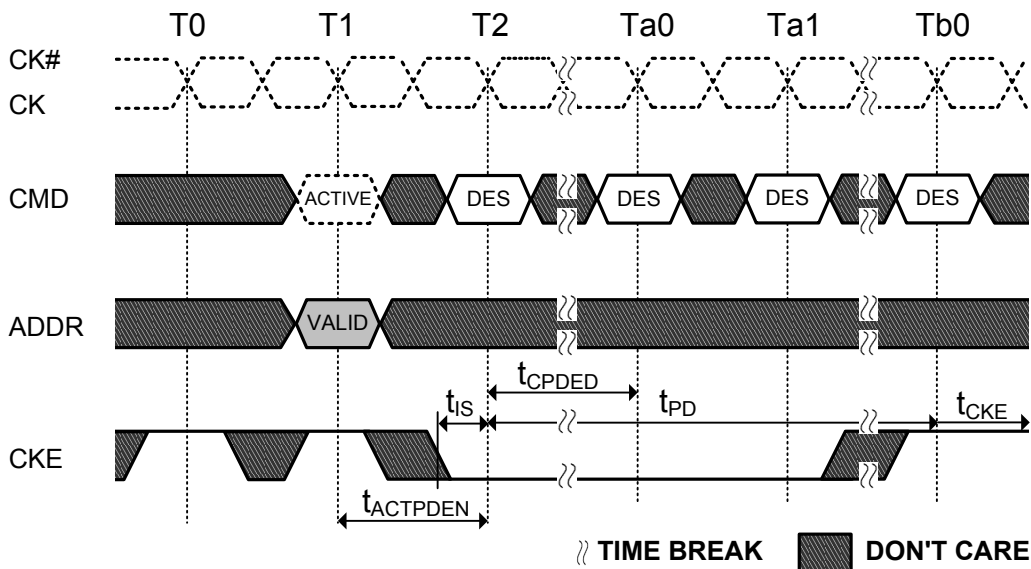
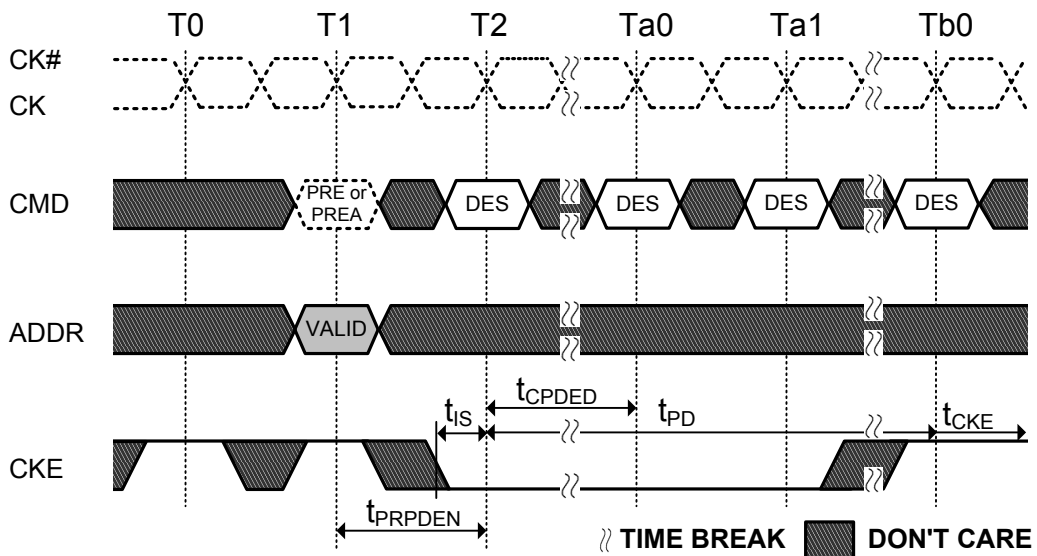
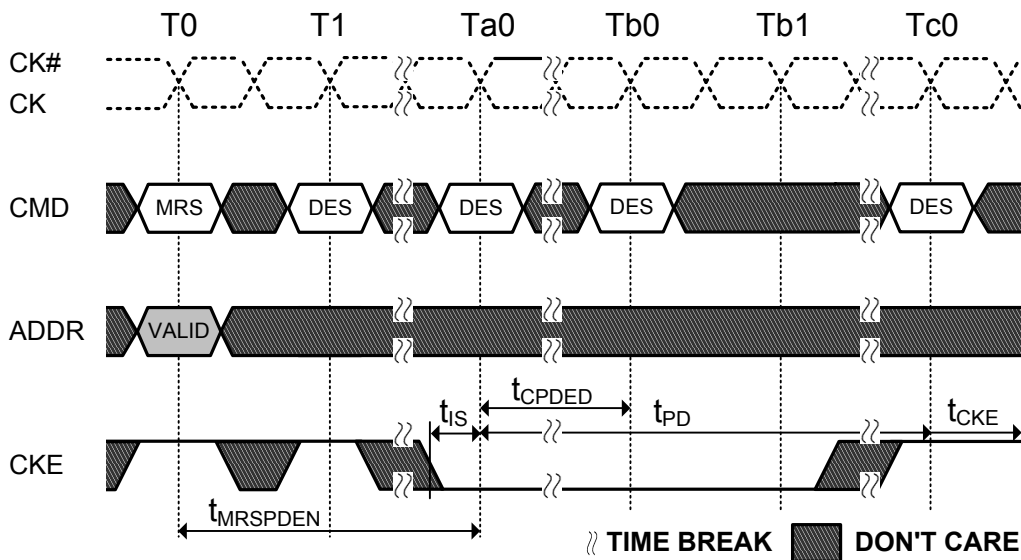


Figure 34. Activate Command Power-Down Entry



**Figure 35. Precharge/Precharge all Command Power-Down Entry**



**Figure 36. MRS Command Power-Down Entry**

## Power-Down Clarifications

When CKE is registered low for power-down entry,  $t_{PD(MIN)}$  must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter  $t_{PD(MIN)}$  is equal to the minimum value of parameter  $t_{CKE(MIN)}$  as shown in the timing parameters table. A detailed example of Case 1 is shown below.

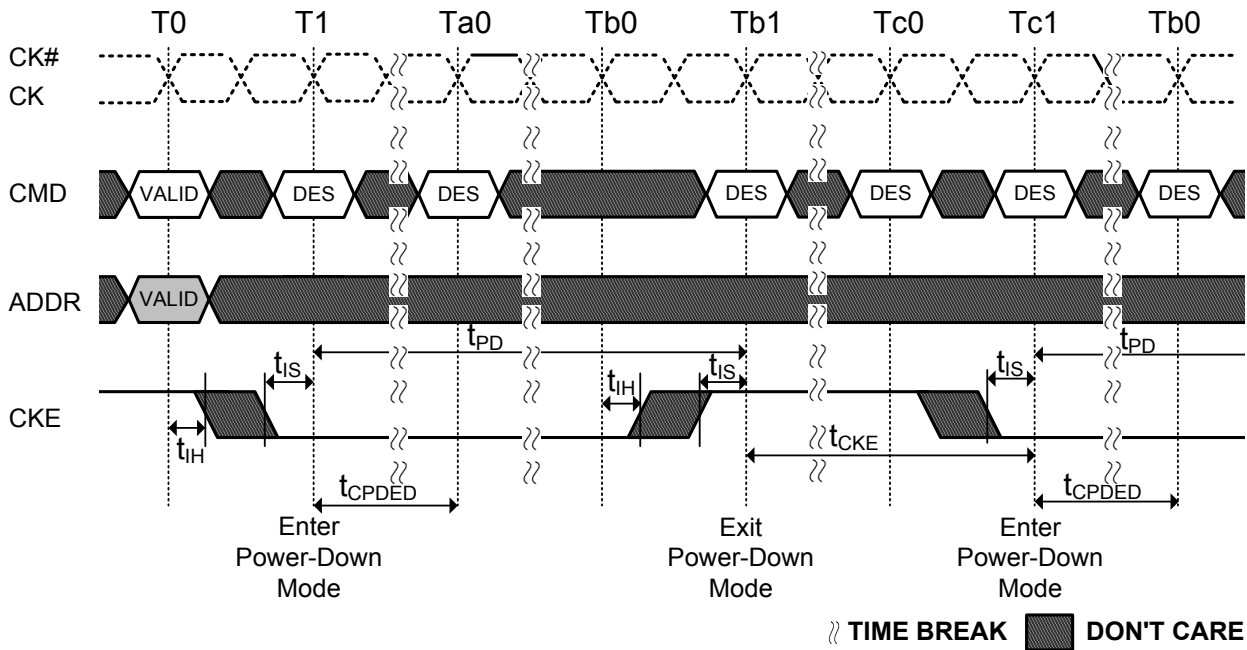
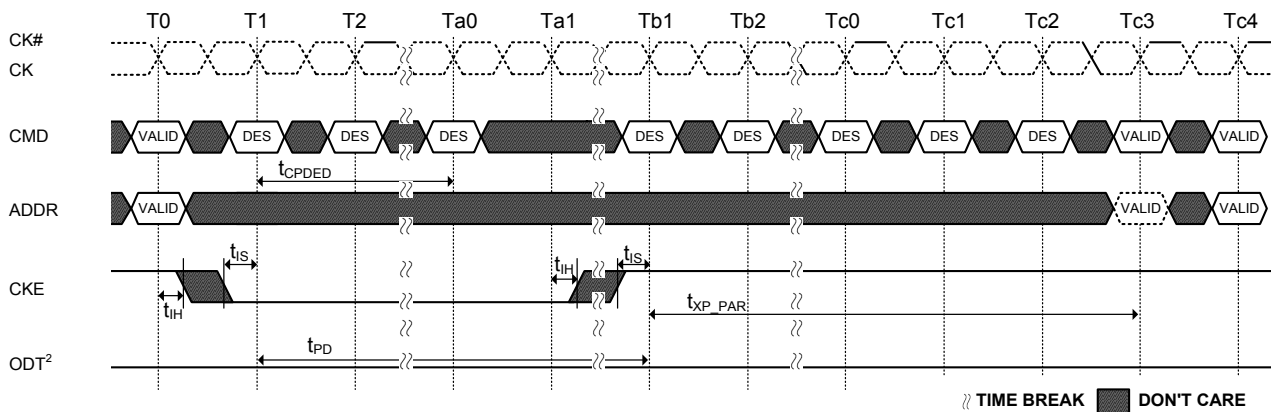


Figure 37. Power-Down Entry/Exit Clarification



### Power Down Entry and Exit timing during Command/Address Parity Mode is Enable

Power Down entry and exit timing during Command/Address Parity mode is enable shown below.



NOTE 1 VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.  
 NOTE 2 ODT pin driven to a valid state, MR5[A5 = 0] (default setting) is shown  
 NOTE 3 CA Parity = Enable

**Figure 38. Power-Down Entry and Exit Timing with C/A Parity**

**Table 22. AC Timing Table**

Symbol	Parameter	Min.	Max.	Unit
$t_{XP\_PAR}$	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled	max (4nCK,6ns) + PL	-	

## Control Gear-down Mode

The following description represents the sequence for the gear-down mode which is specified with MR3 A[3]. This mode is allowed just during initialization and self refresh exit. The DRAM defaults in 1/2 rate (1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS#, CKE and ODT in 1/4rate(2N) mode. For operation in 1/2 rate mode MRS command for gear-down or sync pulse are not required. DRAM defaults in 1/2 rate mode.

General sequence for operation in gear-down during initialization

- DRAM defaults to a 1/2 rate (1N mode) internal clock at power up/reset
- Assertion of Reset
- Assertion of CKE enables the DRAM
- MRS is accessed with a low frequency  $N \times t_{CK}$  gear-down MRS command. ( $Nt_{CK}$  static MRS command qualified by 1N CS#)
- DRAM controller sends 1N sync pulse with a low frequency  $N \times t_{CK}$  NOP command.  $t_{SYNC\_GEAR}$  is an even number of clocks. The sync pulse on even clock boundary from MRS command.
- Initialization sequence, including the expiration of  $t_{DLLK}$  and  $t_{ZQinit}$ , starts in 2N mode after  $t_{CMD\_GEAR}$  from 1N Sync Pulse.

General sequence for operation in gear-down after self refresh exit

- DRAM reset to 1N mode during self refresh
- MRS is accessed with a low frequency  $N \times t_{CK}$  gear-down MRS command. ( $Nt_{CK}$  static MRS command qualified by 1N CS# which meets  $t_{XS}$  or  $t_{XS\_Abort}$  Only Refresh command is allowed to be issued to DRAM before  $Nt_{CK}$  static MRS command.
- DRAM controller sends 1N sync pulse with a low frequency  $N \times t_{CK}$  NOP command.  $t_{SYNC\_GEAR}$  is an even number of clocks Sync pulse is on even clock boundary from MRS command.
- Valid command not requiring locked DLL is available in 2N mode after  $t_{CMD\_GEAR}$  from 1N Sync Pulse.
- Valid command requiring locked DLL is available in 2N mode after  $t_{DLLK}$  from 1N Sync Pulse.

If operation is 1/2 rate(1N) mode after self refresh, no  $N \times t_{CK}$  MRS command or sync pulse is required during self refresh exit. The min exit delay is  $t_{XS}$  or  $t_{XS\_Abort}$  to the first valid command.

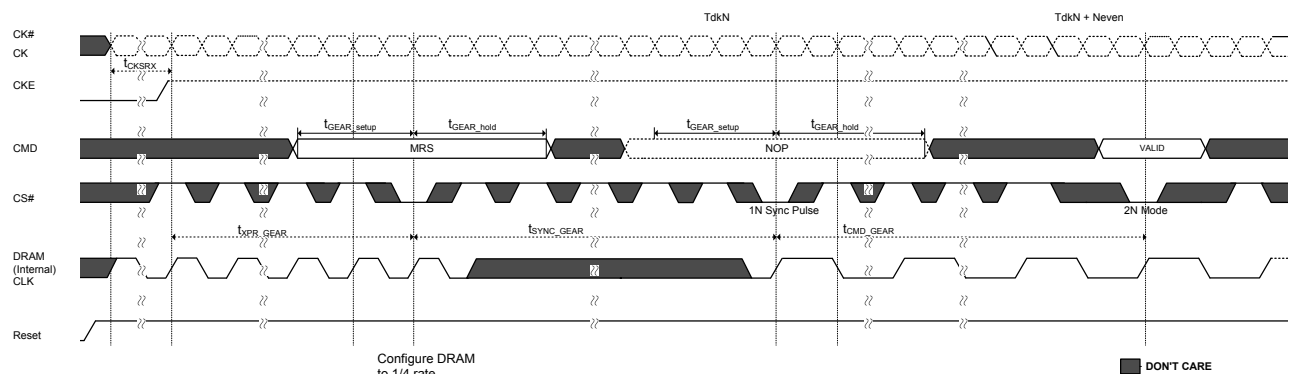
The DRAM may be changed from 1/4 rate ( 2N ) to 1/2 rate ( 1N ) by entering Self Refresh Mode, which will reset to 1N automatically. Changing from 1/4 ( 2N ) to 1/2 rate ( 1N ) by any other means, including setting MR3[A3] from 1 to 0, can result in loss of data and operation of the DRAM uncertain.

For the operation of gear-down mode in 1/4 rate, the following MR settings should be applied.

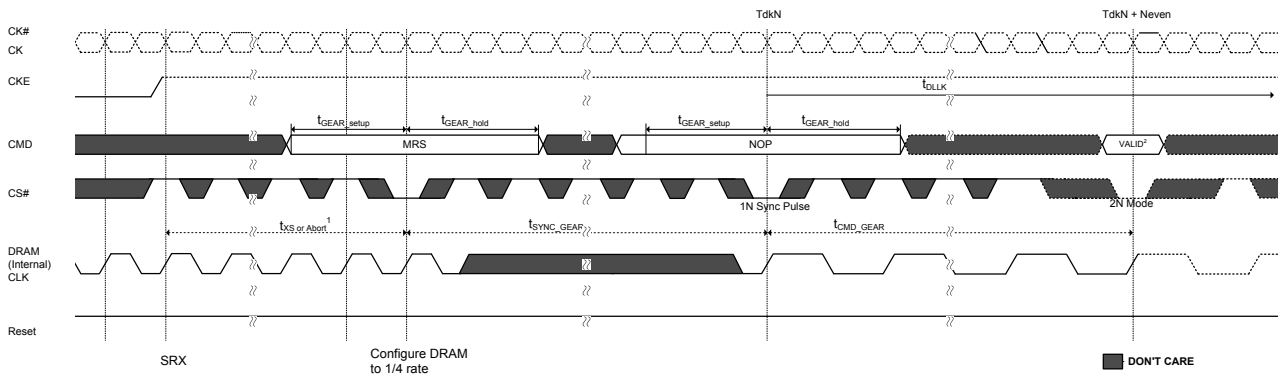
- CAS Latency (MR0 A[6:4,2]) : Even number of clocks
- Write Recovery and Read to Precharge (MR0 A[11:9]) : Even number of clocks
- Additive Latency (MR1 A[4:3]) : 0, CL -2
- CAS Write Latency (MR2 A[5:3]) : Even number of clocks
- CS to Command/Address Latency Mode (MR4 A[8:6]) : Even number of clocks
- CA Parity Latency Mode (MR5 A[2:0]) : Even number of clocks

CAL or CA parity mode must be disabled prior to Gear down MRS command. They can be enabled again after  $t_{SYNC\_GEAR}$  and  $t_{CMD\_GEAR}$  periods are satisfied.

The diagram below illustrates the sequence for control operation in 2N mode during initialization.



**Figure 39. Gear down (2N) mode entry sequence during initialization**



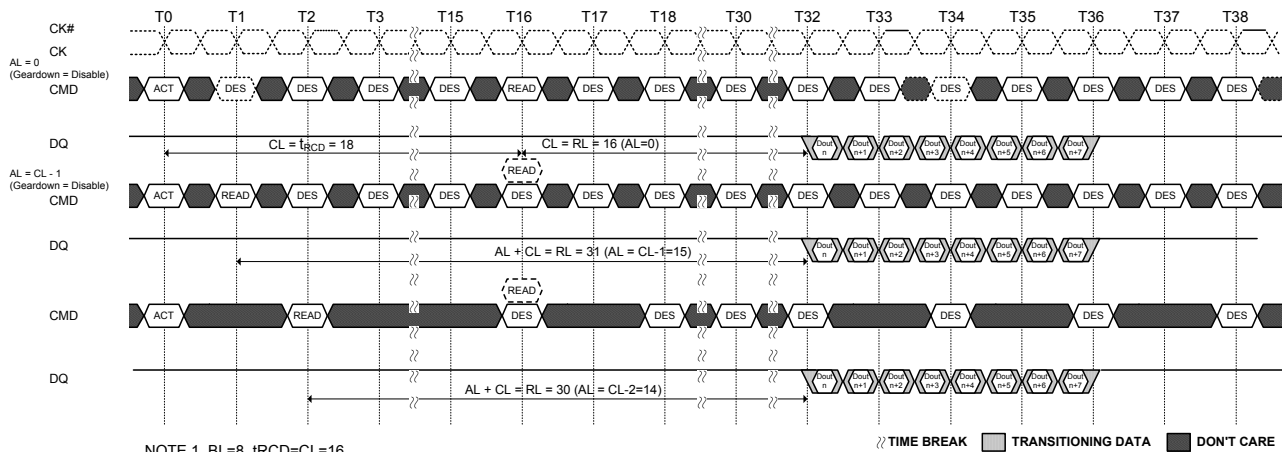
NOTE 1. CKE High Assert to Gear Down Enable Time ( $t_{\text{XS}}$ ,  $t_{\text{XS\_Abort}}$ ) depend on MR setting. A correspondence of  $t_{\text{XS}}$ / $t_{\text{XS\_Abort}}$  and MR Setting is as follows.

- MR4[A9] = 0 :  $t_{\text{XS}}$
- MR4[A9] = 1 :  $t_{\text{XS\_Abort}}$

NOTE 2. Command not requiring locked DLL

NOTE 3. Only DES is allowed during  $t_{\text{SYNC\_GEAR}}$

**Figure 40. Gear down (2N) mode entry sequence after self refresh exit (SRX)**



NOTE 1.  $BL = 8$ ,  $t_{\text{RCD}} = CL = 16$

NOTE 2.  $D_{\text{out } n}$  = data-out from column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

**Figure 41. Comparison Timing Diagram Between Geardown Disable and Enable**

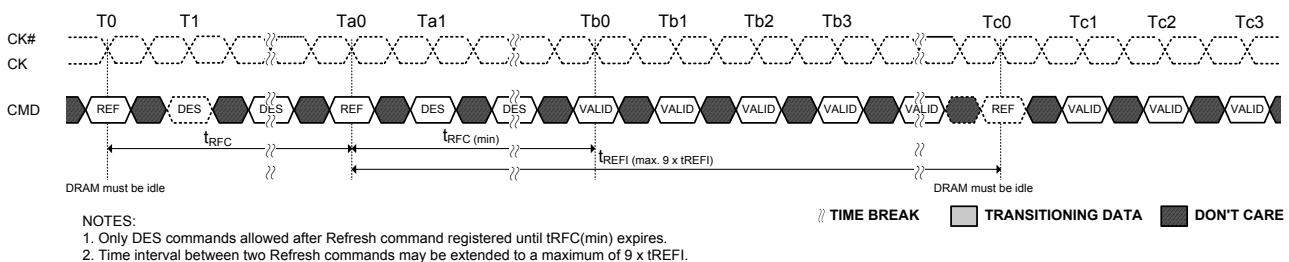
## Refresh Command

The Refresh command (REF) is used during normal operation of the device. This command is non persistent, so it must be issued each time a refresh is required. The device requires Refresh cycles at an average periodic interval of  $t_{REFI}$ . When CS#, RAS#/A16 and CAS#/A15 are held Low and WE#/A14 and ACT# are held High at the rising edge of the clock, the device enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time  $t_{RP(min)}$  before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except DES, must be greater than or equal to the minimum Refresh cycle time  $t_{RFC(min)}$ . The  $t_{RFC}$  timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the device regularly every  $t_{REFI}$  interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed when the device is in 1X refresh mode; a maximum of 16 Refresh commands can be postponed when the device is in 2X refresh mode; and a maximum of 32 Refresh commands can be postponed when the device is in 4X refresh mode.

When 8 consecutive Refresh commands are postponed, the resulting maximum interval between the surrounding Refresh commands is limited to  $9 \times t_{REFI}$ . For both the 2X and 4X refresh modes, the maximum interval between surrounding Refresh commands allowed is limited to  $17 \times t_{REFI}2$  and  $33 \times t_{REFI}4$ , respectively.

A limited number Refresh commands can be pulled-in as well. A maximum of 8 additional Refresh commands can be issued in advance or “pulled-in” in 1X refresh mode, a maximum of 16 additional Refresh commands can be issued when in advance in 2X refresh mode, and a maximum of 32 additional Refresh commands can be issued in advance when in 4X refresh mode. Each of these Refresh commands reduces the number of regular Refresh commands required later by one. Note that pulling in more than the maximum allowed Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to  $9 \times t_{REFI}$ ,  $17 \times t_{REFI}2$ , or  $33 \times t_{REFI}4$ . At any given time, a maximum of 16 additional REF commands can be issued within  $2 \times t_{REFI}$ , 32 additional REF2 commands can be issued within  $4 \times t_{REFI}2$ , and 64 additional REF4 commands can be issued within  $8 \times t_{REFI}4$  (larger densities are limited by  $t_{RFC}1$ ,  $t_{RFC}2$ , and  $t_{RFC}4$ , respectively, which must still be met).



**Figure 42. Refresh Command Timing (Example of 1x Refresh mode)**

## Data Mask (DM), Data Bus Inversion (DBI)

DDR4 SDRAM supports Data Mask (DM) function and Data Bus Inversion (DBI) function in x16 DRAM configuration.

DM#, DBI# functions are supported with dedicated one pin labeled as DM#/DBI#/TDQS. The pin is bi-directional pin for DRAM. The DM#/DBI# pin is Active Low as DDR4 supports  $V_{DDQ}$  reference termination. DM, DBI & TDQS functions are programmable through DRAM Mode Register (MR). The MR bit location is bit A12:A10 in MR5.

Write operation: Either DM or DBI function can be enabled but both functions cannot be enabled simultaneously. When both DM and DBI functions are disabled, DRAM turns off its input receiver and does not expect any valid logic level.

Read operation: Only DBI function applies. When DBI function is disabled, DRAM turns off its output driver and does not drive any valid logic level.

**Table 23. DM vs. DBI Function Matrix**

DM (MR5 bit A10)	Write DBI (MR5 bit A11)	Read DBI (MR5 bit A12)
Enabled	Disabled	Enabled or Disabled
Disabled	Enabled	Enabled or Disabled
Disabled	Disabled	Enabled or Disabled
Disabled	Disabled	Disabled

DM function during Write operation: DRAM masks the write data received on the DQ inputs if DM# was sampled Low on a given byte lane. If DM# was sampled High on a given byte lane, DRAM does not mask the write data and writes into the DRAM core.

DBI function during Write operation: DRAM inverts write data received on the DQ inputs if DBI# was sampled Low on a given byte lane. If DBI# was sampled High on a given byte lane, DRAM leaves the data received on the DQ inputs non-inverted.

DBI function during Read operation: DRAM inverts read data on its DQ outputs and drives DBI# pin Low when the number of '0' data bits within a given byte lane is greater than 4; otherwise DRAM does not invert the read data and drives DBI# pin High.

**Table 24. DQ Frame Format**

Write	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
LDM# or LDBI#	LDM0 or LDBI0	LDM1 or LDBI1	LDM2 or LDBI2	LDM3 or LDBI3	LDM4 or LDBI4	LDM5 or LDBI5	LDM6 or LDBI6	LDM7 or LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDM# or UDBI#	UDM0 or UDBI0	UDM1 or UDBI1	UDM2 or UDBI2	UDM3 or UDBI3	UDM4 or UDBI4	UDM5 or UDBI5	UDM6 or UDBI6	UDM7 or UDBI7
Read	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
LDBI#	LDBI0	LDBI1	LDBI2	LDBI3	LDBI4	LDBI5	LDBI6	LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDBI#	UDBI0	UDBI1	UDBI2	UDBI3	UDBI4	UDBI5	UDBI6	UDBI7

## ZQ Calibration Commands

ZQ Calibration command is used to calibrate DRAM  $R_{ON}$  & ODT values. The device needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of  $t_{ZQinit}$  to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after reset are allowed a timing period of  $t_{ZQoper}$ .

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter  $t_{ZQCS}$ . One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of  $R_{ON}$  and  $R_{TT}$  impedance error within 128 nCK for all speed bins assuming the maximum sensitivities specified in the Output Driver Voltage and ODT Voltage and Temperature Sensitivity tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature ( $T_{driftrate}$ ) and voltage ( $V_{driftrate}$ ) drift rates that the device is subject to in the application, is illustrated. The interval could be defined by the following formula:

---

Where  $T_{sens} = \max(dR_{TT}dT, dR_{ON}dTM)$  and  $V_{sens} = \max(dR_{TT}dV, dR_{ON}dVM)$  define temperature and voltage sensitivities.

For example, if  $T_{sens} = 1.5\%/^{\circ}C$ ,  $V_{sens} = 0.15\%/mV$ ,  $T_{driftrate} = 1^{\circ}C/sec$  and  $V_{driftrate} = 15mV/sec$ , then the interval between ZQCS commands is calculated as:

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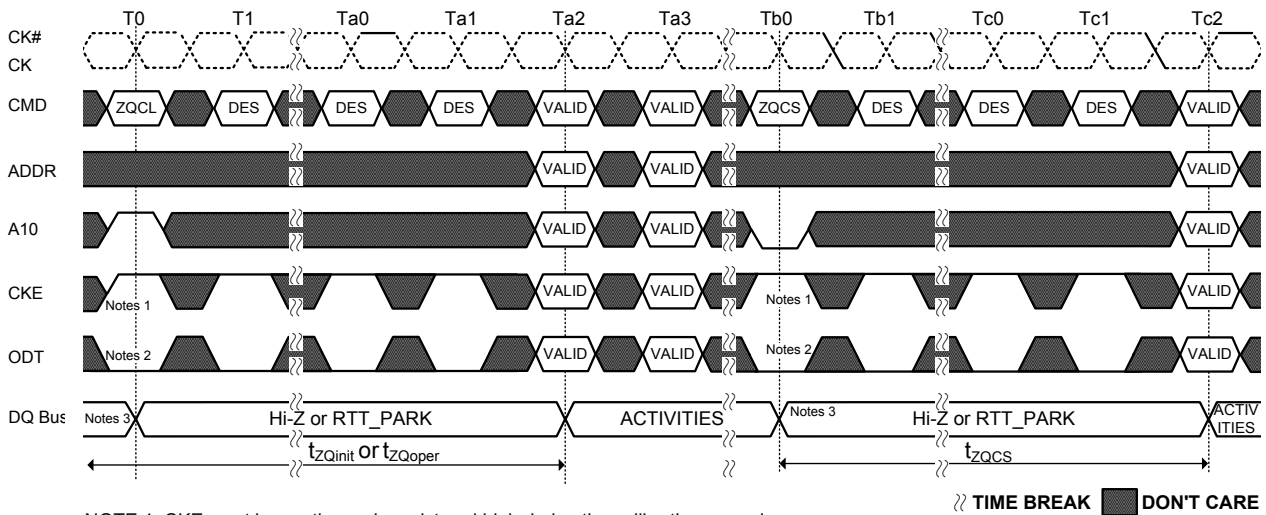
No other activities should be performed on the DRAM channel by the controller for the duration of  $t_{ZQinit}$ ,  $t_{ZQoper}$ , or  $t_{ZQCS}$ . The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the device should disable ZQ current consumption path to reduce power.

All banks must be precharged and  $t_{RP}$  met before ZQCL or ZQCS commands are issued by the controller. See "Command Truth Table" on Section 4.1 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh.

Upon Self-Refresh exit, the device will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is  $t_{XS}$ ,  $t_{XS\_Abort}$ /  $t_{XS\_FAST}$  depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of  $t_{ZQoper}$ ,  $t_{ZQinit}$ , or  $t_{ZQCS}$  between the devices.



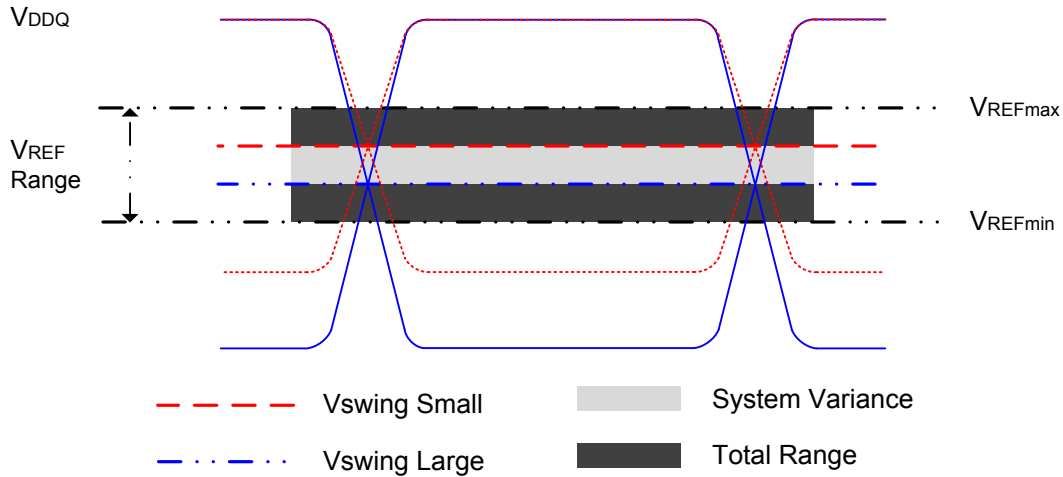
- NOTE 1. CKE must be continuously registered high during the calibration procedure.  
 NOTE 2. During ZQ Calibration, ODT signal must be held LOW and DRAM continues to provide RTT\_PARK.  
 NOTE 3. All devices connected to the DQ bus should be high impedance or RTT\_PARK during the calibration procedure.

**Figure 43. ZQ Calibration Timing**

## DQ V<sub>REF</sub> Training

The DRAM internal DQ V<sub>REF</sub> specification parameters are operating voltage range, stepsize, V<sub>REF</sub> step time, V<sub>REF</sub> full step time and V<sub>REF</sub> valid level.

The voltage operating range specifies the minimum required V<sub>REF</sub> setting range for DDR4 DRAM devices. The minimum range is defined by V<sub>REFmax</sub> and V<sub>REFmin</sub> as depicted in the following figure.

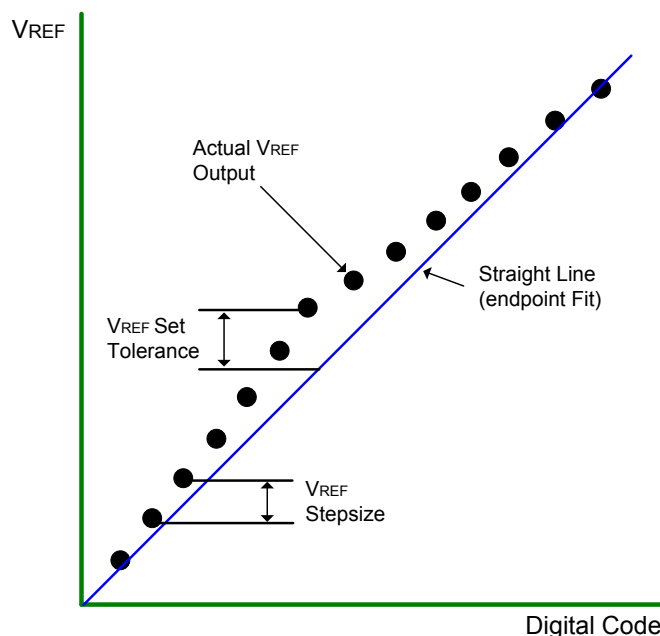


**Figure 44. V<sub>REFDQ</sub> Operating Range (V<sub>REFmin</sub>, V<sub>REFmax</sub>)**

The V<sub>REF</sub> stepsize is defined as the stepsize between adjacent steps. V<sub>REF</sub> stepsize ranges from 0.5% V<sub>DDQ</sub> to 0.8% V<sub>DDQ</sub>. However, for a given design, DRAM has one value for V<sub>REF</sub> step size that falls within the range.

The V<sub>REF</sub> set tolerance is the variation in the V<sub>REF</sub> voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V<sub>REF</sub> set tolerance uncertainty. The range of V<sub>REF</sub> set tolerance uncertainty is a function of number of steps n.

The V<sub>REF</sub> set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max V<sub>REF</sub> values for a specified range. An illustration depicting an example of the stepsize and V<sub>REF</sub> set tolerance is below.



**Figure 45. Example of V<sub>REF</sub> set tolerance (max case only shown) and stepsize**



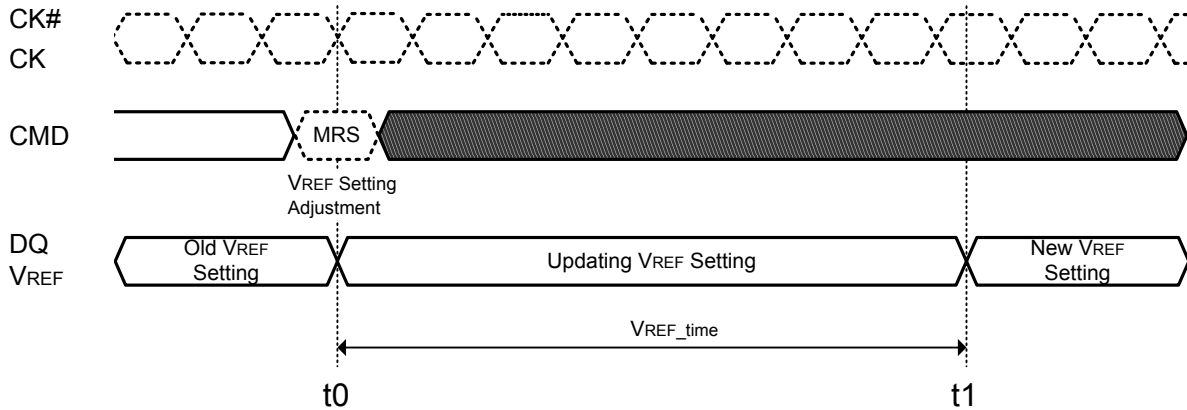
The  $V_{REF}$  increment/decrement step times are defined by  $V_{REF\_time}$ . The  $V_{REF\_time}$  is defined from  $t_0$  to  $t_1$ , where  $t_1$  is referenced to when the  $V_{REF}$  voltage is at the final DC level within the  $V_{REF}$  valid tolerance ( $V_{REF\_val\_tol}$ ).

The  $V_{REF}$  valid level is defined by  $V_{REF\_val}$  tolerance to qualify the step time  $t_1$ . This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any  $V_{REF}$  increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

$V_{REF\_time}$  is the time including up to  $V_{REFmin}$  to  $V_{REFmax}$  or  $V_{REFmax}$  to  $V_{REFmin}$  change in  $V_{REF}$  voltage.

$t_0$  - is referenced to MRS command clock

$t_1$  - is referenced to the  $V_{REF\_val\_tol}$

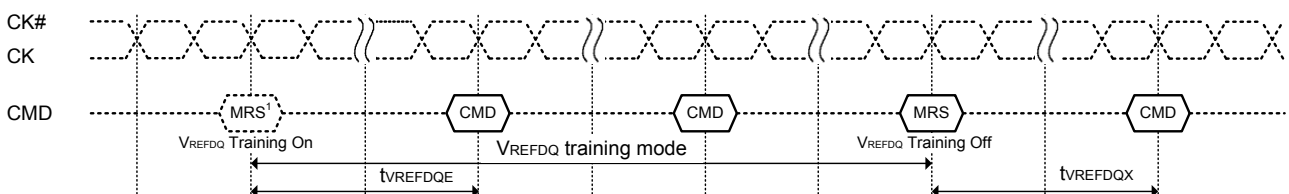


**Figure 46.  $V_{REF\_time}$  timing diagram**

$V_{REFDQ}$  Calibration Mode is entered via MRS command setting MR6 A[7] to 1 (0 disables  $V_{REFDQ}$  Calibration Mode), and setting MR6 A[6] to either 0 or 1 to select the desired range, and MR6 A[5:0] with a “don’t care” setting (there is no default initial setting; whether  $V_{REFDQ}$  training value (MR6 A[5:0]) at training mode entry with MR6 A[7] = 1 is captured by the DRAM or not is vendor specific). The next subsequent MR command is used to set the desired  $V_{REFDQ}$  values at MR6 A[5:0]. Once  $V_{REFDQ}$  Calibration Mode has been entered,  $V_{REFDQ}$  Calibration Mode legal commands may be issued once  $t_{VREFDQE}$  has been satisfied.  $V_{REFDQ}$  Calibration Mode legal commands are ACT, WR, WRA, RD, RDA, PRE, DES, MRS to set  $V_{REFDQ}$  values, and MRS to exit  $V_{REFDQ}$  Calibration Mode. Once  $V_{REFDQ}$  Calibration Mode has been entered, “dummy” write commands may be issued prior to adjusting  $V_{REFDQ}$  value the first time  $V_{REFDQ}$  calibration is performed after initialization. The “dummy” write commands may have bubbles between write commands provided other DRAM timings are satisfied. A possible example command sequence would be: WR1, DES, DES, DES, WR2, DES, DES, DES, WR3, DES, DES, DES, WR4, DES, DES, DES, WR50, DES, DES, DES. Setting  $V_{REFDQ}$  values requires MR6 [7] set to 1, MR6 [6] unchanged from initial range selection, and MR6 A[5:0] set to desired  $V_{REFDQ}$  value; if MR6 [7] is set to 0, MR6 [6:0] are not written.  $V_{REF\_time}$  must be satisfied after each MR6 command to set  $V_{REFDQ}$  value before the internal  $V_{REFDQ}$  value is valid.

If PDA mode is used in conjunction with  $V_{REFDQ}$  calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only  $V_{REFDQ}$  Calibration Mode legal commands noted above that may be used are the MRS commands, i.e. MRS to set  $V_{REFDQ}$  values, and MRS to exit  $V_{REFDQ}$  Calibration Mode.

The last A [6:0] setting written to MR6 prior to exiting  $V_{REFDQ}$  Calibration Mode is the range and value used for the internal  $V_{REFDQ}$  setting.  $V_{REFDQ}$  Calibration Mode may be exited when the DRAM is in idle state. After the MRS command to exit  $V_{REFDQ}$  Calibration Mode has been issued, DES must be issued till  $t_{VREFDQX}$  has been satisfied where any legal command may then be issued.



NOTE 1. The MR command used to enter  $V_{REFDQ}$  Calibration Mode treats MR6 A [5:0] as don’t care while the next subsequent MR command sets  $V_{REFDQ}$  values in MR6 A[5:0].

NOTE 2. Depending on the step size of the latest programmed  $V_{REF}$  value,  $V_{REF\_time}$  must be satisfied before disabling  $V_{REFDQ}$  training mode.

**Figure 47.  $V_{REFDQ}$  training mode entry and exit timing diagram**

**Table 25. AC parameters of V<sub>REFDQ</sub> training**

Symbol	Parameter	Min.	Max.	Unit
t <sub>VREFDQE</sub>	Enter V <sub>REFDQ</sub> training mode to the first valid command delay	150	-	ns
t <sub>VREFDQX</sub>	Exit V <sub>REFDQ</sub> training mode to the first valid command delay	150	-	ns

**Example scripts for V<sub>REFDQ</sub> Calibration Mode**

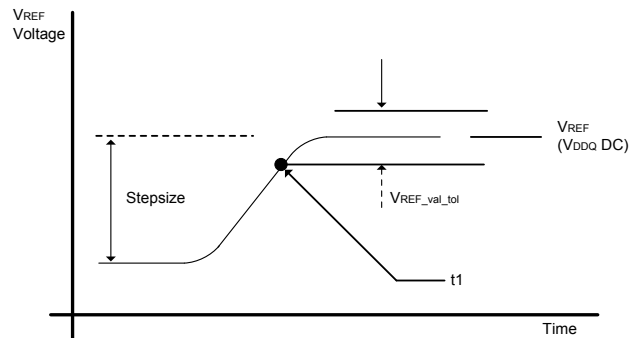
When MR6 [7] = 0 then MR6 [6:0] = XXXXXXXX

Entering V<sub>REFDQ</sub> Calibration if entering range 1:

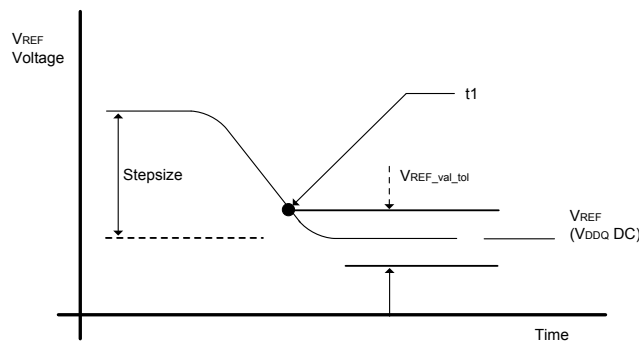
- MR6 [7:6] = 10 & [5:0] = XXXXXX
- All subsequent V<sub>REFDQ</sub> Calibration MR setting commands are MR6 [7:6] = 10 & MR6 [5:0] = VVVVVV - {VVVVVV are desired settings for V<sub>REFDQ</sub>}
- Issue ACT/WR/RD looking for pass/fail to determine V<sub>CENT</sub>(midpoint) as needed
- Just prior to exiting V<sub>REFDQ</sub> Calibration mode:
- Last two V<sub>REFDQ</sub> Calibration MR commands are
- MR6 [7:6] = 10, MR6 [5:0] = VVVVVV' where VVVVVV' = desired value for V<sub>REFDQ</sub>
- MR6 [7] = 0, MR6 [6:0] = XXXXXXXX to exit V<sub>REFDQ</sub> Calibration mode

Entering V<sub>REFDQ</sub> Calibration if entering range 2:

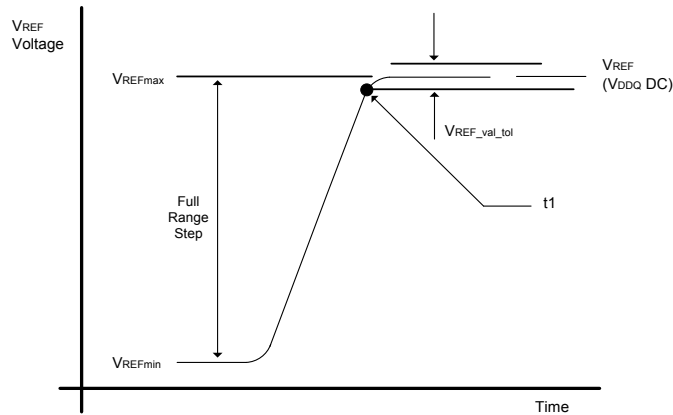
- MR6 [7:6] = 11 & [5:0] = XXXXXX
- All subsequent V<sub>REFDQ</sub> Calibration MR setting commands are MR6 [7:6]=11 & MR6 [5:0]=VVVVVV - {VVVVVV are desired settings for V<sub>REFDQ</sub>}
- Issue ACT/WR/RD looking for pass/fail to determine V<sub>CENT</sub>(midpoint) as needed
- Just prior to exiting V<sub>REFDQ</sub> Calibration mode:
- Last two V<sub>REFDQ</sub> Calibration MR commands are
- MR6 [7:6] = 11, MR6 [5:0] = VVVVVV' where VVVVVV' = desired value for V<sub>REFDQ</sub>
- MR6 [7] = 0, MR6 [6:0] = XXXXXXXX to exit V<sub>REFDQ</sub> Calibration mode



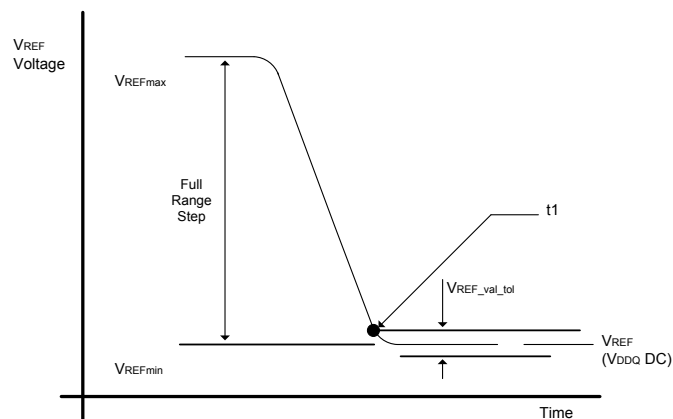
**Figure 48. V<sub>REF</sub> step single stepsize increment case**



**Figure 49. V<sub>REF</sub> step single stepsize decrement case**



**Figure 50. VREF full step from VREFmin to VREFmax case**



**Figure 51. VREF full step from VREFmax to VREFmin case**

**Table 26. DQ Internal VREF Specifications**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
VREF_max_R1	VREF max operating point range1	92%	-	-	VDDQ	1,10
VREF_min_R1	VREF min operating point range1	-	-	60%	VDDQ	1,10
VREF_max_R2	VREF max operating point range2	77%	-	-	VDDQ	1,10
VREF_min_R2	VREF min operating point range2	-	-	45%	VDDQ	1,10
VREF_step	VREF Stepsize	0.50%	0.65%	0.80%	VDDQ	2
VREF_set_tol	VREF Set Tolerance	-1.625%	0.00%	1.625%	VDDQ	3,4,6
		-0.15%	0.00%	0.15%	VDDQ	3,5,7
VREF_time	VREF Step Time	-	-	150	ns	8,11
VREF_val_tol	VREF Valid tolerance	-0.15%	0.00%	0.15%	VDDQ	9

Note 1. VREF DC voltage referenced to VDDQ\_DC. VDDQ\_DC is 1.2V.

Note 2. VREF stepsize increment/decrement range. VREF at DC level.

Note 3.  $V_{REF\_new} = V_{REF\_old} + n \times V_{REF\_step}$ ; n = number of step; if increment use "+"; If decrement use "-".

Note 4. The minimum value of VREF setting tolerance =  $V_{REF\_new} - 1.625\% \times V_{DDQ}$ . The maximum value of VREF setting tolerance =  $V_{REF\_new} + 1.625\% \times V_{DDQ}$  for n>4.

Note 5. The minimum value of VREF setting tolerance =  $V_{REF\_new} - 0.15\% \times V_{DDQ}$ . The maximum value of VREF setting tolerance =  $V_{REF\_new} + 0.15\% \times V_{DDQ}$  for n>4.

Note 6. Measured by recording the min and max values of the VREF output over the range, drawing a straight line between those points and comparing all other VREF output settings to that line.

Note 7. Measured by recording the min and max values of the VREF output across 4 consecutive steps (n = 4), drawing a straight line between those points and comparing all other VREF output settings to that line.

Note 8. Time from MRS command to increment or decrement one step size up to full range of VREF.

Note 9. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VREF valid is to qualify the step times which will be characterized at the component level.

Note 10. DRAM range1 or 2 set by MRS bit MR6, A6.

Note 11. If the VREF monitor is enabled, VREF\_time must be derated by: +10ns if DQ load is 0pF and an additional +15ns/pF of DQ loading.

## Per DRAM Addressability

DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or  $V_{REF}$  values on DRAM devices on a given rank.

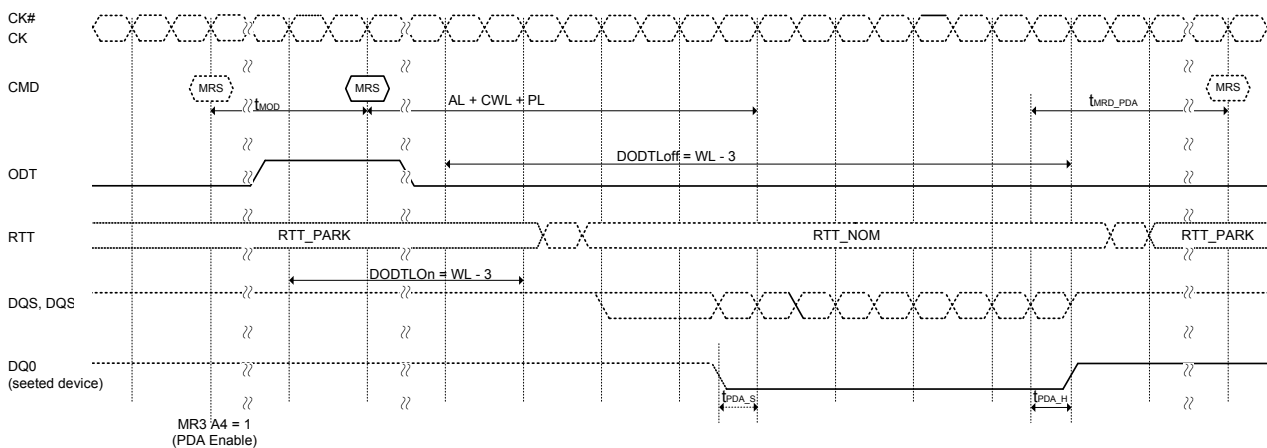
- Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required.
  - BL8 or BC4 may be used.
- Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible.
  - $R_{TT\_PARK}$  MR5 A[8:6] = Enable
  - $R_{TT\_NOM}$  MR1 A[10:8] = Enable
- Enable 'per DRAM addressability (PDA)' mode using MR3 A[4] = 1.
- In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0. The device captures DQ0 by using DQS signals. If the value on DQ0 is low, the DRAM executes the MRS command. If the value on DQ0 is high, the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
- Program the desired devices and mode registers using MRS command and DQ0.
- In the 'per DRAM addressability' mode, only MRS commands are allowed.
- The mode register set command cycle time at PDA mode,  $AL + CWL + BL/2 - 0.5t_{CK} + t_{MRD\_PDA} + (PL)$  is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.
- Remove the device from 'per DRAM addressability' mode by setting MR3 A[4] = 0. (This command will require DQ0 = 0)

**Note:** Removing a device from per DRAM addressability mode will require programming the entire MR3 when the MRS command is issued. This may impact some PDA values programmed within a rank as the exit command is sent to the rank. In order to avoid such a case the PDA Enable/Disable Control bit is located in a mode register that does not have any 'per DRAM addressability' mode controls.

In per DRAM addressability mode, device captures DQ0 using DQS signals the same as in a normal write operation; However, Dynamic ODT is not supported. Extra care required for the ODT setting. If  $R_{TT\_NOM}$  MR1 A[10:8] = Enable, device data termination need to be controlled by ODT pin and apply the same timing parameters (defined below).  $V_{REFDQ}$  value must be set to either its midpoint or  $V_{cent\_DQ}$  (midpoint) in order to capture DQ0 low level for entering PDA mode.

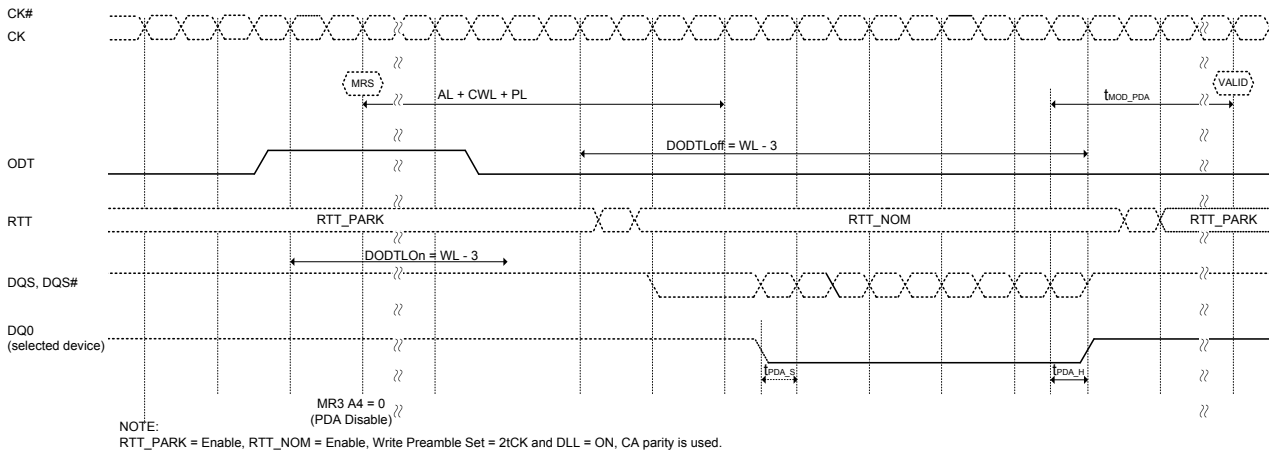
**Table 27. Applied ODT Timing Parameter to PDA Mode**

Symbol	Parameter
DODTLon	Direct ODT turn on latency
DODTLoFF	Direct ODT turn off latency
$t_{ADC}$	$R_{TT}$ change timing skew
$t_{AONAS}$	Asynchronous $R_{TT\_NOM}$ turn-on delay
$t_{AOFAS}$	Asynchronous $R_{TT\_NOM}$ turn-off delay

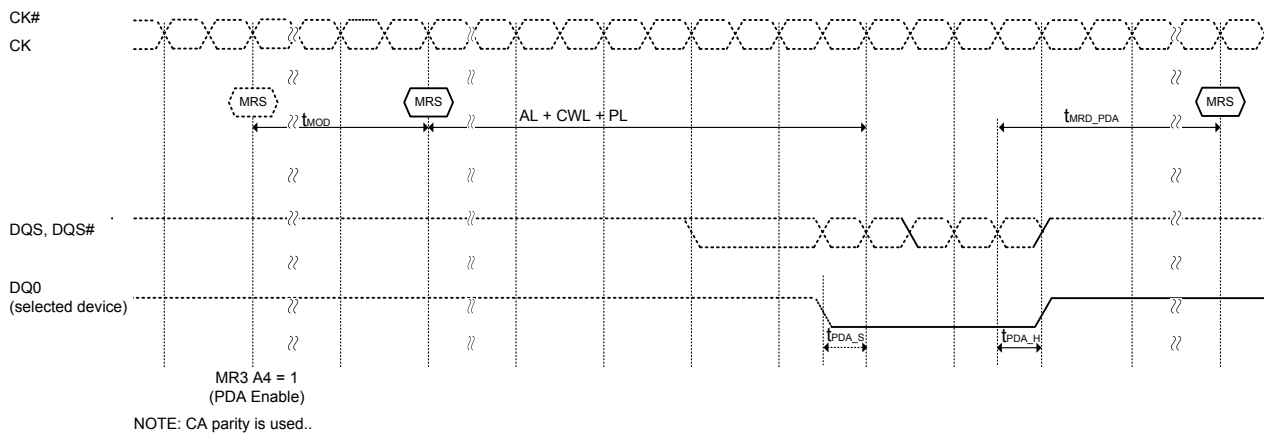


NOTE:  
 $R_{TT\_PARK}$  = Enable,  $R_{TT\_NOM}$  = Enable, Write Preamble Set = 2t<sub>CK</sub> and DLL = ON, CA parity is used.

**Figure 52. MRS w/ per DRAM addressability (PDA) issuing before MRS**



**Figure 53. MRS w/ per DRAM addressability (PDA) Exit**



**Figure 54. PDA using Burst Chop 4**

Since PDA mode may be used to program optimal  $V_{REF}$  for the DRAM, the DRAM may incorrectly read DQ level at the first DQS edge and the last falling DQS edge. It is recommended that DRAM samples DQ0 on either the first falling or second rising DQS edges.

This will enable a common implementation between BC4 and BL8 modes on the DRAM. Controller is required to drive DQ0 to a 'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

## Command Address Parity (CA Parity)

[A2:A0] of MR5 are defined to enable or disable C/A Parity in the DRAM. The default state of the C/A Parity bits is disabled. If C/A parity is enabled by programming a non-zero value to C/A Parity Latency in the mode register (the Parity Error bit must be set to zero when enabling C/A any Parity mode), then the DRAM has to ensure that there is no parity error before executing the command. The additional delay for executing the commands versus a parity disabled mode is programmed in the mode register (MR5, A2:A0) when C/A Parity is enabled (PL: Parity Latency) and is applied to commands that are latched via the rising edge of CK when CS# is low. The command is held for the time of the Parity Latency before it is executed inside the device. This means that issuing timing of internal command is determined with PL. When C/A Parity is enabled, only DES is allowed between valid commands to prevent DRAM from any malfunctioning. CA Parity Mode is supported when DLL-on Mode is enabled, use of CA Parity Mode when DLL-off Mode is enabled is not allowed.

C/A Parity signal (PAR) covers ACT#, RAS#/A16, CAS#/A15, WE#/A14 and the address bus including bank address and bank group bits. The control signals CKE, ODT and CS# are not included. (e.g., for a 4 Gbit x8 monolithic device, parity is computed across BG0, BA1, BA0, A16/RAS#, A15/CAS#, A14/WE#, A13-A0 and ACT#). (The DRAM treats any unused address pins internally as zeros; for example, if a common die has stacked pins but the device is used in a monolithic application, then the address pins used for stacking and not connected are treated internally as zeros.)

The convention of parity is even parity i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity bit is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even.

If a DRAM detects a C/A parity error in any command as qualified by CS# then it must perform the following steps:

- Ignore the erroneous command. Commands in max NnCK window ( $t_{PAR\_UNKNOWN}$ ) prior to the erroneous command are not guaranteed to be executed. When a Read command in this NnCK window is not executed, the DRAM does not activate DQS outputs.
- Log the error by storing the erroneous command and address bits in the error log.
- Set the Parity Error Status bit in the mode register to 1. The Parity Error Status bit must be set before the ALERT# signal is released by the DRAM (i.e.  $t_{PAR\_ALERT\_ON} + t_{PAR\_ALERT\_PW(min)}$ ).
- Assert the ALERT# signal to the host (ALERT# is active low) within  $t_{PAR\_ALERT\_ON}$  time.
- Wait for all in-progress commands to complete. These commands were received  $t_{PAR\_UNKNOWN}$  before the erroneous command. If a parity error occurs on a command issued between the  $t_{XS\_Fast}$  and  $t_{XS}$  window after self-refresh exit then the DRAM may delay the de-assertion of ALERT# signal as a result of any internal on going refresh.
- Wait for  $t_{RAS\_min}$  before closing all the open pages. The DRAM is not executing any commands during the window defined by ( $t_{PAR\_ALERT\_ON} + t_{PAR\_ALERT\_PW}$ ).
- After  $t_{PAR\_ALERT\_PW\_min}$  has been satisfied, the DRAM may de-assert ALERT#.
- After the device has returned to a known pre-charged state it may de-assert ALERT#.
- After ( $t_{PAR\_ALERT\_ON} + t_{PAR\_ALERT\_PW}$ ), the device is ready to accept commands for normal operation. Parity latency will be in effect, however, parity checking will not resume until the memory controller has cleared the Parity Error Status bit by writing a zero. (The DRAM will execute any erroneous commands until the bit is cleared).
- It is possible that the device might have ignored a refresh command during the ( $t_{PAR\_ALERT\_ON} + t_{PAR\_ALERT\_PW}$ ) window or the refresh command is the first erroneous frame so it is recommended that the controller issues extra refresh cycles as needed.
- The Parity Error Status bit may be read any time after ( $t_{PAR\_ALERT\_ON} + t_{PAR\_ALERT\_PW}$ ) to determine which DRAM had the error. The device maintains the Error Log for the first erroneous command until the Parity Error Status bit is reset to zero.

Mode Register for C/A Parity Error is defined as follows. C/A Parity Latency bits are write only, Parity Error Status bit is read/write and error logs are read only bits. The device controller can only program the Parity Error Status bit to zero. If the DRAM controller illegally attempts to write a '1' to the Parity Error Status bit the DRAM does not guarantee that parity will be checked. The DRAM may opt to block the controller from writing a '1' to the Parity Error Status bit.

DDR4 SDRAM supports MR bit for Persistent Parity Error Mode. This mode is enabled by setting MR5 A[9] = 1 and when it is enabled, DRAM resumes checking CA Parity after the ALERT# is deasserted, even if Parity Error Status bit is set as High. If multiple errors occur before the Error Status bit is cleared the error log in MPR page 1 should be treated as 'Don't Care'. In Persistent Parity Error Mode the ALERT# pulse will be asserted and deasserted by the DRAM as defined with the min. and max. value for  $t_{PAR\_ALERT\_PW}$ . The controller must issue Deselect commands once it detects the ALERT# signal, this response time is defined as  $t_{PAR\_ALERT\_RSP}$ . The following figure captures the flow of events on the C/A bus and the ALERT# signal.



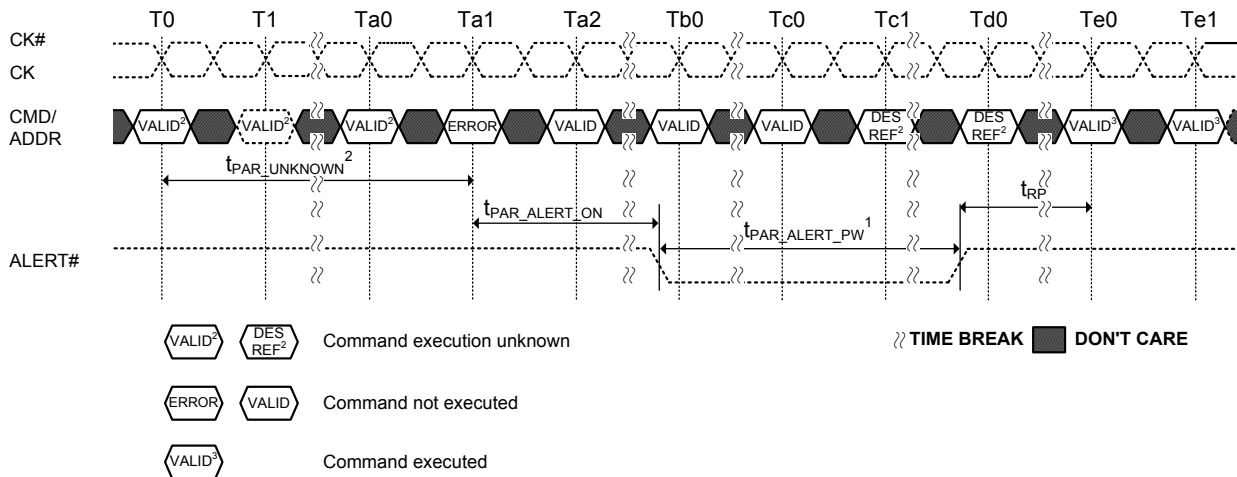
**Table 28. Mode Registers for C/A Parity**

C/A Parity Latency MR5[2:0]*	Speed bins	C/A Parity Error Status MR5[4]	Errant C/A Frame
000 = Disabled	-	0 = Clear	ACT#, BG0, BA0, BA1, PAR, A16/RAS#, A15/CAS#, A14/WE#, A13:A0
001= 4 Clocks	1600,1866,2133		
010= 5 Clocks	2400,2666	1 = Error	
011= 6 Clocks	RFU		
100= 8 Clocks	RFU		

Note 1. Parity Latency is applied to all commands.

Note 2. Parity Latency can be changed only from a C/A Parity disabled state, i.e. a direct change from PL= 4 → PL= 5 is not allowed. Correct sequence is PL= 4 → Disabled → PL= 5.

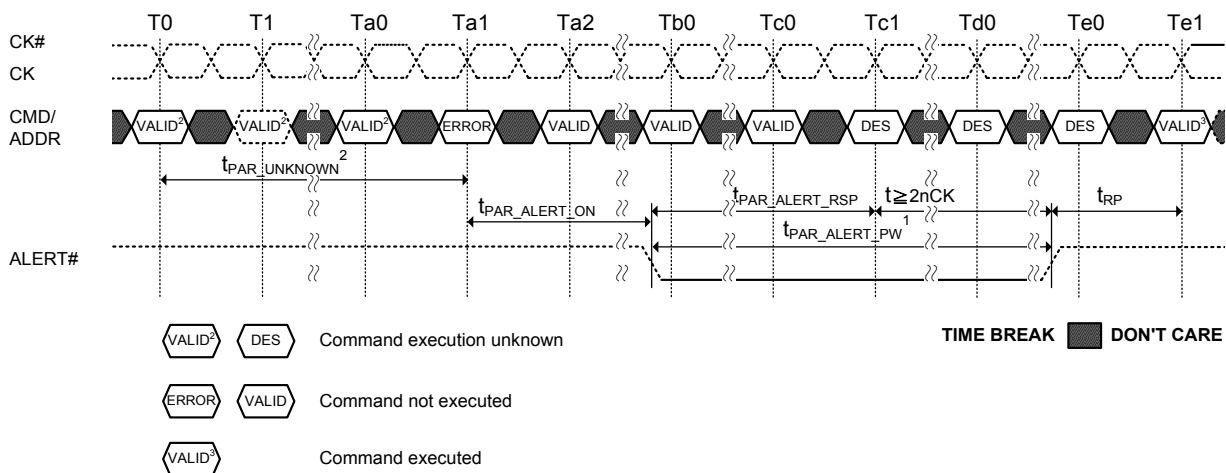
Note 3. Parity Latency is applied to write and read latency. Write Latency = AL+CWL+PL. Read Latency = AL+CL+PL.



NOTE 1. DRAM is emptying queues, Precharge All and parity checking off until Parity Error Status bit cleared.

NOTE 2. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 3. Normal operation with parity latency(CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

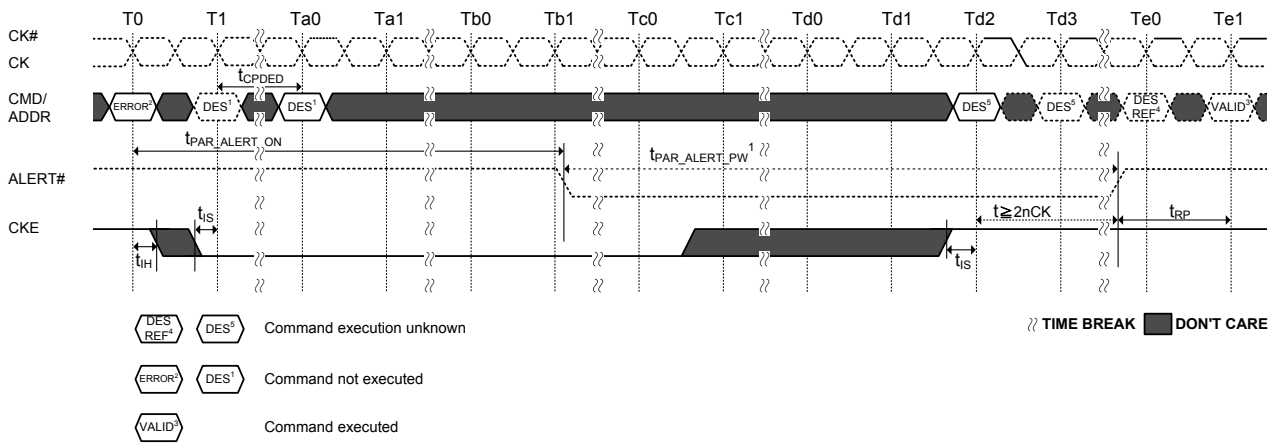
**Figure 55. Normal CA Parity Error Checking Operation**


NOTE 1. DRAM is emptying queues, Precharge All and parity check re-enable finished by tPAR\_ALERT\_PW.

NOTE 2. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.

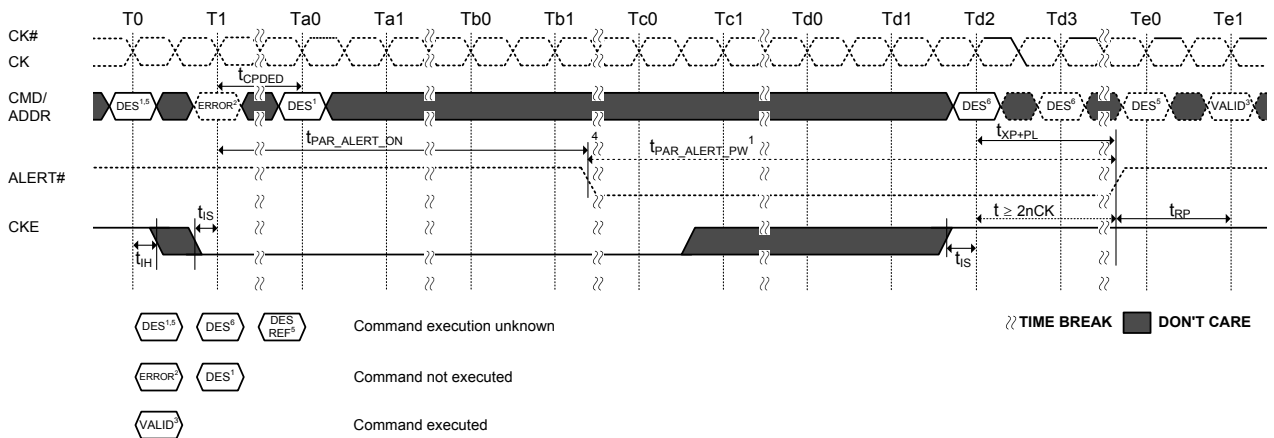
NOTE 3. Normal operation with parity latency and parity checking (CA Parity Persistent Error Mode enabled).

**Figure 56. Persistent CA Parity Error Checking Operation**



- NOTE 1. Deselect command only allowed.  
 NOTE 2. Error could be Precharge or Activate.  
 NOTE 3. Normal operation with parity latency (CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.  
 NOTE 4. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.  
 NOTE 5. Deselect command only allowed CKE may go high prior to Td2 as long as DES commands are issued.

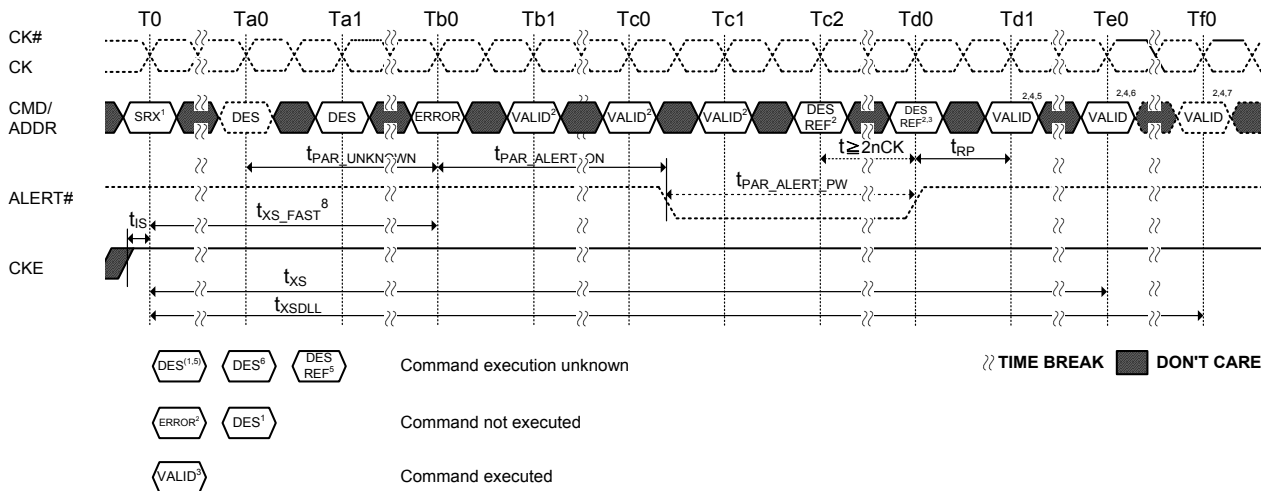
**Figure 57. CA Parity Error Checking - PDE/PDX**



- NOTE 1. Deselect command only allowed.  
 NOTE 2. SelfRefresh command error. DRAM masks the intended SRE command enters Precharge Power Down.  
 NOTE 3. Normal operation with parity latency (CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.  
 NOTE 4. Controller can not disable clock until it has been able to have detected a possible C/A Parity error.  
 NOTE 5. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.  
 NOTE 6. Deselect command only allowed CKE may go high prior to Tc2 as long as DES commands are issued.

**Figure 58. CA Parity Error Checking - SRE Attempt**





- NOTE 1. SelfRefresh Abort = Disable: MR4 [A9=0]  
 NOTE 2 Input commands are bounded by tXSDLL, tXS, tXS\_ABORT and tXS\_FAST timing.  
 NOTE 3 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.  
 NOTE 4 Normal operation with parity latency(CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.  
 NOTE 5 Only MRS (limited to those described in the Self-Refresh Operation section), ZQCS or ZQCL command allowed.  
 NOTE 6 Valid commands not requiring a locked DLL  
 NOTE 7 Valid commands requiring a locked DLL  
 NOTE 8 This figure shows the case from which the error occurred after tXS\_FAST\_An error also occur after tXS\_ABORT and tXS.

**Figure 59. CA Parity Error Checking - SRX**

### Command/Address parity entry and exit timings

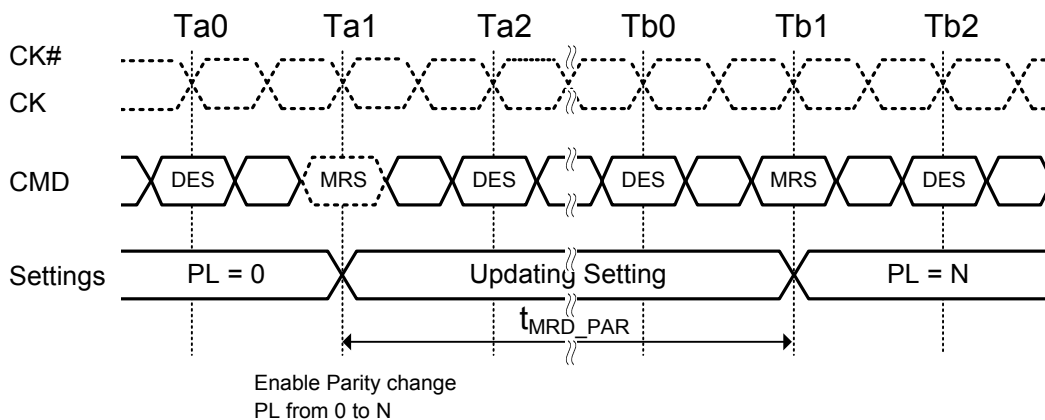
When in CA Parity mode, including entering and exiting CA Parity mode, users must wait  $t_{MRD\_PAR}$  before issuing another MRS command, and wait  $t_{MOD\_PAR}$  before any other commands.

$$t_{MOD\_PAR} = t_{MOD} + PL$$

$$t_{MRD\_PAR} = t_{MOD} + PL$$

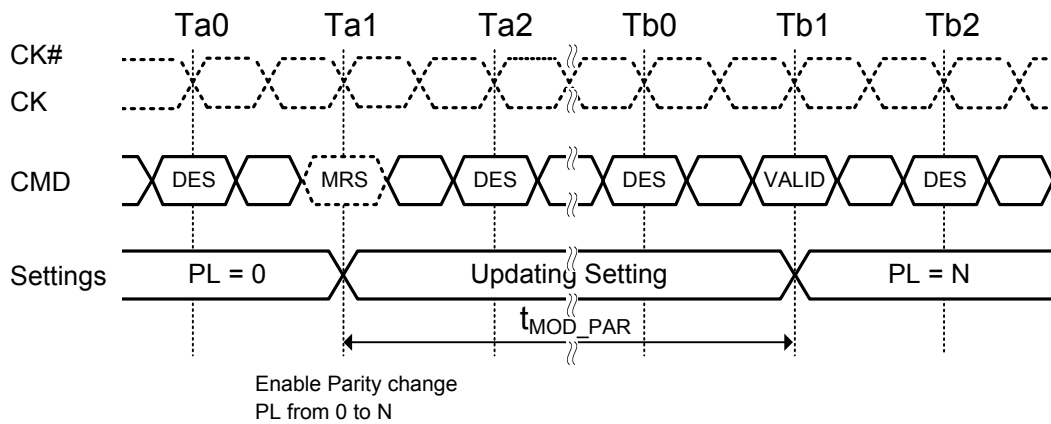
For CA parity entry, PL in the equations above is the parity latency programmed with the MRS command entering CA parity mode.

For CA parity exit, PL in the equations above is the programmed parity latency prior to the MRS command exiting CA parity mode.



- NOTE 1.  $t_{MRD\_PAR} = t_{MOD} + N$ ; where N is the programmed parity latency with the MRS command entering CA parity mode.  
 NOTE 2. Parity check is not available at Ta1 of MRS command due to PL=0 being valid.  
 NOTE 3. In case parity error happens at Tb1 of MRS command,  $t_{PAR\_ALERT\_ON}$  is ' $N[nCK] + 6[ns]$ '.

**Figure 60. Parity entry timing example -  $t_{MRD\_PAR}$**

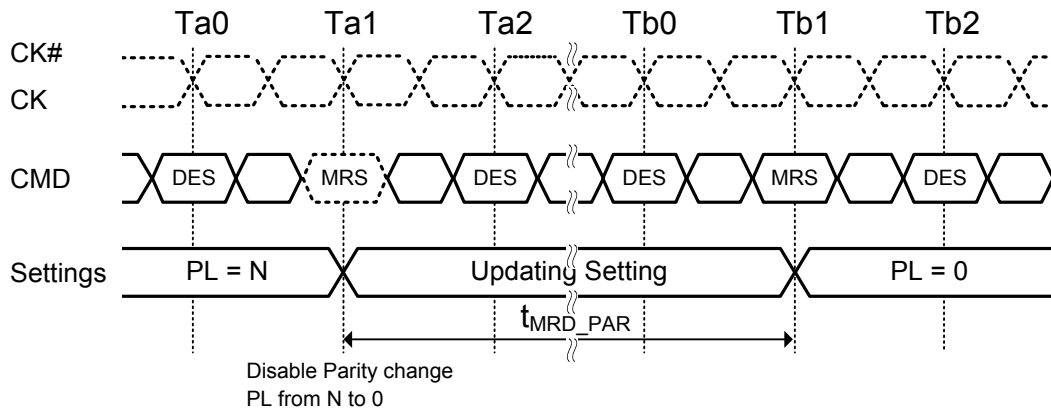


NOTE 1.  $t_{MOD\_PAR} = t_{MOD} + N$ ; where N is the programmed parity latency with the MRS command entering CA parity mode.

NOTE 2. Parity check is not available at Ta1 of MRS command due to PL=0 being valid.

NOTE 3. In case parity error happens at Tb1 of VALID command,  $t_{PAR\_ALERT\_ON}$  is ' $N[nCK] + 6[ns]$ '.

**Figure 61. Parity entry timing example -  $t_{MOD\_PAR}$**

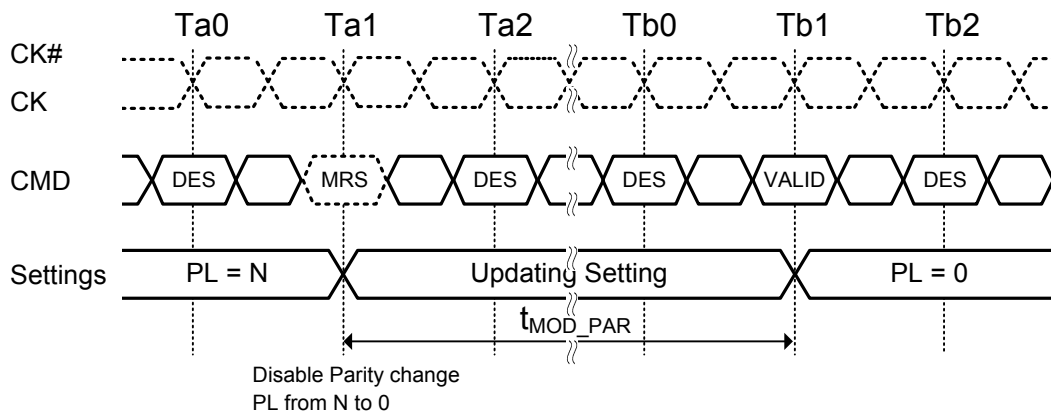


NOTE 1.  $t_{MRD\_PAR} = t_{MOD} + N$ ; where N is the programmed parity latency prior to the MRS command exiting CA parity mode.

NOTE 2. In case parity error happens at Ta1 of MRS command,  $t_{PAR\_ALERT\_ON}$  is ' $N[nCK] + 6[ns]$ '.

NOTE 3. Parity check is not available at Tb1 of MRS command due to disabling parity mode.

**Figure 62. Parity exit timing example -  $t_{MRD\_PAR}$**



NOTE 1.  $t_{MOD\_PAR} = t_{MOD} + N$ ; where N is the programmed parity latency prior to the MRS command exiting CA parity mode.

NOTE 2. In case parity error happens at Ta1 of MRS command,  $t_{PAR\_ALERT\_ON}$  is ' $N[nCK] + 6[ns]$ '.

NOTE 3. Parity check is not available at Tb1 of VALID command due to disabling parity mode.

**Figure 63. Parity exit timing example -  $t_{MOD\_PAR}$**

## Multipurpose Register

The Multipurpose Register (MPR) function, MPR access mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical pages, MPR Page 0 through MPR Page 3, with each page having four 8-bit registers, MPR0 through MPR3.

MPR mode enable and page selection is done with MRS commands. Data bus inversion (DBI) is not allowed during MPR Read operation. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and  $t_{RP}$  met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

Once the MPR access mode is enabled (MR3 A[2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF, and Reset; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. The mode register location is specified with the Read command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode and Self Refresh command are not allowed during MPR enable mode.

No other command can be issued within  $t_{RFC}$  after a REF command has been issued; 1x refresh (only) is to be used during MPR access mode. While in MPR access mode, MPR read or write sequences must be completed prior to a Refresh command.

### MR3 Setting for the MPR Access Mode

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting CS#, RAS#/A16, CAS#/A15 and WE#/A14 low, ACT#, BA0 and BA1 high and BG0 low while controlling the states of the address pins, Refer to the MR3 definition table for more detail.

**Table 29. DRAM Address to MPR UI Translation**

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM address – Ax	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI – UIx	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

**Table 30. MPR Data Format**

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note	
MPR page0 (Training Pattern)											
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)	
	01 = MPR1	0	0	1	1	0	0	1	1		
	10 = MPR2	0	0	0	0	1	1	1	1		
	11 = MPR3	0	0	0	0	0	0	0	0		
MPR page1 (CA Parity Error Log)											
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-only	
	01 = MPR1	CAS#/A15	WE#/A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]		
	10 = MPR2	PAR	ACT#	-	BG[0]	BA[1]	BA[0]	don't care	RAS#/A16		
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency* <sup>1</sup>			don't care	don't care	don't care		
MPR page2 (MRS Readout)											
BA1:BA0	00 = MPR0	hPPR	sPPR	R <sub>TT_WR</sub>	Temperature sensor* <sup>2</sup>		CRC Write Enable	R <sub>TT_WR</sub>		Read-only	
		-	-	MR2	-	-	MR2	MR2			
		-	-	A11	-	-	A12	A10	A9		
	01 = MPR1	V <sub>REFDQ</sub> Training range	V <sub>REFDQ</sub> Training Value						Geardown Enable		
		MR6	MR6						MR3		
		A6	A5	A4	A3	A2	A1	A0	A3		
	10 = MPR2	CAS Latency				RFU	CAS Write Latency				
		MR0				-	MR2				
		A6	A5	A4	A2	-	A5	A4	A3		
	11 = MPR3	R <sub>TT_NOM</sub>			R <sub>TT_PARK</sub>			Driver Impedance			
		MR1			MR5			MR1			
		A10	A9	A6	A8	A7	A6	A2	A1		
MPR page3 (RFU)* <sup>3</sup>											
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	Read-only	
	01 = MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care		
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care		
	11 = MPR3	don't care	don't care	don't care	don't care	MAC	MAC	MAC	MAC		

Note 1. MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

Note 2. MR bit for Temperature Sensor Readout

- MR3 bit A5=1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.
- MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0 bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh (> t <sub>REFI</sub> )
0	1	1X refresh rate(= t <sub>REFI</sub> )
1	0	2X refresh rate(1/2 * t <sub>REFI</sub> )
1	1	Reserved

Note 3. Restricted, except for MPR3 [3:0]

### MPR Reads

MPR reads are supported using BL8 and BC4 modes. Burst length on-the-fly is not supported for MPR reads. Data bus inversion (DBI) is not allowed during MPR Read operation; the device will ignore the Read DBI enable setting in MR5 [A12] when in MPR mode. Read commands for BC4 are supported with a starting column address of A[2:0] = 000 or 100. After power-up, the content of MPR Page 0 has the default values, which are defined in MPR Data Format table. MPR page 0 can be rewritten via an MPR Write command. The device maintains the default values unless it is rewritten by the DRAM controller. If the DRAM controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or there is power loss.

Timing in MPR mode:

- Reads (back-to-back) from Page 0 may use  $t_{\text{CCD}_S}$  or  $t_{\text{CCD}_L}$  timing between Read commands.
- Reads (back-to-back) from Pages 1, 2, or 3 may not use  $t_{\text{CCD}_S}$  timing between Read commands;  $t_{\text{CCD}_L}$  must be used for timing between Read commands. The following steps are required to use the MPR to read out the contents of a mode register (MPR Page x, MPRy).
  1. The DLL must be locked if enabled.
  2. Precharge all; wait until  $t_{\text{RP}}$  is satisfied.
  3. MRS command to MR3 A[2] = 1 (Enable MPR data flow), MR3 A[12:11] = MPR read format, and MR3 A[1:0] MPR page.
    - a. MR3 A[12:11] MPR read format:
      - 1) 00 = Serial read format
      - 2) 01 = Parallel read format
      - 3) 10 = Staggered read format
      - 4) 11 = RFU
    - b. MR3[1:0] MPR page:
      - 1) 00 = MPR Page 0
      - 2) 01 = MPR Page 1
      - 3) 10 = MPR Page 2
      - 4) 11 = MPR Page 3
  4.  $t_{\text{MRD}}$  and  $t_{\text{MOD}}$  must be satisfied.
  5. Redirect all subsequent Read commands to specific MPRx location.
  6. Issue RD or RDA command.
    - a. BA1 and BA0 indicate MPRx location:
      - 1) 00 = MPR0
      - 2) 01 = MPR1
      - 3) 10 = MPR2
      - 4) 11 = MPR3
    - b. A12/BC# = 0 or 1; BL8 or BC4 fixed-only, BC4 OTF not supported.
      - 1) If BL = 8 and MR0 A[1:0] = 01, A12/BC# must be set to 1 during MPR Read commands.
    - c. A2 = burst-type dependant:
      - 1) BL8: A2 = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
      - 2) BL8: A2 = 1 not allowed
      - 3) BC4: A2 = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
      - 4) BC4: A2 = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T
    - d. A[1:0] = 00, data burst is fixed nibble start at 00.
    - e. Remaining address inputs, including A10, BG0 are "Don't Care."
  7. After RL = AL + CL, DRAM bursts data from MPRx location; MPR readout format determined by MR3 A[12:10] and MR3 A[1:0].
  8. Steps 5 through 7 may be repeated to read additional MPRx locations.
  9. After the last MPRx Read burst,  $t_{\text{MPRR}}$  must be satisfied prior to exiting.
  10. Issue MRS command to exit MPR mode; MR3 A[2] = 0.
  11. After the  $t_{\text{MOD}}$  sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

## MPR Readout Serial Format

The serial format is required when enabling the MPR function to read out the contents of an MRx, temperature sensor status, and the command address parity error frame. However, data bus calibration locations (four 8-bit registers) can be programmed to read out any of the three formats. The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings).

Serial format implies that the same pattern is returned on all DQ lanes, as shown the table below, which uses values programmed into the MPR via [7:0] as 0111 1111.

**Table 31. MPR Readout Serial Format**

x4 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
x8 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
x16 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

## MPR Readout Parallel Format

Parallel format implies that the MPR data is returned in the first data UI and then repeated in the remaining UIs of the burst, as shown in the table below. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode. In this example, the pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). The x16 configuration, the same pattern is repeated on both the upper and lower bytes.

**Table 32. MPR Readout Serial Format**

x4 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
x8 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
x16 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

## MPR Readout Staggered Format

Staggered format of data return is defined as the staggering of the MPR data across the lanes. In this mode, an RD/RDA command is issued to a specific data pattern location and then the data is returned on the DQ from each of the different data pattern locations. For the x4 configuration, an RD/RDA to data pattern location 0 will result in data from location 0 being driven on DQ0, data from location 1 being driven on DQ1, data from location 2 being driven on DQ2, and so on, as shown below. Similarly, an RD/RDA command to data pattern location 1 will result in data from location 1 being driven on DQ0, data from location 2 being driven on DQ1, data from location 3 being driven on DQ2, and so on. Examples of different starting locations are also shown.

**Table 33. MPR Readout Staggered Format, x4**

x4 Read MPR0 Command		x4 Read MPR1 Command		x4 Read MPR2 Command		x4 Read MPR3 Command	
Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2

It is expected that the DRAM can respond to back-to-back RD/RDA commands to the MPR for all DDR4 frequencies so that a sequence (such as the one that follows) can be created on the data bus with no bubbles or clocks between read data. In this case, the system memory controller issues a sequence of RD(MPR0), RD(MPR1), RD(MPR2), RD(MPR3), RD(MPR0), RD(MPR1), RD(MPR2), and RD(MPR3).

**Table 34. MPR Readout Staggered Format, x4 – Consecutive Reads**

Stagger	UI[7:0]	UI[15:8]	UI[23:16]	UI[31:24]	UI[39:32]	UI[47:40]	UI[55:48]	UI[63:56]
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

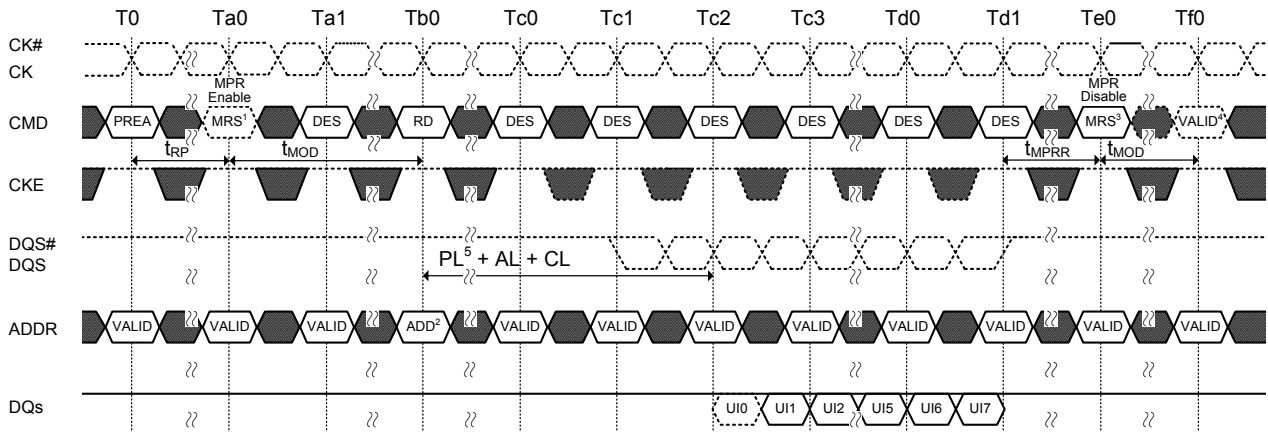
For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case. A read example to MPR0 for x8 and x16 configurations is shown below.

**Table 35. MPR Readout Staggered Format, x8 and x16**

x8 Read MPR0 Command		x16 Read MPR0 Command			
Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3

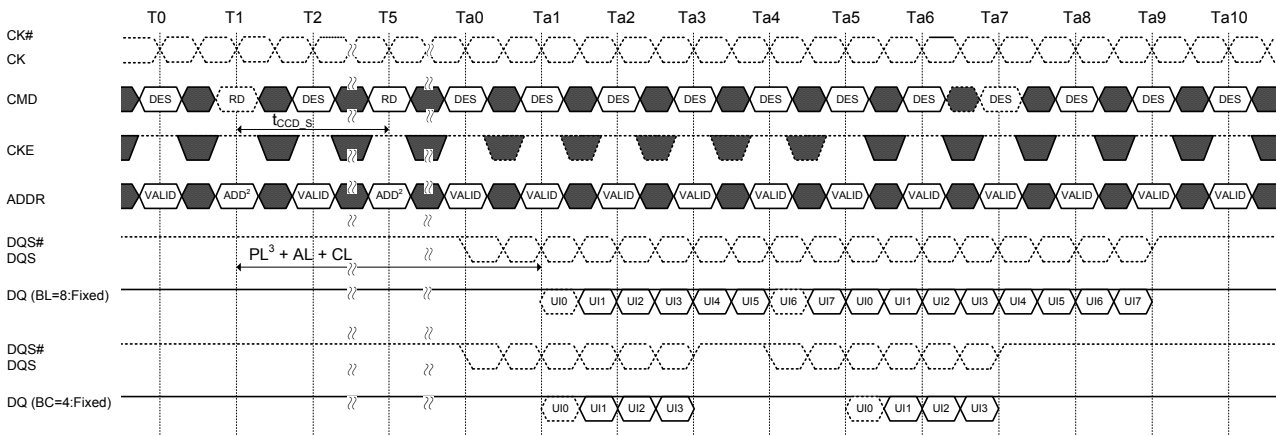


## MPR Read Waveforms



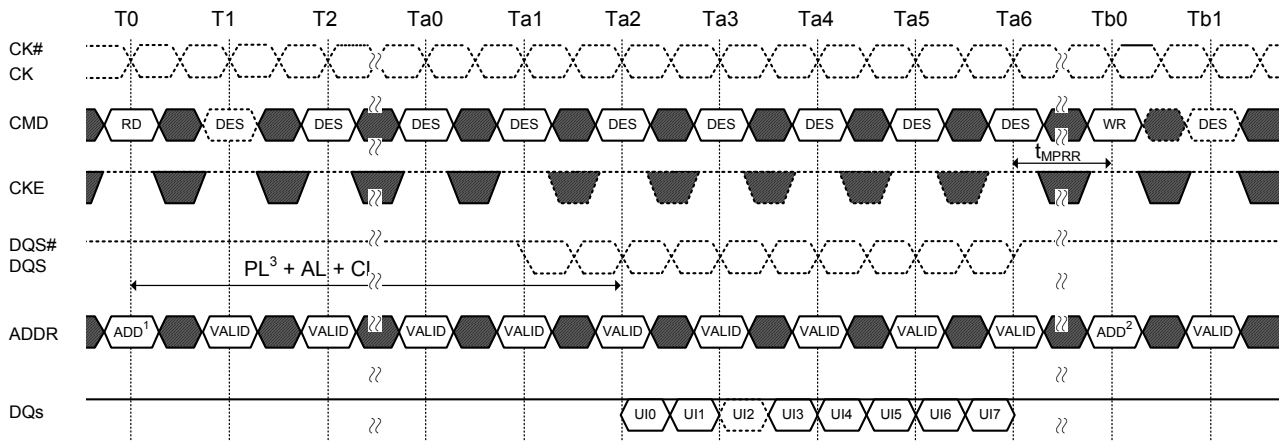
- NOTE 1. Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)  
 - Redirect all subsequent read and writes to MPR locations
- NOTE 2. Address setting  
 - A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)  
 - A[2] = "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)  
 - BA1 and BA0 indicate the MPR location  
 - A10 and other address pins are don't care including BG0. A12 is don't care when MR0 A[1:0] = "00" or "10", and must be '1'b when MR0 A[1:0] = "01"
- NOTE 3. Multi-Purpose Registers Read/Write Disable (MR3 A2 = 0)
- NOTE 4. Continue with regular DRAM command.
- NOTE 5. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

**Figure 64. MPR Read Timing**



- NOTE 1. t<sub>CCD\_S</sub> = 4, Read Preamble = 1tCK
- NOTE 2. Address setting  
 - A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)  
 - A[2] = "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7) (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)  
 - BA1 and BA0 indicate the MPR location  
 - A10 and other address pins are don't care including BG0. A12 is don't care when MR0 A[1:0] = "00" or "10", and must be '1'b when MR0 A[1:0] = "01"
- NOTE 3. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

**Figure 65. MPR Back to Back Read Timing**



**NOTE 1. Address setting**

- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)
- A[2] = "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG0. A12 is don't care when MR0 A[1:0] = "00", and must be '1'b when MR0 A[1:0] = "01"

**NOTE 2. Address setting**

- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

**NOTE 3.** PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

**Figure 66. MPR Read to Write Timing**

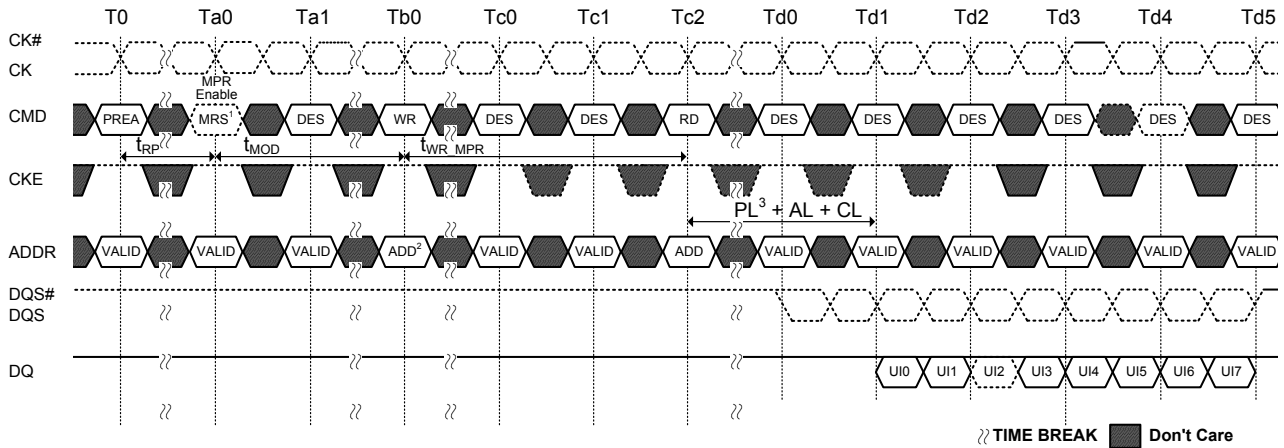
### MPR Writes

MPR access mode allows 8-bit writes to the MPR Page 0 using the address bus A[7:0]. Data bus inversion (DBI) is not allowed during MPR Write operation. The DRAM will maintain the new written values unless re-initialized or there is power loss.

The following steps are required to use the MPR to write to mode register MPR Page 0.

1. The DLL must be locked if enabled.
2. Precharge all; wait until  $t_{RP}$  is satisfied.
3. MRS command to MR3 A[2] = 1 (enable MPR data flow) and MR3 A[1:0] = 00 (MPR Page 0); writes to 01, 10, and 11 are not allowed.
4.  $t_{MRD}$  and  $t_{MOD}$  must be satisfied.
5. Redirect all subsequent Write commands to specific MPRx location.
6. Issue WR or WRA command:
  - a. BA1 and BA0 indicate MPRx location
    - 1) 00 = MPR0
    - 2) 01 = MPR1
    - 3) 10 = MPR2
    - 4) 11 = MPR3
  - b. A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[7:0].
  - c. Remaining address inputs, including A10, and BG0 are "Don't Care"
7.  $t_{WR\_MPR}$  must be satisfied to complete MPR Write.
8. Steps 5 through 7 may be repeated to write additional MPRx locations.
9. After the last MPRx write,  $t_{MPRR}$  must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3 A[2] = 0.
11. When the  $t_{MOD}$  sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

## MPR Write Waveforms



NOTE 1. Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

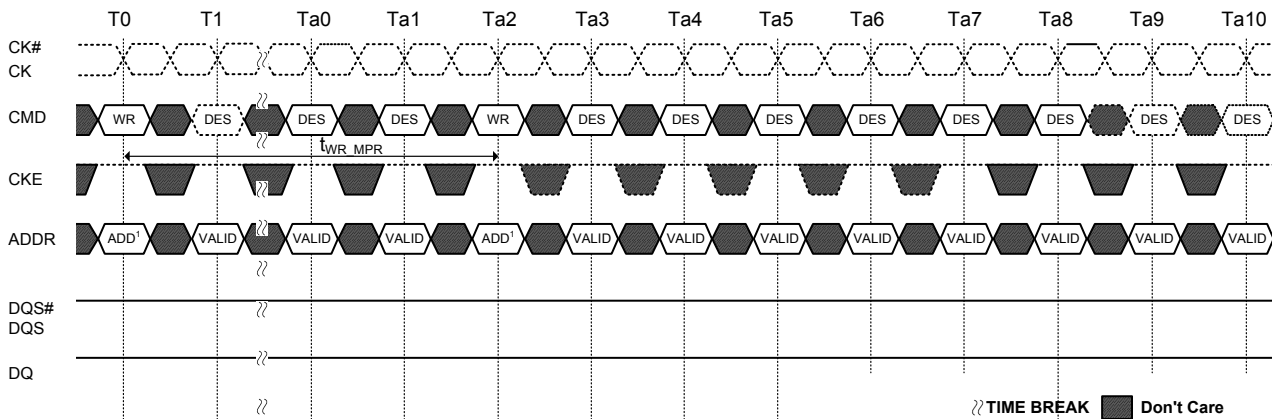
NOTE 2. Address setting - BA1 and BA0 indicate the MPR location

- A [7:0] = data for MPR

- A10 and other address pins are don't care.

NOTE 3. PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

**Figure 67. MPR Write Timing and Write to Read Timing**



NOTE 1. Address setting

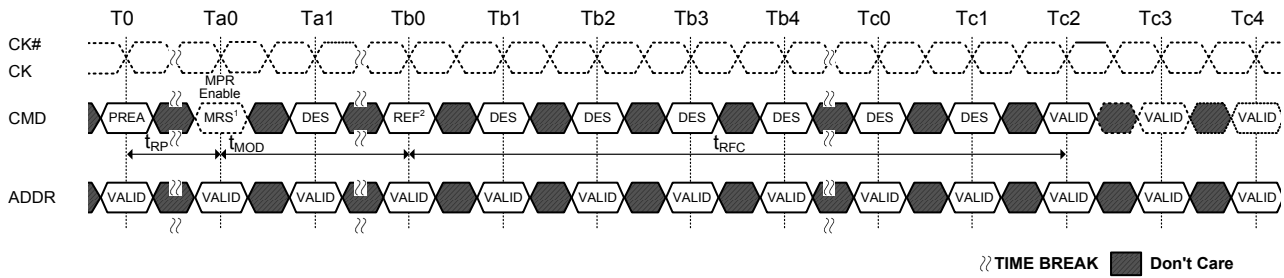
- BA1 and BA0 indicate the MPR location

- A [7:0] = data for MPR

- A10 and other address pins are don't care.

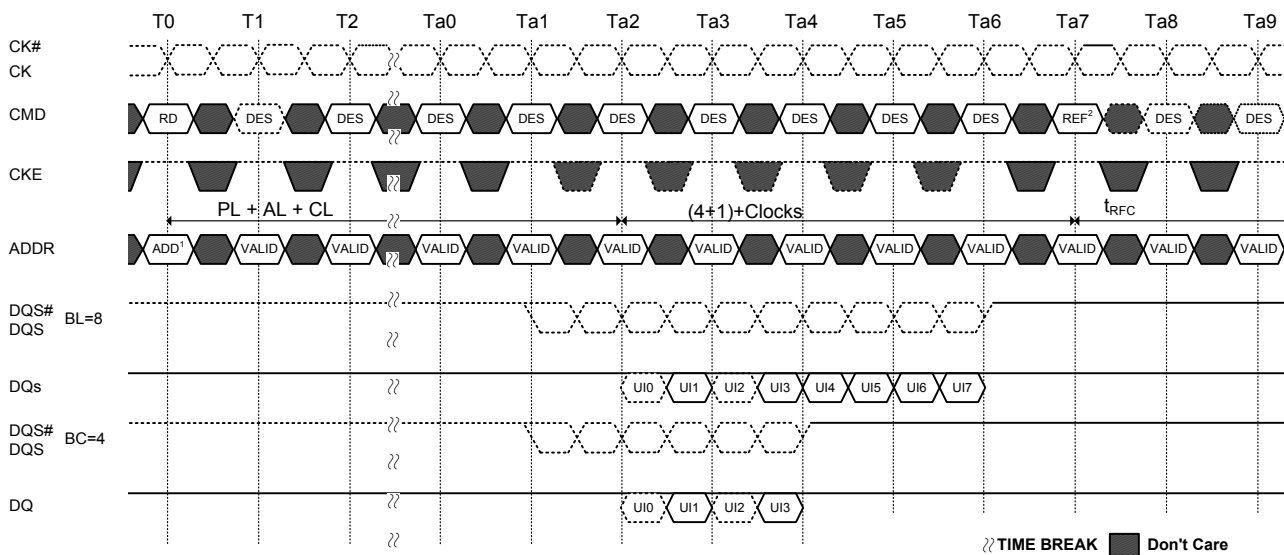
**Figure 68. MPR Back to Back Write Timing**

## MPR Refresh Waveforms



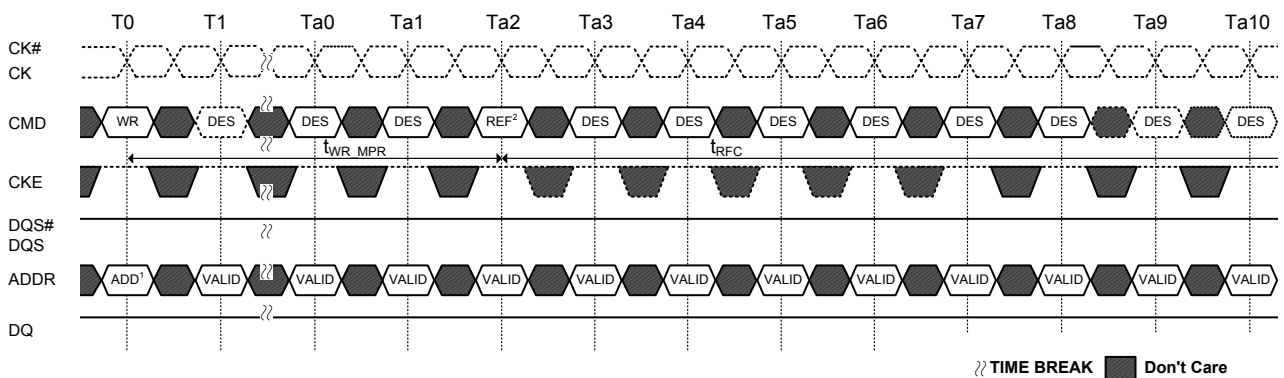
NOTE 1. Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)  
 - Redirect all subsequent read and writes to MPR locations  
 NOTE 2. 1x Refresh is only allowed when MPR mode is Enable.

**Figure 69. Refresh Command Timing**



NOTE 1. Address setting  
 - A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)  
 - A[2] = "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)  
 - BA1 and BA0 indicate the MPR location  
 - A10 and other address pins are don't care including BG0. A12 is don't care when MR0 A[1:0] = "00" or "10", and must be '1'b when MR0 A[1:0] = "01"  
 NOTE 2. 1x Refresh is only allowed when MPR mode is Enable.

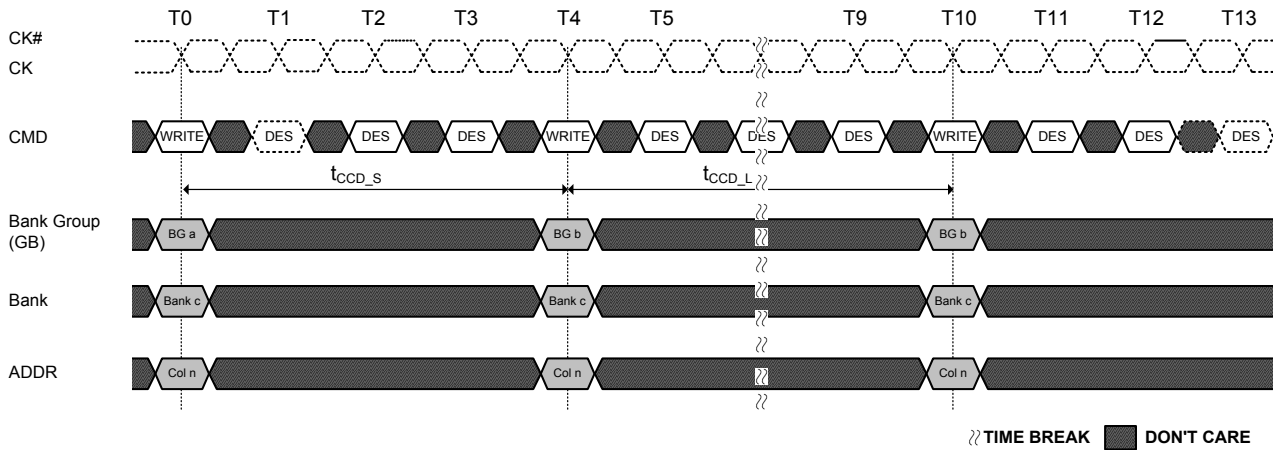
**Figure 70. Read to Refresh Command Timing**



NOTE 1. Address setting - BA1 and BA0 indicate the MPR location - A [7:0] = data for MPR  
 - A10 and other address pins are don't care.  
 NOTE 2. 1x Refresh is only allowed when MPR mode is Enable.

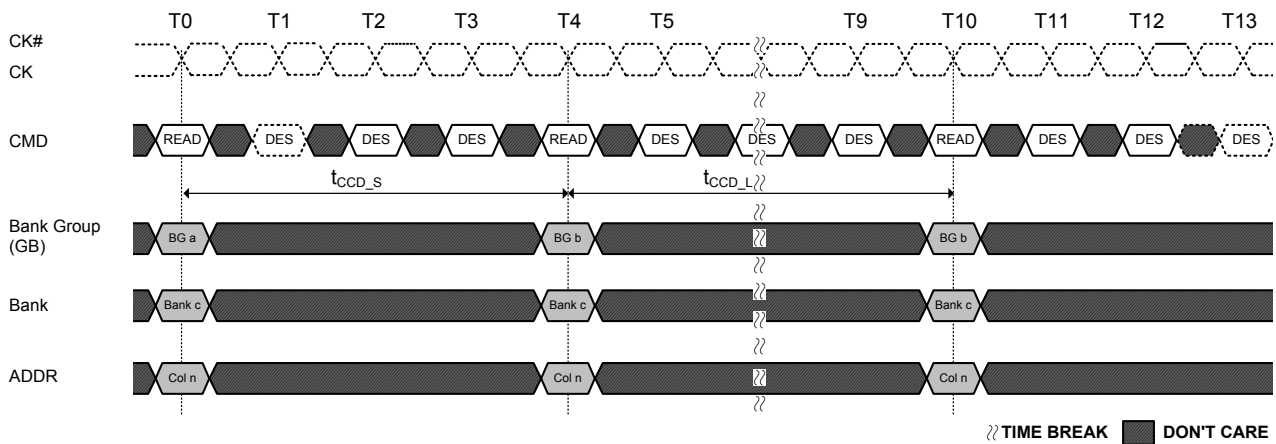
**Figure 71. Write to Refresh Command Timing**

## DDR4 Key Core Timing



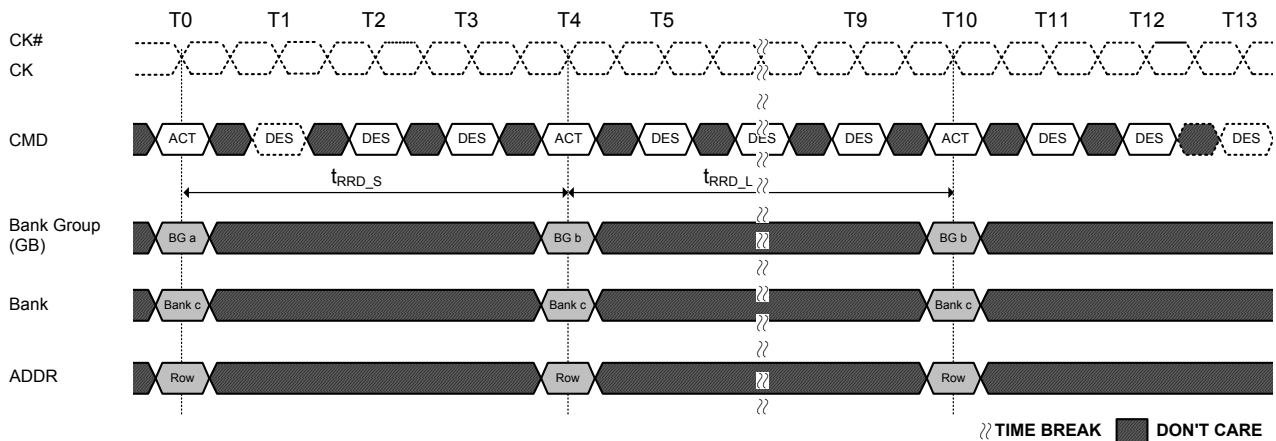
NOTE 1.  $t_{CCD\_S}$  : CAS#-to-CAS# delay (short) : Applies to consecutive CAS# to different Bank Group (i.e., T0 to T4).  
 NOTE 2.  $t_{CCD\_L}$  : CAS#-to-CAS# delay (long) : Applies to consecutive CAS# to the same Bank Group (i.e., T4 to T10).

**Figure 72.  $t_{CCD}$  Timing (WRITE to WRITE Example)**



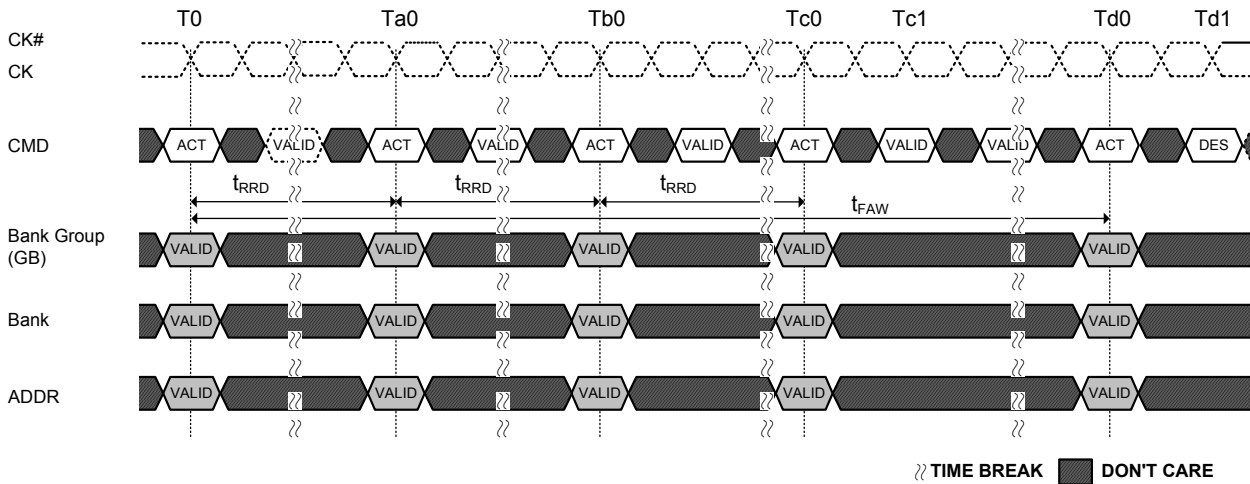
NOTE 1.  $t_{CCD\_S}$  : CAS#-to-CAS# delay (short) : Applies to consecutive CAS# to different Bank Group (i.e., T0 to T4).  
 NOTE 2.  $t_{CCD\_L}$  : CAS#-to-CAS# delay (long) : Applies to consecutive CAS# to the same Bank Group (i.e., T4 to T10).

**Figure 73.  $t_{CCD}$  Timing (READ to READ Example)**

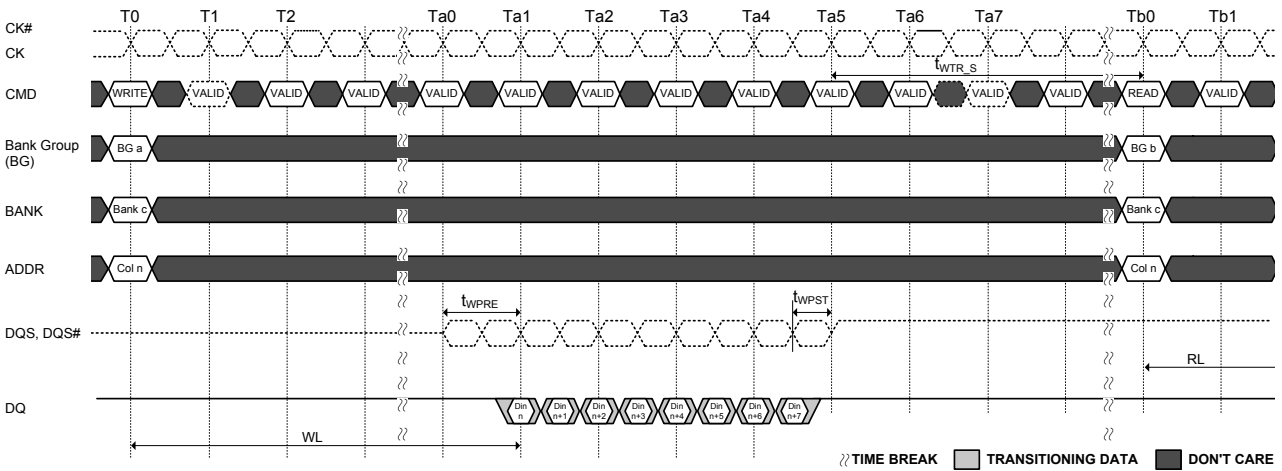


NOTE 1.  $t_{RRD\_S}$  : ACTIVATE to ACTIVATE Command period (short) : Applies to consecutive ACTIVATE Commands to different Bank Group (i.e., T0 to T4).  
 NOTE 2.  $t_{RRD\_L}$  : ACTIVATE to ACTIVATE Command period (long) : Applies to consecutive ACTIVATE Commands to the different Banks of the same Bank Group (i.e., T4 to T10).

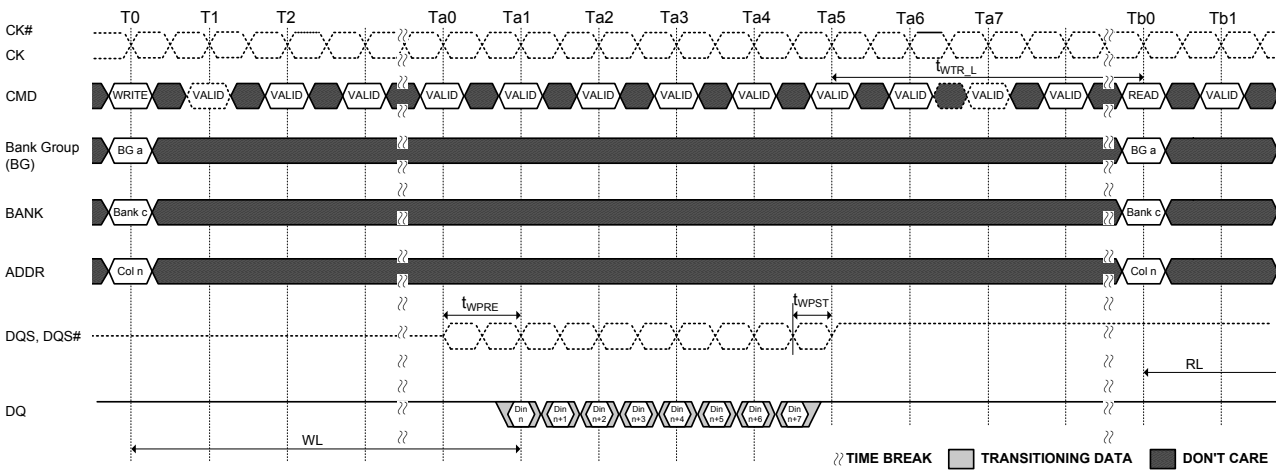
**Figure 74.  $t_{RRD}$  Timing**



**Figure 75. t<sub>FAW</sub> Timing**



**Figure 76. t<sub>WTR\_S</sub> Timing (WRITE to READ, Different Bank Group, CRC and DM Disabled)**



**Figure 77. t<sub>WTR\_L</sub> Timing (WRITE to READ, Same Bank Group, CRC and DM Disabled)**

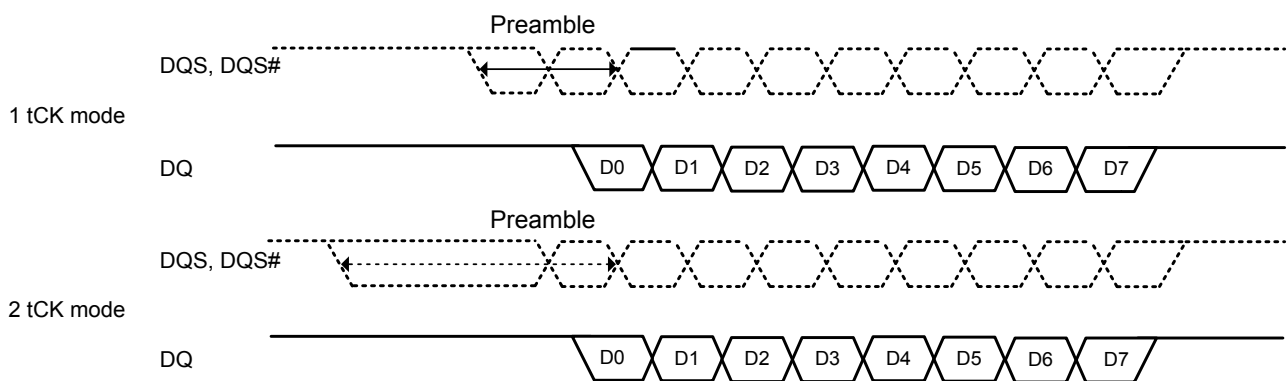
## Programmable Preamble

The DQS preamble can be programmed to one or the other of 1  $t_{CK}$  and 2  $t_{CK}$  preamble; selectable via MRS (MR4 A[12:11]). The 1  $t_{CK}$  preamble applies to all speed-Grade and The 2  $t_{CK}$  preamble is valid for DDR4-2400 /2666 speed-Grade.

## Write Preamble

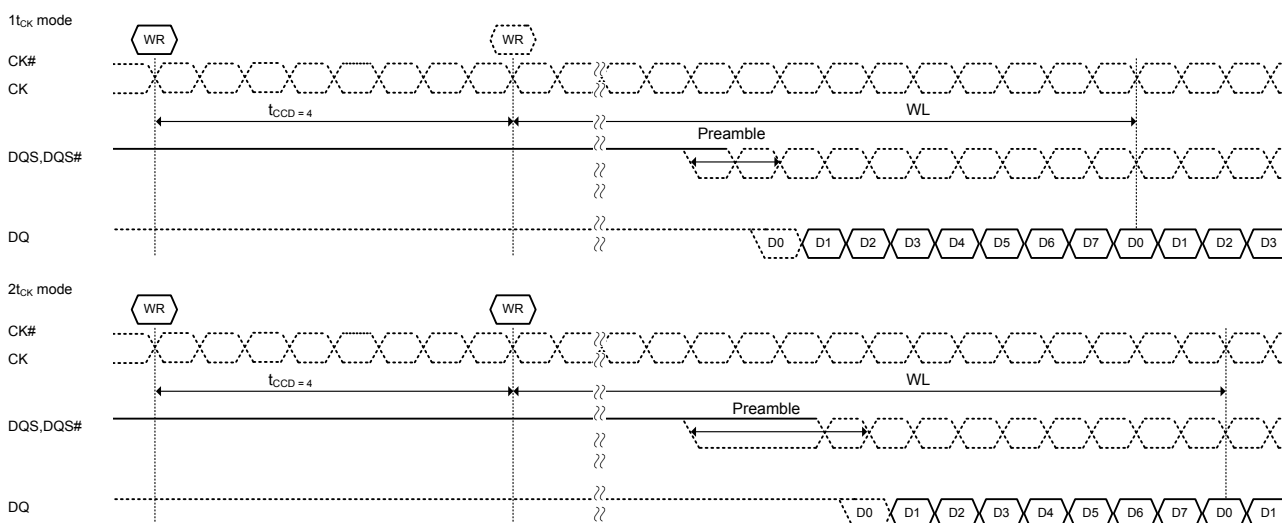
DDR4 supports a programmable write preamble. The 1  $t_{CK}$  or 2  $t_{CK}$  Write Preamble is selected via MR4 A[12]. Write preamble modes of 1  $t_{CK}$  and 2  $t_{CK}$  are shown below.

When operating in 2  $t_{CK}$  Write preamble mode in MR2 CWL (CAS Write Latency), CWL of 1<sup>st</sup> Set needs to be incremented by 2 nCK and CWL of 2<sup>nd</sup> Set does not need increment of it.  $t_{WTR}$  must be increased by one clock cycle from the  $t_{WTR}$  required in the applicable speed bin table. WR must be programmed to a value one or two clock cycle(s), depending on available settings, greater than the WR setting required per the applicable speed bin table.



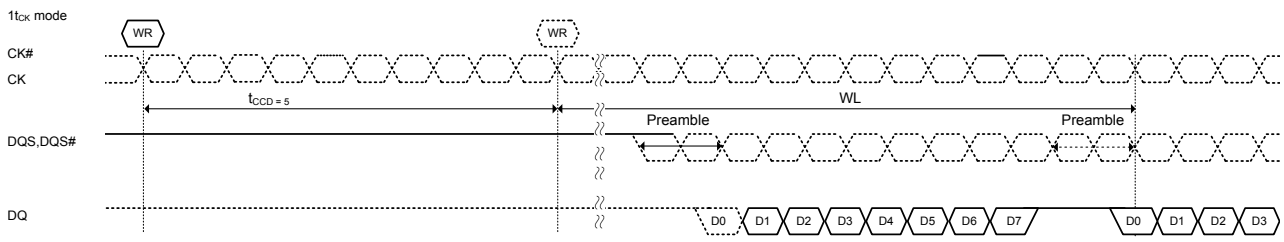
**Figure 78. 1 $t_{CK}$  vs. 2 $t_{CK}$  WRITE Preamble Mode**

The timing diagrams contained in  $t_{CCD}=4$  (AL=PL=0),  $t_{CCD}=5$  and  $t_{CCD}=6$  (AL=PL=0) illustrate 1 and 2  $t_{CK}$  preamble scenarios for consecutive write commands with  $t_{CCD}$  timing of 4, 5 and 6 nCK, respectively. Setting  $t_{CCD}$  to 5nCK is not allowed in 2  $t_{CK}$  preamble mode.



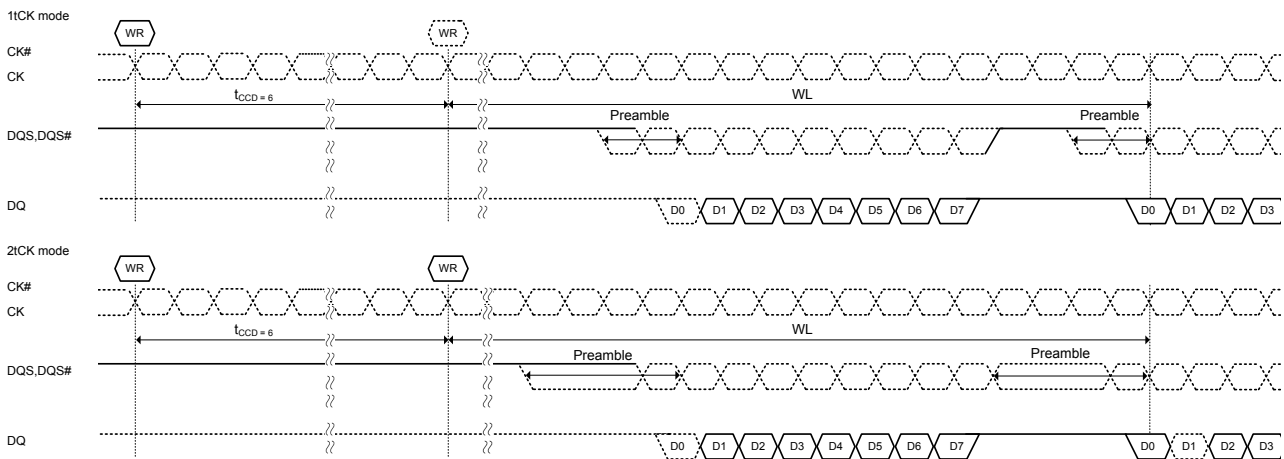
**Figure 79.  $t_{CCD}=4$  (AL=PL=0)**





2t<sub>CK</sub> mode: t<sub>CCD</sub>=5 is not allowed in 2t<sub>CK</sub> mode

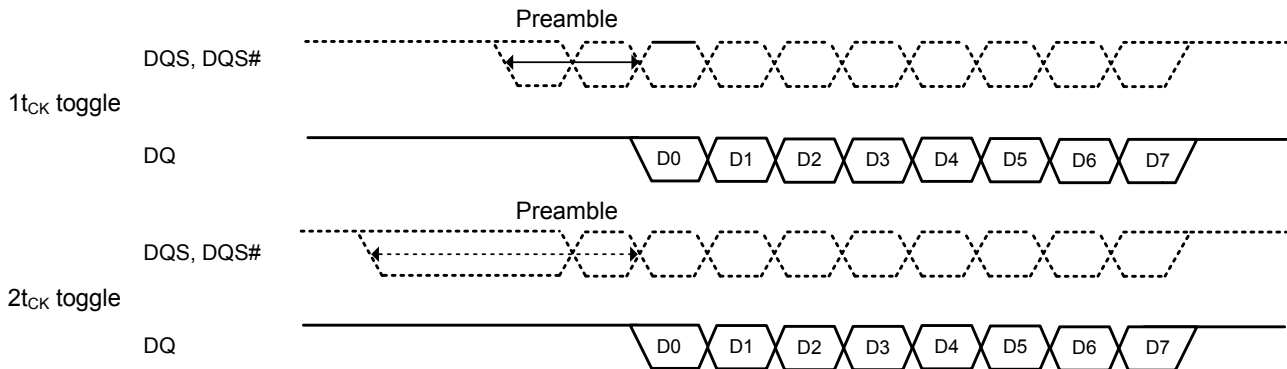
**Figure 80. t<sub>CCD</sub>=5 (AL=PL=0)**



**Figure 81. t<sub>CCD</sub>=6 (AL=PL=0)**

## Read Preamble

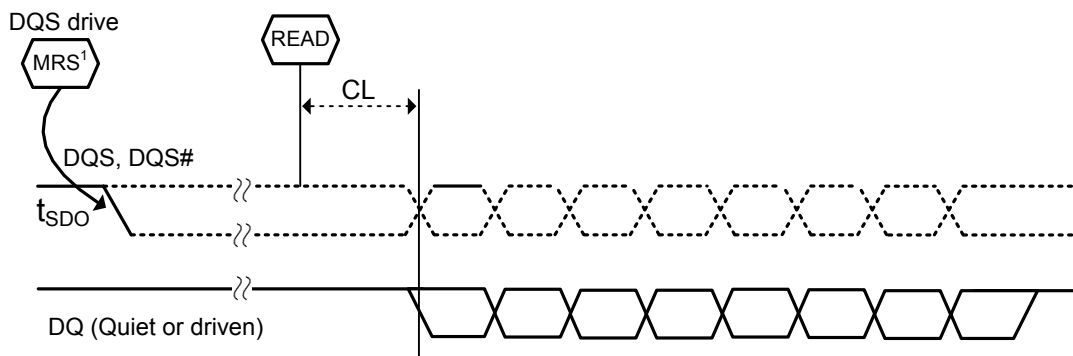
DDR4 supports a programmable read preamble. The  $1 t_{CK}$  and  $2 t_{CK}$  Read preamble is selected via MR4 A[11]. Read preamble modes of  $1 t_{CK}$  and  $2 t_{CK}$  are shown as follows:



**Figure 82.  $1t_{CK}$  vs.  $2t_{CK}$  READ Preamble Mode**

## Read Preamble Training

DDR4 supports Read preamble training via MPR reads; that is, Read preamble training is allowed only when the DRAM is in the MPR access mode. The Read preamble training mode can be used by the DRAM controller to train or "read level" its DQS receivers. Read preamble training is entered via an MRS command (MR4 A[10] = 1 is enabled and MR4 A[10] = 0 is disabled). After the MRS command is issued to enable Read preamble training, the DRAM DQS signals are driven to a valid level by the time  $t_{SDO}$  is satisfied. During this time, the data bus DQ signals are held quiet, i.e. driven high. The DQS signal remains driven low and the DQS# signal remains driven high until an MPR Page0 Read command is issued (MPR0 through MPR3 determine which pattern is used), and when CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting. To exit Read preamble training mode, an MRS command must be issued, MR4 A[10] = 0.



NOTE 1. Read Preamble Training mode is enabled by MR4 A10 = [1]

**Figure 83. READ Preamble Training**

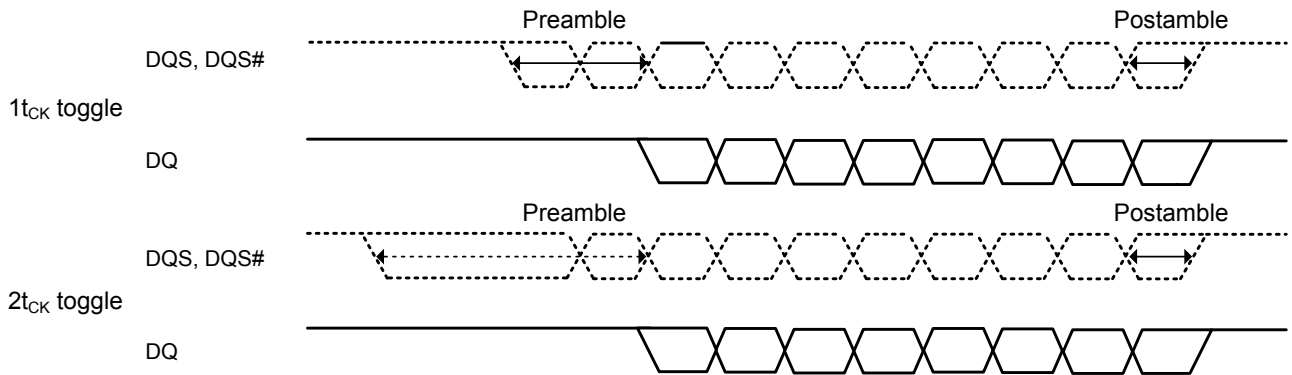
**Table 36. AC Timing Table**

Symbol	Parameter	Min.	Max.	Unit
$t_{SDO}$	Delay from MRS Command to Data Strobe Drive Out	-	$t_{MOD} + 9ns$	

## Postamble

### Read Postamble

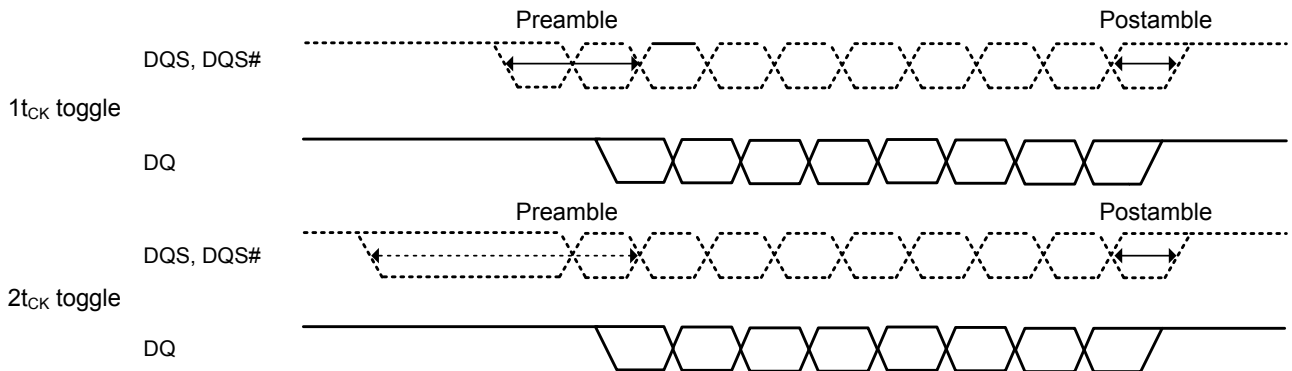
Whether the  $1 t_{CK}$  or  $2 t_{CK}$  Read Preamble Mode is selected, the Read Postamble remains the same at  $1/2 t_{CK}$ .  
 DDR4 will support a fixed read postamble.  
 Read postamble of nominal  $0.5 t_{CK}$  for preamble modes  $1, 2 t_{CK}$  are shown below:



**Figure 84. READ Postamble**

### Write Postamble

Whether the  $1 t_{CK}$  or  $2 t_{CK}$  Write preamble mode is selected, the Write postamble remains the same at  $1/2 t_{CK}$ .  
 DDR4 will support a fixed Write postamble.  
 Write postamble nominal is  $0.5 t_{CK}$  for preamble modes  $1, 2 t_{CK}$  are shown below:



**Figure 85. WRITE Postamble**

## Activate Command

The Activate command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0 in x16 select the bank group; BA0-BA1 inputs selects the bank within the bank group, and the address provided on inputs A0-A14 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

## Precharge Command

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time ( $t_{RP}$ ) after the Precharge command is issued, except in the case of concurrent auto precharge, where a Read or Write command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A Precharge command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last Precharge command issued to the bank.

If A10 is high when Read or Write command is issued, then auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed ( $t_{RAS}$  satisfied) so that the auto precharge command may be issued with any read. Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array. The bank will be available for a subsequent row activation a specified time ( $t_{RP}$ ) after hidden Precharge command (AutoPrecharge) is issued to that bank.

## Read Operation

### Read Timing Definitions

Read timings are shown below and are applicable in normal operation mode, i.e. when the DLL is enabled and locked.

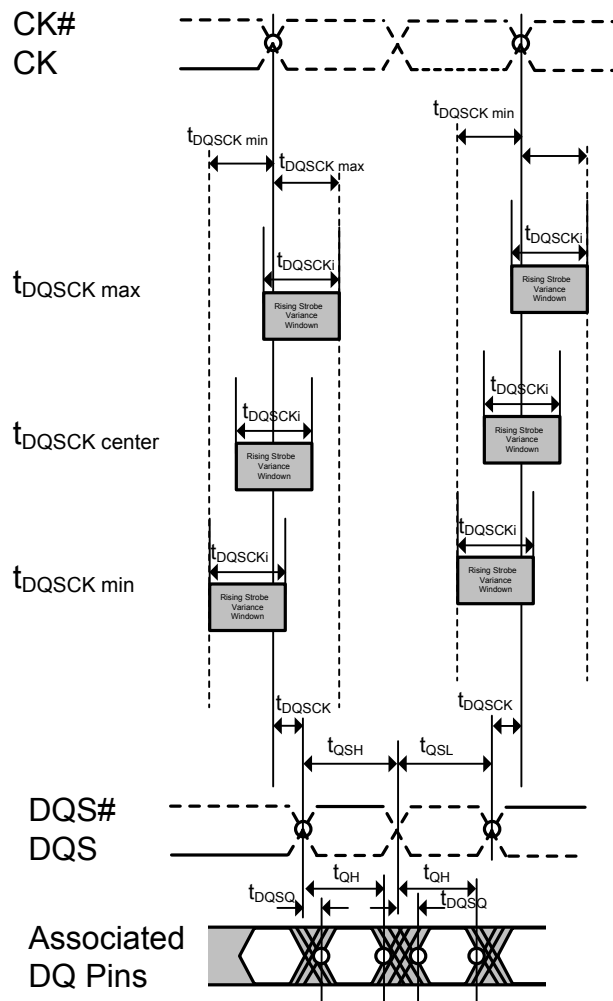
Rising data strobe edge parameters:

- $t_{DQ\text{SCK min}}$  describes the allowed range for a rising data strobe edge relative to CK, CK#.
- $t_{DQ\text{SCK}}$  is the actual position of a rising strobe edge relative to CK, CK#.
- $t_{Q\text{SH}}$  describes the DQS, DQS# differential output high time.
- $t_{DQ\text{SQ}}$  describes the latest valid transition of the associated DQ pins.
- $t_{Q\text{H}}$  describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- $t_{Q\text{SL}}$  describes the DQS, DQS# differential output low time.
- $t_{DQ\text{SQ}}$  describes the latest valid transition of the associated DQ pins.
- $t_{Q\text{H}}$  describes the earliest invalid transition of the associated DQ pins.

$t_{DQ\text{SQ}}$ : both rising/falling edges of DQS, no  $t_{AC}$  defined.



**Figure 86. READ Timing Definition**

## Read Timing; Clock to Data Strobe relationship

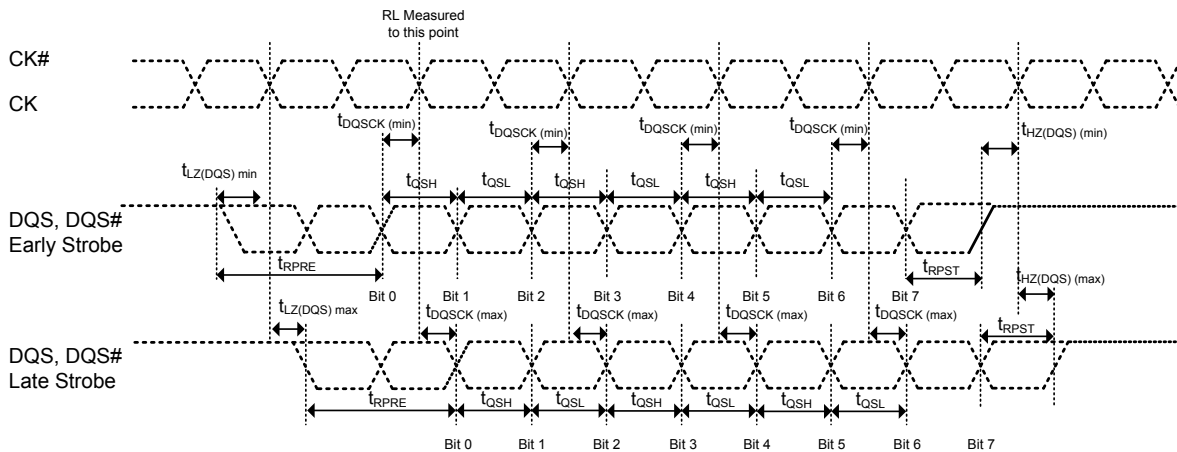
The clock to data strobe relationship is shown below and is applicable in normal operation mode, i.e. when the DLL is enabled and locked.

Rising data strobe edge parameters:

- $t_{DQSCk}$  min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- $t_{DQSCk}$  is the actual position of a rising strobe edge relative to CK, CK#.
- $t_{QSH}$  describes the data strobe high pulse width.

Falling data strobe edge parameters:

- $t_{QSL}$  describes the data strobe low pulse width.
- $t_{LZ(DQS)}$ ,  $t_{HZ(DQS)}$  for preamble/postamble.



NOTE 1. Within a burst, rising strobe edge can be varied within  $t_{DQSCk}$  while at the same voltage and temperature. However incorporate the device, voltage and temperature variation, rising strobe edge variance window,  $t_{DQSCk}$  can shift between  $t_{DQSCk(min)}$  and  $t_{DQSCk(max)}$ . A timing of this window's right inside edge (latest) from rising CK, CK# is limited by a device's actual  $t_{DQSCk(max)}$ . A timing of this window's left inside edge (earliest) from rising CK, CK# is limited by  $t_{DQSCk(min)}$ .

NOTE 2. Notwithstanding note 1, a rising strobe edge with  $t_{DQSCk(max)}$  at T(n) can not be immediately followed by a rising strobe edge with  $t_{DQSCk(min)}$  at T(n+1). This is because other timing relationships ( $t_{QSH}$ ,  $t_{QSL}$ ) exist: if  $t_{DQSCk(n+1)} < 0$ :

$$t_{DQSCk(n)} < 1.0 t_{CK} - (t_{QSHmin} + t_{QSLmin}) - |t_{DQSCk(n+1)}|$$

NOTE 3. The DQS, DQS# differential output high time is defined by  $t_{QSH}$  and the DQS, DQS# differential output low time is defined by  $t_{QSL}$ .

NOTE 4. Likewise,  $t_{LZ(DQS)min}$  and  $t_{HZ(DQS)min}$  are not tied to  $t_{DQSCkmin}$  (early strobe case) and  $t_{LZ(DQS)max}$  and  $t_{HZ(DQS)max}$  are not tied to  $t_{DQSCkmax}$  (late strobe case).

NOTE 5. The minimum pulse width of read preamble is defined by  $t_{RPST(min)}$ .

NOTE 6. The maximum read postamble is bound by  $t_{DQSCk(min)}$  plus  $t_{QSH(min)}$  on the left side and  $t_{HZ(DQS)max}$  on the right side.

NOTE 7. The minimum pulse width of read postamble is defined by  $t_{RPST(min)}$ .

NOTE 8. The maximum read preamble is bound by  $t_{LZ(DQS)min}$  on the left side and  $t_{DQSCk(max)}$  on the right side.

**Figure 87. Clock to Data Strobe Relationship**

## Read Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown below and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- $t_{DQSQ}$  describes the latest valid transition of the associated DQ pins.
- $t_{QH}$  describes the earliest invalid transition of the associated DQ pins.

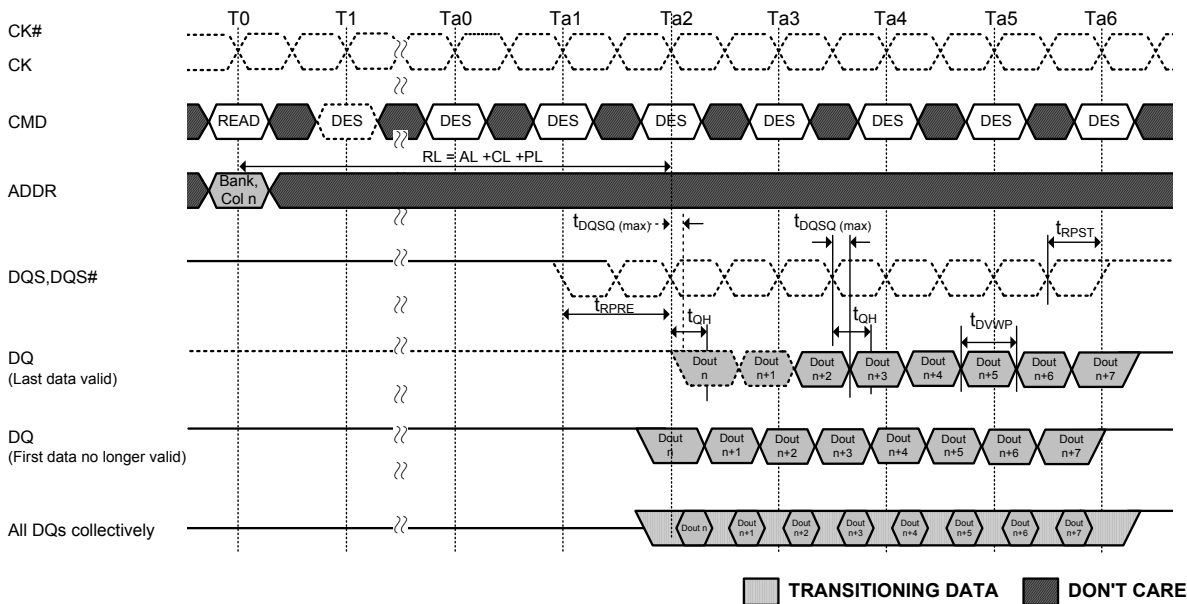
Falling data strobe edge parameters:

- $t_{DQSQ}$  describes the latest valid transition of the associated DQ pins.
- $t_{QH}$  describes the earliest invalid transition of the associated DQ pins.

$t_{DQSQ}$ : both rising/falling edges of DQS, no tAC defined.

Data Valid Window:

- $t_{DVWD}$  is the Data Valid Window per device per UI and is derived from  $(t_{QH} - t_{DQSQ})$  of each UI on a given DRAM. This parameter will be characterized and guaranteed by design.
- $t_{DVWP}$  is Data Valid Window per pin per UI and is derived from  $(t_{QH} - t_{DQSQ})$  of each UI on a pin of a given DRAM. This parameter will be characterized and guaranteed by design.



NOTE 1. BL = 8, AL = 0, CL = 11, Preamble =  $1_{iCK}$

NOTE 2. Dout n = data-out from column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5. Output timings are referenced to VDDQ, and DLL on for locking.

NOTE 6.  $t_{DQSQ}$  defines the skew between DQS,DQS# to Data and does not define DQS, DQS# to Clock.

NOTE 7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

Figure 88. Data Strobe to Data Relationship

### t<sub>LZ(DQS)</sub>, t<sub>LZ(DQ)</sub>, t<sub>HZ(DQS)</sub>, t<sub>HZ(DQ)</sub> Calculation

t<sub>HZ</sub> and t<sub>LZ</sub> transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving t<sub>HZ(DQS)</sub> and t<sub>HZ(DQ)</sub>, or begins driving t<sub>LZ(DQS)</sub>, t<sub>LZ(DQ)</sub>.

t<sub>LZ</sub> shows a method to calculate the point when the device is no longer driving t<sub>HZ(DQS)</sub> and t<sub>HZ(DQ)</sub>, or begins driving t<sub>LZ(DQS)</sub>, t<sub>LZ(DQ)</sub>, by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters t<sub>LZ(DQS)</sub>, t<sub>LZ(DQ)</sub>, t<sub>HZ(DQS)</sub>, and t<sub>HZ(DQ)</sub> are defined as single ended.

**Table 37. Reference Voltage for t<sub>LZ(DQ)</sub>, t<sub>HZ(DQ)</sub> Timing Measurements**

Symbol	Parameter	Vsw1	Vsw2	Unit
t <sub>LZ(DQ)</sub>	DQ low-impedance time from CK, CK#	$(0.70 - 0.04) \times V_{DDQ}$	$(0.70 + 0.04) \times V_{DDQ}$	V
t <sub>HZ(DQ)</sub>	DQ high impedance time from CK, CK#	$(0.70 - 0.04) \times V_{DDQ}$	$(0.70 + 0.04) \times V_{DDQ}$	V

**Table 38. Reference Voltage for t<sub>LZ(DQS#)</sub>, t<sub>HZ(DQS)</sub> Timing Measurements**

Symbol	Parameter	Vsw1	Vsw2	Unit
t <sub>LZ(DQS#)</sub>	DQS# low-impedance time from CK, CK#	$(0.70 - 0.04) \times V_{DDQ}$	$(0.70 + 0.04) \times V_{DDQ}$	V
t <sub>HZ(DQS)</sub>	DQS high impedance time from CK, CK#	$(0.70 - 0.04) \times V_{DDQ}$	$(0.70 + 0.04) \times V_{DDQ}$	V

**Table 39. Reference Voltage for t<sub>RPRE</sub> Timing Measurements**

Symbol	Parameter	Vsw1	Vsw2	Unit
t <sub>RPRE</sub>	DQS, DQS# differential Read Preamble	$(0.30 - 0.04) \times V_{DDQ}$	$(0.30 + 0.04) \times V_{DDQ}$	V

**Table 40. Reference Voltage for t<sub>RPST</sub> Timing Measurements**

Symbol	Parameter	Vsw1	Vsw2	Unit
t <sub>RPST</sub>	DQS, DQS# differential Read Postamble	$(-0.30 - 0.04) \times V_{DDQ}$	$(-0.30 + 0.04) \times V_{DDQ}$	V



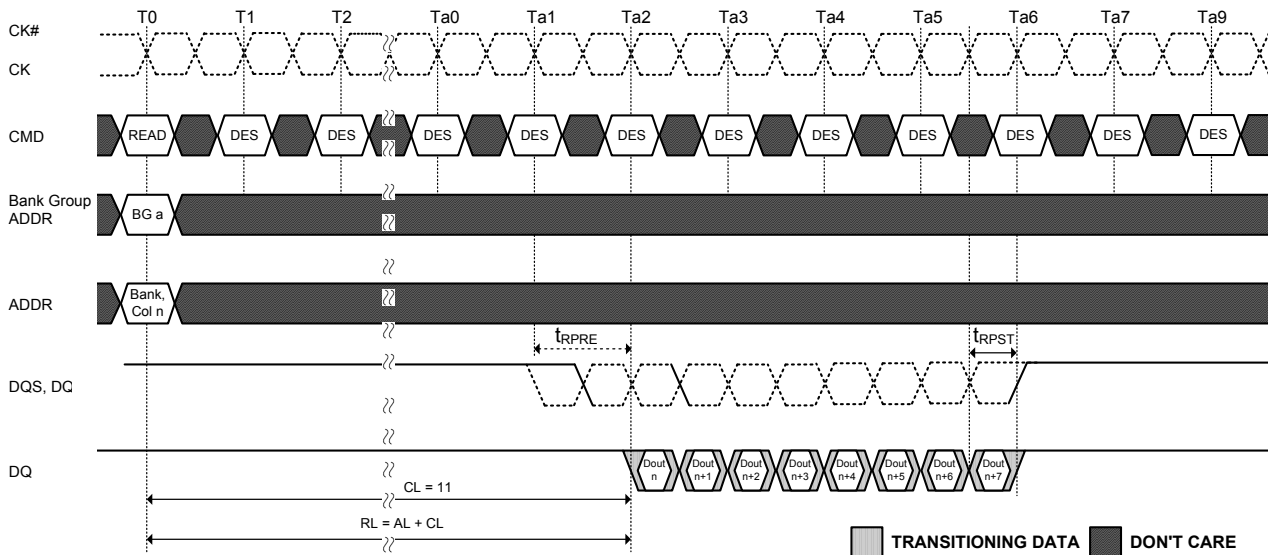
## Read Burst Operation

DDR4 Read command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF during the Read or Write (auto-precharge can be enabled or disabled).

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

Read commands can issue precharge automatically with a read with auto-precharge command (RDA); and is enabled by A10 high.

- Read command with A10 = 0 (RD) performs standard Read, bank remains active after read burst.
- Read command with A10 = 1 (RDA) performs Read with auto-precharge, back goes in to precharge after read burst.



NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 1t<sub>CK</sub>

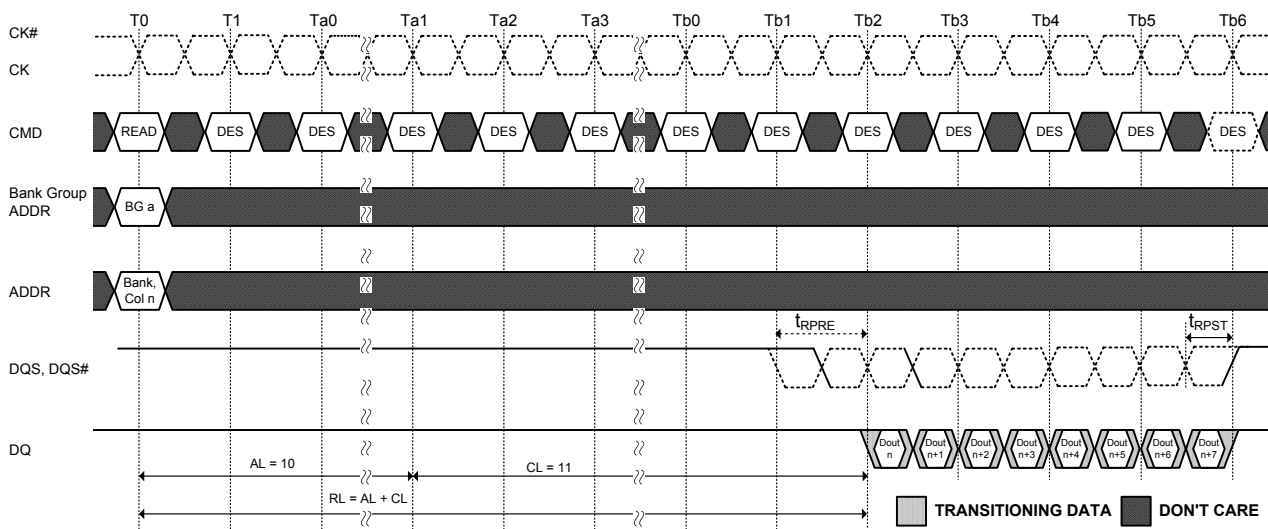
NOTE 2. Dout n = data-out from column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

**Figure 89. READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)**



NOTE 1. BL = 8, RL = 21, AL = (CL-1), CL = 11, Preamble = 1t<sub>CK</sub>

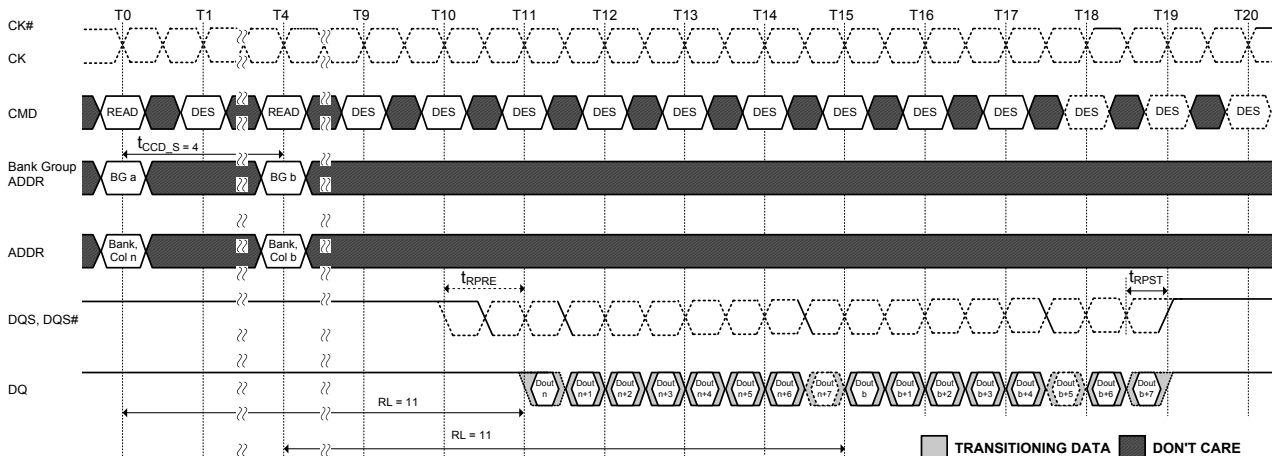
NOTE 2. Dout n = data-out from column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

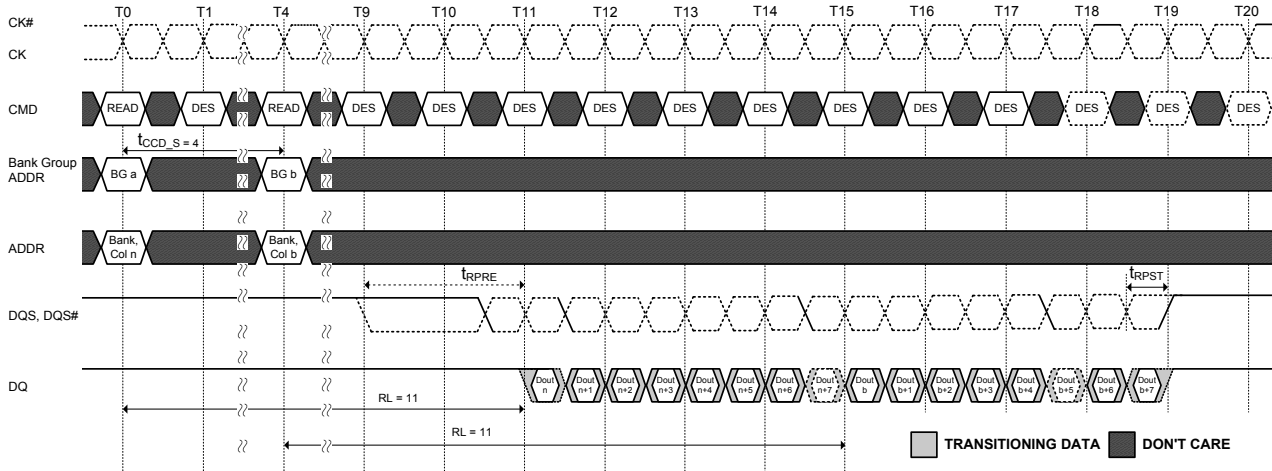
NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

**Figure 90. READ Burst Operation RL = 21 (AL = 10, CL = 11, BL8)**



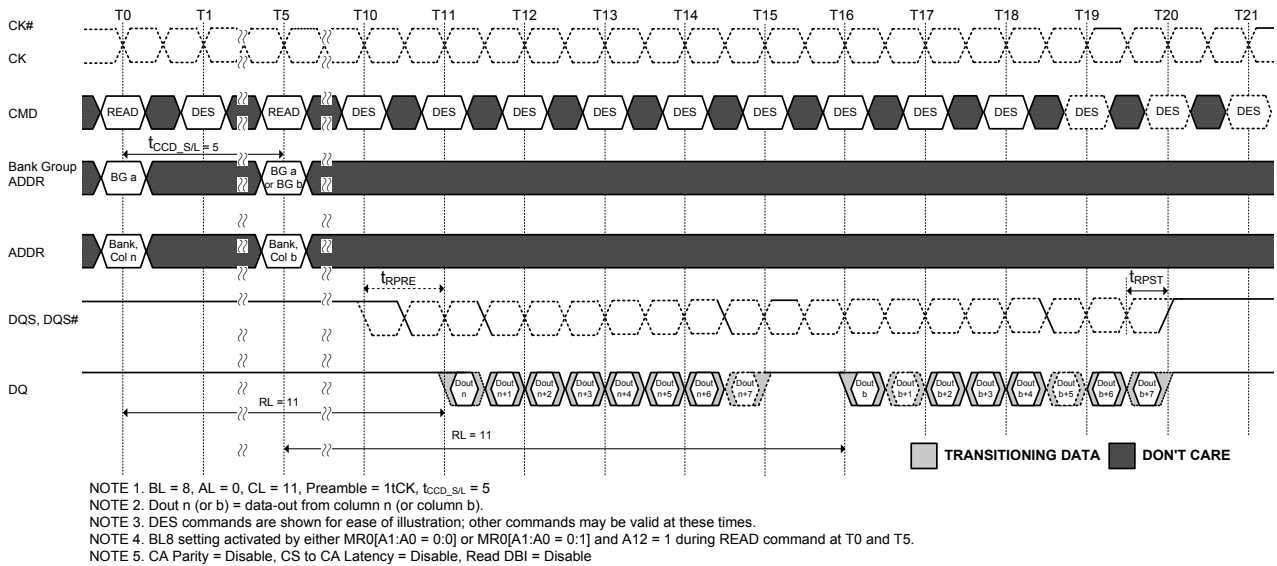
- NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK  
 NOTE 2. Dout n (or b) = data-out from column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

**Figure 91. Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group**

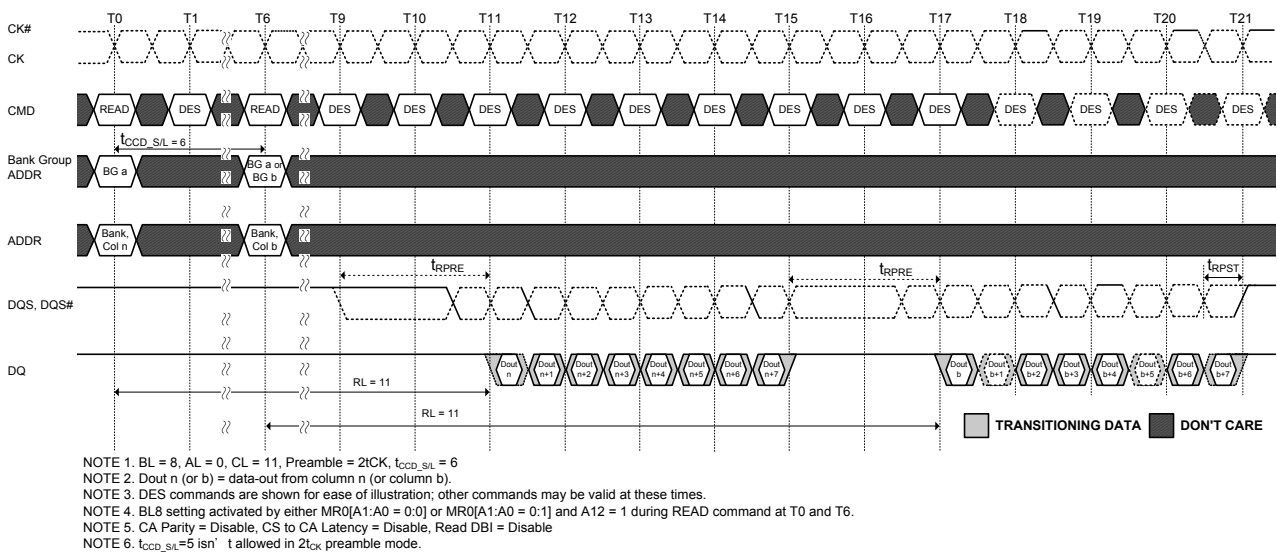


- NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK  
 NOTE 2. Dout n (or b) = data-out from column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

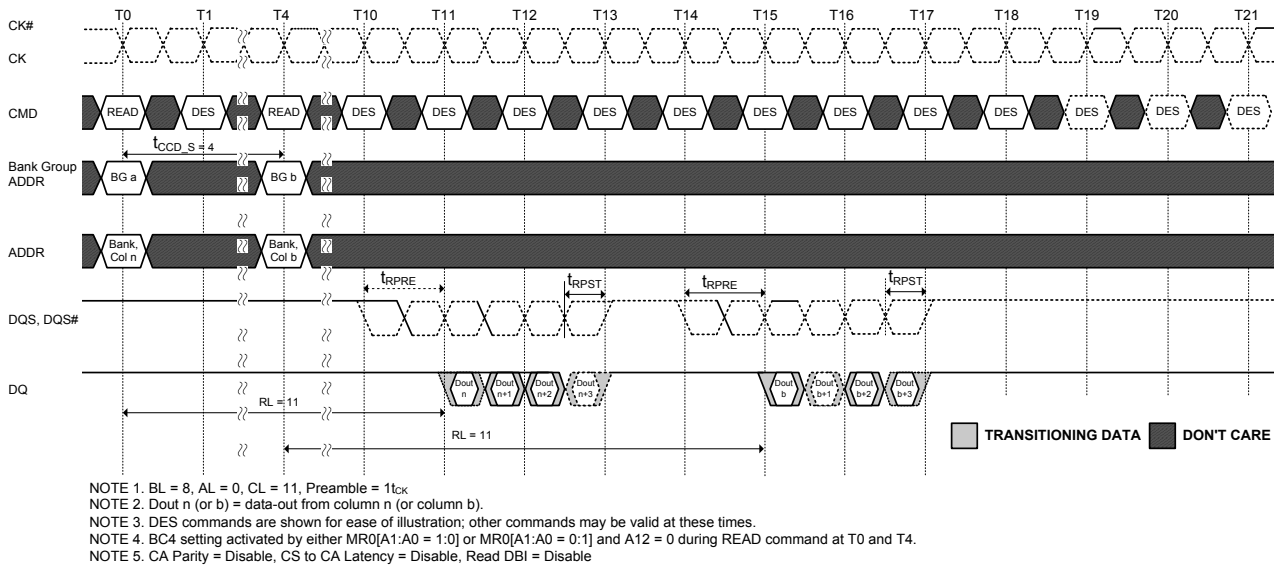
**Figure 92. Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group**



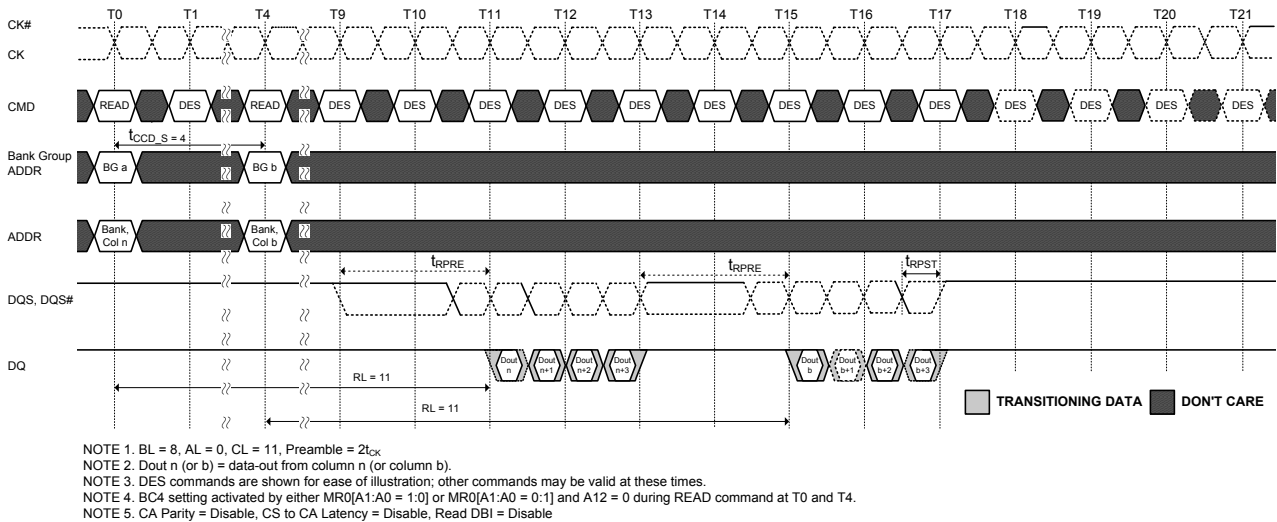
**Figure 93. Nonconsecutive READ (BL8) with 1t<sub>CK</sub> Preamble in Same or Different Bank Group**



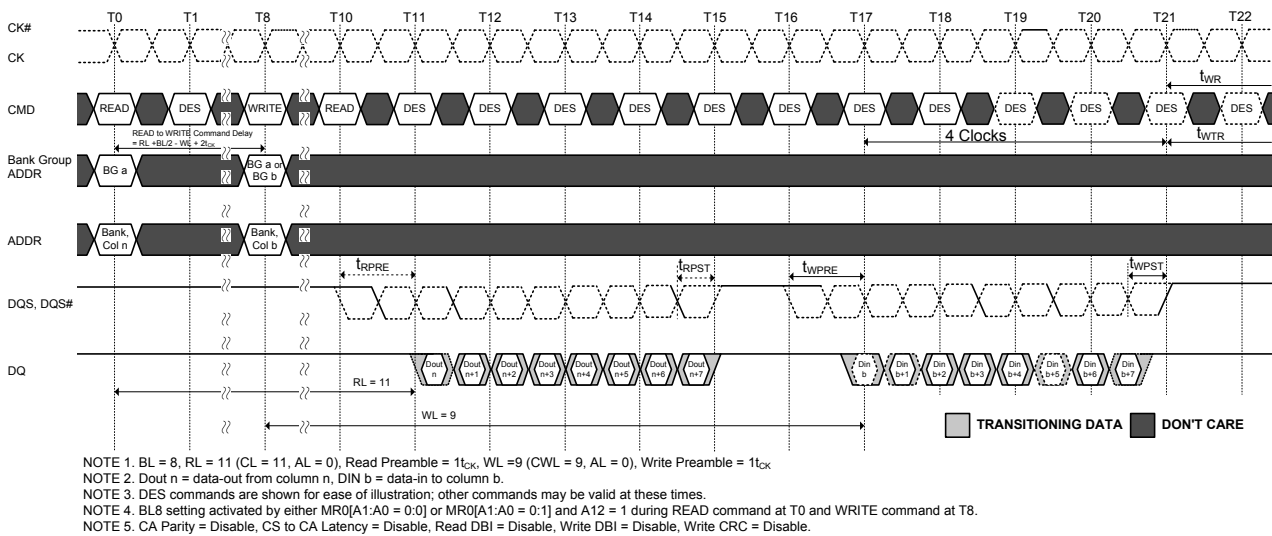
**Figure 94. Nonconsecutive READ (BL8) with 2t<sub>CK</sub> Preamble in Same or Different Bank Group**



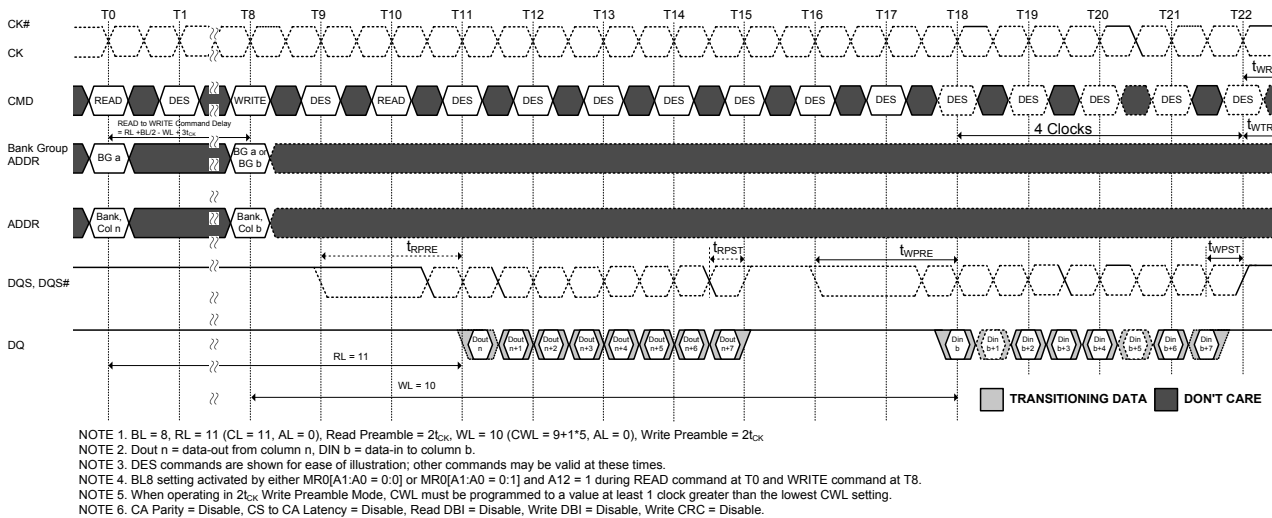
**Figure 95. READ (BC4) to READ (BC4) with 1t<sub>CK</sub> Preamble in Different Bank Group**



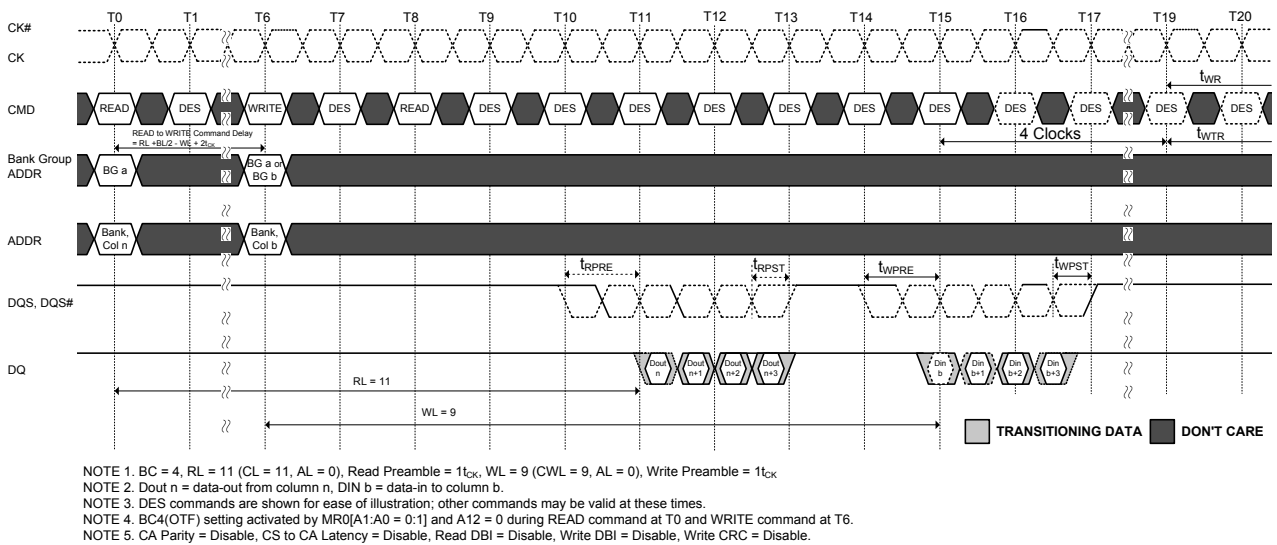
**Figure 96. READ (BC4) to READ (BC4) with 2t<sub>CK</sub> Preamble in Different Bank Group**



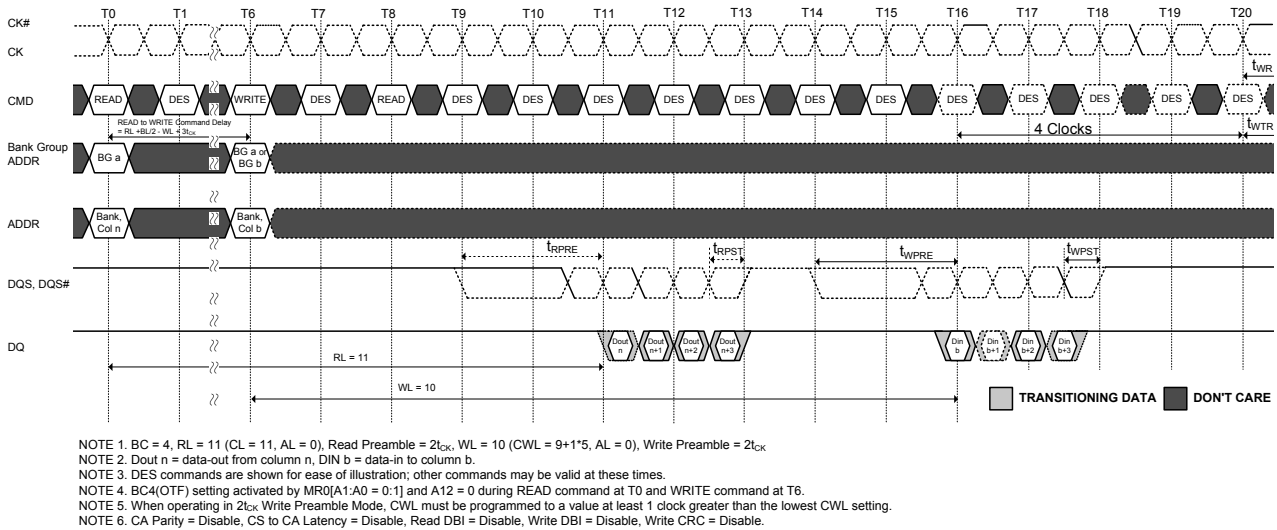
**Figure 97. READ (BL8) to WRITE (BL8) with  $1t_{CK}$  Preamble in Same or Different Bank Group**



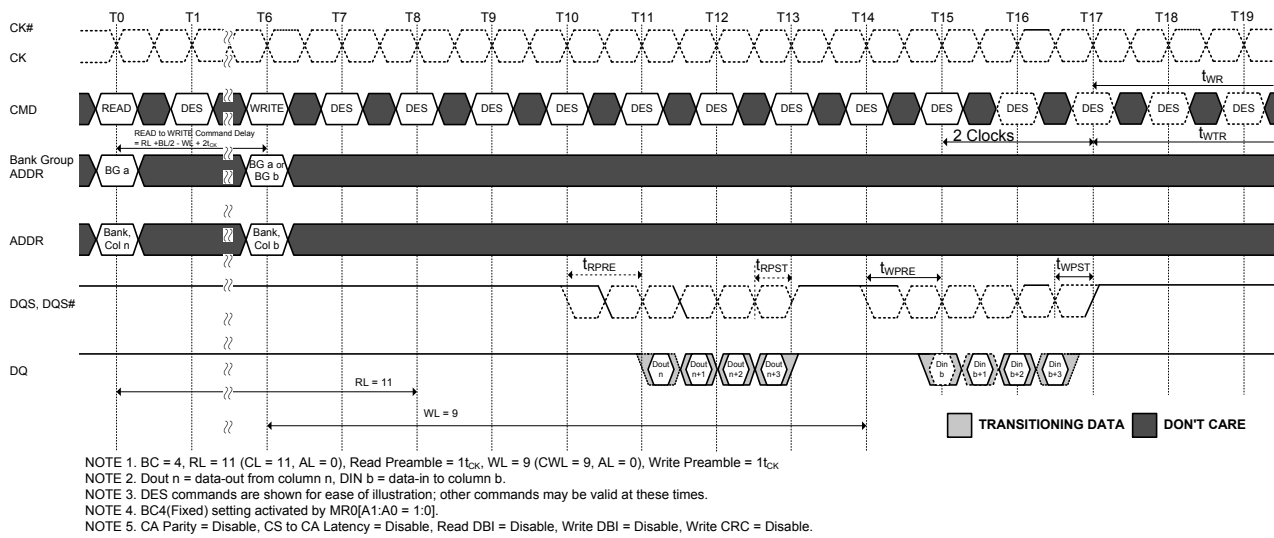
**Figure 98. READ (BL8) to WRITE (BL8) with  $2t_{CK}$  Preamble in Same or Different Bank Group**



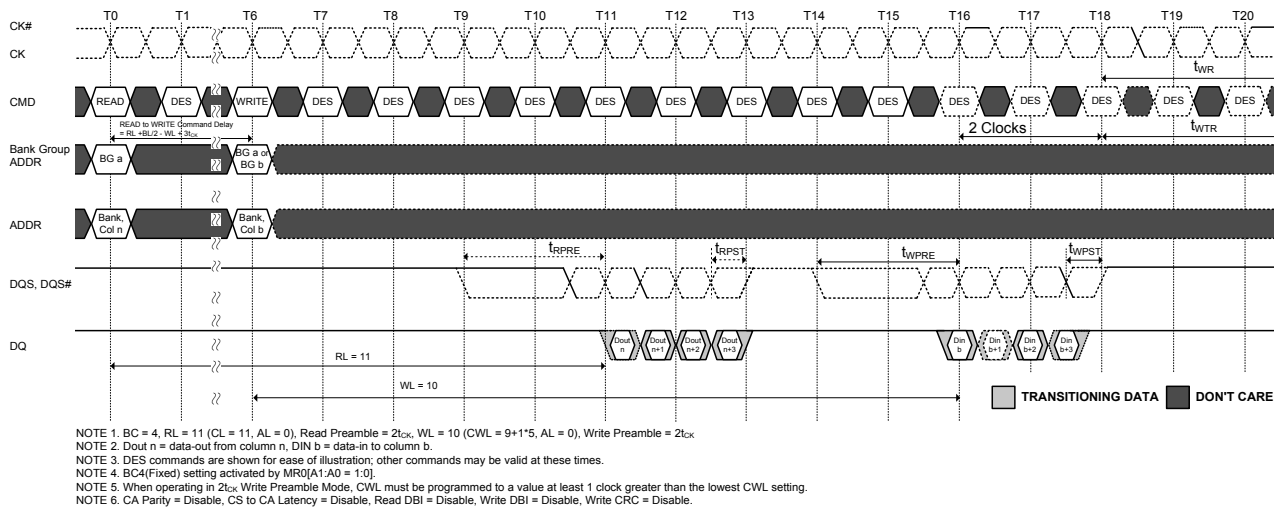
**Figure 99. READ (BC4) OTF to WRITE (BC4) OTF with  $1t_{CK}$  Preamble in Same or Different Bank Group**



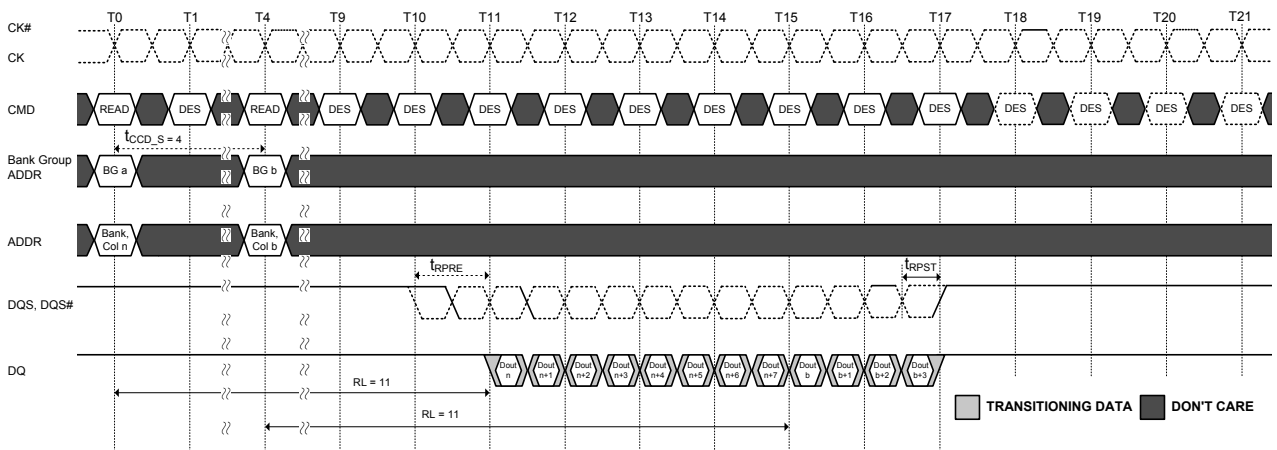
**Figure 100. READ (BC4) OTF to WRITE (BC4) OTF with  $2t_{CK}$  Preamble in Same or Different Bank Group**



**Figure 101. READ (BC4) Fixed to WRITE (BC4) Fixed with  $1t_{CK}$  Preamble in Same or Different Bank Group**

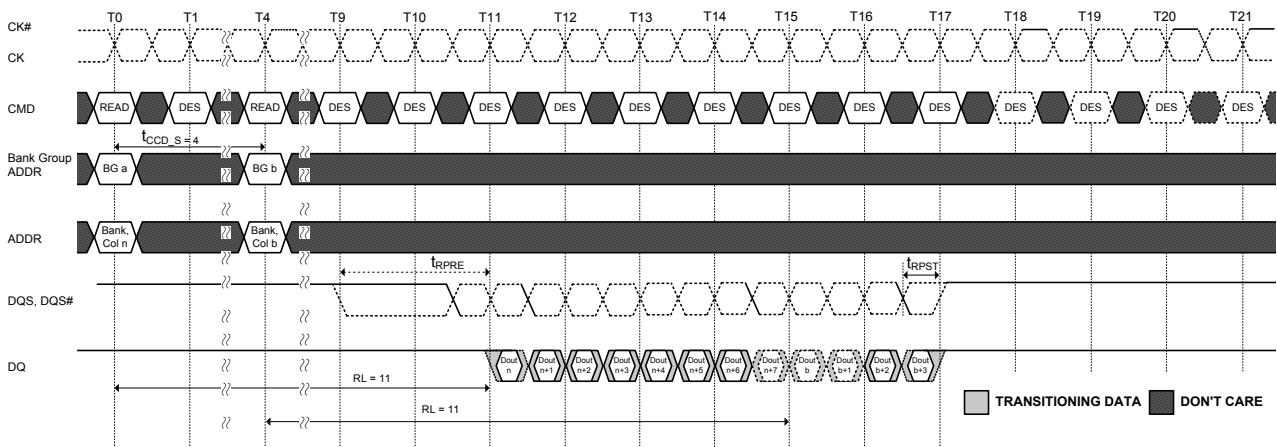


**Figure 102. READ (BC4) Fixed to WRITE (BC4) Fixed with  $2t_{CK}$  Preamble in Same or Different Bank Group**



NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 1t<sub>CK</sub>  
 NOTE 2. Dout n (or b) = data-out from column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0  
 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

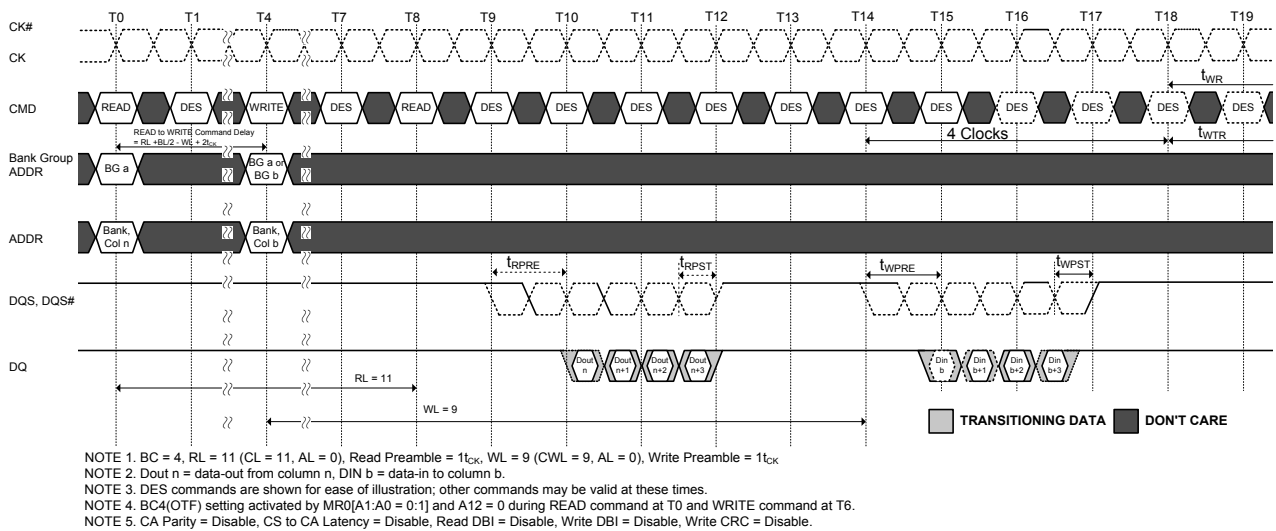
**Figure 103. READ (BL8) to READ (BC4) OTF with 1t<sub>CK</sub> Preamble in Different Bank Group**



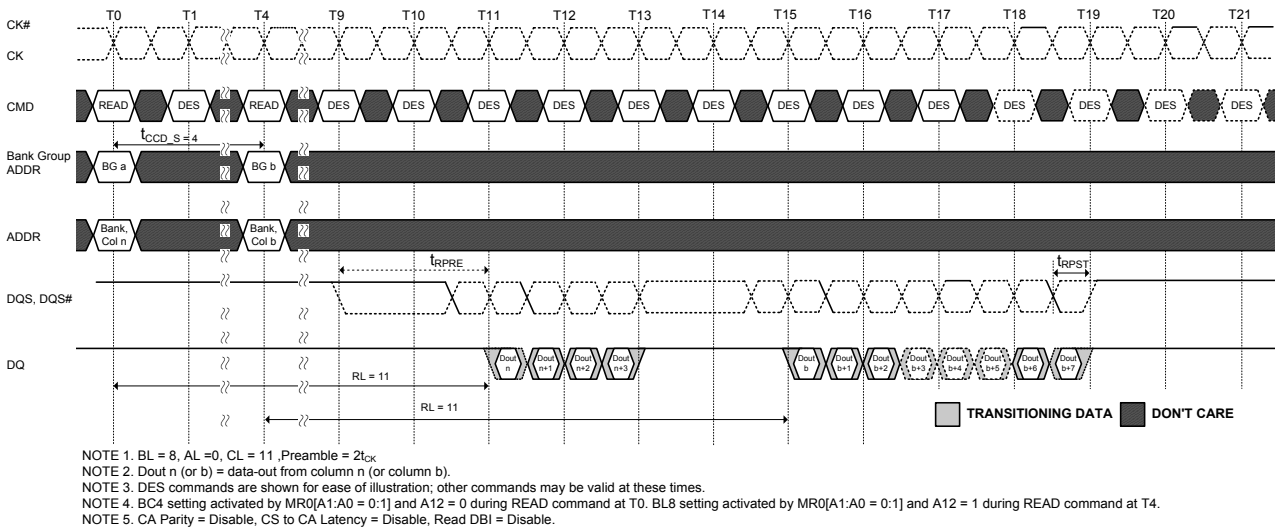
NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 2t<sub>CK</sub>  
 NOTE 2. Dout n (or b) = data-out from column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

**Figure 104. READ (BL8) to READ (BC4) OTF with 2t<sub>CK</sub> Preamble in Different Bank Group**

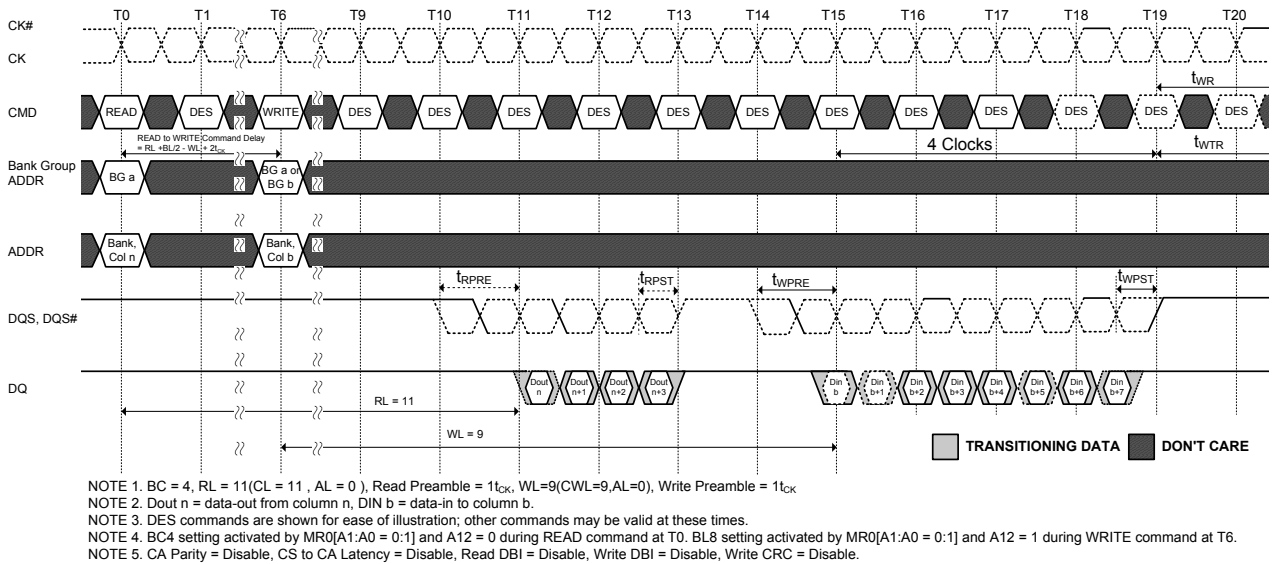




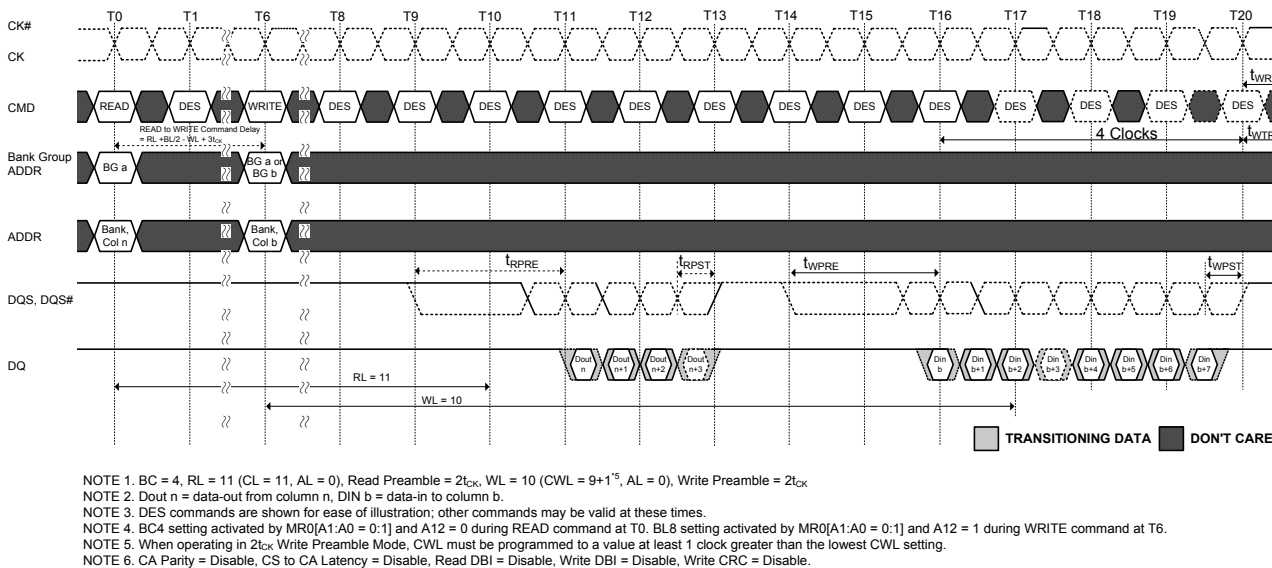
**Figure 105. READ (BC4) to READ (BL8) OTF with  $1t_{CK}$  Preamble in Different Bank Group**



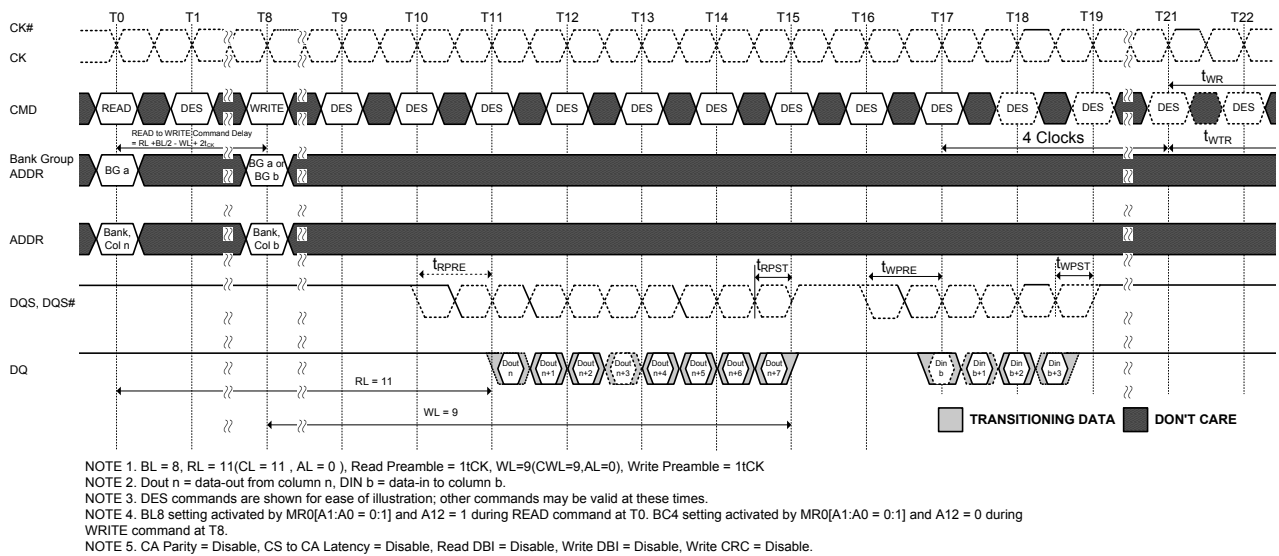
**Figure 106. READ (BC4) to READ (BL8) OTF with  $2t_{CK}$  Preamble in Different Bank Group**



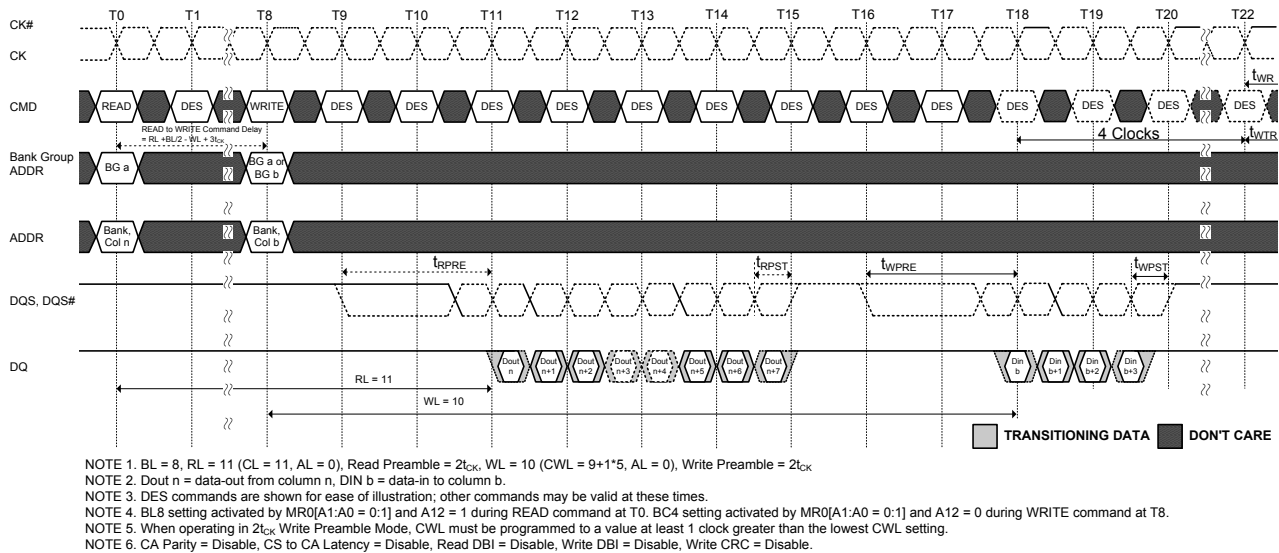
**Figure 107. READ (BC4) to WRITE (BL8) OTF with  $1t_{CK}$  Preamble in Same or Different Bank Group**



**Figure 108. READ (BC4) to WRITE (BL8) OTF with  $2t_{CK}$  Preamble in Same or Different Bank Group**



**Figure 109. READ (BL8) to WRITE (BC4) OTF with 1t<sub>CK</sub> Preamble in Same or Different Bank Group**



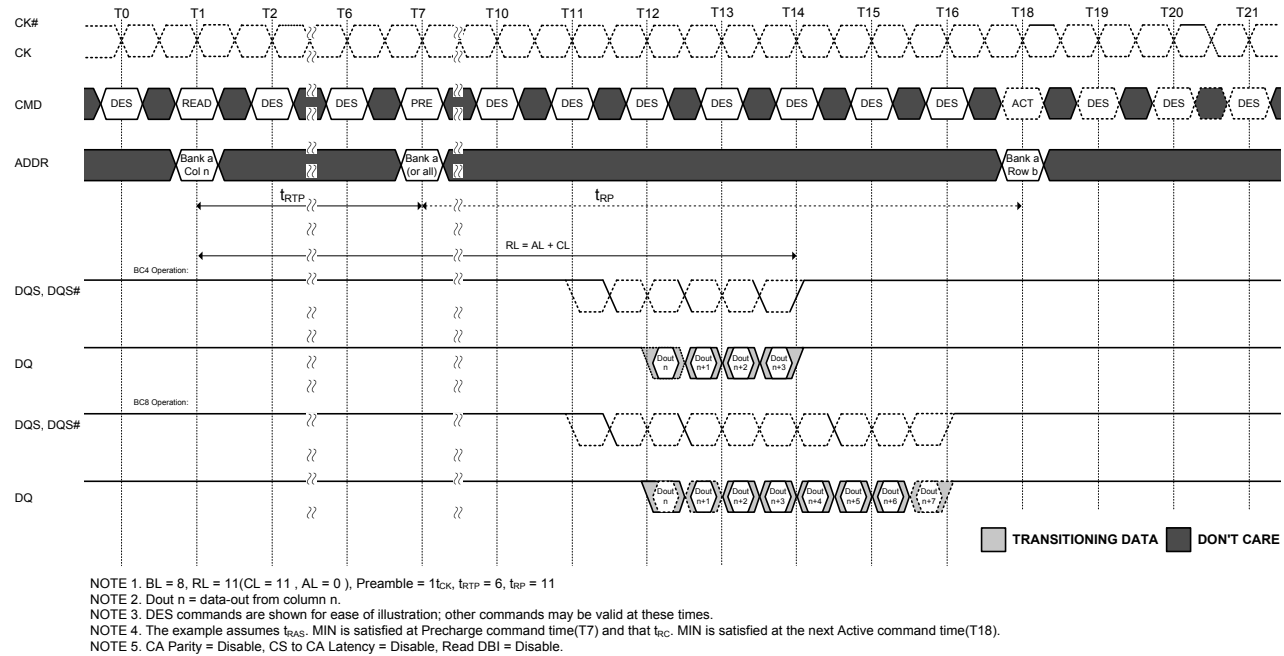
**Figure 110. READ (BL8) to WRITE (BC4) OTF with 2t<sub>CK</sub> Preamble in Same or Different Bank Group**

## Burst Read Operation followed by a Precharge

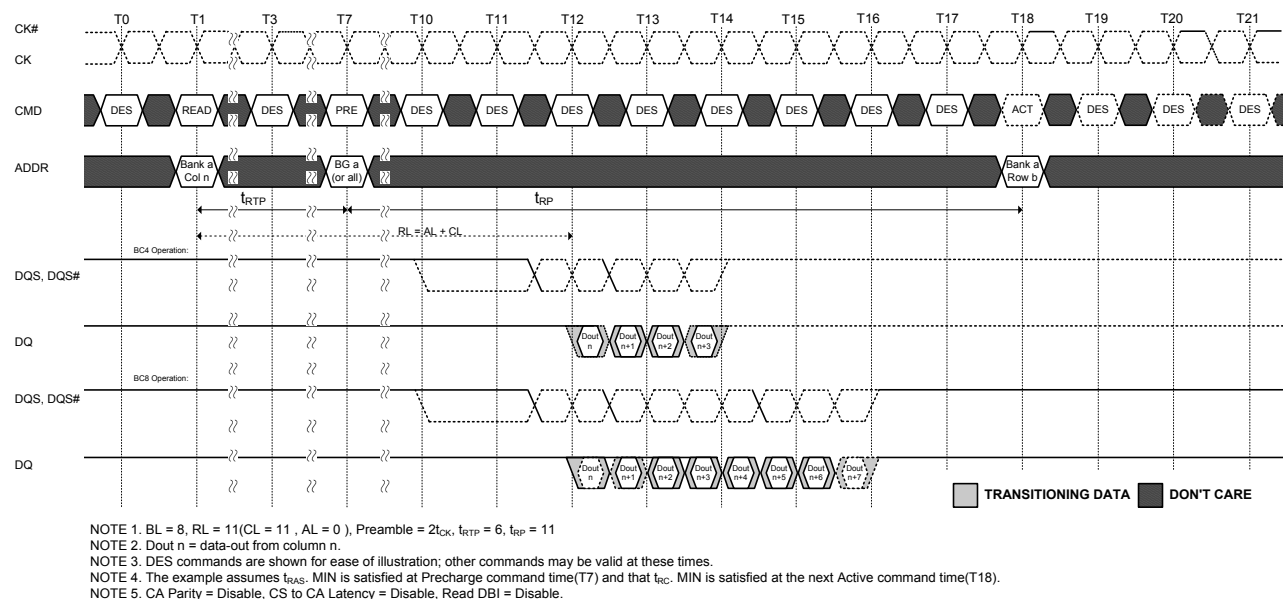
The minimum external Read command to Precharge command spacing to the same bank is equal to  $AL + t_{RTP}$  with  $t_{RTP}$  being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing,  $t_{RAS}$ , must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by  $t_{RTP(min)}$ . A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time ( $t_{RP,MIN}$ ) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time ( $t_{RC,MIN}$ ) from the previous bank activation has been satisfied.

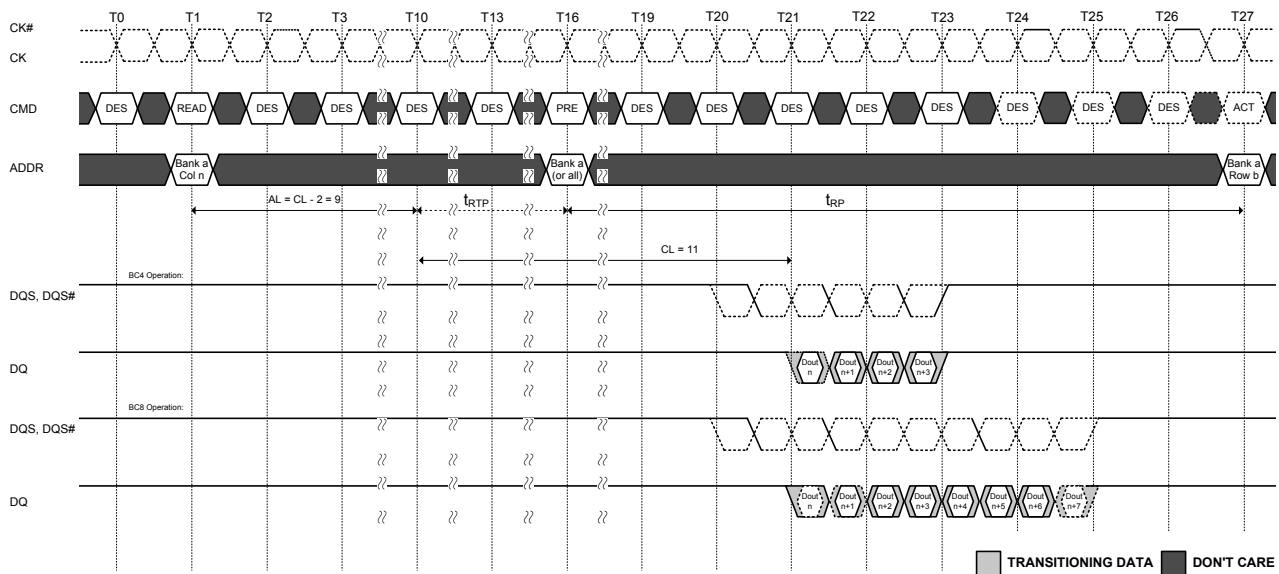
Examples of Read commands followed by Precharge are show in Read to Precharge with  $1t_{CK}$  Preamble to Read to Precharge with Additive Latency and  $1t_{CK}$  Preamble.



**Figure 111. READ to PRECHARGE with  $1t_{CK}$  Preamble**

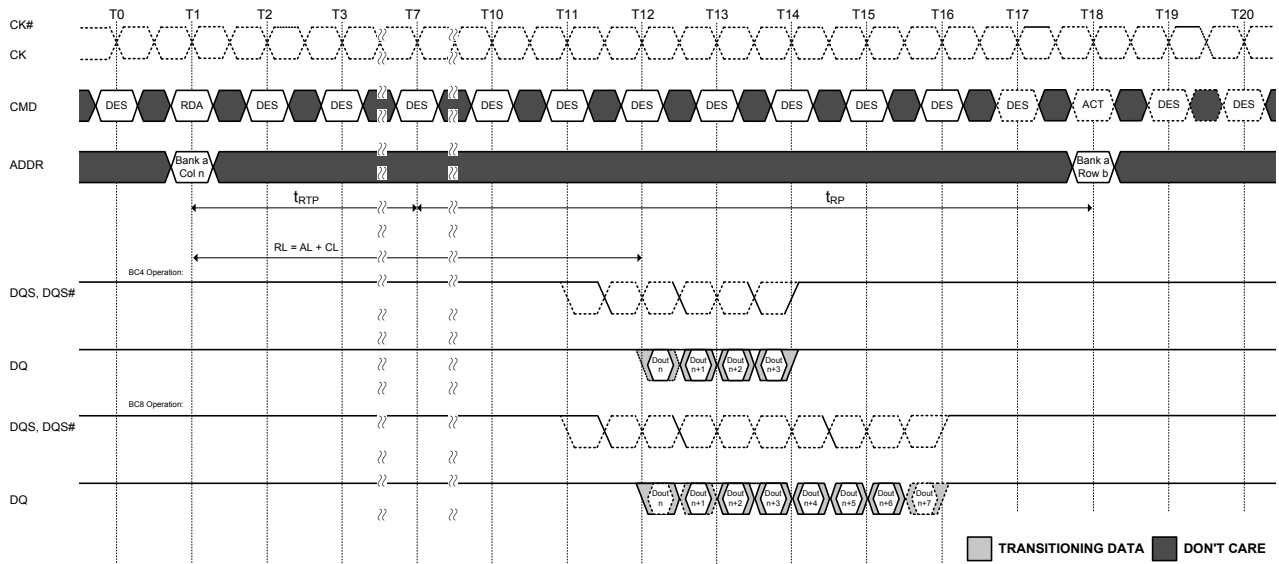


**Figure 112. READ to PRECHARGE with  $2t_{CK}$  Preamble**



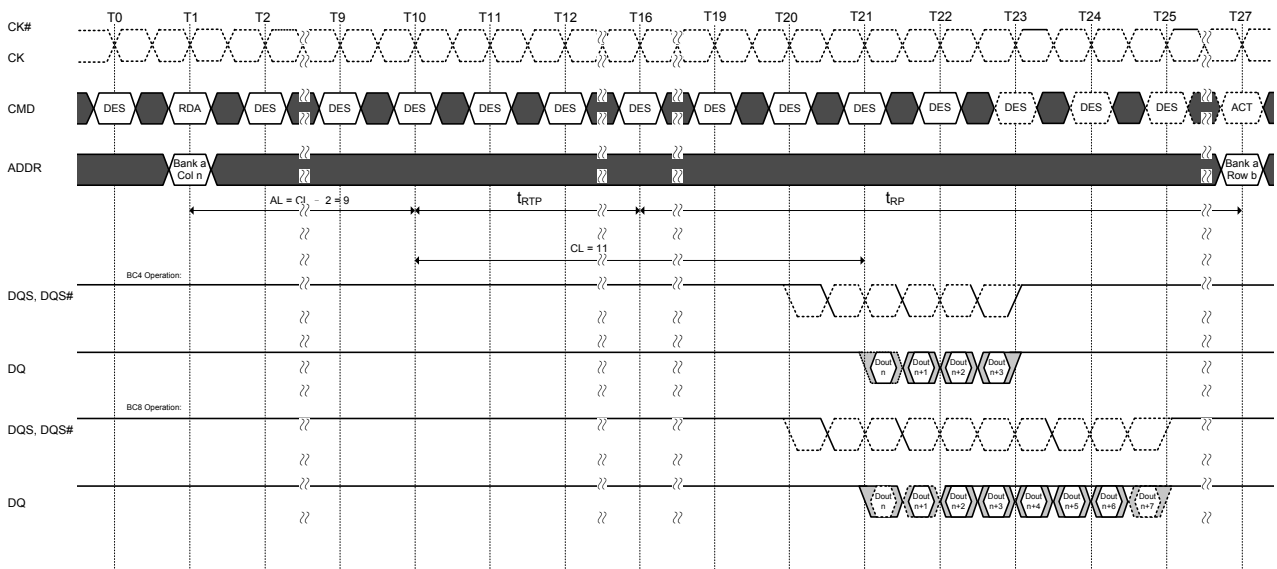
NOTE 1. BL = 8, RL = 20 (CL = 11, AL = CL - 2), Preamble =  $1t_{CK}$ ,  $t_{RTP} = 6$ ,  $t_{RP} = 11$   
 NOTE 2. Dout n = data-out from column n.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. The example assumes  $t_{RAS}$ . MIN is satisfied at Precharge command time(T16) and that  $t_{RC}$ . MIN is satisfied at the next Active command time(T27).  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

**Figure 113. READ to PRECHARGE with Additive Latency and  $1t_{CK}$  Preamble**



NOTE 1. BL = 8, RL = 11 (CL = 11, AL = 0), Preamble =  $1t_{CK}$ ,  $t_{RTP} = 6$ ,  $t_{RP} = 11$   
 NOTE 2. Dout n = data-out from column n.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4.  $t_{RTP} = 6$  setting activated by MR0[A11:9 = 001]  
 NOTE 5. The example assumes  $t_{RC}$ . MIN is satisfied at the next Active command time(T18).  
 NOTE 6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

**Figure 114. READ with Auto Precharge and  $1t_{CK}$  Preamble**

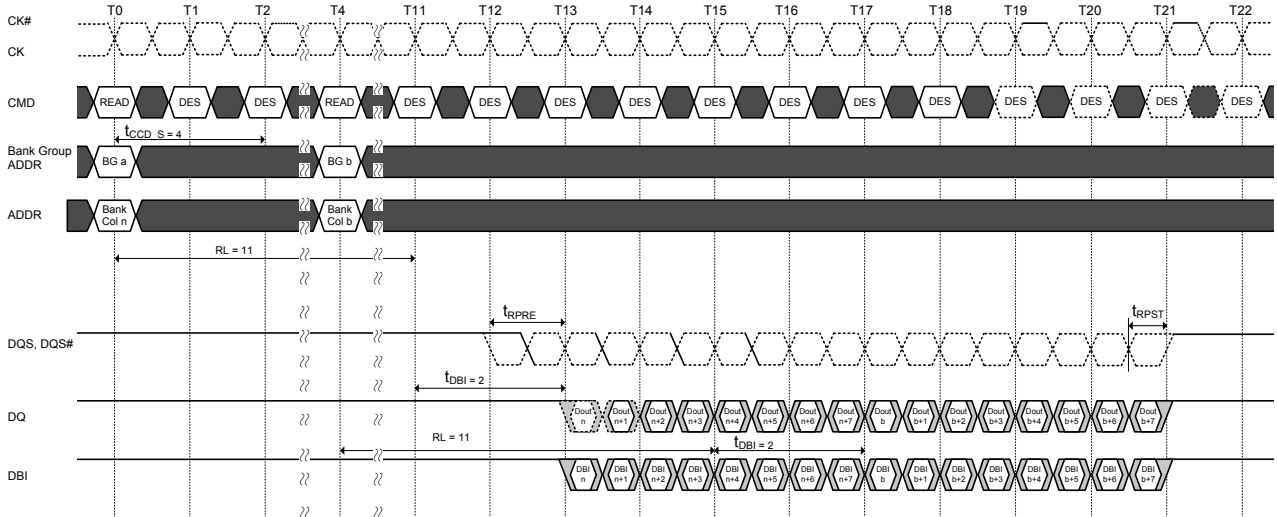


NOTE 1. BL = 8, RL = 20 (CL = 11, AL = CL - 2), Preamble = 1t<sub>CK</sub>, t<sub>RTP</sub> = 6, t<sub>RP</sub> = 11  
 NOTE 2. Dout n = data-out from column n.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. t<sub>RTP</sub> = 6 setting activated by MR0[A11:9 = 001]  
 NOTE 5. The example assumes t<sub>RC</sub> MIN is satisfied at the next Active command time (T27).  
 NOTE 6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

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**Figure 115. READ with Auto Precharge, Additive Latency and 1t<sub>CK</sub> Preamble**

### Burst Read Operation with Read DBI (Data Bus Inversion)

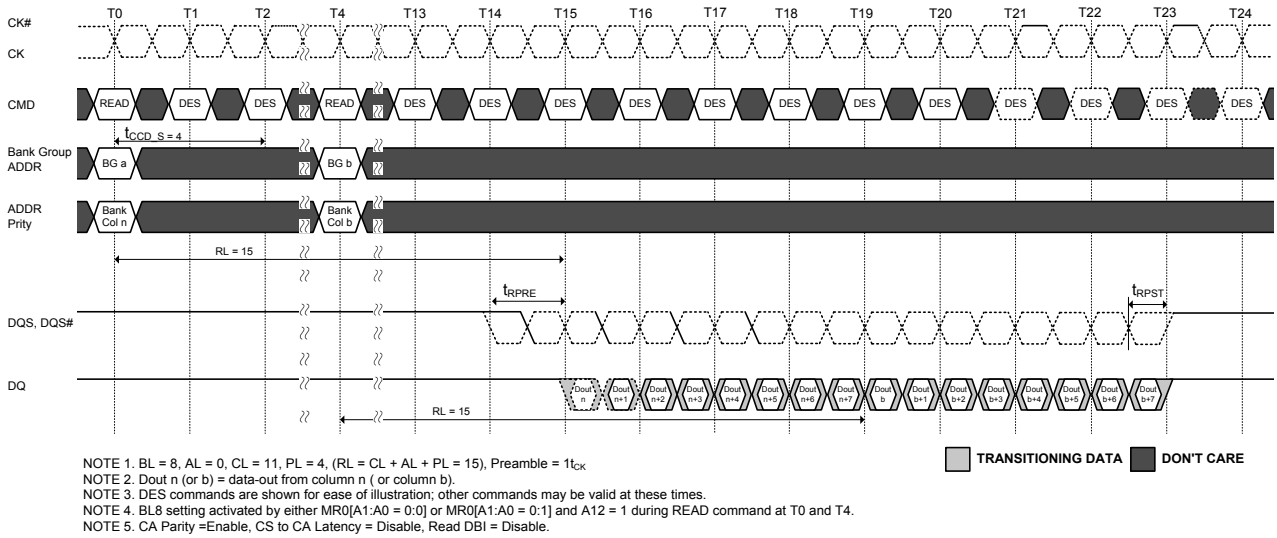


NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 1t<sub>CK</sub>, t<sub>DBI</sub> = 2t<sub>CK</sub>  
 NOTE 2. Dout n (or b) = data-out from column n ( or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Enable.

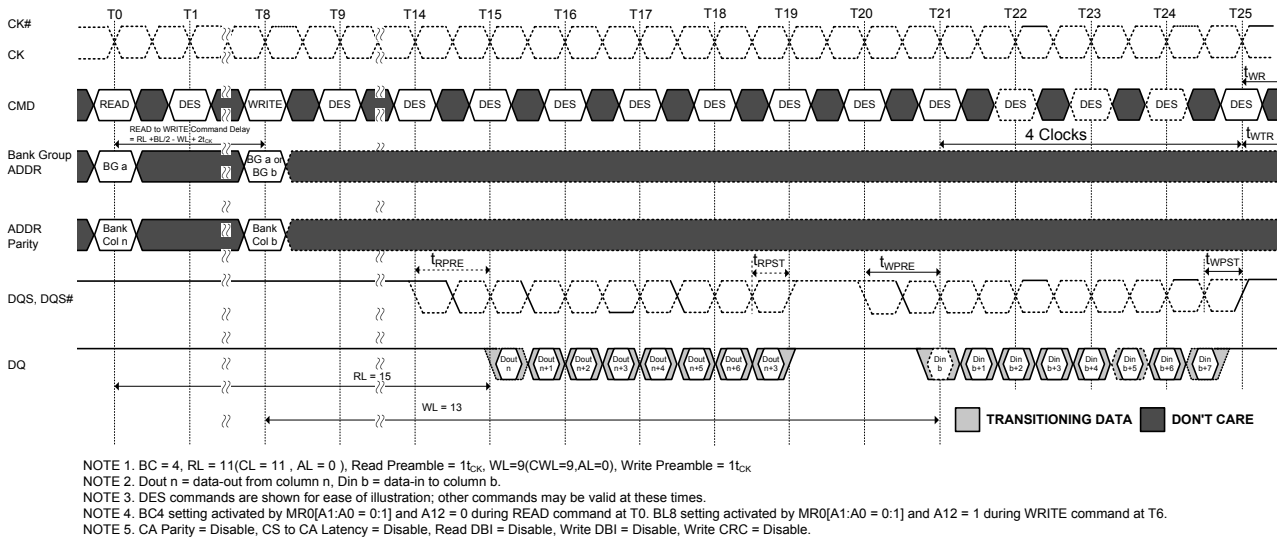
TRANSITIONING DATA DON'T CARE

**Figure 116. Consecutive READ (BL8) with 1t<sub>CK</sub> Preamble and DBI in Different Bank Group**

## Burst Read Operation with Command/Address Parity



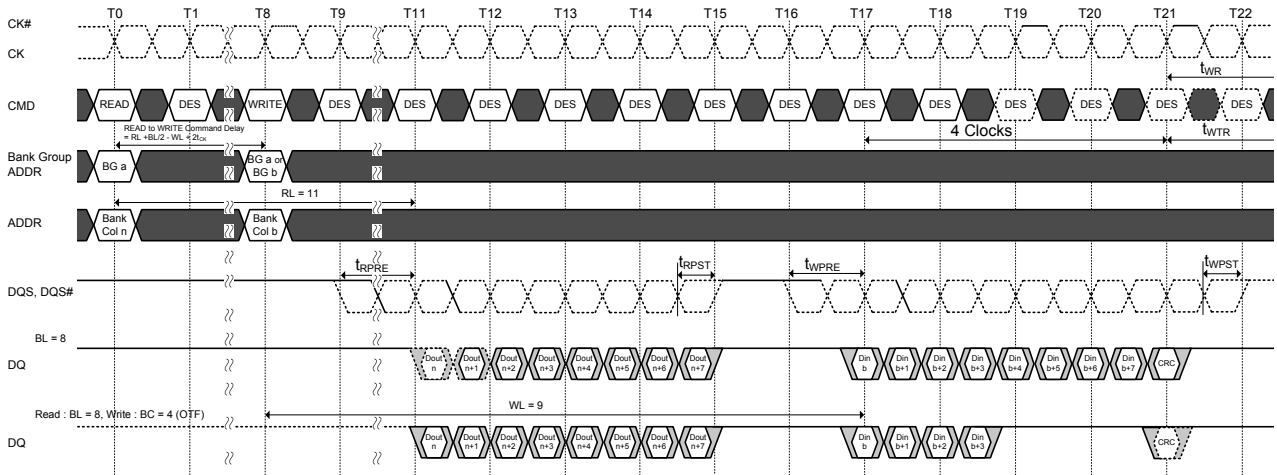
**Figure 117. Consecutive READ (BL8) with 1t<sub>CK</sub> Preamble and CA Parity in Different Bank Group**



**Figure 118. READ (BL8) to WRITE (BL8) with 1t<sub>CK</sub> Preamble and CA parity in Same or Different Bank Group**

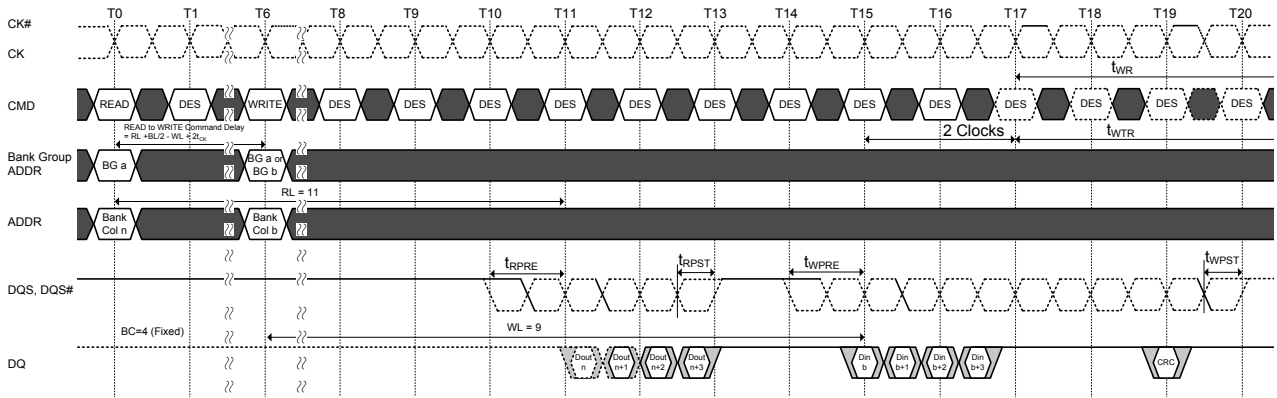


## Read to Write with Write CRC



- NOTE 1. BL = 8 ( or BC = 4 : OTF for Write), RL = 11 (CL = 11, AL = 0), Read Preamble = 1t<sub>CK</sub>, WL=9 (CWL=9, AL=0), Write Preamble = 1t<sub>CK</sub>  
 NOTE 2. Dout n = data-out from column n. Din b = data-in to column b.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.  
 NOTE 5. BC4 setting activated by MR0[A1:0 = 0:1] and A12 = 0 during Write command at T8.  
 NOTE 6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

**Figure 119. READ (BL8) to WRITE (BL8 or BC4: OTF) with 1t<sub>CK</sub> Preamble and Write CRC in Same or Different Bank Group**

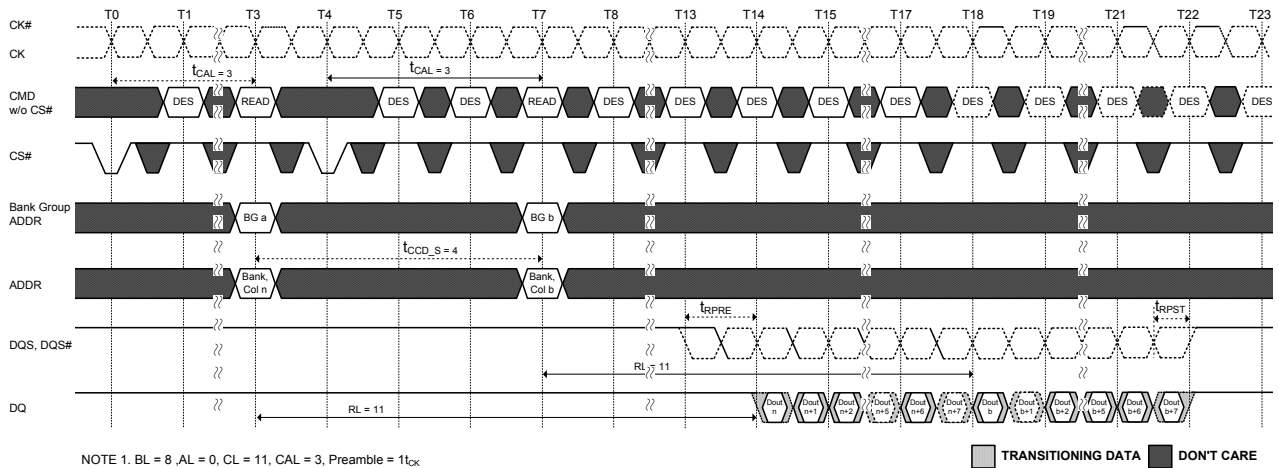


- NOTE 1. BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), Read Preamble = 1t<sub>CK</sub>, WL=9 (CWL=9, AL=0), Write Preamble = 1t<sub>CK</sub>  
 NOTE 2. Dout n = data-out from column n. Din b = data-in to column b.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BC4 setting activated by MR0[A1:A0 = 1:0].  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

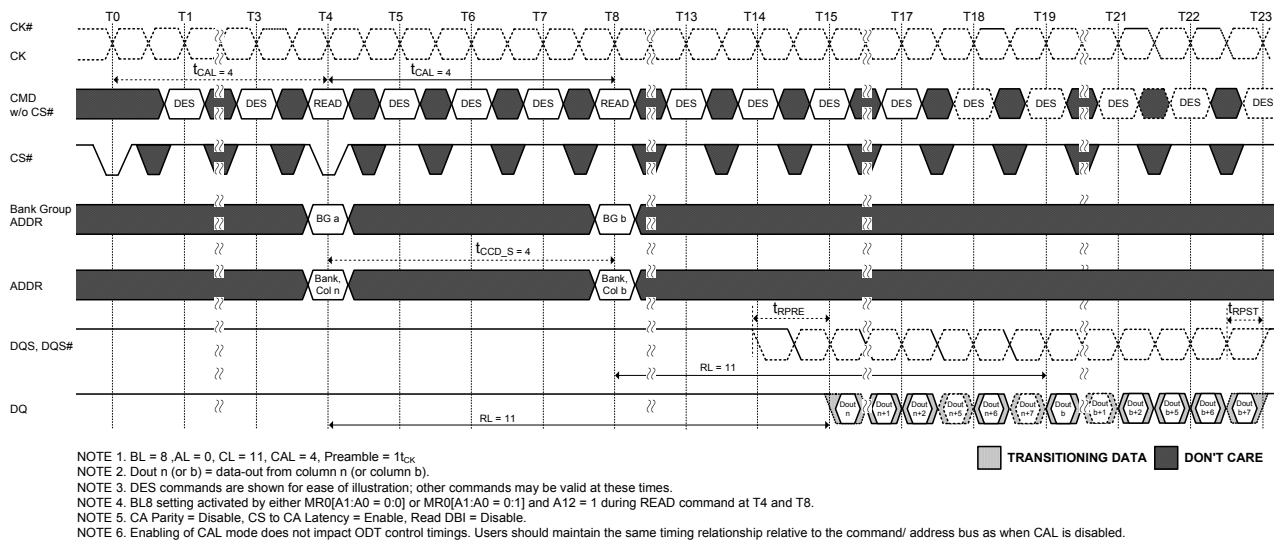
**Figure 120. READ (BC4:Fixed) to WRITE (BC4: Fixed) with 1t<sub>CK</sub> Preamble and Write CRC in Same or Different Bank Group**



## Read to Read with CS to CA Latency



**Figure 121. Consecutive READ (BL8) with CAL(3) and 1t<sub>CK</sub> Preamble in Different Bank Group**



**Figure 122. Consecutive READ (BL8) with CAL(4) and 1t<sub>CK</sub> Preamble in Different Bank Group**

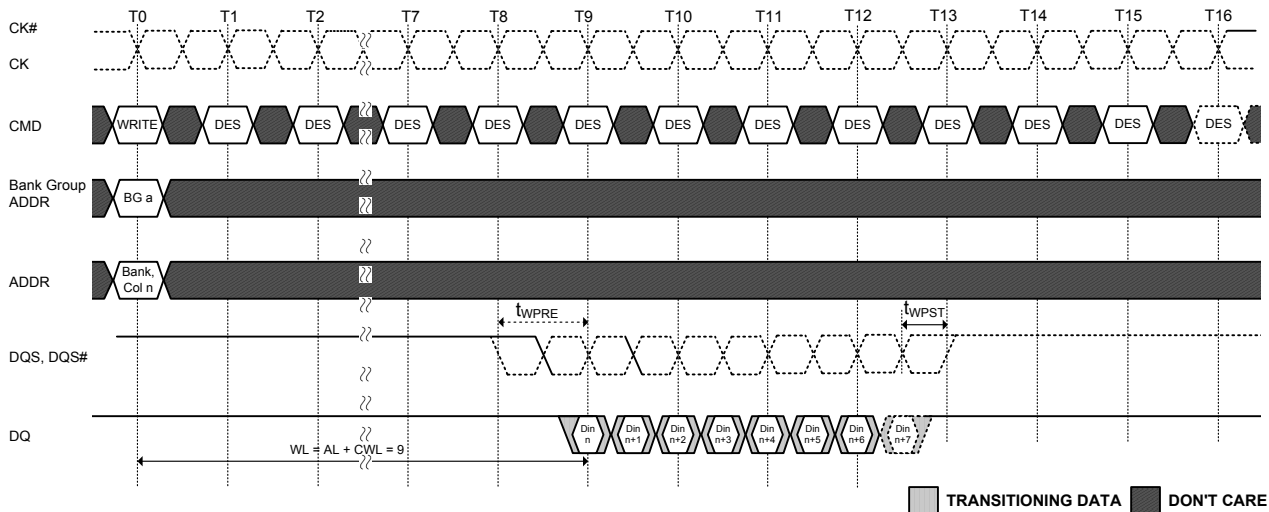




## Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



NOTE 1. BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1t<sub>CK</sub>

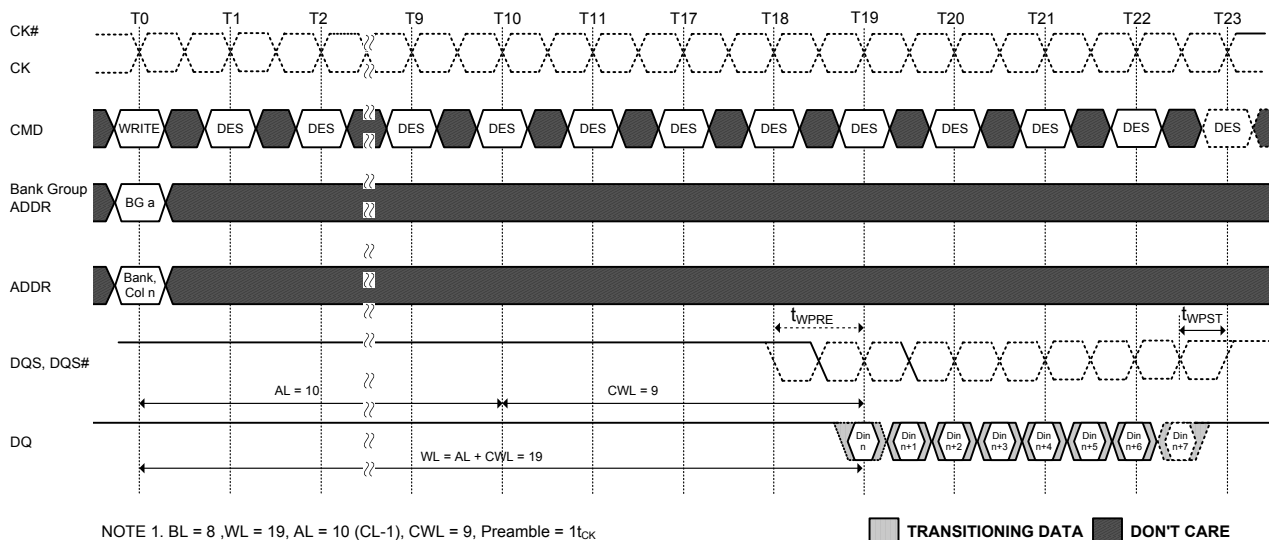
NOTE 2. Din n = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

**Figure 125. WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)**



NOTE 1. BL = 8, WL = 19, AL = 10 (CL-1), CWL = 9, Preamble = 1t<sub>CK</sub>

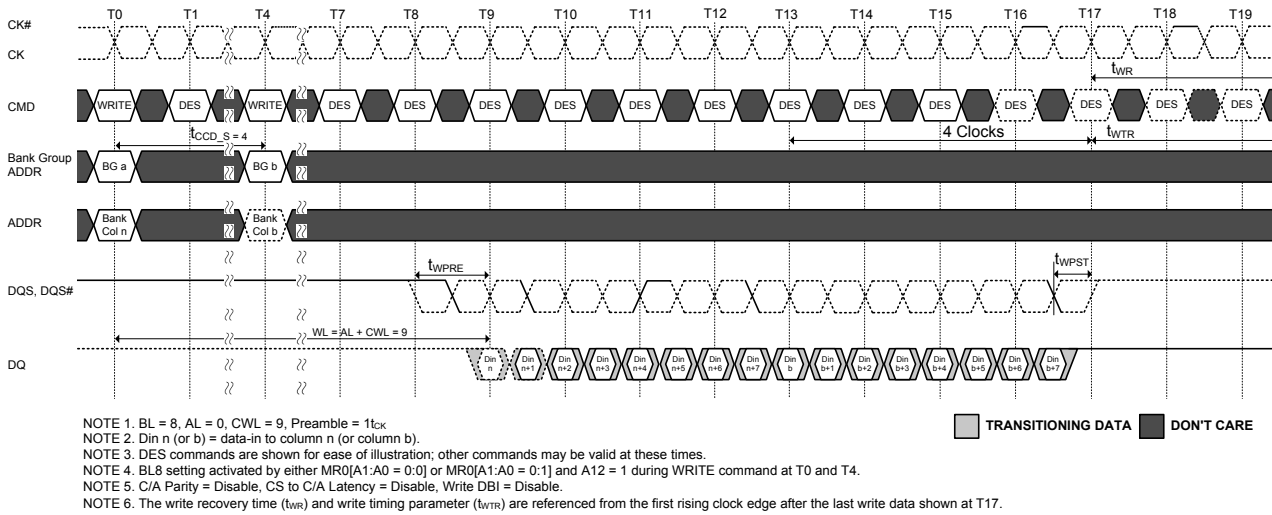
NOTE 2. Din n = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

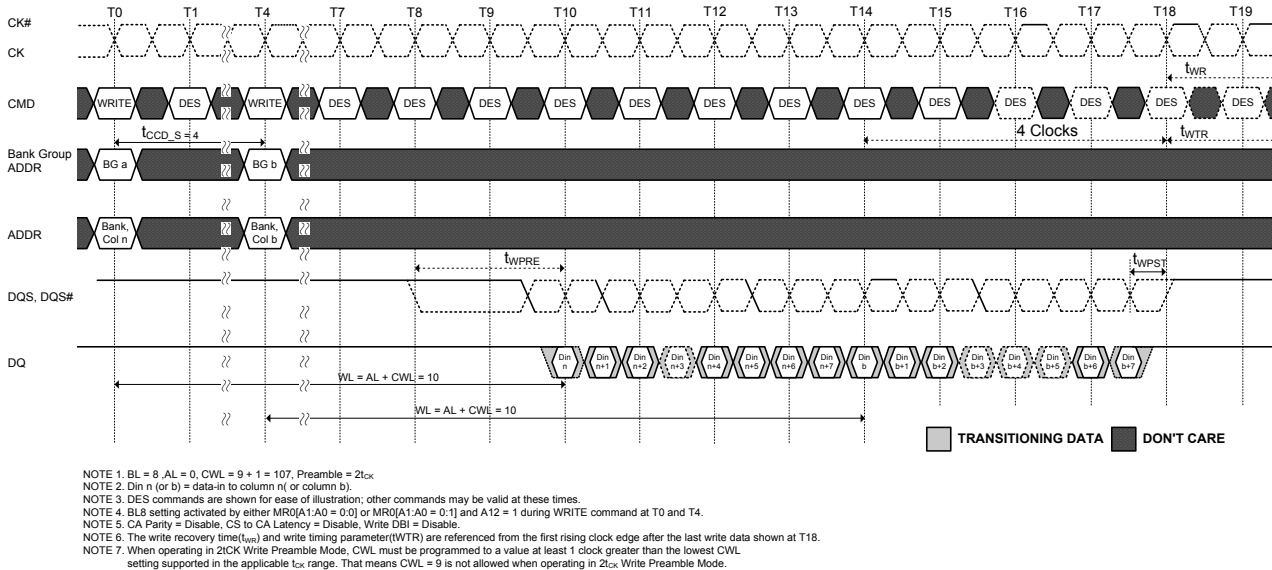
NOTE 4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

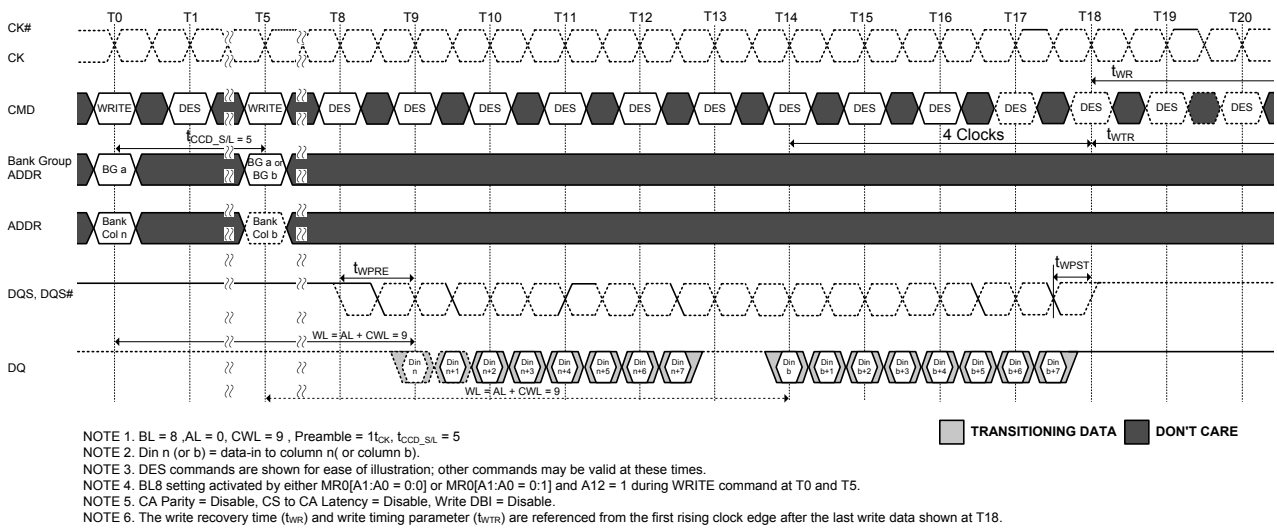
**Figure 126. WRITE Burst Operation WL = 19 (AL = 10, CWL = 9, BL8)**



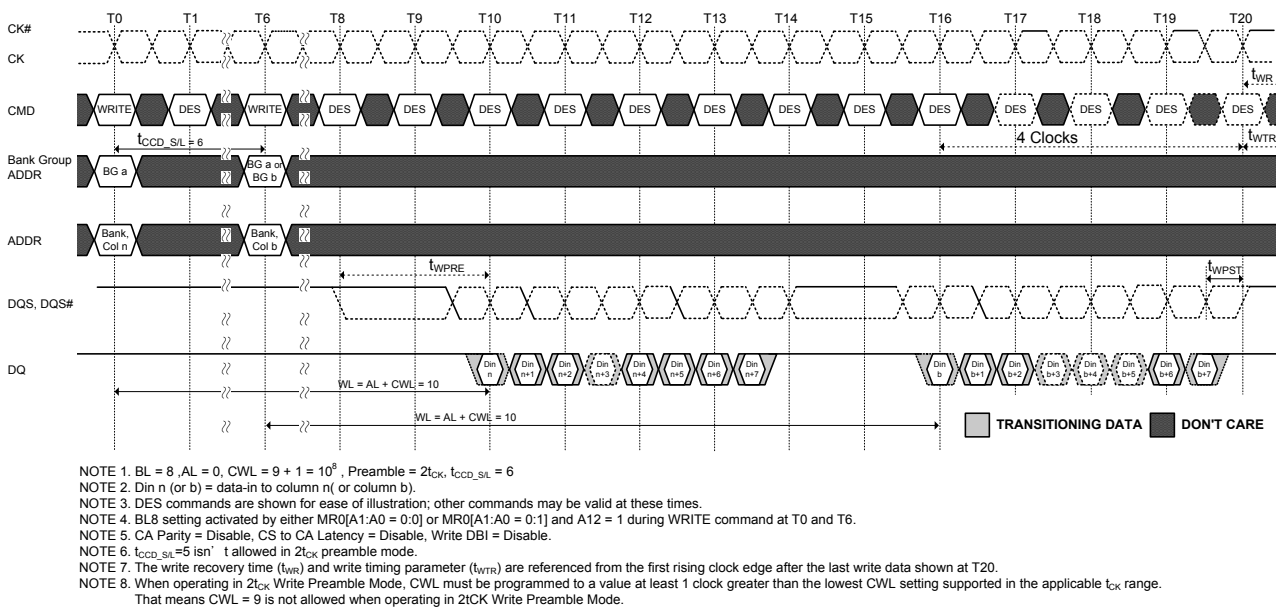
**Figure 127. Consecutive WRITE (BL8) with  $1t_{CK}$  Preamble in Different Bank Group**



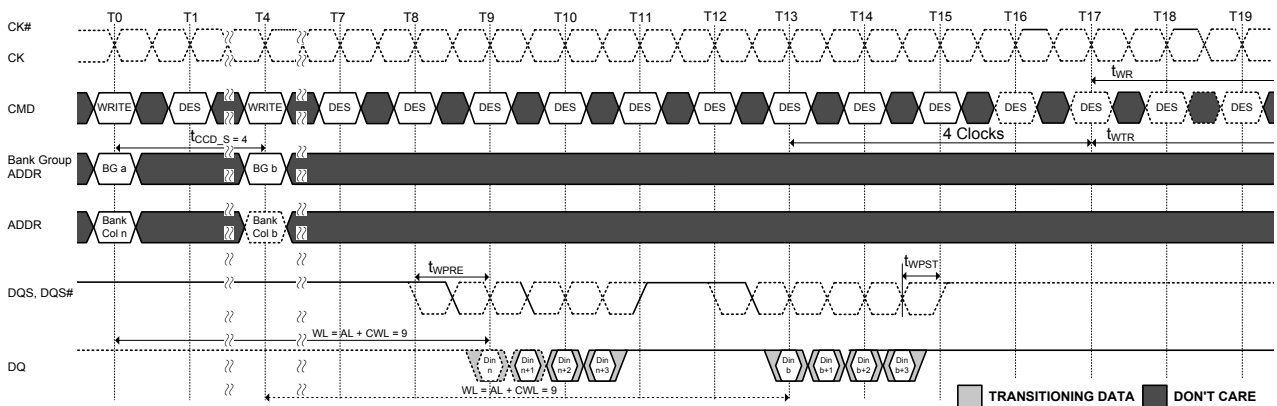
**Figure 128. Consecutive WRITE (BL8) with  $2t_{CK}$  Preamble in Different Bank Group**



**Figure 129. Nonconsecutive WRITE (BL8) with  $1t_{CK}$  Preamble in Same or Different Bank Group**

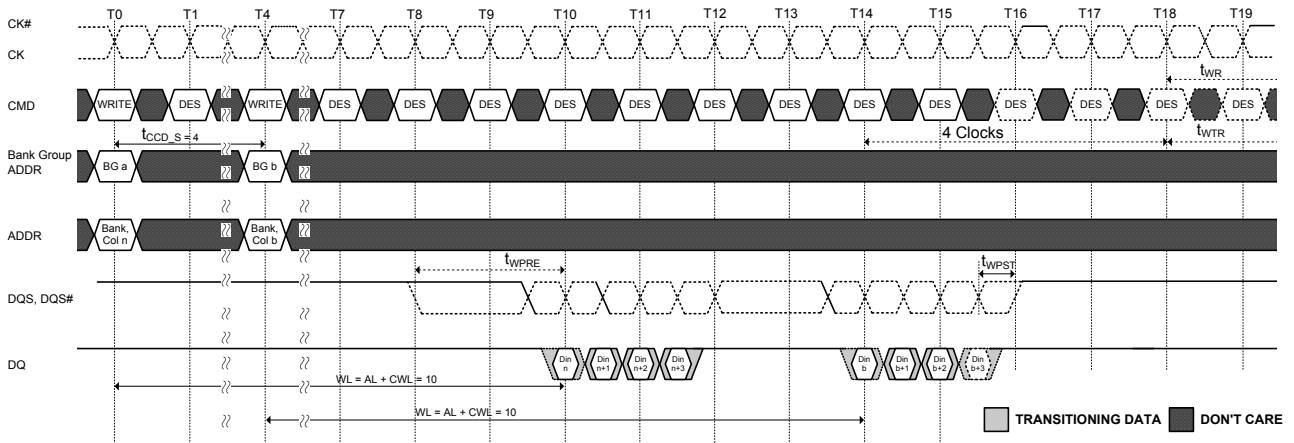


**Figure 130. Nonconsecutive WRITE (BL8) with  $2t_{CK}$  Preamble in Same or Different Bank Group**



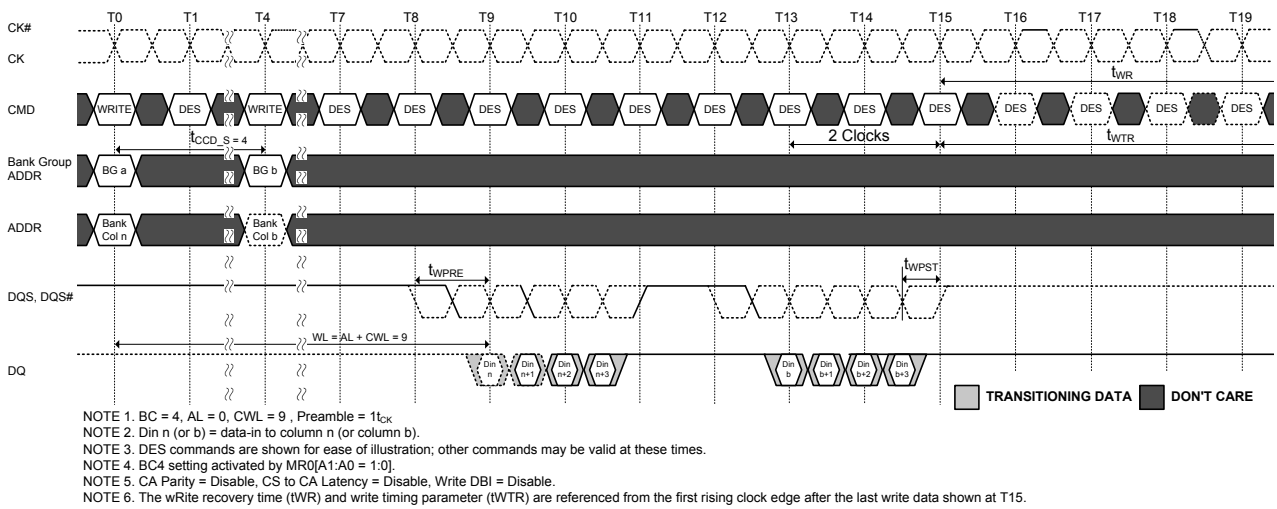
NOTE 1. BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$   
 NOTE 2. Din n (or b) = data-in to column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.  
 NOTE 6. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T17.

**Figure 131. WRITE (BC4) OTF to WRITE (BC4) OTF with  $1t_{CK}$  Preamble in Different Bank Group**

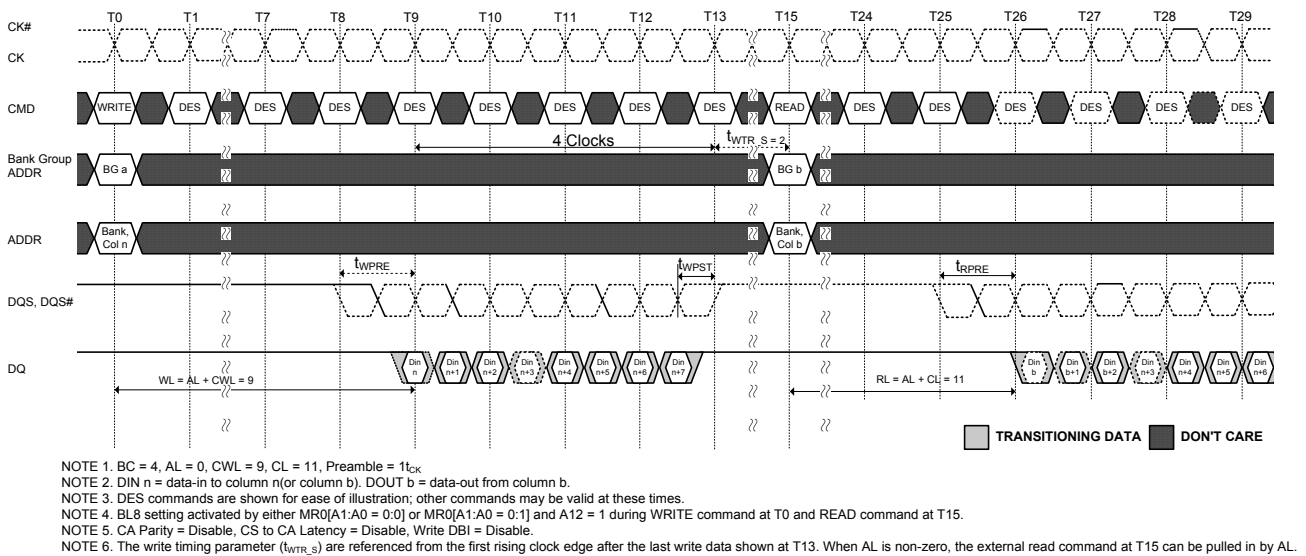


NOTE 1. BC = 4, AL = 0, CWL =  $9 + 1 = 10^7$ , Preamble =  $2t_{CK}$   
 NOTE 2. Din n (or b) = data-in to column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.  
 NOTE 6. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T18.  
 NOTE 7. When operating in  $2t_{CK}$  Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable  $t_{CK}$  range. That means CWL = 9 is not allowed when operating in  $2t_{CK}$  Write Preamble Mode.

**Figure 132. WRITE (BC4) OTF to WRITE (BC4) OTF with  $2t_{CK}$  Preamble in Different Bank Group**

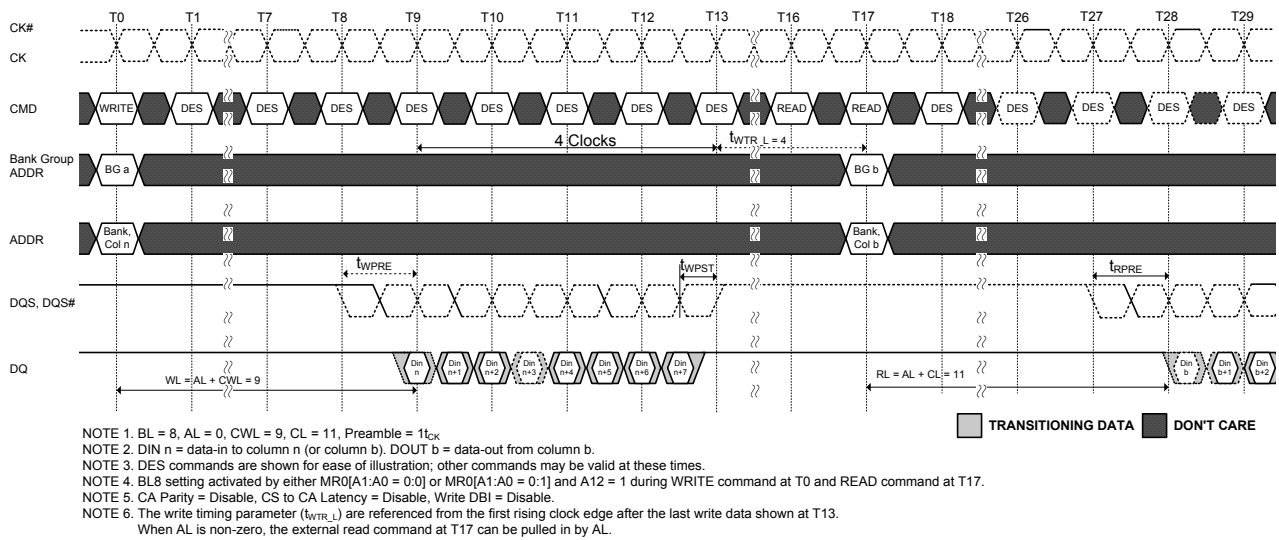


**Figure 133. WRITE (BC4) Fixed to WRITE (BC4) Fixed with  $1t_{CK}$  Preamble in Different Bank Group**

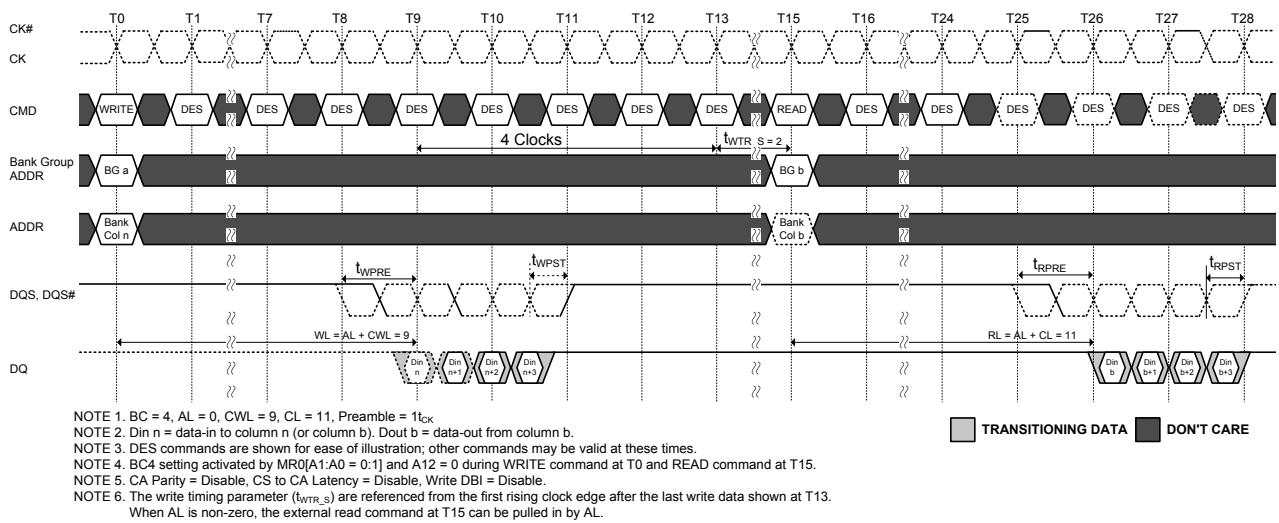


**Figure 134. WRITE (BL8) to READ (BL8) with  $1t_{CK}$  Preamble in Different Bank Group**

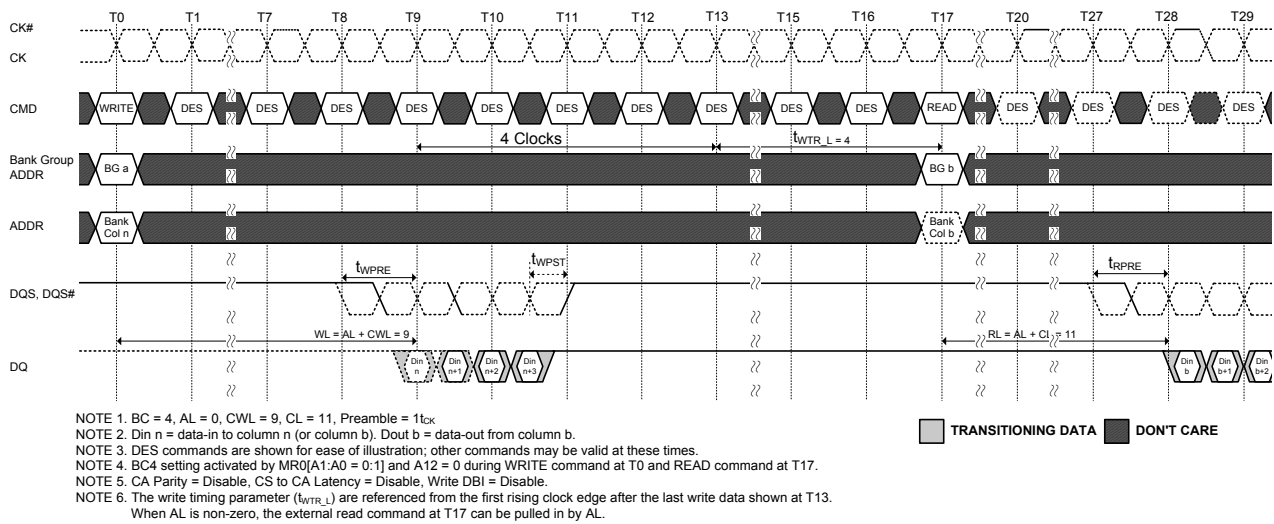




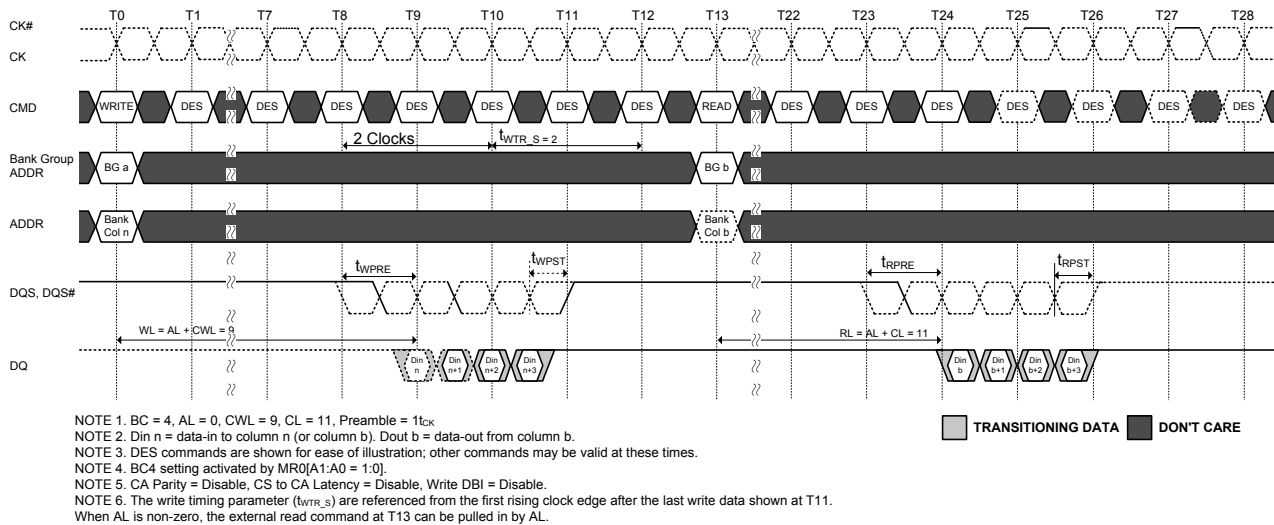
**Figure 135. WRITE (BL8) to READ (BL8) with  $1t_{CK}$  Preamble in Same Bank Group**



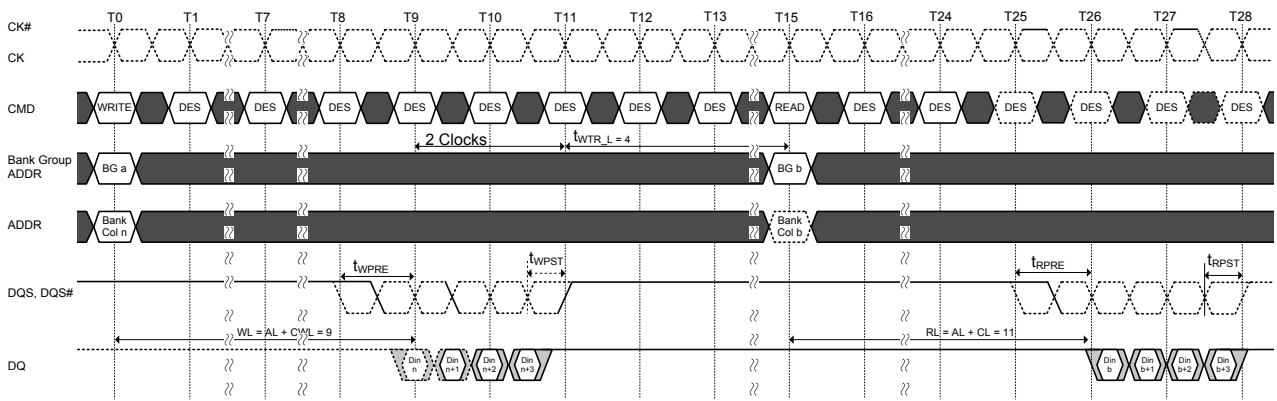
**Figure 136. WRITE (BC4)OTF to READ (BC4)OTF with  $1t_{CK}$  Preamble in Different Bank Group**



**Figure 137. WRITE (BC4)OTF to READ (BC4)OTF with  $1t_{CK}$  Preamble in Same Bank Group**



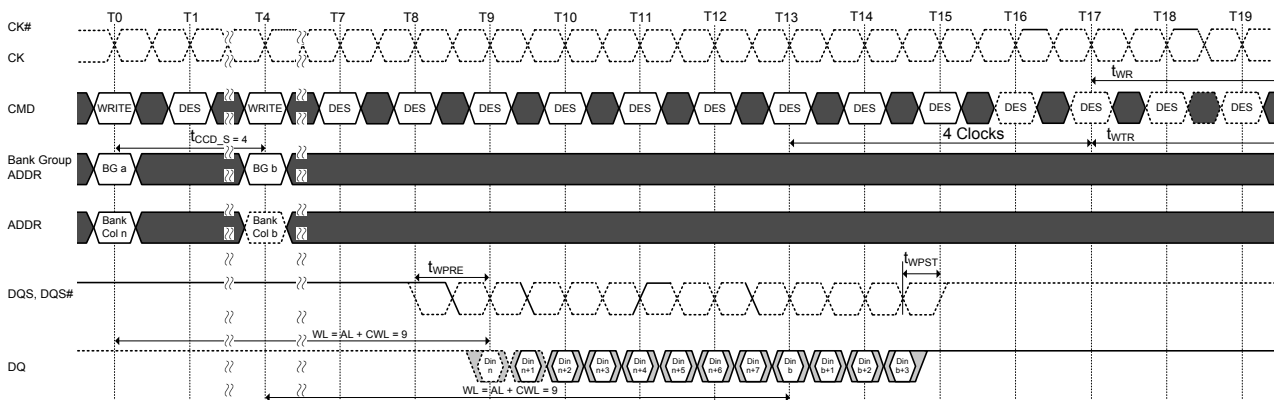
**Figure 138. WRITE (BC4)Fixed to READ (BC4)Fixed with  $1t_{CK}$  Preamble in Different Bank Group**



NOTE 1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble =  $1t_{CK}$   
 NOTE 2. Din n = data-in to column n (or column b). Dout b = data-out from column b.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BC4 setting activated by MR0[A1:A0 = 1:0].  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.  
 NOTE 6. The write timing parameter ( $t_{WTR\_L}$ ) are referenced from the first rising clock edge after the last write data shown at T11.  
 When AL is non-zero, the external read command at T15 can be pulled in by AL.

■ TRANSITIONING DATA ■ DON'T CARE

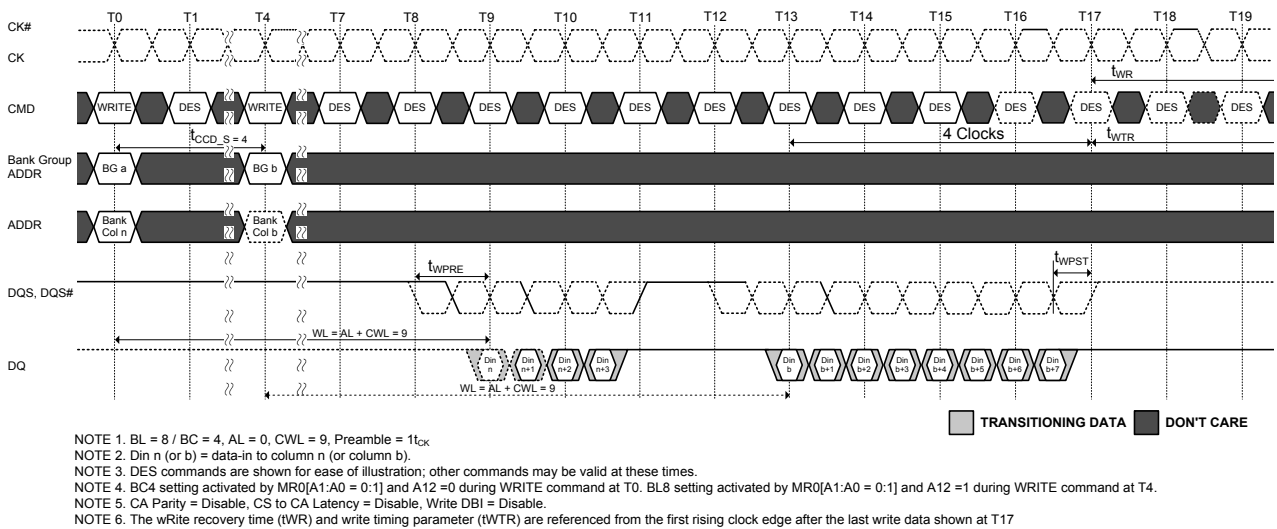
**Figure 139. WRITE (BC4)Fixed to READ (BC4)Fixed with  $1t_{CK}$  Preamble in Same Bank Group**



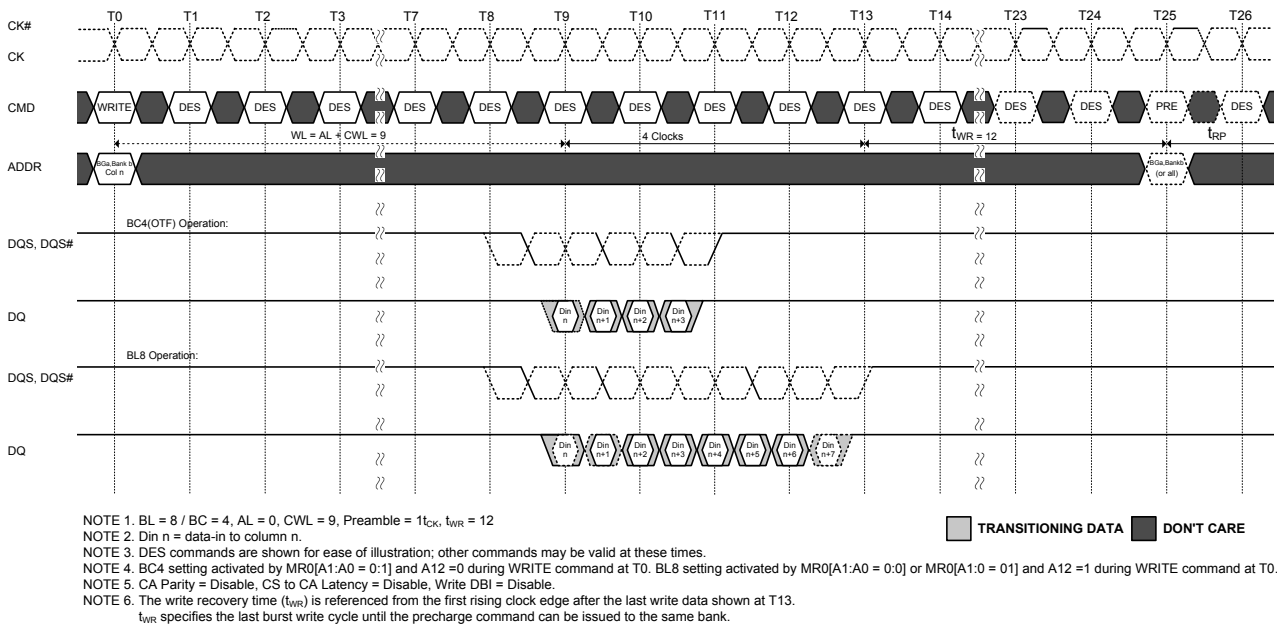
NOTE 1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$   
 NOTE 2. Din n (or b) = data-in to column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T4.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.  
 NOTE 6. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write Data shown at T17.

■ TRANSITIONING DATA ■ DON'T CARE

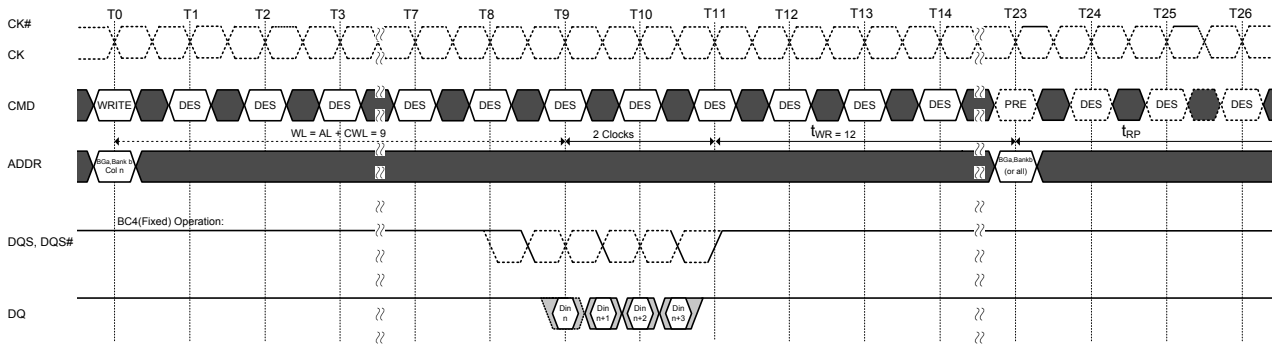
**Figure 140. WRITE (BL8) to WRITE (BC4) OTF with  $1t_{CK}$  Preamble in Different Bank Group**



**Figure 141. WRITE (BC4)OTF to WRITE (BL8) with  $1t_{CK}$  Preamble in Different Bank Group**



**Figure 142. WRITE (BL8/BC4) OTF to PRECHARGE Operation with  $1t_{CK}$  Preamble**



NOTE 1. BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ ,  $t_{WR} = 12$   
 NOTE 2. Din n = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BC4 setting activated by MR0[A1:A0 = 1:0].

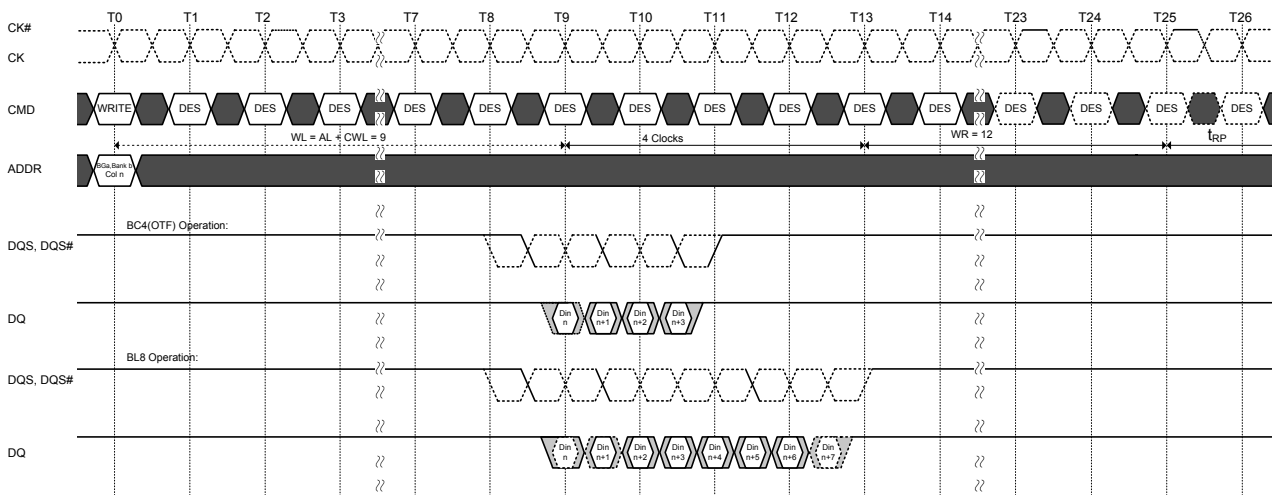
NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6. The write recovery time ( $t_{WR}$ ) is referenced from the first rising clock edge after the last write data shown at T11.

$t_{WR}$  specifies the last burst write cycle until the precharge command can be issued to the same bank.

TRANSITIONING DATA    DON'T CARE

**Figure 143. WRITE (BC4) Fixed to PRECHARGE Operation with  $1t_{CK}$  Preamble**



NOTE 1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ , WR = 12

NOTE 2. Din n = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0.

BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.

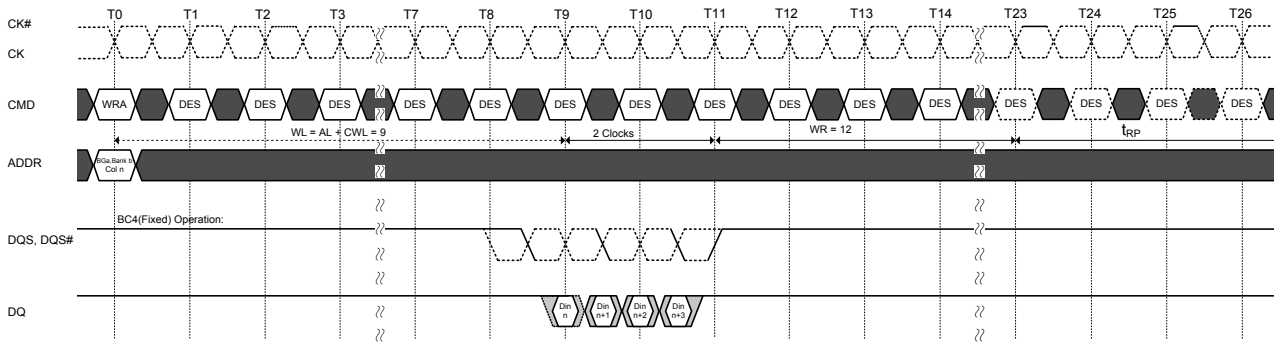
NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6. The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at T13.

WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

TRANSITIONING DATA    DON'T CARE

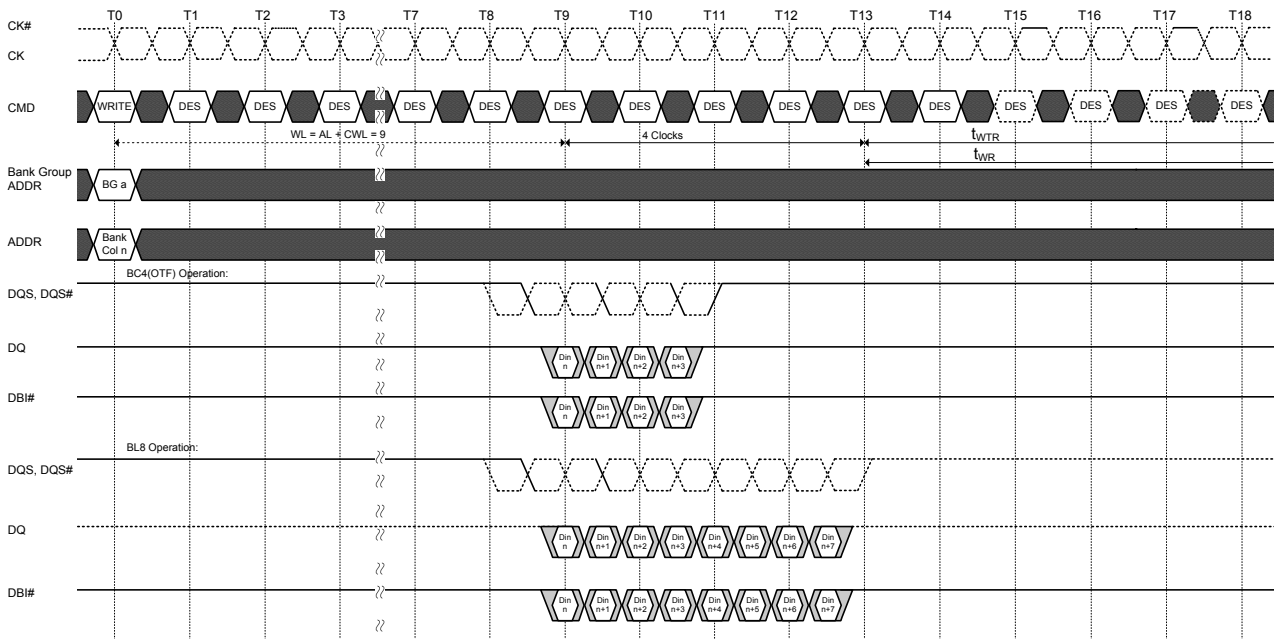
**Figure 144. WRITE (BL8/BC4) OTF with Auto PRECHARGE Operation and  $1t_{CK}$  Preamble**



NOTE 1. BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ , WR = 12  
 NOTE 2. Din n = data-in to column n.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BC4 setting activated by MR0[A1:A0 = 1:0].  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.  
 NOTE 6. The write recovery time ( $t_{WR}$ ) is referenced from the first rising clock edge after the last write data shown at T11.  
 WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

TRANSITIONING DATA    DON'T CARE

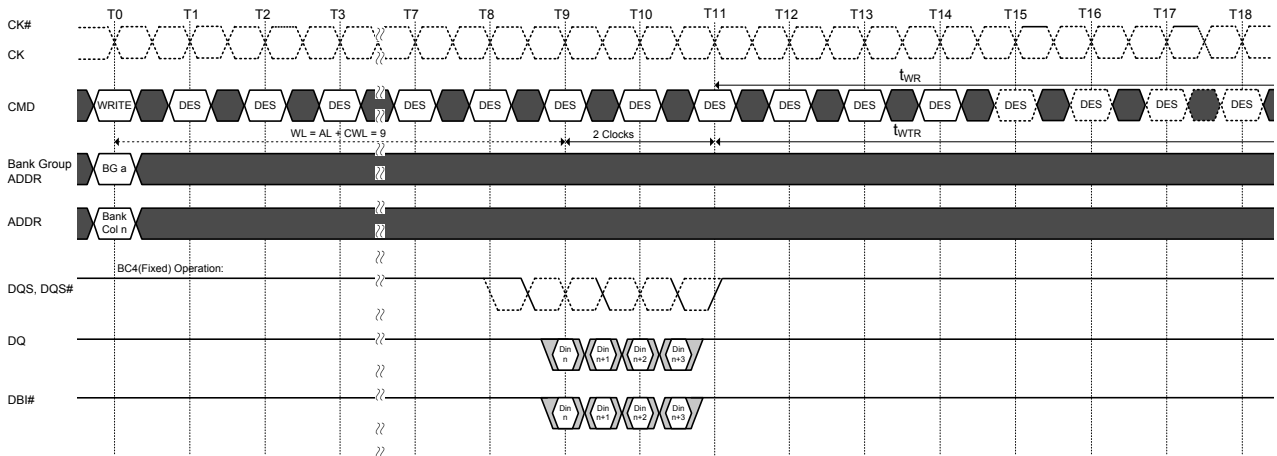
**Figure 145. WRITE (BC4) Fixed with Auto PRECHARGE Operation and  $1t_{CK}$  Preamble**



NOTE 1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$   
 NOTE 2. Din n = data-in to column n.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0.  
 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.  
 NOTE 6. The write recovery time ( $t_{WR\_DBI}$ ) and write timing parameter ( $t_{WTR\_DBI}$ ) are referenced from the first rising clock edge after the last write data shown at T13.

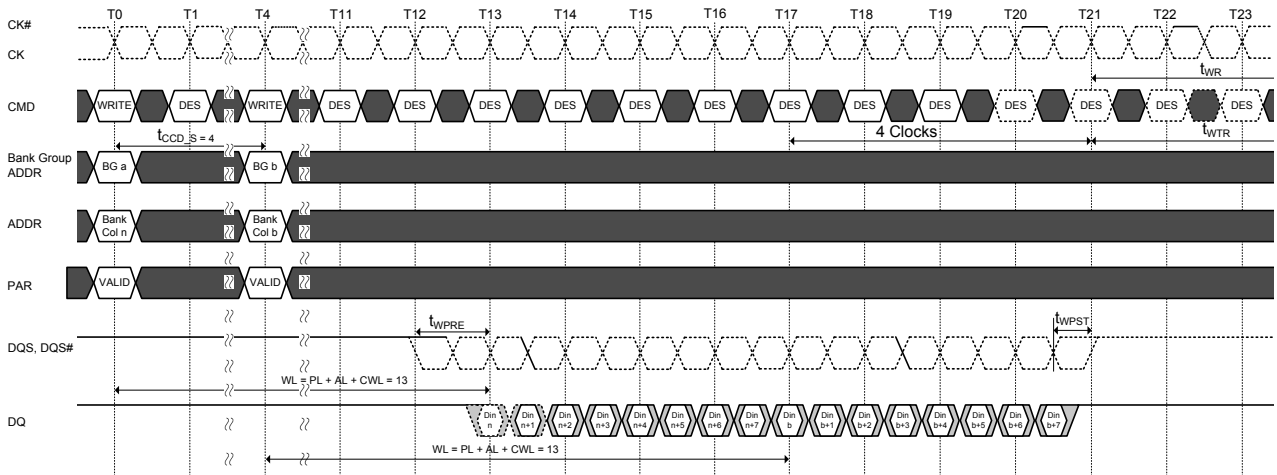
TRANSITIONING DATA    DON'T CARE

**Figure 146. WRITE (BL8/BC4) OTF with  $1t_{CK}$  Preamble and DBI**



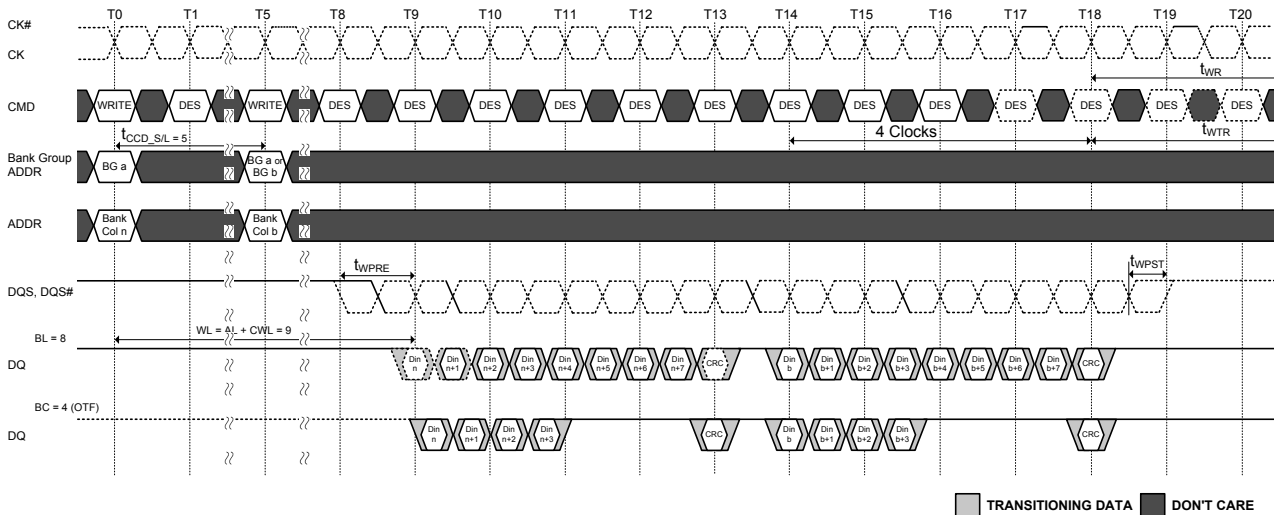
- NOTE 1. BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$   
 NOTE 2. Din n = data-in to column n.  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BC4 setting activated by MR0[A1:A0] = 1:0].  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.  
 NOTE 6. The write recovery time ( $t_{WR\_DBI}$ ) and write timing parameter ( $t_{WTR\_DBI}$ ) are referenced from the first rising clock edge after the last write data shown at T11.

**Figure 147. WRITE (BC4) Fixed with  $1t_{CK}$  Preamble and DBI**



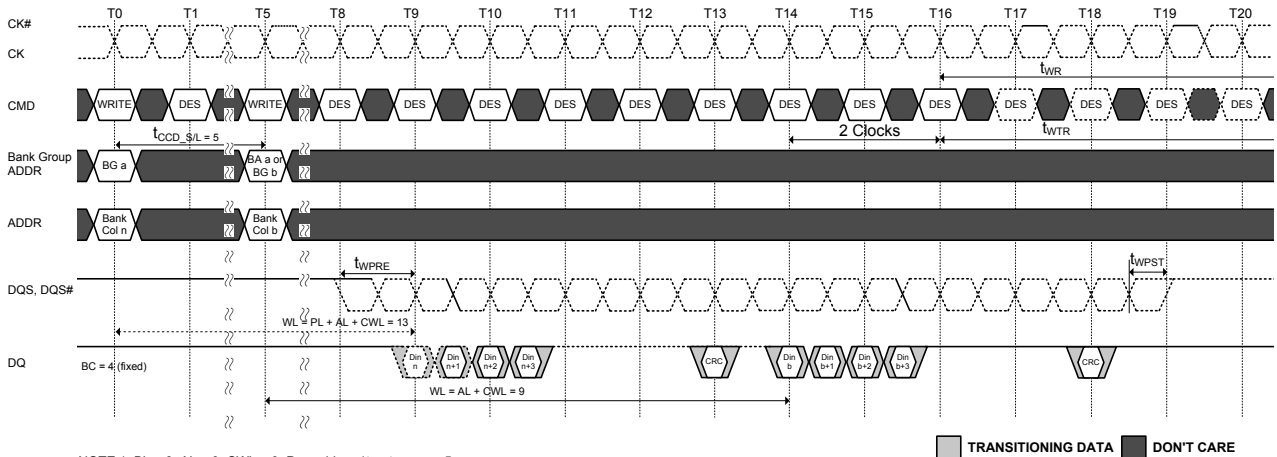
- NOTE 1. BL = 8, AL = 0, CWL = 9, PL = 4, Preamble =  $1t_{CK}$   
 NOTE 2. Din n (or b) = data-in to column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MR0[A1:A0] = 0:0] or MR0[A1:A0] = 0:1] and A12 = 1 during WRITE command at T0 and T4.  
 NOTE 5. CA Parity = Enable, CS to CA Latency = Disable, Write DBI = Disable.  
 NOTE 6. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T21.

**Figure 148. Consecutive WRITE (BL8) with  $1t_{CK}$  Preamble and CA Parity in Different Bank Group**



NOTE 1. BL = 8/BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ ,  $t_{CCD\_SIL} = 5$   
 NOTE 2. Din n (or b) = data-in to column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T5.  
 NOTE 5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T5.  
 NOTE 6. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.  
 NOTE 7. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T18

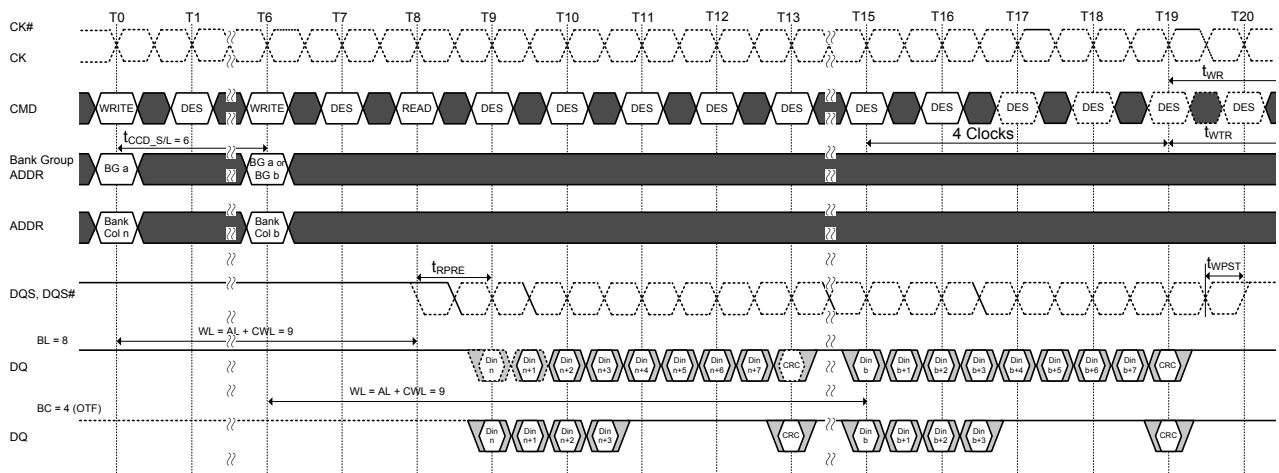
**Figure 149. Consecutive WRITE (BL8/BC4) OTF with  $1t_{CK}$  Preamble and Write CRC in Same or Different Bank Group**



NOTE 1. BL = 8, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ ,  $t_{CCD\_SIL} = 5$   
 NOTE 2. Din n (or b) = data-in to column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BC4 setting activated by MR0[A1:A0 = 1:0] at T0 and T5.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.  
 NOTE 6. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T16.

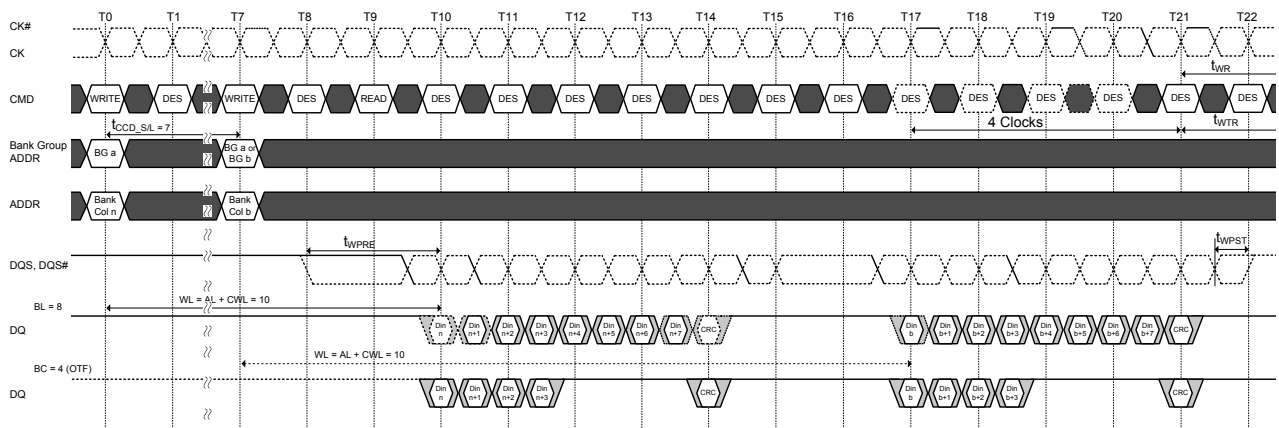
**Figure 150. Consecutive WRITE (BC4) Fixed with  $1t_{CK}$  Preamble and Write CRC in Same or Different Bank Group**





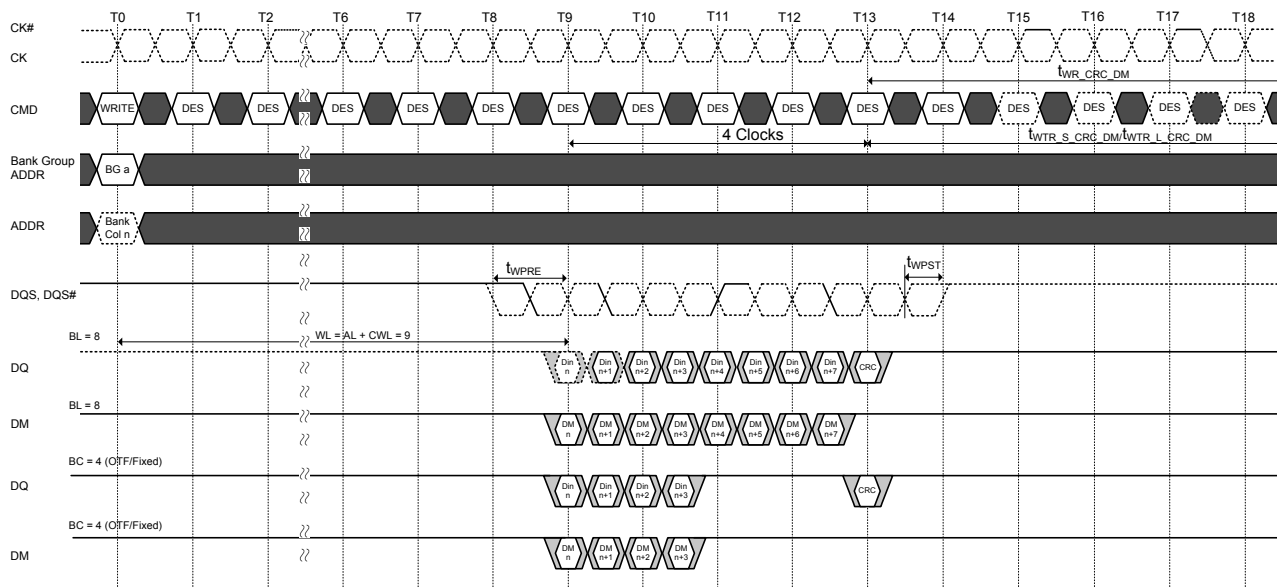
NOTE 1. BL = 8, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ ,  $t_{CCD\_SIL} = 6$   
 NOTE 2. Din n (or b) = data-in to column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MR0[A1A:0 = 0:0] or MR0[A1A:0 = 0:1] and A12 = 1 during WRITE command at T0 and T6.  
 NOTE 5. BC4 setting activated by MR0[A1A:0 = 0:1] and A12 = 0 during WRITE command at T0 and T6.  
 NOTE 6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.  
 NOTE 7. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T19.

**Figure 151. Nonconsecutive WRITE (BL8/BC4) OTF with  $1t_{CK}$  Preamble and Write CRC in Same or Different Bank Group**



NOTE 1. BL = 8, AL = 0, CWL = 9 + 1 = 10, Preamble =  $2t_{CK}$ ,  $t_{CCD\_SIL} = 7$   
 NOTE 2. Din n (or b) = data-in to column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MR0[A1A:0 = 0:0] or MR0[A1A:0 = 0:1] and A12 = 1 during WRITE command at T0 and T7.  
 NOTE 5. BC4 setting activated by MR0[A1A:0 = 0:1] and A12 = 0 during WRITE command at T0 and T7.  
 NOTE 6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.  
 NOTE 7.  $t_{CCD\_SIL} = 6$  isn't allowed in  $2t_{CK}$  preamble mode.  
 NOTE 8. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T21.  
 NOTE 9. When operating in  $2t_{CK}$  Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL Setting supported in the applicable  $t_{CK}$  range. That means CWL = 9 is not allowed when operating in  $2t_{CK}$  Write Preamble Mode.

**Figure 152. Nonconsecutive WRITE (BL8/BC4) OTF with  $2t_{CK}$  Preamble and Write CRC in Same or Different Bank Group**



■ TRANSITIONING DATA ■ DON'T CARE

NOTE 1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$   
NOTE 2. Din n = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.

NOTE 5. BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.

NOTE 6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable, DM = Enable.

NOTE 7. The write recovery time ( $t_{WR\_CRC\_DM}$ ) and write timing parameter ( $t_{WR\_S\_CRC\_DM}/t_{WR\_L\_CRC\_DM}$ ) are referenced from the first rising clock edge after the last write data shown at T13.

**Figure 153. WRITE (BL8/BC4) OTF/Fixed with  $1t_{CK}$  Preamble and Write CRC and DM in Same or Different Bank Group**

## Read and Write Command Interval

**Table 43. Minimum Read and Write Command Timings**

Bank Group	Access type	Timing Parameter	Note
Same	Minimum Read to Write	$CL - CWL + RBL / 2 + 1 t_{CK} + t_{WPRE}$	1,2
	Minimum Read after Write	$CWL + WBL / 2 + t_{WTR\_L}$	1,3
Different	Minimum Read to Write	$CL - CWL + RBL / 2 + 1 t_{CK} + t_{WPRE}$	1,2
	Minimum Read after Write	$CWL + WBL / 2 + t_{WTR\_S}$	1,3

Note 1. These timings require extended calibrations times  $t_{ZQinit}$  and  $t_{ZQCS}$ .

Note 2. RBL: Read burst length associated with Read command

RBL = 8 for fixed 8 and on-the-fly mode 8

RBL = 4 for fixed BC4 and on-the-fly mode BC4

Note 3. WBL: Write burst length associated with Write command

WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4

WBL = 4 for fixed BC4 only

## Write Timing Violations

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

### Motivation

Generally, if Write timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain violations as specified below, the DRAM is guaranteed to not “hang up” and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

### Data Setup and Hold Offset Violations

Should the data to strobe timing requirements ( $t_{DQS\_off}$ ,  $t_{DQH\_off}$ ,  $t_{DQS\_dd\_off}$ ,  $t_{DQH\_dd\_off}$ ) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory locations addressed with this write command.

In the example (Write Burst Operation WL = 9 (AL = 0, CWL = 9, BL8), the relevant strobe edges for write burst A are associated with the clock edges: T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5.

Subsequent reads from that location might results in unpredictable read data, however the DRAM will work properly otherwise.

### Strobe and Strobe to Clock Timing Violations

Should the strobe timing requirements ( $t_{DQSH}$ ,  $t_{DQSL}$ ,  $t_{WPRE}$ ,  $t_{WPST}$ ) or the strobe to clock timing requirements ( $t_{DSS}$ ,  $t_{DSH}$ ,  $t_{DQSS}$ ) be violated for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending Write command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise with the following constraints:

- 1) Both Write CRC and data burst OTF are disabled; timing specifications other than  $t_{DQSH}$ ,  $t_{DQSL}$ ,  $t_{WPRE}$ ,  $t_{WPST}$ ,  $t_{DSS}$ ,  $t_{DSH}$ ,  $t_{DQSS}$  are not violated.
- 2) The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the Write-Latency position.
- 3) A Read command following an offending Write command from any open bank is allowed.
- 4) One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued  $t_{CCD\_L}$  later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending writes. Reads from these Writes may provide incorrect data.
- 5) One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued  $t_{CCD\_S}$  later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending writes. Reads from these Writes may provide incorrect data.
- 6) Once one or more precharge commands(PRE or PREA) are issued to DDR4 after offending write command and all banks become precharged state(idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.

## Connectivity Test Mode

### Introduction

The DDR4 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR4 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for all x16 width devices independent of density.

Contrary to other conventional shift register based test mode, where test patterns are shifted in and out of the memory devices serially in each clock, DDR4's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR4 memory device at the same time, significantly enhancing the speed of the connectivity check. RESET# is registered to High and  $V_{REFCA}$  must be stable prior to entering CT mode. Once put in the CT mode, the DDR4 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity check test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, any ODT is turned off.

A reset of the DDR4 memory device is required after exiting the CT mode.

### Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the DDR4 memory device are classified as one of the following types:

- 1) Test Enable (TEN) pin: when asserted high, this pin causes the DDR4 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR4 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent; additionally, the DRAM will set the internal  $V_{REFDQ}$  to  $V_{DDQ} \times 0.5$  during CT mode (this is the only time the DRAM takes direct control over setting the internal  $V_{REFDQ}$ ). The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.
- 2) Chip Select (CS#) pin: when asserted low, this pin enables the test output pins in the DDR4 memory device. When de-asserted, the output pins in the DDR4 memory device will be tri-stated. The CS# pin in the DDR4 memory device serves as the CS# pin when in CT mode.
- 3) Test Input: a group of pins that are used during normal DDR4 DRAM operation are designated test input pins. These pins are used to enter the test pattern in CT mode.
- 4) Test Output: a group of pins that are used during normal DDR4 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.
- 5) RESET#: Fixed high level is required during CT mode same as normal function.

**Table 44. Pin Classification of DDR4 Memory Device in Connectivity Test (CT) Mode**

CT Mode Pins		Pin Names during Normal Memory Operation
Test Enable		TEN
Chip Select		CS#
Test Input	A	BA0-1, BG0, A0-A9, A10/AP, A12/BC#, A13, WE#/A14, CAS#/A15, RAS#/A16, CKE, ACT#, ODT, CK, CK#, PAR
	B	LDM#/LDBI#, UDM#/UDBI#
	C	ALERT#
	D	RESET#
Test Output		DQ0 – DQ15, LDQS, LDQS#, UDQS, UDQS#

**Table 45. TEN Pin Weak Pull Down Strength Range**

Symbol	Description	Min.	Max.	Unit
TEN	TEN pin should be internally pulled low to prevent DDR4 SDRAM from conducting Connectivity Test mode in case that TEN is not used.	0.05	10	$\mu$ A

Note 1. The host controller should use good enough strength when activating connectivity test mode to avoid current fighting at TEN signal and inability of connectivity test mode.

**Logic Equations --- Min Term Equations**

The test input and output pins are related by the following equations, where INV denotes a logical inversion operation and XOR a logical exclusive OR operation:

MT0 = XOR (A1, A6, PAR)  
MT1 = XOR (A8, ALERT#, A9)  
MT2 = XOR (A2, A5, A13)  
MT3 = XOR (A0, A7, A11)  
MT4 = XOR (CK#, ODT, CAS#/A15)  
MT5 = XOR (CKE, RAS#/A16, A10/AP)  
MT6 = XOR (ACT#, A4, BA1)  
MT7 = XOR (x16: UDM#/UDBI#, LDM#/LDBI#, CK)  
MT8 = XOR (WE#/A14, A12/BC#, BA0)  
MT9 = XOR (BG0, A3, RESET# and TEN)

**Output equations for x16 devices**

DQ0 = MT0  
DQ1 = MT1  
DQ2 = MT2  
DQ3 = MT3  
DQ4 = MT4  
DQ5 = MT5  
DQ6 = MT6  
DQ7 = MT7  
DQ8 = INV DQ0  
DQ9 = INV DQ1  
DQ10 = INV DQ2  
DQ11 = INV DQ3  
DQ12 = INV DQ4  
DQ13 = INV DQ5  
DQ14 = INV DQ6  
DQ15 = INV DQ7  
LDQS = MT8  
LDQS# = MT9  
UDQSU = INV LDQS  
UDQSU# = INV LDQS#

## Input level and Timing Requirement

During CT Mode, input levels are defined below.

TEN pin: CMOS rail-to-rail with DC high and low at 80% and 20% of  $V_{DD}$

CS#: Pseudo differential signal referring to  $V_{REFCA}$

Test Input pin A: Pseudo differential signal referring to  $V_{REFCA}$

Test Input pin B: Pseudo differential signal referring to internal  $V_{REF}$   $0.5 \times V_{DD}$

RESET#: CMOS DC high above 70 %  $V_{DD}$

ALERT#: Terminated to  $V_{DD}$ . Swing level is TBD

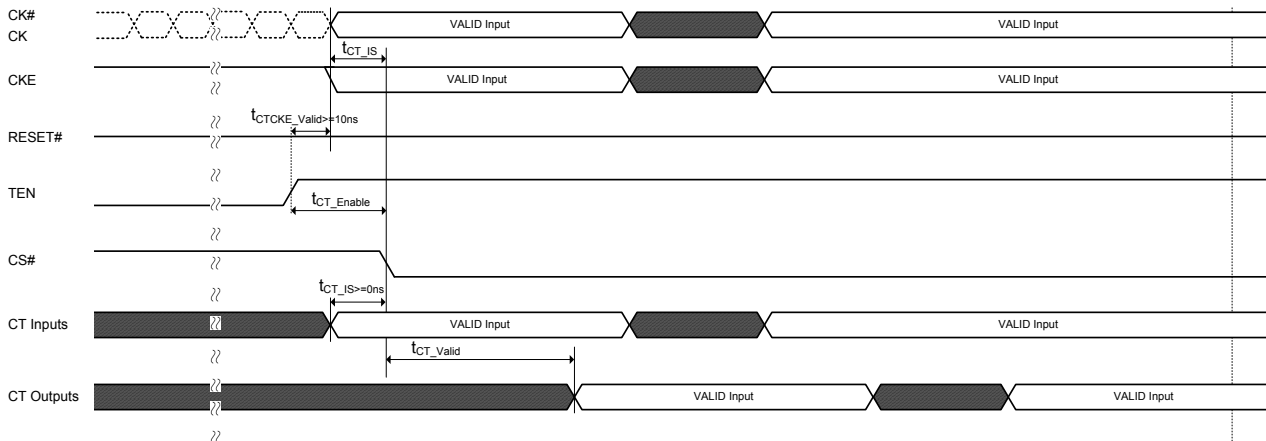
Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK and CK# signals will be ignored and the DDR4 memory device enter into the CT mode after  $t_{CT\_Enable}$ . In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on; once the DRAM is initialized and  $V_{REFDQ}$  is calibrated, CT Mode may no longer be used.

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR4 memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required.

All output signals at the test output pins will be stable within  $t_{CT\_Valid}$  after the test inputs have been applied to the test input pins with TEN input and CS# input maintained High and Low respectively.



**Figure 154. Timing Diagram for Connectivity Test(CT) Mode**

**Table 46. AC parameters for Connectivity Test (CT) Mode**

Symbol	Min.	Max.	Unit
$t_{CT\_IS}$	0	-	ns
$t_{CT\_Enable}$	200	-	ns
$t_{CT\_Valid}$	-	200	ns

## Connectivity Test ( CT ) Mode Input Levels

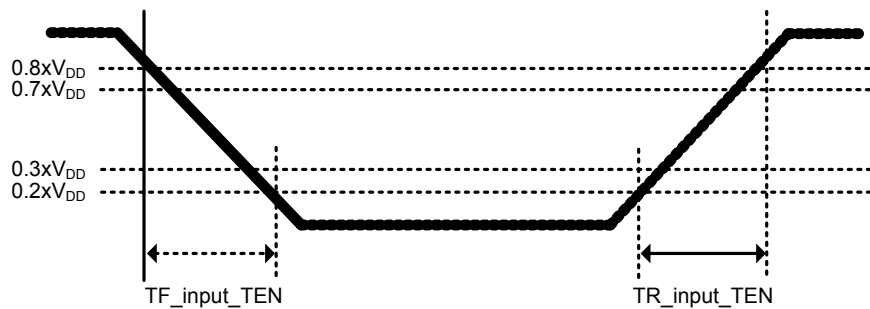
Following input parameters will be applied for DDR4 SDRAM Input Signal during Connectivity Test Mode.

**Table 47. CMOS rail to rail Input Levels for TEN**

Parameter	Symbol	Min.	Max.	Unit	Note
TEN AC Input High Voltage	$V_{IH(AC)\_TEN}$	$0.8 \times V_{DD}$	$V_{DD}$	V	1
TEN DC Input High Voltage	$V_{IH(DC)\_TEN}$	$0.7 \times V_{DD}$	$V_{DD}$	V	
TEN DC Input Low Voltage	$V_{IL(DC)\_TEN}$	$V_{SS}$	$0.3 \times V_{DD}$	V	
TEN AC Input Low Voltage	$V_{IL(AC)\_TEN}$	$V_{SS}$	$0.2 \times V_{DD}$	V	2
TEN Input signal Falling time	$T_{F\_input\_TEN}$	-	10	ns	
TEN Input signal Rising time	$T_{R\_input\_TEN}$	-	10	ns	

Note 1. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.

Note 2. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

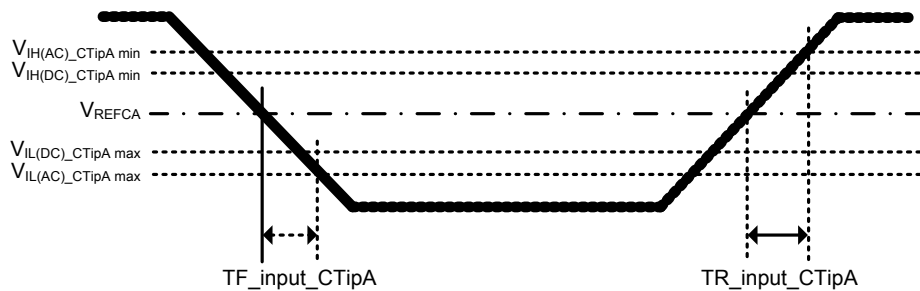


**Figure 155. TEN Input Slew Rate Definition**

**Table 48. Single-Ended AC and DC Input levels for CS#, BA0-1, BG0, A0-A9, A10/AP, A12/BC#, A13, WE#/A14, CAS#/A15, RAS#/A16, CKE, ACT#, ODT, CK, CK# and PAR**

Parameter	Symbol	Min.	Max.	Unit	Note
CTipA AC Input High Voltage	$V_{IH(AC)\_CTipA}$	$V_{REFCA} + 0.2$	-	V	1
CTipA DC Input High Voltage	$V_{IH(DC)\_CTipA}$	$V_{REFCA} + 0.15$	$V_{DD}$	V	
CTipA DC Input Low Voltage	$V_{IL(DC)\_CTipA}$	$V_{SS}$	$V_{REFCA} - 0.15$	V	
CTipA AC Input Low Voltage	$V_{IL(AC)\_CTipA}$	-	$V_{REFCA} - 0.2$	V	1
CTipA Input signal Falling time	$T_{F\_input\_CTipA}$	-	5	ns	
CTipA Input signal Rising time	$T_{R\_input\_CTipA}$	-	5	ns	

Note 1. See "Overshoot and Undershoot Specifications".



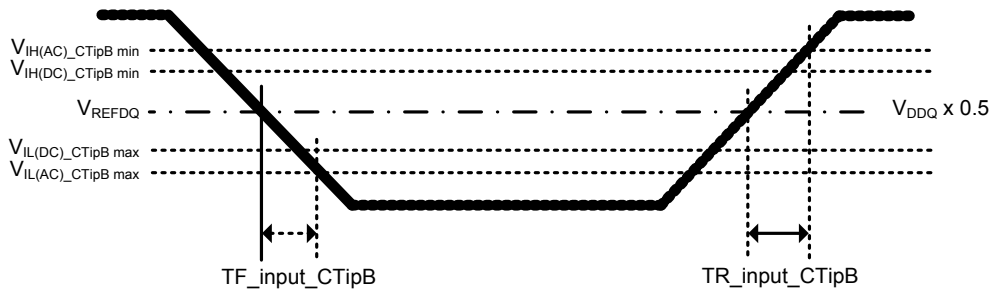
**Figure 156. CS# and Input A Slew Rate Definition**

**Table 49. Single-Ended AC and DC Input levels for LDM#/LDBI#, UDM#/UDBIU#**

Parameter	Symbol	Min.	Max.	Unit	Note
CTipB AC Input High Voltage	$V_{IH(AC)\_CTipB}$	$V_{REFDQ} + 0.3$	-	V	2
CTipB DC Input High Voltage	$V_{IH(DC)\_CTipB}$	$V_{REFDQ} + 0.2$	$V_{DDQ}$	V	
CTipB DC Input Low Voltage	$V_{IL(DC)\_CTipB}$	$V_{SSQ}$	$V_{REFDQ} - 0.2$	V	
CTipB AC Input Low Voltage	$V_{IL(AC)\_CTipB}$	-	$V_{REFCA} - 0.3$	V	2
CTipB Input signal Falling time	$T_{F\_input\_CTipB}$	-	5	ns	
CTipB Input signal Rising time	$T_{R\_input\_CTipB}$	-	5	ns	

Note 1.  $V_{REFDQ}$  is  $V_{DDQ} \times 0.5$

Note 2. See "Overshoot and Undershoot Specifications".



**Figure 157. Input B Slew Rate Definition**

### Input Levels for RESET#

RESET# input condition is the same as normal operation.

### Input Levels for ALERT#

TBD



## CRC Polynomial and logic equation

The CRC polynomial used by DDR4 is the ATM-8 HEC,  $X^8+X^2+X+1$ .

A combinatorial logic block implementation of this 8-bit CRC for 72-bits of data contains 272 two-input XOR gates contained in eight 6 XOR gate deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

The error coverage from the DDR4 polynomial used is shown in the following table.

**Table 50. CRC Error Detection Coverage**

Error Type	Detection Capability
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random one Multi-bit UI vertical column error detection excluding DBI bits	100%

## CRC Combinatorial Logic Equations

```

module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
//initial condition all 0 implied
// "^" = XOR
function [7:0]
nextCRC8_D72;
input [71:0] Data;
input [71:0] D;
reg [7:0] CRC;
begin
D = Data;

NewCRC[0] =
D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^
D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;

NewCRC[1] =
D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^
D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];

NewCRC[2] =
D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^
D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];

NewCRC[3] =
D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^
D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];

NewCRC[4] =
D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];

NewCRC[5] =
D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];

NewCRC[6] =
D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];

NewCRC[7] =
D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D72 = NewCRC;

```

## Write CRC for x4, x8 and x16 devices

The Controller generates the CRC checksum and forms the write data frames as below tables.

For a x8 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the DBI# lane if DBI function is enabled.

For a x16 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the LDBI# and UDBI# lanes if DBI function is enabled.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the ALERT# signal if there is a mis-match.

A x8 device has a CRC tree with 72 input bits. The upper 8 bits are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled then the inputs of the upper 8 bits D[71:64] are '1's.

A x16 device has two identical CRC trees with 72 input bits each. The upper 8 bits are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled then the inputs of the upper 8 bits [D(143:136) and D(71:64)] are '1's.

A x4 device has a CRC tree with 32 input bits. The input for the upper 40 bits D[71:32] are '1's.

DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

**Table 51. CRC Data Mapping for x4 Devices, BL8**

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	CRC4
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	CRC5
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	CRC6
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	CRC7

**Table 52. CRC Data Mapping for x8 Devices, BL8**

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
DM#/DBI#	D64	D65	D66	D67	D68	D69	D70	D71	1	1

A x16 device is treated as two x8 devices; a x16 device will have two identical CRC trees implemented. CRC[7:0] covers data bits D[71:0], and CRC[15:8] covers data bits D[143:72].

**Table 53. CRC Data Mapping for x16 Devices, BL8**

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
LDM#/LDBI#	D64	D65	D66	D67	D68	D69	D70	D71	1	1
DQ8	D72	D73	D74	D75	D76	D77	D78	D79	CRC8	1
DQ9	D80	D81	D82	D83	D84	D85	D86	D87	CRC9	1
DQ10	D88	D89	D90	D91	D92	D93	D94	D95	CRC10	1
DQ11	D96	D97	D98	D99	D100	D101	D102	D103	CRC11	1
DQ12	D104	D105	D106	D107	D108	D109	D110	D111	CRC12	1
DQ13	D112	D113	D114	D115	D116	D117	D118	D119	CRC13	1
DQ14	D120	D121	D122	D123	D124	D125	D126	D127	CRC14	1
DQ15	D128	D129	D130	D131	D132	D133	D134	D135	CRC15	1
UDM#/UDBI#	D136	D137	D138	D139	D140	D141	D142	D143	1	1

## CRC Error Handling

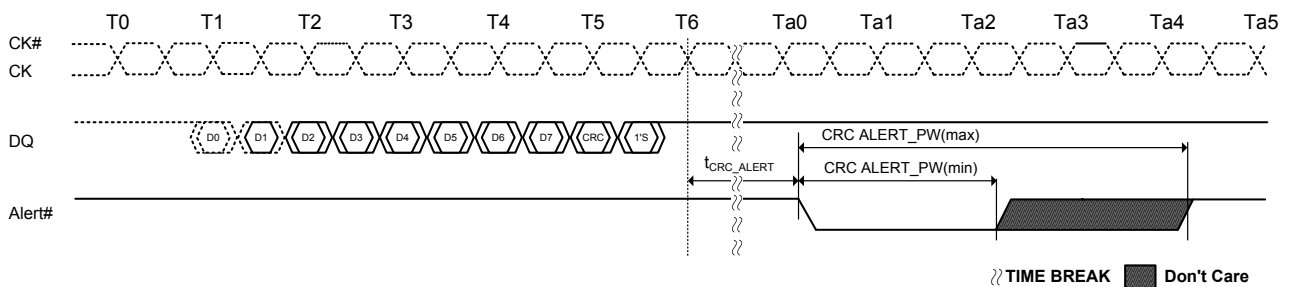
CRC Error mechanism shares the same ALERT# signal for reporting errors on writes to DRAM. The controller has no way to distinguish between CRC errors and Command/Address/Parity errors other than to read the DRAM mode registers. This is a very time consuming process in a multi-rank configuration.

To speed up recovery for CRC errors, CRC errors are only sent back as a pulse. The minimum pulse-width is six clocks. The latency to ALERT# signal is defined as  $t_{\text{CRC\_ALERT}}$  in the figure below.

DRAM will set CRC Error Clear bit in A3 of MR5 to '1' and CRC Error Status bit in MPR3 of page1 to '1' upon detecting a CRC error. The CRC Error Clear bit remains set at '1' until the host clears it explicitly using an MRS command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst case delay for ALERT# (during init) and can back up the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than six clocks at the controller if there are multiple CRC errors as the ALERT# is a daisy chain bus.



NOTE 1. CRC ALERT\_PW IS Specified from the point Where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.

**Figure 158. CRC Error Reporting**

**Table 54. CRC Error Timing Parameters**

Symbol	Parameter	Min.	Max.	Unit
$t_{\text{CRC\_ALERT}}$	CRC error to ALERT# Latency	-	13	ns
CRC ALERT_PW	CRC ALERT_PW	6	10	tck

## CRC Frame Format with BC4

DDR4 SDRAM supports CRC function for Write operation for Burst Chop 4 (BC4). The CRC function is programmable using DRAM mode register and can be enabled for writes.

When CRC is enabled the data frame length is fixed at 10UI for both BL8 and BC4 operations. DDR4 SDRAM also supports burst length on the fly with CRC enabled. This is enabled using mode register.

## CRC with BC4 Data Bit Mapping

For a x4 device, the CRC tree inputs are 16 data bits, and the inputs for the remaining bits are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs to D[11:8], and so forth, for the CRC tree.

**Table 55. CRC Data Mapping for x4 Devices, BC4**

Function	Transfer (A2 = 0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	CRC4
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	CRC5
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	CRC6
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	CRC7
Function	Transfer (A2 = 1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	CRC4
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	CRC5
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	CRC6
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	CRC7

For a x8 device, the CRC tree inputs are 36 data bits in transfer's four through seven as 1's.

When A2 = 0, the input bits D[67:64]) are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[67:64]) are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs to D[11:8], and so forth, for the CRC tree. The input bits D[71:68]) are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[71:68]) are 1.

**Table 56. CRC Data Mapping for x8 Devices, BC4**

Function	Transfer (A2 = 0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
DM#/DBI#	D64	D65	D66	D67	1	1	1	1	1	1
Function	Transfer (A2 = 1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
DM#/DBI#	D68	D69	D70	D71	1	1	1	1	1	1

There are two identical CRC trees for x16 devices, each have CRC tree inputs of 36 bits.

When A2 = 0, input bits D[67:64] are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[67:64] are 1s. The input bits D[139:136] are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[139:136] are 1s.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs for D[11:8], and so forth, for the CRC tree. Input bits D[71:68] are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[71:68] are 1s. The input bits D[143:140] are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[143:140] are 1s.

**Table 57. CRC Data Mapping for x16 Devices, BC4**

Function	Transfer (A2 = 0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
LDM#/LDBI#	D64	D65	D66	D67	1	1	1	1	1	1
DQ8	D72	D73	D74	D75	1	1	1	1	CRC8	1
DQ9	D80	D81	D82	D83	1	1	1	1	CRC9	1
DQ10	D88	D89	D90	D91	1	1	1	1	CRC10	1
DQ11	D96	D97	D98	D99	1	1	1	1	CRC11	1
DQ12	D104	D105	D106	D107	1	1	1	1	CRC12	1
DQ13	D112	D113	D114	D115	1	1	1	1	CRC13	1
DQ14	D120	D121	D122	D123	1	1	1	1	CRC14	1
DQ15	D128	D129	D130	D131	1	1	1	1	CRC15	1
UDM#/UDBI#	D136	D137	D138	D139	1	1	1	1	1	1
Function	Transfer (A2 = 1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
LDM#/LDBI#	D68	D69	D70	D71	1	1	1	1	1	1
DQ8	D76	D77	D78	D79	1	1	1	1	CRC8	1
DQ9	D84	D85	D86	D87	1	1	1	1	CRC9	1
DQ10	D92	D93	D94	D95	1	1	1	1	CRC10	1
DQ11	D100	D101	D102	D103	1	1	1	1	CRC11	1
DQ12	D108	D109	D110	D111	1	1	1	1	CRC12	1
DQ13	D116	D117	D118	D119	1	1	1	1	CRC13	1
DQ14	D124	D125	D126	D127	1	1	1	1	CRC14	1
DQ15	D132	D133	D134	D135	1	1	1	1	CRC15	1
UDM#/UDBI#	D140	D141	D142	D143	1	1	1	1	1	1

Example shown below of CRC tree when X8 is used in BC4 mode, x4 and x16 have similar differences.

**CRC equations for x8 device in BC4 mode with A2=0 are as follows:**

$$\begin{aligned}
 \text{CRC}[0] &= D[69]=1 \wedge D[68]=1 \wedge D[67] \wedge D[66] \wedge D[64] \wedge D[63]=1 \wedge D[60]=1 \wedge D[56] \wedge D[54]=1 \wedge D[53]=1 \wedge D[52]=1 \wedge D[50] \wedge \\
 &D[49] \wedge D[48] \wedge D[45]=1 \wedge D[43] \wedge D[40] \wedge D[39]=1 \wedge D[35] \wedge D[34] \wedge D[31]=1 \wedge D[30]=1 \wedge D[28]=1 \wedge D[23]=1 \wedge \\
 &D[21]=1 \wedge D[19] \wedge D[18] \wedge D[16] \wedge D[14]=1 \wedge D[12]=1 \wedge D[8] \wedge D[7]=1 \wedge D[6] =1 \wedge D[0] ; \\
 \text{CRC}[1] &= D[70]=1 \wedge D[66] \wedge D[65] \wedge D[63]=1 \wedge D[61]=1 \wedge D[60]=1 \wedge D[57] \wedge D[56] \wedge D[55]=1 \wedge D[52]=1 \wedge D[51] \wedge D[48] \wedge \\
 &D[46]=1 \wedge D[45]=1 \wedge D[44]=1 \wedge D[43] \wedge D[41] \wedge D[39]=1 \wedge D[36]=1 \wedge D[34] \wedge D[32] \wedge D[30]=1 \wedge D[29]=1 \wedge D[28]=1 \\
 &\wedge D[24] \wedge D[23]=1 \wedge D[22]=1 \wedge D[21]=1 \wedge D[20]=1 \wedge D[18] \wedge D[17] \wedge D[16] \wedge D[15]=1 \wedge D[14]=1 \wedge D[13]=1 \wedge \\
 &D[12]=1 \wedge D[9] \wedge D[6]=1 \wedge D[1] \wedge D[0]; \\
 \text{CRC}[2] &= D[71]=1 \wedge D[69]=1 \wedge D[68]=1 \wedge D[63]=1 \wedge D[62]=1 \wedge D[61]=1 \wedge D[60]=1 \wedge D[58] \wedge D[57] \wedge D[54]=1 \wedge D[50] \wedge D[48] \\
 &\wedge D[47]=1 \wedge D[46]=1 \wedge D[44]=1 \wedge D[43] \wedge D[42] \wedge D[39]=1 \wedge D[37]=1 \wedge D[34] \wedge D[33] \wedge D[29]=1 \wedge D[28]=1 \wedge D[25] \wedge \\
 &D[24] \wedge D[22]=1 \wedge D[17] \wedge D[15]=1 \wedge D[13]=1 \wedge D[12]=1 \wedge D[10] \wedge D[8] \wedge D[6]=1 \wedge D[2] \wedge D[1] \wedge D[0]; \\
 \text{CRC}[3] &= D[70]=1 \wedge D[69]=1 \wedge D[64] \wedge D[63]=1 \wedge D[62]=1 \wedge D[61]=1 \wedge D[59] \wedge D[58] \wedge D[55]=1 \wedge D[51] \wedge D[49] \wedge D[48] \wedge \\
 &D[47]=1 \wedge D[45]=1 \wedge D[44]=1 \wedge D[43] \wedge D[40] \wedge D[38]=1 \wedge D[35] \wedge D[34] \wedge D[30]=1 \wedge D[29]=1 \wedge D[26] \wedge D[25] \wedge \\
 &D[23]=1 \wedge D[18] \wedge D[16] \wedge D[14]=1 \wedge D[13]=1 \wedge D[11] \wedge D[9] \wedge D[7]=1 \wedge D[3] \wedge D[2] \wedge D[1]; \\
 \text{CRC}[4] &= D[71]=1 \wedge D[70]=1 \wedge D[65] \wedge D[64] \wedge D[63]=1 \wedge D[62]=1 \wedge D[60]=1 \wedge D[59] \wedge D[56] \wedge D[52]=1 \wedge D[50] \wedge D[49] \wedge \\
 &D[48] \wedge D[46]=1 \wedge D[45]=1 \wedge D[44]=1 \wedge D[41] \wedge D[39]=1 \wedge D[36]=1 \wedge D[35] \wedge D[31]=1 \wedge D[30]=1 \wedge D[27] \wedge D[26] \wedge \\
 &D[24] \wedge D[19] \wedge D[17] \wedge D[15]=1 \wedge D[14]=1 \wedge D[12]=1 \wedge D[10] \wedge D[8] \wedge D[4]=1 \wedge D[3] \wedge D[2]; \\
 \text{CRC}[5] &= D[71]=1 \wedge D[66] \wedge D[65] \wedge D[64] \wedge D[63]=1 \wedge D[61]=1 \wedge D[60]=1 \wedge D[57] \wedge D[53]=1 \wedge D[51] \wedge D[50] \wedge D[49] \wedge \\
 &D[47]=1 \wedge D[46]=1 \wedge D[45]=1 \wedge D[42] \wedge D[40] \wedge D[37]=1 \wedge D[36]=1 \wedge D[32] \wedge D[31]=1 \wedge D[28]=1 \wedge D[27] \wedge D[25] \wedge \\
 &D[20]=1 \wedge D[18] \wedge D[16] \wedge D[15]=1 \wedge D[13]=1 \wedge D[11] \wedge D[9] \wedge D[5]=1 \wedge D[4]=1 \wedge D[3]; \\
 \text{CRC}[6] &= D[67] \wedge D[66] \wedge D[65] \wedge D[64] \wedge D[62]=1 \wedge D[61]=1 \wedge D[58] \wedge D[54]=1 \wedge D[52]=1 \wedge D[51] \wedge D[50] \wedge D[48] \wedge D[47]=1 \\
 &\wedge D[46]=1 \wedge D[43] \wedge D[41] \wedge D[38]=1 \wedge D[37]=1 \wedge D[33] \wedge D[32] \wedge D[29]=1 \wedge D[28]=1 \wedge D[26] \wedge D[21]=1 \wedge D[19] \wedge \\
 &D[17] \wedge D[16] \wedge D[14]=1 \wedge D[12]=1 \wedge D[10] \wedge D[6]=1 \wedge D[5]=1 \wedge D[4]=1; \\
 \text{CRC}[7] &= D[68]=1 \wedge D[67] \wedge D[66] \wedge D[65] \wedge D[63]=1 \wedge D[62]=1 \wedge D[59] \wedge D[55]=1 \wedge D[53]=1 \wedge D[52]=1 \wedge D[51] \wedge D[49] \wedge \\
 &D[48] \wedge D[47]=1 \wedge D[44]=1 \wedge D[42] \wedge D[39]=1 \wedge D[38]=1 \wedge D[34] \wedge D[33] \wedge D[30]=1 \wedge D[29]=1 \wedge D[27] \wedge D[22]=1 \wedge \\
 &D[20]=1 \wedge D[18] \wedge D[17] \wedge D[15] =1 \wedge D[13]=1 \wedge D[11] \wedge D[7]=1 \wedge D[6]=1 \wedge D[5]=1;
 \end{aligned}$$

**CRC equations for x8 device in BC4 mode with A2=1 are as follows:**

$$\begin{aligned}
 \text{CRC}[0] &= 1 \wedge 1 \wedge D[71] \wedge D[70] \wedge D[68] \wedge 1 \wedge 1 \wedge D[60] \wedge 1 \wedge 1 \wedge 1 \wedge D[54] \wedge D[53] \wedge D[52] \wedge 1 \wedge D[47] \wedge D[44] \wedge 1 \wedge D[39] \wedge \\
 &D[38] \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[23] \wedge D[22] \wedge D[20] \wedge 1 \wedge 1 \wedge 1 \wedge D[12] \wedge 1 \wedge 1 \wedge 1 \wedge D[4] ; \\
 \text{CRC}[1] &= 1 \wedge D[70] \wedge D[69] \wedge 1 \wedge 1 \wedge 1 \wedge D[61] \wedge D[60] \wedge 1 \wedge 1 \wedge D[55] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge D[47] \wedge D[45] \wedge 1 \wedge 1 \wedge D[38] \wedge \\
 &D[36] \wedge 1 \wedge 1 \wedge 1 \wedge D[28] \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[22] \wedge D[21] \wedge D[20] \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[13] \wedge 1 \wedge D[5] \wedge D[4]; \\
 \text{CRC}[2] &= 1 \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[62] \wedge D[61] \wedge 1 \wedge D[54] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[47] \wedge D[46] \wedge 1 \wedge 1 \wedge D[38] \wedge D[37] \wedge 1 \wedge 1 \wedge \\
 &\wedge D[29] \wedge D[28] \wedge 1 \wedge D[21] \wedge 1 \wedge 1 \wedge 1 \wedge D[14] \wedge D[12] \wedge 1 \wedge D[6] \wedge D[5] \wedge D[4]; \\
 \text{CRC}[3] &= 1 \wedge 1 \wedge D[68] \wedge 1 \wedge 1 \wedge 1 \wedge D[63] \wedge D[62] \wedge 1 \wedge D[55] \wedge D[53] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[47] \wedge D[44] \wedge 1 \wedge D[39] \wedge D[38] \wedge \\
 &1 \wedge 1 \wedge D[30] \wedge D[29] \wedge 1 \wedge D[22] \wedge D[20] \wedge 1 \wedge 1 \wedge D[15] \wedge D[13] \wedge 1 \wedge D[7] \wedge D[6] \wedge D[5]; \\
 \text{CRC}[4] &= 1 \wedge 1 \wedge D[69] \wedge D[68] \wedge 1 \wedge 1 \wedge 1 \wedge D[63] \wedge D[60] \wedge 1 \wedge D[54] \wedge D[53] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge D[45] \wedge 1 \wedge 1 \wedge D[39] \wedge 1 \wedge 1 \wedge \\
 &\wedge D[31] \wedge D[30] \wedge D[28] \wedge D[23] \wedge D[21] \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[14] \wedge D[12] \wedge 1 \wedge D[7] \wedge D[6]; \\
 \text{CRC}[5] &= 1 \wedge D[70] \wedge D[69] \wedge D[68] \wedge 1 \wedge 1 \wedge 1 \wedge D[61] \wedge D[55] \wedge D[54] \wedge D[53] \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[46] \wedge D[44] \wedge 1 \wedge 1 \wedge D[36] \wedge \\
 &1 \wedge 1 \wedge D[31] \wedge D[29] \wedge 1 \wedge D[22] \wedge D[20] \wedge 1 \wedge 1 \wedge D[15] \wedge D[13] \wedge 1 \wedge 1 \wedge D[7]; \\
 \text{CRC}[6] &= D[71] \wedge D[70] \wedge D[69] \wedge D[68] \wedge 1 \wedge 1 \wedge D[62] \wedge 1 \wedge 1 \wedge D[55] \wedge D[54] \wedge D[52] \wedge 1 \wedge 1 \wedge D[47] \wedge D[45] \wedge 1 \wedge 1 \wedge D[37] \wedge \\
 &D[36] \wedge 1 \wedge 1 \wedge D[30] \wedge 1 \wedge D[23] \wedge D[21] \wedge D[20] \wedge 1 \wedge 1 \wedge D[14] \wedge 1 \wedge 1 \wedge 1; \\
 \text{CRC}[7] &= 1 \wedge D[71] \wedge D[70] \wedge D[69] \wedge 1 \wedge 1 \wedge D[63] \wedge 1 \wedge 1 \wedge 1 \wedge D[55] \wedge D[53] \wedge D[52] \wedge 1 \wedge 1 \wedge D[46] \wedge 1 \wedge 1 \wedge D[38] \wedge D[37] \wedge \\
 &1 \wedge 1 \wedge D[31] \wedge 1 \wedge 1 \wedge D[22] \wedge D[21] \wedge 1 \wedge 1 \wedge D[15] \wedge 1 \wedge 1 \wedge 1;
 \end{aligned}$$

### Simultaneous DM and CRC Functionality

When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the write operation and discards the data. For a x16, when the DRAM detects an error in CRC tree, DDR4 DRAMs may mask all DQs or half the DQs depending upon the specific vendor implementation behavior. Both implementations are valid. For the DDR4 DRAMs that masking half the DQs, DQ0 through DQ7 will be masked if the lower byte CRC tree had the error and DQ8 through DQ15 will be masked if the upper byte CRC tree had the error.

### Simultaneous MPR Write, Per DRAM Addressability and CRC Functionality

The following combination of DDR4 features are prohibited for simultaneous operation:

- 1) MPR Write and Write CRC (Note: MPR Write is via Address pins)
- 2) Per DRAM Addressability and Write CRC (Note: Only MRS are allowed during PDA and also DQ0 is used for PDA detection)

## Post Package Repair (hPPR)

DDR4 supports Fail Row address repair as optional feature for 4Gb. Supporting hPPR is identified via datasheet and SPD in Module so should refer to DRAM manufacturer's Datasheet. PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With hPPR, DDR4 can correct 1Row per Bank Group

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended hPPR mode entry and repair. (i.e. Command/Address training period)

DDR4 defines two hard fail row address repair sequences and users can choose to use among those 2 command sequences. The first command sequence uses a WRA command and ensures data retention with Refresh operations except for the 2banks containing the rows being repaired, with BA[0] a don't care. Second command sequence is to use WR command and Refresh operation can't be performed in the sequence. So, the second command sequence doesn't ensure data retention for target DRAM.

When hard PPR Mode is supported, entry into hPPR Mode is to be is protected through a sequential MRS guard key to prevent unintentional hPPR programming. When soft PPR Mode, i.e. sPPR, is supported, entry into sPPR Mode is to be protected through a sequential MRS guard key to prevent unintentional sPPR programming. The sequential MRS guard key for hPPR mode and sPPR is the same Guard Key, i.e. hPPR/sPPR Guard Key.

The hPPR/sPPR Guard Key requires a sequence of four MR0 commands to be executed immediately after entering hPPR mode (setting MR4 bit 13 to a "1") or immediately after entering sPPR mode (setting MR4 bit 5 to a "1"). The hPPR/sPPR Guard Key's sequence must be entered in the specified order as stated and shown in the spec below. Any interruption of the hPPR/sPPR Guard Key sequence from other MR commands or non-MR commands such as ACT, WR, RD, PRE, REF, ZQ, NOP, RFU is not allowed. Although interruption of the hPPR/sPPR Guard Key entry is not allowed, if the hPPR/sPPR Guard Key is not entering in the required order or is interrupted by other commands, the hPPR Mode or sPPR Mode will not execute and the offending command terminating hPPR/sPPR Mode may or may not execute correctly; however, the offending command will not cause the DRAM to "lock up". Additionally, when the hPPR or sPPR entry sequence is interrupted, subsequent ACT and WR commands will be conducted as normal DRAM commands. If a hPPR operation was prematurely terminated, the MR4 bit 13 must be re-set "0" prior to performing another hPPR or sPPR operation. If a sPPR operation was prematurely terminated, the MR4 bit 5 must be re-set to "0" prior to performing another sPPR or hPPR operation. The DRAM does not provide an error indication if an incorrect hPPR/sPPR Guard Key sequence is entered.

**Table 58. hPPR and sPPR MR0 Guard Key Sequences**

Guard Keys	BG1:0 <sup>(1)</sup>	BA1:0	A16:A12	A11	A10	A9	A8	A7	A6:A0
1 <sup>st</sup> MR0	00	00	X	1	1	0	0	1	1111111
2 <sup>nd</sup> MR0	00	00	X	0	1	1	1	1	1111111
3 <sup>rd</sup> MR0	00	00	X	1	0	1	1	1	1111111
4 <sup>th</sup> MR0	00	00	X	0	0	1	1	1	1111111

Note 1. BG1 is 'Don't Care' in x16

Note 2. A6:A0 can be either '1111111' or 'Don't Care'. And, it depends on vendor's implementation. '1111111' is allowed in all DDR4 density but 'Don't Care' in A6:A0 is only allowed in 4Gb die DDR4 product.

Note 3. After completing hPPR and sPPR mode, MR0 must be re-programmed to pre-PPR mode state if the DRAM is to be accessed.



### Hard Fail Row Address Repair (WRA Case)

The following is procedure of hPPR with WRA command.

1. Before entering 'hPPR' mode, All banks must be Precharged; DBI and CRC Modes must be disabled.
2. Enable hPPR using MR4 bit "A13=1" and wait  $t_{MOD}$ .
3. Issue guard Key as four consecutive MR0 commands each with a unique address field A[17:0]. Each MR0 command should space by  $t_{MOD}$ .
4. Issue ACT command with Fail Row address.
5. After  $t_{RCD}$ , Issue WRA with Valid address. DRAM will consider Valid address with WRA command as 'Don't Care'.
6. After WL (WL = CWL + AL + PL), All DQs of target DRAM should be low for  $4t_{CK}$ . If high is driven to All DQs of a DRAM consecutively for equal to or longer than  $2t_{CK}$ , then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither low for  $4t_{CK}$  nor high for equal to or longer than  $2t_{CK}$ , then hPPR mode execution is unknown.
7. Wait  $t_{PGM}$  to allow DRAM repair target Row Address internally and issue PRE.
8. Wait  $t_{PGM\_Exit}$  after PRE which allow DRAM to recognize repaired Row address.
9. Exit hPPR with setting MR4 bit "A13=0".
10. DDR4 will accept any valid command after  $t_{PGMPST}$ .
11. In more than one fail address repair case, Repeat step 2 to 9.

In addition to that, hPPR mode allows REF commands from PL + WL + BL/2 +  $t_{WR}$  +  $t_{RP}$  after WRA command during  $t_{PGM}$  and  $t_{PGMPST}$  for proper repair; provided multiple REF commands are issued at a rate of  $t_{REFI}$  or  $t_{REFI}/2$ , however back-to-back REF commands must be separated by at least  $t_{REFI}/4$  when the DRAM is in hPPR mode. Upon receiving REF command, DRAM performs normal Refresh operation and ensure data retention with Refresh operations except for the 2banks containing the rows being repaired, with BA[0] don't care. Other command except REF during  $t_{PGM}$  can cause incomplete repair so no other command except REF is allowed during  $t_{PGM}$ . Once hPPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after hPPR exit with MR4 [A13=0] and  $t_{PGMPST}$ .

### Hard Fail Row Address Repair (WR Case)

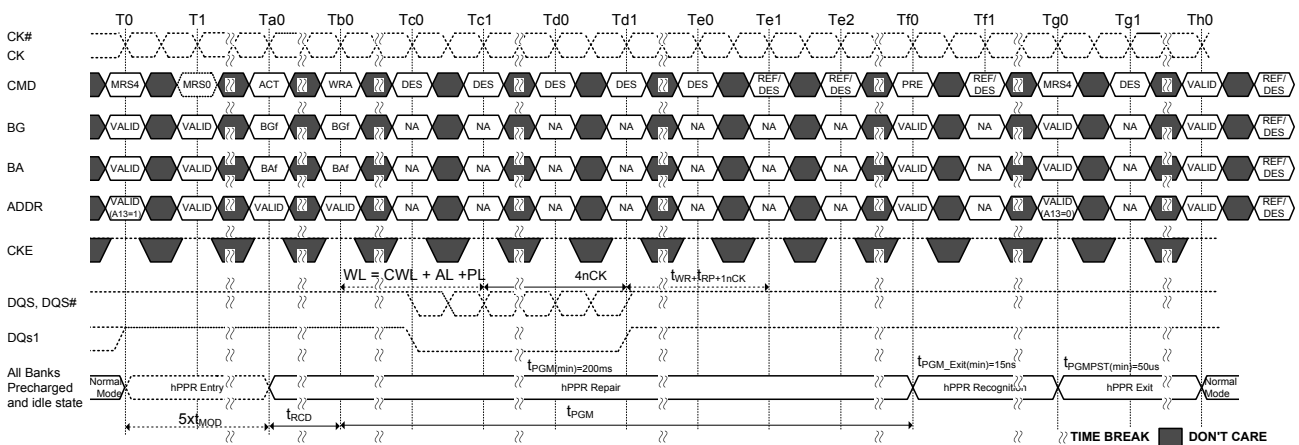
The following is procedure of hPPR PPR with WR command.

1. Before entering hPPR mode, all banks must be precharged; DBI and CRC modes must be disabled.
2. Enable hPPR using MR4 bit "A13=1" and wait  $t_{MOD}$ .
3. Issue guard Key as four consecutive MR0 commands each with a unique address field A [17:0]. Each MR0 command should space by  $t_{MOD}$ .
4. Issue ACT command with row address.
5. After  $t_{RCD}$ , issue WR with valid address. DRAM consider the valid address with WR command as 'Don't Care'.
6. After WL (WL = CWL + AL + PL), All DQs of target DRAM should be low for  $4t_{CK}$ . If high is driven to All DQs of a DRAM consecutively for equal to or longer than first  $2t_{CK}$ , then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither low for  $4t_{CK}$  nor high for equal to or longer than first  $2t_{CK}$ , then hPPR mode execution is unknown.
7. Wait  $t_{PGM}$  to allow DRAM repair target Row Address internally and issue PRE.
8. Wait  $t_{PGM\_Exit}$  after PRE which allow DRAM to recognize repaired Row address.
9. Exit hPPR with setting MR4 bit "A13=0".
10. DDR4 will accept any valid command after  $t_{PGMPST}$ .
11. In more than one fail address repair case, Repeat step 2 to 10.

In this sequence, Refresh command is not allowed between hPPR MRS entry and exit.

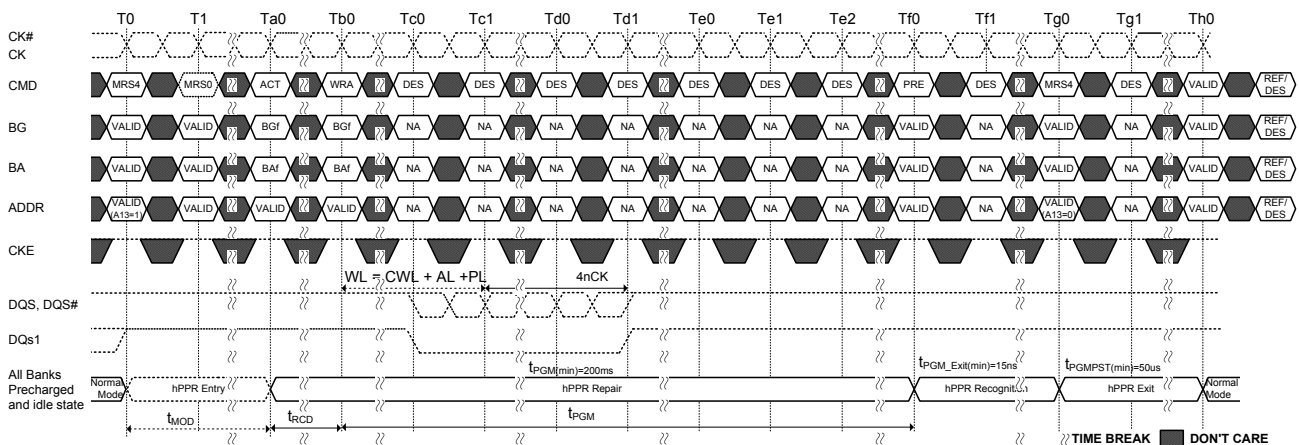
Once hPPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after hPPR exit with MR4 [A13=0] and  $t_{PGMPST}$ .





NOTE 1. Allow REF(1X) from PL+WL+BL/2+t<sub>WR</sub>+t<sub>rep</sub> after WR  
 NOTE 2. Timing diagram shows possible commands but not all shown can be issued at same time; for example if REF is issued at Te1, DES must be issued at Te2 as REF would be illegal at Te2. Likewise, DES must be issued t<sub>REFC</sub> prior to PRE at Tf0. All regular timings must still be satisfied.

**Figure 159. Hard Fail Row Repair (WRA Case)**



**Figure 160. Hard Fail Row Repair (WR Case)**

### Programming hPPR and sPPR support in MPR0 page2

hPPR and sPPR is optional feature of DDR4 4Gb so Host can recognize if DRAM is supporting hPPR and sPPR or not by reading out MPR0 Page2.

MPR page2;

hard PPR is supported: [7] = 1

hard PPR is not supported: [7] = 0

soft PPR is supported: [6] = 1

soft PPR is not supported: [6] = 0

### Required Timing Parameters

Repair requires additional time period to repair Hard Fail Row Address into spare Row address and the followings are requirement timing parameters for hPPR.

**Table 59. hPPR Timing Parameters**

Symbol	Parameter	Min.	Max.	Unit
t <sub>PGM</sub>	hPPR Programming Time	2000	-	ms
t <sub>PGM_Exit</sub>	hPPR Exit Time	15	-	ns

## Soft Post Package Repair (sPPR)

Soft Post Package Repair (sPPR) is a way to quickly, but temporarily, Repair a row element in a Bank Group on a DDR4 DRAM device, contrasted to hard Post Package Repair which takes longer but is permanent repair of a row element. There are some limitations and differences between sPPR and hPPR.

**Table 60. Description and Comparison of hPPR and sPPR**

Topic	Soft Repair	Hard Repair	Note
Persistence of Repair	Volatile – repair persists while power is within operating range	Non-Volatile – repair is permanent after the repair cycle	sPPR cleared after power off or device reset
$t_{PGM}$ (hPPR and sPPR programming Time)	$WL + 4t_{CK} + t_{WR}$	$>2000ms(t_{PGM})$	
# of Repair elements	1 per BG	1 per BG	Once hPPR is used within a BG, sPPR is no longer supported in that BG
Simultaneous use of soft and hard repair within a BG	Previous hPPR are allowed before soft repair to a different BG	Any outstanding sPPR must be cleared before a hard repair	Clearing sPPR occurs by either: (a) power down and power-up sequence or (b) Reset and re-initialize.
Repair Sequence	1 method – WR cmd.	2 methods WRA and WR	
Bank <sup>(1)</sup> not having row repair retains array data	Yes	Yes, if WRA sequence; No, if WR sequence	WRA sequence requires use of REF commands
Bank <sup>(1)</sup> having row repair retain array data	Yes, except for seed and associated rows	No	sPPR must be performed outside of REF window ( $t_{RFC}$ )

Note 1. If a BA pin is defined to be an “sPPR associated row” to the seed row, both states of the BA address input are affected. For example if BA0 is selected as an “sPPR associated row” to the seed row, addresses in both BA0 = 0 and BA0 = 1 are equally affected.

sPPR mode is entered in a similar fashion as hPPR, sPPR uses MR4 bit A5 while hPPR uses MR4 bit A13; sPPR requires the same guard key sequence as hPPR to qualify the MR4 PPR entry. Prior to sPPR entry, either an hPPR exit command or an sPPR exit command should be performed, whichever was the last PPR entry. After sPPR entry, an ACT command will capture the target bank and target row, herein seed row, where the row repair will be made. After  $t_{RCD}$  time, a WR command is used to select the individual DRAM, through the DQ bits, to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE command, the sPPR mode can be exited and normal operation can resume. The DRAM will retain the sPPR change as long as  $V_{DD}$  remains within the operating region. If the DRAM power is removed or the DRAM is reset, all sPPR changes will revert to the unrepaired state. sPPR changes must be cleared by either a power-up sequence or re-initialization by reset signal before hPPR mode is enabled.

DDR4 sPPR can repair one row per Bank Group, however when the hPPR resources for a bank group have been used, sPPR resources are no longer available for that bank group. If an sPPR or hPPR repair sequence is issued to a bank group with PPR resource un-available, the DRAM will ignore the programming sequence. sPPR mode is optional for 4Gb density DDR4 device.

The bank receiving sPPR change is expected to retain array data in all other rows except for the seed row and its associated row addresses. If the user does not require the data in the array in the bank under sPPR repair to be retained, then the handling of the seed row’s associated row addresses is not of interest and can be ignored. If the user requires the data in the array to be retained in the bank under sPPR mode, then prior to executing the sPPR mode, the seed row and its associated row addresses should be backed up and restored after sPPR has been completed. sPPR associated seed row addresses are specified in the table below.

**Table 61. sPPR Associated Row Address**

sPPR Associated Row Addresses						
BA0	A16	A15	A14	A13	A1	A0

## Soft Repair of a Fail Row Address

The following is the procedure of sPPR with WR command. Note that during the soft repair sequence, no refresh is allowed.

1. Before entering 'sPPR' mode, all banks must be Precharged; DBI and CRC Modes must be disabled.
2. Enable sPPR using MR4 bit "A5=1" and wait  $t_{MOD}$ .
3. Issue Guard Key as four consecutive MR0 commands each with a unique address field A[17:0]. Each MR0 command should space by  $t_{MOD}$ . MR0 Guard Key sequence is same as hPPR.
4. Issue ACT command with the Bank and Row Fail address, Write data is used to select the individual DRAM in the Rank for repair.
5. A WR command is issued after  $t_{RCD}$ , with valid column address. The DRAM will ignore the column address given with the WR command.
6. After WL ( $WL = CWL + AL + PL$ ), All DQs of Target DRAM should be low for  $4t_{CK}$ . If high is driven to All DQs of a DRAM consecutively for equal to or longer than first  $2t_{CK}$ , then DRAM does not conduct sPPR. If all DQs are neither low for  $4t_{CK}$  nor high for equal to or longer than first  $2t_{CK}$ , then sPPR mode execution is unknown.
7. Wait  $t_{WR}$  for the internal repair register to be written and then issue PRE to the Bank.
8. Wait 20ns after PRE which allow DRAM to recognize repaired Row address.
9. Exit PPR with setting MR4 bit "A5=0" and wait  $t_{MOD}$ .
10. One soft repair address per Bank Group is allowed before a hard repair is required. When more than one sPPR request is made to the same BG, the most recently issued sPPR address would replace the early issued one. In the case of conducting soft repair address in a different Bank Group, Repeat Step 2 to 9. During a soft Repair, Refresh command is not allowed between sPPR MRS entry and exit.

Once sPPR mode is exited, to confirm if target row is repaired correctly, the host can verify the repair by writing data into the target row and reading it back after sPPR exit with MR4 [A5=0].

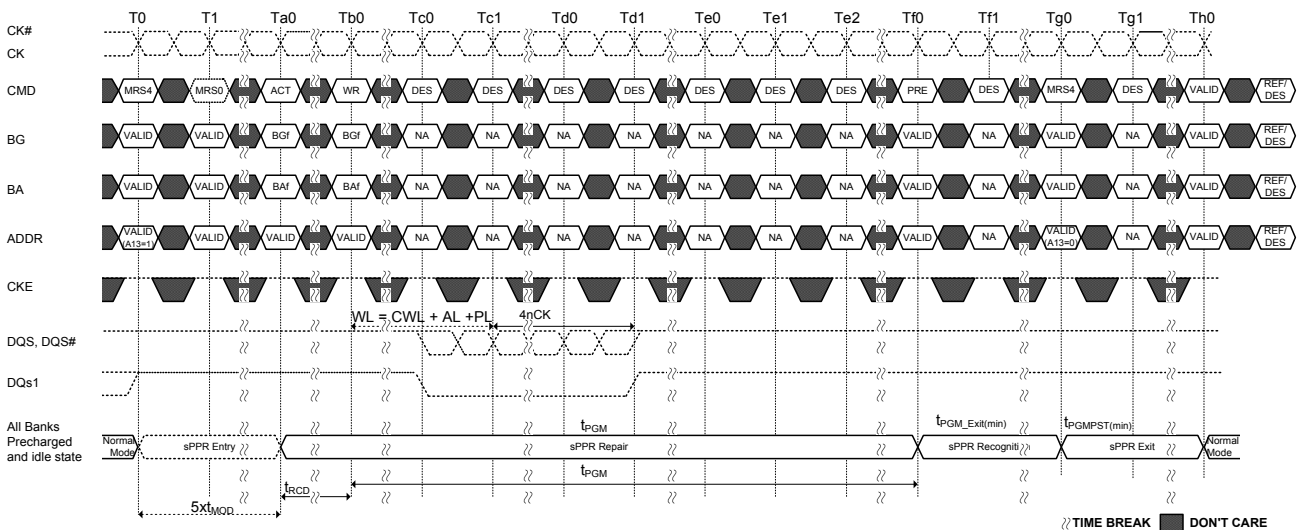
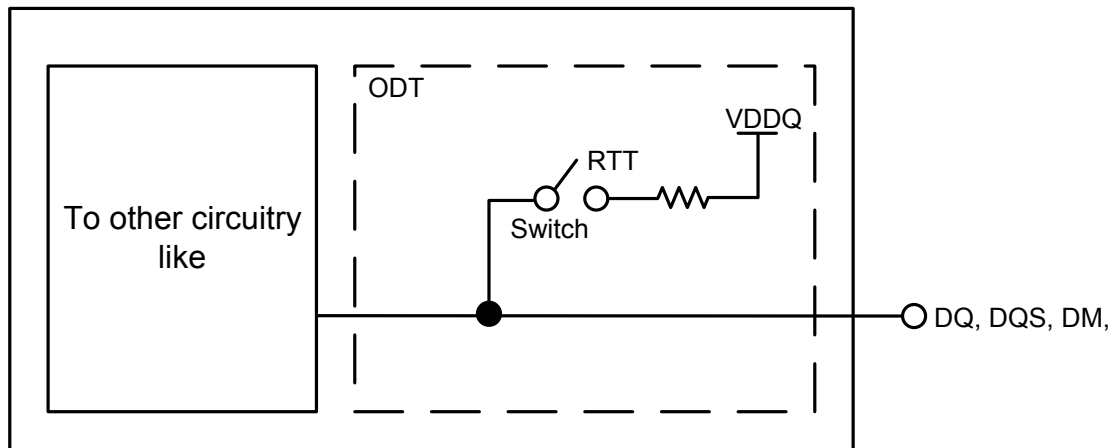


Figure 161. Fail Row Soft PPR (WR Case)

## On-Die Termination

ODT (On-Die Termination) is a feature of the DDR4 SDRAM that allows the DRAM to change termination resistance for x16 configuration, ODT is applied to each DQ0-15, UDQS, UDQS#, LDQS, LDQS#, UDM# and LDM# signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode. A simple functional representation of the DRAM ODT feature is shown below.



**Figure 162. Functional Representation of ODT**

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and Mode Register Setting and other control information, see below. The value of  $R_{TT}$  is determined by the settings of mode register bits (see Mode Register). The ODT pin will be ignored if the mode register MR1 is programmed to disable  $R_{TT\_NOM}$  (MR1 A [10:8] = 000) and in self refresh mode.

## ODT Mode Register and ODT State Table

The ODT Mode of DDR4 device has 4 states, Data Termination Disable,  $R_{TT\_WR}$ ,  $R_{TT\_NOM}$  and  $R_{TT\_PARK}$ . And the ODT Mode is enabled if any of MR1 A[10:8] or MR2 A[10:9] or MR5 A[8:6] are non zero. When enabled, the value of  $R_{TT}$  is determined by the settings of these bits.

After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Controller can control each  $R_{TT}$  condition with WR/RD command and ODT pin

- $R_{TT\_WR}$ : The rank that is being written to provide termination regardless of ODT pin status (either high or low)
- $R_{TT\_NOM}$ : DRAM turns ON  $R_{TT\_NOM}$  if it sees ODT asserted (except ODT is disabled by MR1).
- $R_{TT\_PARK}$ : Default parked value set via MR5 to be enabled and ODT pin is driven low.
- Data Termination Disable: DRAM driving data upon receiving Read command disables the termination after RL-X and stays off for a duration of  $BL/2 + X$  clock cycles. (X is 2 for  $1t_{CK}$  and 3 for  $2t_{CK}$  preamble mode).

The  $R_{TT}$  values have the following priority:

which means if there is Write command along with ODT pin high, then DRAM turns on  $R_{TT\_WR}$  not  $R_{TT\_NOM}$ , and also if there is Read command, then DRAM disables data termination regardless of ODT pin and goes into driving mode.

- Data termination disable
- $R_{TT\_WR}$
- $R_{TT\_NOM}$
- $R_{TT\_PARK}$

**Table 62. Termination State Table**

$R_{TT\_PARK}$ MR5[8:6]	$R_{TT\_NOM}$ MR1[10:8]	ODT pin	DRAM termination state	Note
Enabled	Enabled	High	$R_{TT\_NOM}$	1,2
		Low	$R_{TT\_PARK}$	1,2
	Disabled	Don't care <sup>3</sup>	$R_{TT\_PARK}$	1,2,3
Disabled	Enabled	High	$R_{TT\_NOM}$	1,2
		Low	Hi-Z	1,2
	Disabled	Don't care <sup>3</sup>	Hi-Z	1,2,3

Note 1. When a read command is executed, DRAM termination state will be High-Z for defined period independent of ODT pin and MR setting of  $R_{TT\_PARK}/R_{TT\_NOM}$ . This is described in the ODT during Read section.

Note 2. If  $R_{TT\_WR}$  is enabled,  $R_{TT\_WR}$  will be activated by write command for defined period time independent of ODT pin and MR setting of  $R_{TT\_PARK}/R_{TT\_NOM}$ . This is described in the Dynamic ODT section.

Note 3. If  $R_{TT\_NOM}$  MR is disabled, ODT receiver power will be turned off to save power.

On-die termination effective resistances are defined and can be selected by any or all of the following options:

- MR1 A[10:8] ( $R_{TT\_NOM}$ ) - Disable, 240Ω, 120Ω, 80Ω, 60Ω, 48Ω, 40Ω, and 34Ω.
- MR2 A[11:9] ( $R_{TT\_WR}$ ) - Disable, 240Ω, 120Ω, and 80Ω.
- MR5 A[8:6] ( $R_{TT\_PARK}$ ) - Disable, 240Ω, 120Ω, 80Ω, 60Ω, 48Ω, 40Ω, and 34Ω.

ODT is applied to the following inputs:

- x16: DQs, LDM#, UDM#, LDQS, LDQS#, UDQS, and UDQS# inputs.

### ODT Definition of Voltages and Currents

On die termination effective  $R_{TT}$  values supported are 240, 120, 80, 60, 48, 40, 34 ohms.

$$R_{TT} = \frac{V_{DDQ} - V_{out}}{|I_{out}|}$$

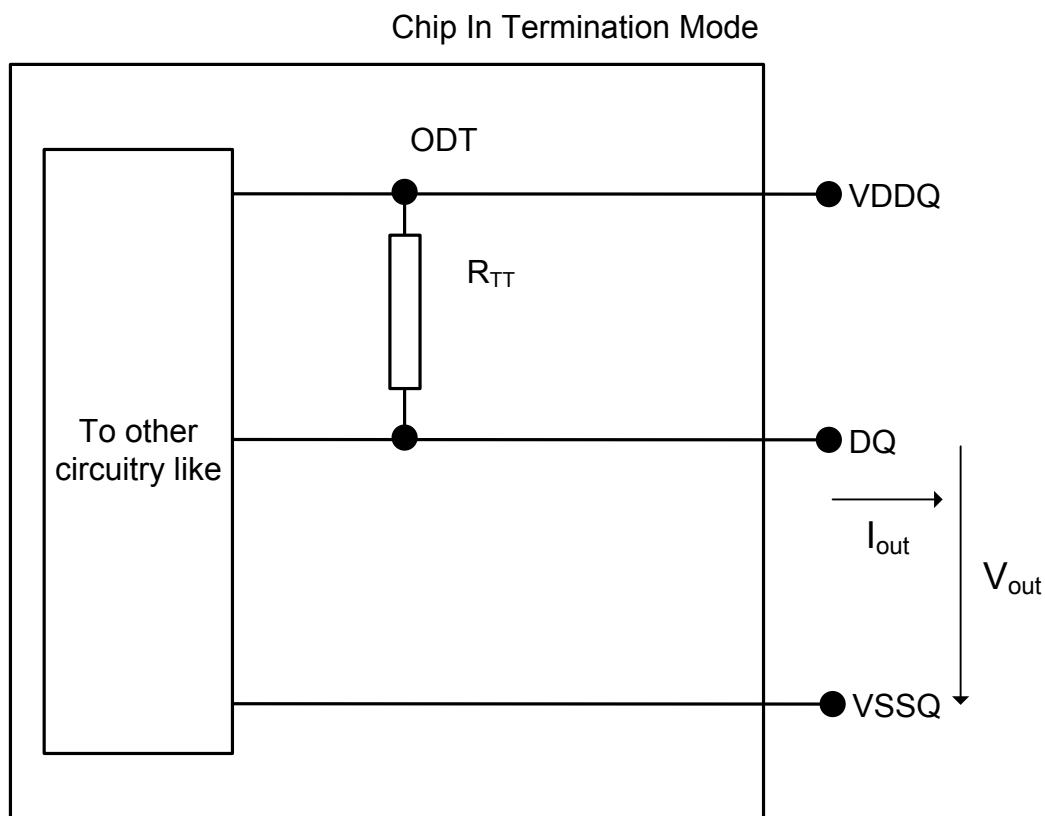


Figure 163. On Die Termination

**Table 63. ODT Electrical Characteristics RZQ=240Ω ±1% entire temperature operation range; after proper ZQ calibration**

R <sub>TT</sub>	V <sub>out</sub>	Min.	Nom.	Max.	Unit	Note
240Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ	1,2,3
	V <sub>OHDc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ	1,2,3
120Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/2	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/2	1,2,3
	V <sub>OHDc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/2	1,2,3
80Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/3	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/3	1,2,3
	V <sub>OHDc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/3	1,2,3
60Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/4	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/4	1,2,3
	V <sub>OHDc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/4	1,2,3
48Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/5	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/5	1,2,3
	V <sub>OHDc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/5	1,2,3
40Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/6	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/6	1,2,3
	V <sub>OHDc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/6	1,2,3
34Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/7	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/7	1,2,3
	V <sub>OHDc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mismatch within byte	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0	-	10	%	1,2,4,5,6

Note 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

Note 2. Pull-up ODT resistors are recommended to be calibrated at 0.8 x V<sub>DDQ</sub>. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 x V<sub>DDQ</sub> and 1.1 x V<sub>DDQ</sub>.

Note 3. The tolerance limits are specified under the condition that V<sub>DDQ</sub>=V<sub>DD</sub> and V<sub>SSQ</sub>=V<sub>SS</sub>.

Note 4. DQ to DQ mismatch within byte variation for a given component including DQS and DQS#. (characterized)

Note 5. R<sub>TT</sub> variance range ratio to R<sub>TT</sub> Nominal value in a given component, including DQS and DQS#.

$$\text{DQ-DQ Mismatch in a Device} = \frac{R_{TT\text{Max}} - R_{TT\text{Min}}}{R_{TT\text{NOM}}} \times 100$$

Note 6. This parameter of x16 device is specified for Upper byte and Lower byte.

## Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power-down mode (regardless of MR1 bit A10)
- Precharge power-down mode

In synchronous ODT mode,  $R_{TT\_NOM}$  will be turned on DODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off DODTLoFF clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the Write Latency ( $WL = CWL + AL + PL$ ) by:  $DODTLon = WL - 2$ ;  $DODTLoFF = WL - 2$ . When operating in  $2t_{CK}$  Preamble Mode, The ODT latency must be 1 clock smaller than in  $1t_{CK}$  Preamble Mode;  $DODTLon = WL - 3$ ;  $DODTLoFF = WL - 3$ . ( $WL = CWL + AL + PL$ )

## ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) and the Parity Latency (PL) programmed into the Mode Register MR1 applies to ODT Latencies as shown below:

**Table 64. ODT Latency**

Symbol	Parameter	1 $t_{CK}$ Preamble	2 $t_{CK}$ Preamble	Unit
DODTLon	Direct ODT turn on Latency	$CWL + AL + PL - 2$	$CWL + AL + PL - 3$	$t_{CK}$
DODTLoFF	Direct ODT turn off Latency	$CWL + AL + PL - 2$	$CWL + AL + PL - 3$	$t_{CK}$
RODTLoFF	Read command to internal ODT turn off Latency	$CL + AL + PL - 2$	$CL + AL + PL - 3$	$t_{CK}$
RODTLoN4	Read command to $R_{TT\_PARK}$ turn on Latency in BC4	$RODTLoFF + 4$	$RODTLoFF + 5$	$t_{CK}$
RODTLoN8	Read command to $R_{TT\_PARK}$ turn on Latency in BC8/BL8	$RODTLoFF + 6$	$RODTLoFF + 7$	$t_{CK}$
ODTH4	ODT Assertion time, BC4 mode	4	5	$t_{CK}$
ODTH8	ODT Assertion time, BL8 mode	6	7	$t_{CK}$

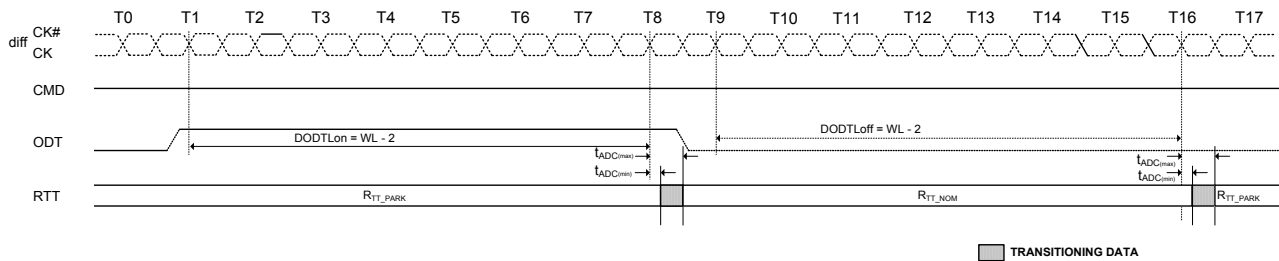


## Timing Parameter

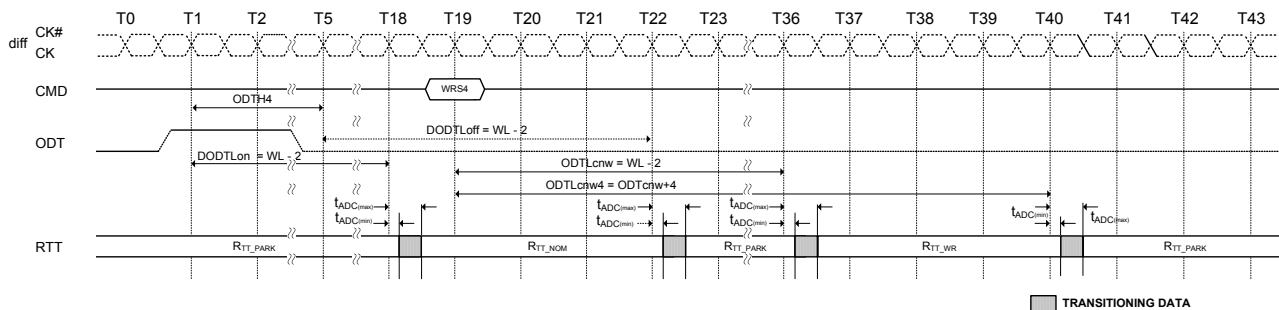
In synchronous ODT mode, the following parameters apply:

- DODTLon, DODTLoFF, RODTLoFF, RODTLon4, RODTLon8,  $t_{ADC(MIN)}$  (MAX)-
- $t_{ADC(MIN)}$  and  $t_{ADC(MAX)}$  are minimum and maximum  $R_{TT}$  change timing skew between different termination values. These timing parameters apply to both the synchronous ODT mode and the data termination disable mode.

When ODT is asserted, it must remain high until minimum ODT<sub>H4</sub> (BL = 4) or ODT<sub>H8</sub> (BL = 8) is satisfied. Additionally, depending on CRC or  $2t_{CK}$  preamble setting in MRS, ODT<sub>H</sub> should be adjusted.



**Figure 164. Synchronous ODT Timing Example for CWL=9, AL=0, PL=0; DODTLon=WL-2=7; DODTLoFF=WL-2=7**

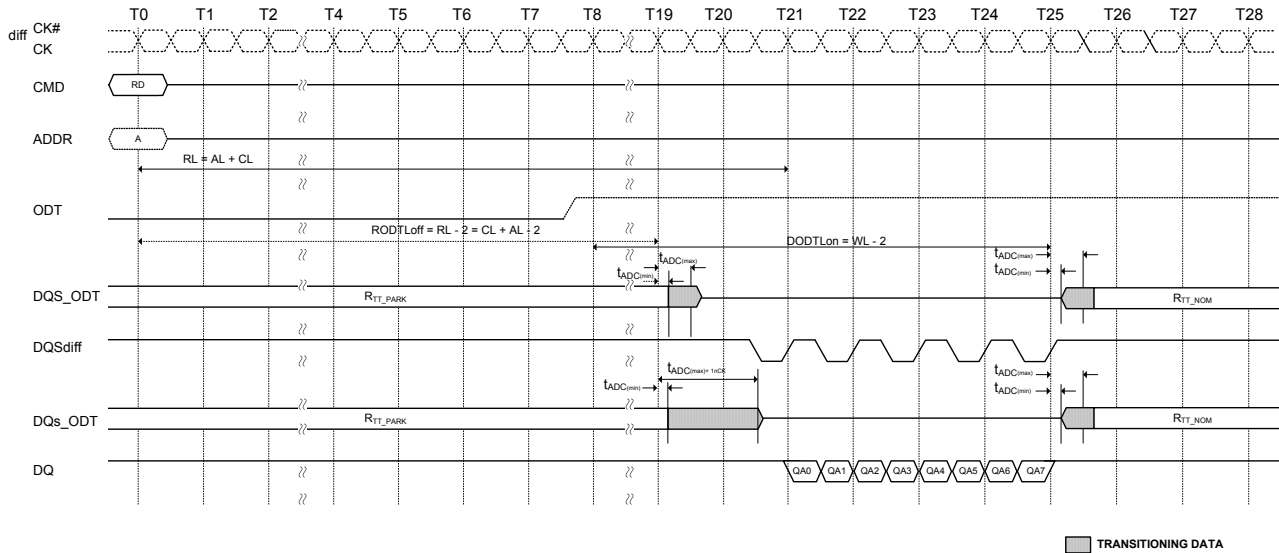


**Figure 165. Synchronous ODT example with BL=4, CWL=9, AL=10, PL=0; DODTLon/off=WL-2=17, ODTcnw=WL-2=17**

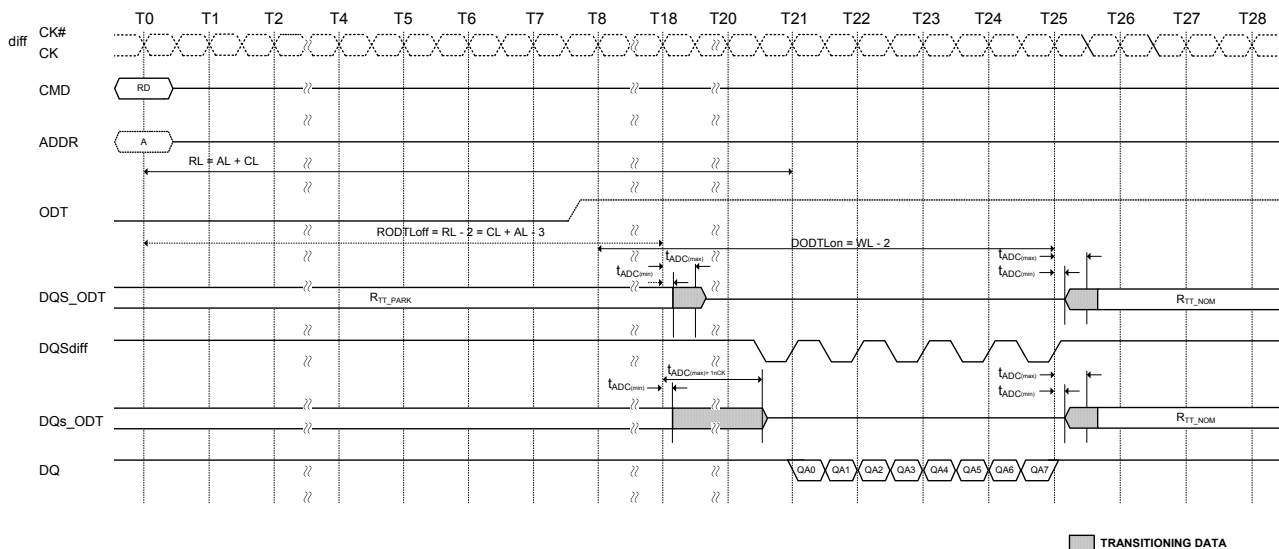
ODT must be held high for at least ODT<sub>H4</sub> after assertion (T1). ODT<sub>H</sub> is measured from ODT first registered high to ODT first registered low, or from registration of Write command. Note that ODT<sub>H4</sub> should be adjusted depending on CRC or  $2t_{CK}$  preamble setting.

## ODT During Reads

Because the DDR4 DRAM cannot terminate with  $R_{TT}$  and drive with  $R_{ON}$  at the same time;  $R_{TT}$  may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T25, the device turns on the termination when it stops driving, which is determined by  $t_{HZ}$ . If the DRAM stops driving early (that is,  $t_{HZ}$  is early), then  $t_{ADC(MIN)}$  timing may apply. If the DRAM stops driving late (that is,  $t_{HZ}$  is late), then the DRAM complies with  $t_{ADC(MAX)}$  timing.



**Figure 166. Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon=AL+CWL-2=17; DODTLoft=AL+CWL-2=17; 1tCK preamble)**



**Figure 167. Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon=AL+CWL-2=17; DODTLoft=AL+CWL-2=17; 2tCK preamble)**

## Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the device can be changed without issuing an MRS command. This requirement is supported by the dynamic ODT feature, described below.

### Functional Description

The dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to 1.

- Three  $R_{TT}$  values are available:  $R_{TT\_NOM}$ ,  $R_{TT\_WR}$ , and  $R_{TT\_PARK}$ .
  - The value for  $R_{TT\_NOM}$  is preselected via bits MR1 A[10:8].
  - The value for  $R_{TT\_WR}$  is preselected via bits MR2 A[11:9].
  - The value for  $R_{TT\_PARK}$  is preselected via bits MR5 A[8:6].
- During operation without write commands, the termination is controlled as follows:
  - Nominal termination strength  $R_{TT\_NOM}$  or  $R_{TT\_PARK}$  is selected.
  - $R_{TT\_NOM}$  on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff; and  $R_{TT\_PARK}$  is on when ODT is LOW.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - Latency ODTLcnw after the write command, termination strength  $R_{TT\_WR}$  is selected.
  - Latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength  $R_{TT\_WR}$  is deselected.
  - One or two clocks will be added into or subtracted from ODTLcwn8 and ODTLcwn4, depending on write CRC Mode and/or 2  $t_{CK}$  preamble enablement. The following table shows latencies and timing parameters which are relevant for the on-die termination control in dynamic ODT mode.

The dynamic ODT feature is not supported in DLL-off mode. MRS command must be used to set  $R_{TT\_WR}$ , MR2 A[11:9] = 000, to disable dynamic ODT externally.

**Table 65. Latencies and timing parameters relevant for Dynamic ODT with 1 $t_{CK}$  preamble mode and CRC disabled**

Name and Description	Abbr.	Defined from	Define to	Definition for all DDR4 speed bins	Unit
ODT Latency for changing from $R_{TT\_PARK}/R_{TT\_NOM}$ to $R_{TT\_WR}$	ODTLcnw	Registering external write command	Change $R_{TT}$ strength from $R_{TT\_PARK}/R_{TT\_NOM}$ to $R_{TT\_WR}$	ODTLcnw = WL - 2	$t_{CK}$
ODT Latency for change from $R_{TT\_WR}$ to $R_{TT\_PARK}/R_{TT\_NOM}$ (BL = 4)	ODTLcwn4	Registering external write command	Change $R_{TT}$ strength from $R_{TT\_WR}$ to $R_{TT\_PARK}/R_{TT\_NOM}$	ODTLcwn4 = 4 + ODTLcnw	$t_{CK}$
ODT Latency for change from $R_{TT\_WR}$ to $R_{TT\_PARK}/R_{TT\_NOM}$ (BL = 8)	ODTLcwn8	Registering external write command	Change $R_{TT}$ strength from $R_{TT\_WR}$ to $R_{TT\_PARK}/R_{TT\_NOM}$	ODTLcwn8 = 6 + ODTLcnw	$t_{CK}$
RTT change skew	$t_{ADC}$	ODTLcnw ODTLcwn	$R_{TT}$ Valid	$t_{ADC(min)} = 0.3$ $t_{ADC(max)} = 0.7$	$t_{CK}$

**Table 66. Latencies and timing parameters relevant for Dynamic ODT with 1 $t_{CK}$  and 2 $t_{CK}$  preamble mode and CRC enabled/disabled**

Symbol	1 $t_{CK}$ Preamble		2 $t_{CK}$ Preamble		Unit
	CRC off	CRC on	CRC off	CRC on	
ODTLcnw	WL - 2	WL - 2	WL - 3	WL - 3	$t_{CK}$
ODTLcwn4	ODTLcnw +4	ODTLcnw +7	ODTLcnw +5	ODTLcnw +8	$t_{CK}$
ODTLcwn8	ODTLcnw +6	ODTLcnw +7	ODTLcnw +7	ODTLcnw +8	$t_{CK}$

## ODT Timing Diagrams

The following pages provide example timing diagrams

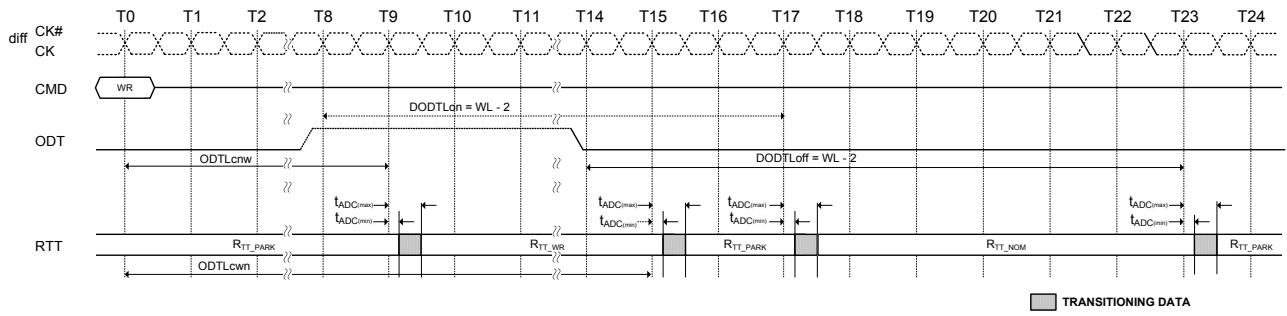


Figure 168. ODT timing (Dynamic ODT, 1tCK preamble, CL=14, CWL=11, BL=8, AL=0, CRC Disabled)

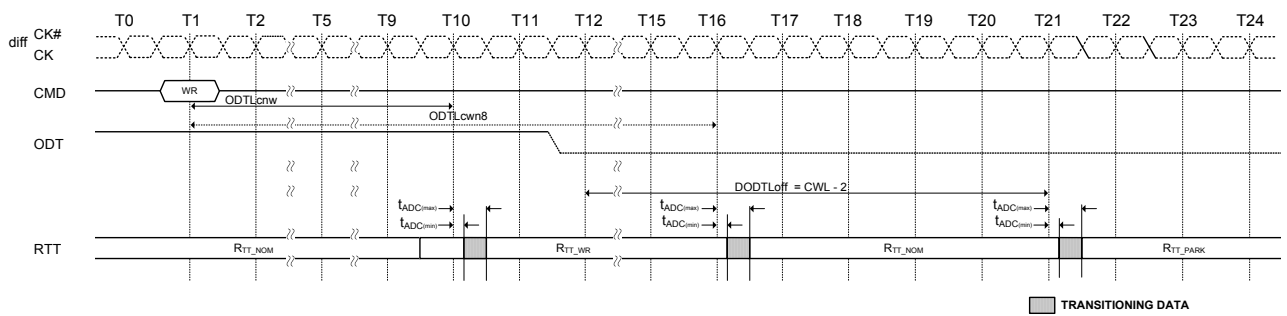


Figure 169. Dynamic ODT overlapped with Rtt\_NOM (CL=14, CWL=11, BL=8, AL=0, CRC Disabled)

## Asynchronous ODT Mode

Asynchronous ODT mode is selected when DLL is disabled by MR1 bit A0='0'b.

In asynchronous ODT timing mode, internal ODT command is not delayed by either the Additive latency (AL) or relative to the external ODT signal ( $R_{TT\_NOM}$ ). In asynchronous ODT mode, the following timing parameters apply  $t_{AONAS,min,max}$ ,  $t_{AOFAS,min,max}$ .

Minimum  $R_{TT\_NOM}$  turn-on time ( $t_{AONASmin}$ ) is the point in time when the device termination circuit leaves  $R_{TT\_PARK}$  and ODT resistance begins to change. Maximum  $R_{TT\_NOM}$  turn on time ( $t_{AONASmax}$ ) is the point in time when the ODT resistance is reached  $R_{TT\_NOM}$ .

$t_{AONASmin}$  and  $t_{AONASmax}$  are measured from ODT being sampled high.

Minimum  $R_{TT\_NOM}$  turn-off time ( $t_{AOFASmin}$ ) is the point in time when the devices termination circuit starts to leave  $R_{TT\_NOM}$ .

Maximum  $R_{TT\_NOM}$  turn-off time ( $t_{AOFASmax}$ ) is the point in time when the on-die termination has reached  $R_{TT\_PARK}$ .

$t_{AOFASmin}$  and  $t_{AOFASmax}$  are measured from ODT being sampled low.

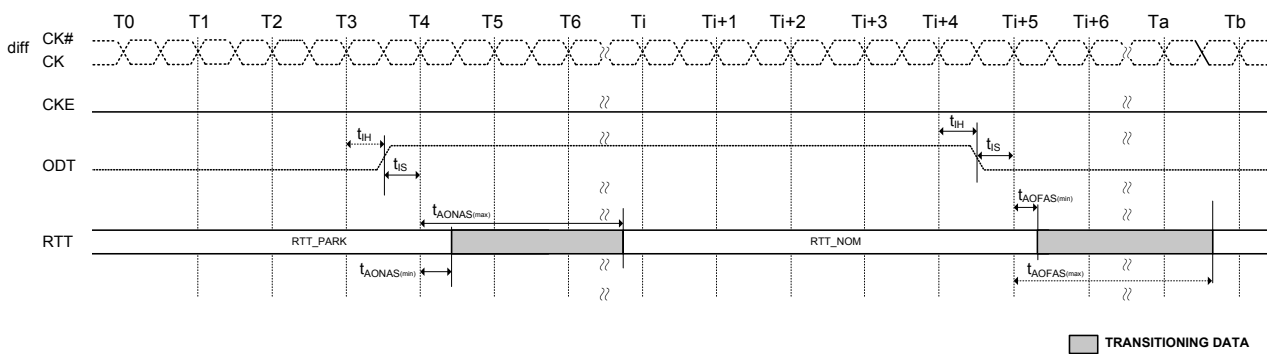
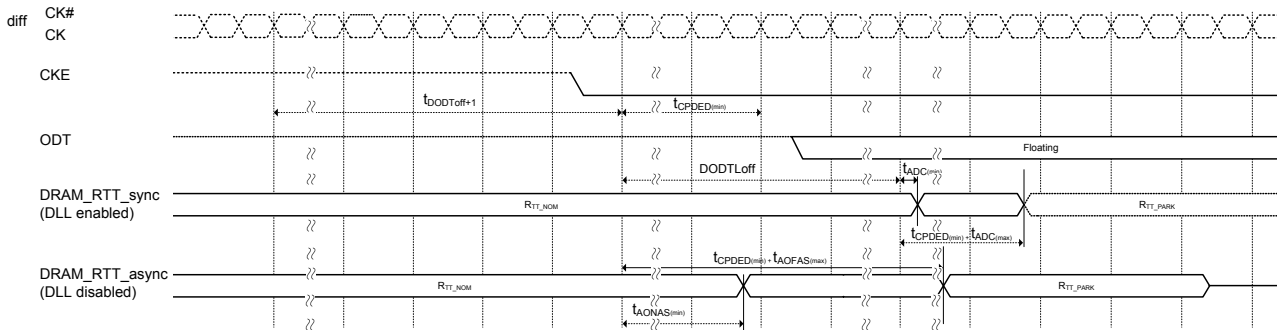


Figure 170. Asynchronous ODT Timing on DDR4 SDRAM with DLL-off

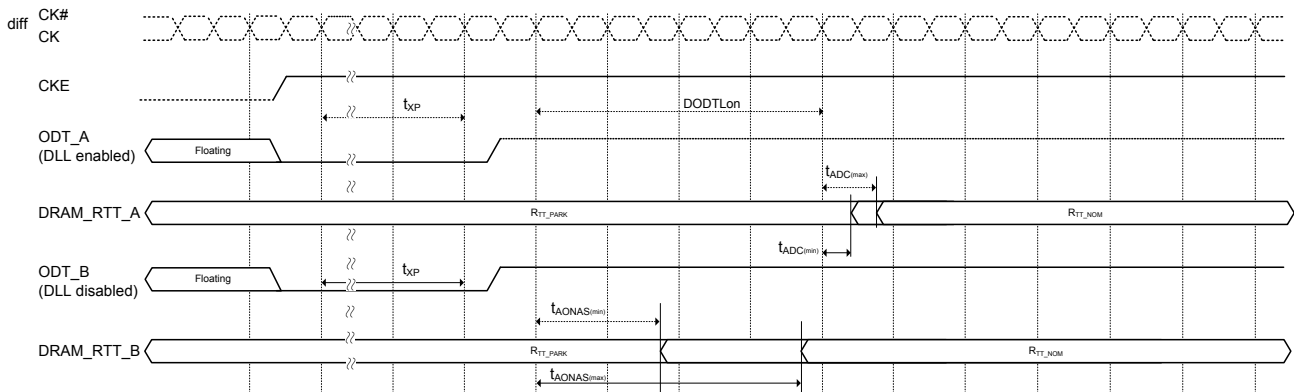
## ODT buffer disabled mode for Power down

DRAM does not provide  $R_{TT\_NOM}$  termination during power down when ODT input buffer deactivation mode is enabled in MR5 bit A5. To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down (from  $t_{DODToff+1}$  prior to CKE low till  $t_{CPDED}$  after CKE low). The ODT signal may be floating after  $t_{CPDEDmin}$  has expired. In this mode,  $R_{TT\_NOM}$  termination corresponding to sampled ODT at the input after CKE is first registered low (and  $t_{ANPD}$  before that) may be either  $R_{TT\_NOM}$  or  $R_{TT\_PARK}$ .  $t_{ANPD}$  is equal to  $(WL-1)$  and is counted backwards from PDE.



**Figure 171. ODT timing for power down entry with ODT buffer disable mode**

When exit from power down, along with CKE being registered high, ODT input signal must be re-driven and maintained low until  $t_{XP}$  is met.

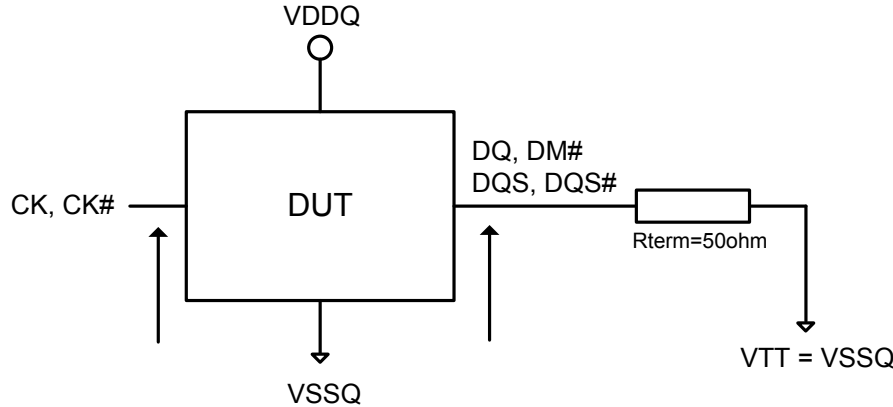


**Figure 172. ODT timing for power down exit with ODT buffer disable mode**

## ODT Timing Definitions

### Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined below



Timing Reference Point

**Figure 173. ODT Timing Reference Load**

### ODT Timing Definitions

Definitions for  $t_{ADC}$ ,  $t_{AONAS}$  and  $t_{AOFAS}$  are provided in the table and measurement reference settings are provided in the subsequent. The  $t_{ADC}$  for the Dynamic ODT case and Read Disable ODT cases are represented by  $t_{ADC}$  of Direct ODT Control case.

**Table 67. ODT Timing Definitions**

Symbol	Begin Point Definition	End Point Definition
$t_{ADC}$	Rising edge of CK,CK# defined by the end point of DODTLoff	Extrapolated point at $V_{RTT\_NOM}$
	Rising edge of CK,CK# defined by the end point of DODTLon	Extrapolated point at $V_{SSQ}$
	Rising edge of CK,CK# defined by the end point of ODTLcwn	Extrapolated point at $V_{RTT\_NOM}$
	Rising edge of CK,CK# defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at $V_{SSQ}$
$t_{AONAS}$	Rising edge of CK,CK# with ODT being first registered high	Extrapolated point at $V_{SSQ}$
$t_{AOFAS}$	Rising edge of CK,CK# with ODT being first registered low	Extrapolated point at $V_{RTT\_NOM}$

**Table 68. Reference Settings for ODT Timing Measurements**

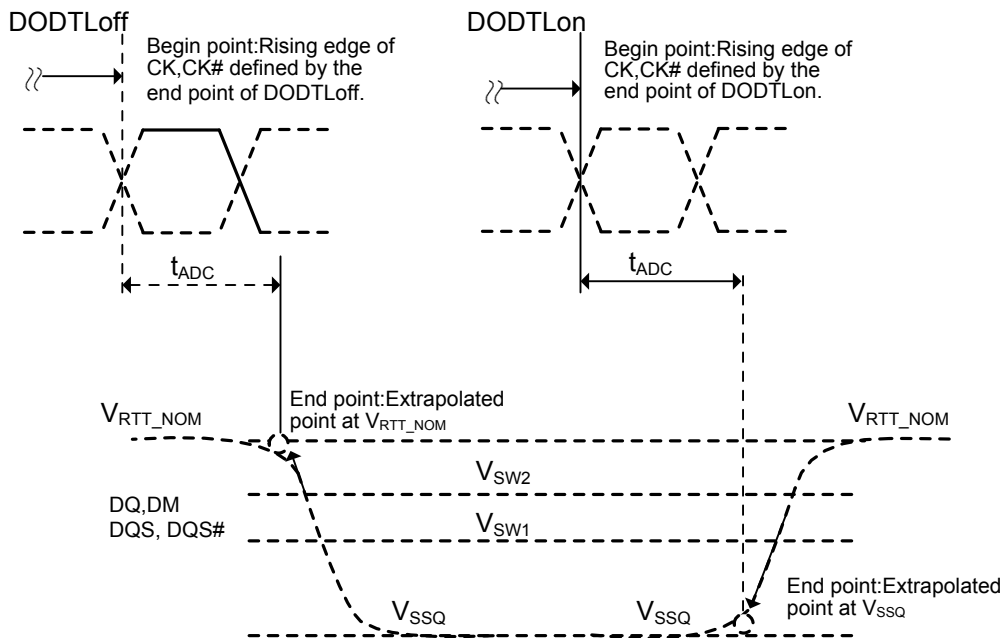
Measured Parameter	$R_{TT\_PARK}$	$R_{TT\_NOM}$	$R_{TT\_WR}$	Vsw1	Vsw2	Note
$t_{ADC}$	Disable	RZQ/7	-	0.20V	0.40V	1,2
	-	RZQ/7	Hi-Z	0.20V	0.40V	1,3
$t_{AONAS}$	Disable	RZQ/7	-	0.20V	0.40V	1,2
$t_{AOFAS}$	Disable	RZQ/7	-	0.20V	0.40V	1,2

Note 1. MR setting is as follows.

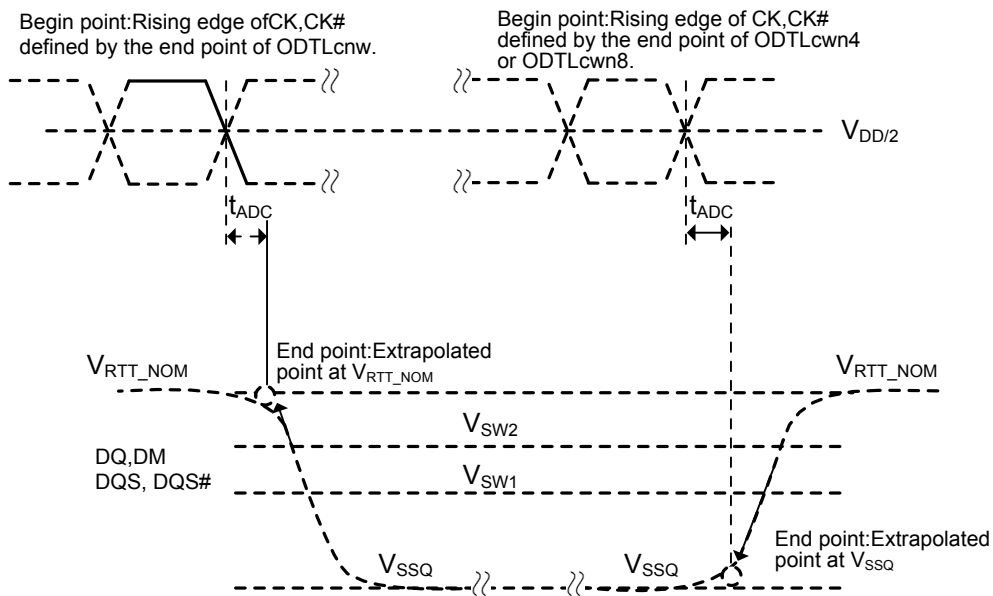
- MR1 A10=1, A9=1, A8=1 ( $R_{TT\_NOM\_Setting}$ )
- MR5 A8=0, A7=0, A6=0 ( $R_{TT\_PARK}$  Setting)
- MR2 A11=0, A10=1, A9=1 ( $R_{TT\_WR}$  Setting)

Note 2. ODT state change is controlled by ODT pin.

Note 3. ODT state change is controlled by Write Command.

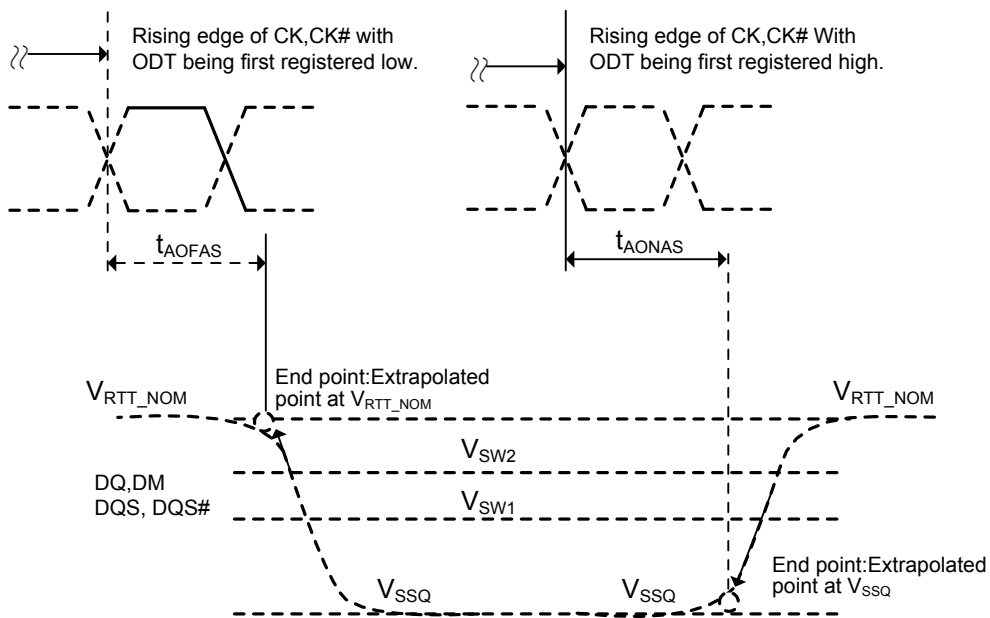


**Figure 174. Definition of  $t_{ADC}$  at Direct ODT Control**



**Figure 175. Definition of  $t_{ADC}$  at Dynamic ODT Control**





**Figure 176. Definition of  $t_{AOFAS}$  and  $t_{AONAS}$**

**Table 69. Absolute Maximum DC Ratings**

Symbol	Parameter	Values	Unit	Note
V <sub>DD</sub>	Voltage on V <sub>DD</sub> pin relative to V <sub>SS</sub>	-0.3 ~ 1.5	V	1,3
V <sub>DDQ</sub>	Voltage on V <sub>DDQ</sub> pin relative to V <sub>SS</sub>	-0.3 ~ 1.5	V	1,3
V <sub>PP</sub>	Voltage on V <sub>PP</sub> pin relative to V <sub>SS</sub>	-0.3 ~ 3.0	V	4
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin except V <sub>REFCA</sub> relative to V <sub>SS</sub>	-0.3 ~ 1.5	V	1,3,5
T <sub>STG</sub>	Storage Temperature	-55 ~ 100	°C	1,2

Note 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Note 3. V<sub>DD</sub> and V<sub>DDQ</sub> must be within 300 mV of each other at all times; and V<sub>REFCA</sub> must be not greater than 0.6 x V<sub>DDQ</sub>. When V<sub>DD</sub> and V<sub>DDQ</sub> are less than 500 mV; V<sub>REFCA</sub> may be equal to or less than 300 mV.

Note 4. V<sub>PP</sub> must be equal or greater than V<sub>DD</sub>/V<sub>DDQ</sub> at all times.

Note 5. Refer to overshoot area above 1.5 V.

**Table 70. Temperature Range**

Symbol	Parameter	Values	Unit	Note
T <sub>OPER</sub>	Commercial Operating Temperature Range	0 ~ 95	°C	1,2
	Industrial Operating Temperature Range	-40 ~ 95	°C	1,2

Note 1. Operating temperature is the case surface temperature on center/top of the DRAM.

Note 2. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are guaranteed in this range, but the following additional apply.

- a. Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1x refresh (tREFI to 7.8us) in the Extended Temperature Range.

**Table 71. Recommended DC Operating Conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V <sub>DD</sub>	Supply Voltage	1.14	1.2	1.26	V	1,2,3
V <sub>DDQ</sub>	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
V <sub>PP</sub>	DRAM Activating Power Supply	2.375	2.5	2.75	V	3

Note 1. Under all conditions V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.

Note 2. V<sub>DDQ</sub> tracks with V<sub>DD</sub>. AC parameters are measured with V<sub>DD</sub> and V<sub>DDQ</sub> tied together.

Note 3. DC bandwidth is limited to 20MHz.

## AC and DC Input Measurement Levels

**Table 72. Single-Ended AC and DC Input Levels for Command and Address**

Symbol	Parameter	DDR4-2400		DDR4-2666		Unit	Note
		Min.	Max.	Min.	Max.		
$V_{IH,CA(DC75)}$	DC input logic high	$V_{REFCA} + 0.075$	$V_{DD}$	TBD	TBD	V	
$V_{IL,CA(DC75)}$	DC input logic low	$V_{SS}$	$V_{REFCA} - 0.075$	TBD	TBD	V	
$V_{IH,CA(AC100)}$	AC input logic high	$V_{REF} + 0.1$	$V_{DD}$	TBD	TBD	V	1
$V_{IL,CA(AC100)}$	AC input logic low	-	$V_{REF} - 0.1$	TBD	TBD	V	1
$V_{REFCA(DC)}$	Reference Voltage for ADD, CMD inputs	$0.49 \times V_{DD}$	$0.51 \times V_{DD}$	TBD	TBD	V	2,3

Note 1. See "Overshoot and Undershoot Specifications"

Note 2. The AC peak noise on  $V_{REFCA}$  may not allow  $V_{REFCA}$  to deviate from  $V_{REFCA(DC)}$  by more than  $\pm 1\% V_{DD}$  (for reference: approx.  $\pm 12mV$ )

Note 3. For reference: approx.  $V_{DD}/2 \pm 12 mV$

## Differential swing requirements for clock (CK – CK#)

**Table 73. Differential AC and DC Input Levels**

Symbol	Parameter	Min.	Max.	Unit	Note
$V_{IH,diff}$	Differential input high	TBD	-	V	1,3
$V_{IL,diff}$	Differential input low	-	TBD	V	1,3
$V_{IH,diff(AC)}$	Differential input high ac	$2 \times (V_{IH(AC)} - V_{REF})$	-	V	2,3
$V_{IL,diff(AC)}$	Differential input low ac	-	$2 \times (V_{IL(AC)} - V_{REF})$	V	2,3

Note 1. Used to define a differential signal slew-rate.

Note 2. For CK - CK# use  $V_{IH,CA}/V_{IL,CA(AC)}$  of ADD/CMD and  $V_{REFCA}$ ;

Note 3. These values are not defined; however, the differential signals CK - CK#, need to be within the respective limits ( $V_{IH,CA(DC)max}$ ,  $V_{IL,CA(DC)min}$ ) for single-ended signals as well as the limitations for overshoot and undershoot.

## Single-ended requirements for differential signals

**Table 74. Differential swing requirements for clock (CK – CK#)**

Symbol	Parameter	Min.	Max.	Unit	Note
$V_{SEH}$	Single-ended high-level for CK, CK#	TBD	-	V	1-3
$V_{SEL}$	Single-ended low-level for CK, CK#	-	TBD	V	1-3

Note 1. For CK – CK# use  $V_{IH,CA}/V_{IL,CA(AC)}$  of ADD/CMD

Note 2.  $V_{IH,CA}/V_{IL,CA(AC)}$  for ADD/CMD is based on  $V_{REFCA}$

Note 3. These values are not defined; however, the differential signals CK – CK#, need to be within the respective limits ( $V_{IH,CA(DC)max}$ ,  $V_{IL,CA(DC)min}$ ) for single-ended signals as well as the limitations for overshoot and undershoot.

## Address, Command and Control Overshoot and Undershoot specifications

**Table 75. AC overshoot/undershoot for Address, Command and Control pins**

Symbol	Parameter	DDR4-2400	DDR4-2666	Unit	Note
$V_{AOSP}$	Maximum peak amplitude above $V_{AOS}$	0.06	TBD	V	
$V_{AOS}$	Upper boundary of overshoot area $A_{AOS1}$	$V_{DD} + 0.24$	TBD	V	1
$V_{AUS}$	Maximum peak amplitude allowed for undershoot	0.30	TBD	V	
$A_{AOS2}$	Maximum overshoot area per 1 $t_{CK}$ above $V_{AOS}$	0.0055	TBD	V-ns	
$A_{AOS1}$	Maximum overshoot area per 1 $t_{CK}$ between $V_{DD}$ and $V_{AOS}$	0.1699	TBD	V-ns	
$A_{AUS}$	Maximum undershoot area per 1 $t_{CK}$ below $V_{SS}$	0.1762	TBD	V-ns	

(A0-A13, BG0, BA0-BA1, ACT#, RAS#/A16, CAS#/A15, WE#/A14, CS#, CE, ODT)

Note 1. The value of  $V_{AOS}$  matches  $V_{DD}$  absolute max as defined in "Absolute Maximum DC Ratings". Absolute Maximum DC Ratings if  $V_{DD}$  equals  $V_{DD}$  max as defined in "Recommended DC Operating Conditions". If  $V_{DD}$  is above the recommended operating conditions,  $V_{AOS}$  remains at  $V_{DD}$  absolute max as defined in "Absolute Maximum DC Ratings"

## Clock Overshoot and Undershoot Specifications

**Table 76. AC overshoot/undershoot specification for Clock**

Symbol	Parameter	DDR4-2400	DDR4-2666	Unit	Note
$V_{COSP}$	Maximum peak amplitude above $V_{COS}$	0.06	TBD	V	
$V_{COS}$	Upper boundary of overshoot area $A_{DOS1}$	$V_{DD} + 0.24$	TBD	V	1
$V_{CUS}$	Maximum peak amplitude allowed for undershoot	0.30	TBD	V	
$A_{COS2}$	Maximum overshoot area per 1 UI above $V_{COS}$	0.0025	TBD	V-ns	
$A_{COS1}$	Maximum overshoot area per 1 UI between $V_{DD}$ and $V_{DOS}$	0.0750	TBD	V-ns	
$A_{CUS}$	Maximum undershoot area per 1 UI below $V_{SS}$	0.0762	TBD	V-ns	

(CK, CK#)

Note 1. The value of  $V_{COS}$  matches  $V_{DD}$  absolute max as defined in "Absolute Maximum DC Ratings". Absolute Maximum DC Ratings if  $V_{DD}$  equals  $V_{DD}$  max as defined in "Recommended DC Operating Conditions". If  $V_{DD}$  is above the recommended operating conditions,  $V_{COS}$  remains at  $V_{DD}$  absolute max as defined in "Absolute Maximum DC Ratings"

## Data, Strobe and Mask Overshoot and Undershoot Specifications

**Table 77. AC overshoot/undershoot specification for Clock**

Symbol	Parameter	DDR4-2400	DDR4-2666	Unit	Note
$V_{DOSP}$	Maximum peak amplitude above $V_{DOS}$	0.16	TBD	V	
$V_{DOS}$	Upper boundary of overshoot area $A_{DOS1}$	$V_{DDQ} + 0.24$	TBD	V	1
$V_{DUS}$	Lower boundary of undershoot area $A_{DUS1}$	0.30	TBD	V	2
$V_{DUSP}$	Maximum peak amplitude below $V_{DUS}$	0.10	TBD	V	
$A_{DOS2}$	Maximum overshoot area per 1 UI above $V_{DOS}$	0.0100	TBD	V-ns	
$A_{DOS1}$	Maximum overshoot area per 1 UI between $V_{DDQ}$ and $V_{DOS}$	0.0700	TBD	V-ns	
$A_{CUS1}$	Maximum undershoot area per 1 UI between $V_{SSQ}$ and $V_{DUS1}$	0.0700	TBD	V-ns	
$A_{CUS2}$	Maximum undershoot area per 1 UI below $V_{DUS}$	0.0100	TBD	V-ns	

(DQ, DQS, DQS#, DM#, DBI#)

Note 1. The value of  $V_{DOS}$  matches ( $V_{IN}$ ,  $V_{OUT}$ ) max as defined in "Absolute Maximum DC Ratings". Absolute Maximum DC Ratings if  $V_{DDQ}$  equals  $V_{DDQ}$  max as defined in "Recommended DC Operating Conditions". If  $V_{DDQ}$  is above the recommended operating conditions,  $V_{DOS}$  remains at ( $V_{IN}$ ,  $V_{OUT}$ ) max as defined in "Absolute Maximum DC Ratings"

Note 2. The value of  $V_{DUS}$  matches ( $V_{IN}$ ,  $V_{OUT}$ ) min as defined in "Absolute Maximum DC Ratings".

**Table 78. Capacitance**

Symbol	Parameter	DDR4-2400/2666		Unit	Note
		Min.	Max.		
C <sub>IO</sub>	Input/output capacitance	0.55	1.15	pF	1,2,3
C <sub>DIO</sub>	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,11
C <sub>DDQS</sub>	Input/output capacitance delta DQS and DQS#	-	0.05	pF	1,2,3,5
C <sub>CK</sub>	Input capacitance, CK and CK#	0.2	0.7	pF	1,3
C <sub>DCK</sub>	Input capacitance delta CK and CK#	-	0.05	pF	1,3,4
C <sub>I</sub>	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.7	pF	1,3,6
C <sub>DI_CTRL</sub>	Input capacitance delta (All CTRL pins only)	-0.1	0.1	pF	1,3,7,8
C <sub>DI_ADD_CMD</sub>	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	pF	1,2,9,10
C <sub>ALERT</sub>	Input/output capacitance of ALERT	0.5	1.5	pF	1,3
C <sub>ZQ</sub>	Input/output capacitance of ZQ	-	2.3	pF	1,3,12
C <sub>TEN</sub>	Input capacitance of TEN	0.2	2.3	pF	1,3,13

Note 1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by deem bedding the package L and C parasitic. The capacitance is measured with V<sub>DD</sub>, V<sub>DDQ</sub>, V<sub>SS</sub>, V<sub>SSQ</sub> applied with all other signal pins floating. Measurement procedure TBD. Used to define a differential signal slew-rate.

Note 2. DQ, DM#, DQS, DQS#. Although the DM pins have different functions, the loading matches DQ and DQS.

Note 3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

Note 4. Absolute value CK-CK#.

Note 5. Absolute value of C<sub>IO</sub>(DQS) - C<sub>IO</sub>(DQS#).

Note 6. C<sub>I</sub> applies to ODT, CS#, CKE, A0-A16, BA0-BA1, BG0, RAS#/A16, CAS#/A15, WE#/A14, ACT# and PAR.

Note 7. C<sub>DI\_CTRL</sub> applies to ODT, CS# and CKE.

Note 8. C<sub>DI\_CTRL</sub> = C<sub>I</sub>(CTRL) - 0.5 x ( C<sub>I</sub>(CLK) + C<sub>I</sub>(CLK#)).

Note 9. C<sub>DI\_ADD\_CMD</sub> applies to, A0-A16, BA0-BA1, BG0, RAS#/A16, CAS#/A15, WE#/A14, ACT# and PAR.

Note 10. C<sub>DI\_ADD\_CMD</sub> = C<sub>I</sub>(ADD\_CMD) - 0.5 x ( C<sub>I</sub>(CLK) + C<sub>I</sub>(CLK#)).

Note 11. C<sub>DIO</sub> = C<sub>IO</sub>(DQ,DM) - 0.5 x (C<sub>IO</sub>(DQS) + C<sub>IO</sub>(DQS#)).

Note 12. Maximum external load capacitance on ZQ pin: TBD pF.

Note 13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to V<sub>SS</sub>. In this case C<sub>TEN</sub> might not be valid and system shall verify TEN signal with vendor specific information.

**Table 79. DRAM package electrical specifications**

Symbol	Parameter	DDR4-2400/2666		Unit	Note
		Min.	Max.		
Z <sub>IO</sub>	Input/output Zpkg	45	85	Ω	1,2,4,5,10
T <sub>dIO</sub>	Input/output Pkg Delay	14	42	ps	1,3,4,5,10
L <sub>io</sub>	Input/Output Lpkg	-	3.4	nH	10,11
C <sub>io</sub>	Input/Output Cpkg	-	0.82	pF	10,12
Z <sub>IO DQS</sub>	DQS, DQS# Zpkg	45	85	Ω	1,2,5,10
T <sub>dIO DQS</sub>	DQS, DQS# Pkg Delay	14	45	ps	1,3,5,10
L <sub>io DQS</sub>	DQS Lpkg	-	3.4	nH	10,11
C <sub>io DQS</sub>	DQS Cpkg	-	0.82	pF	10,12
DZ <sub>DIO DQS</sub>	Delta Zpkg UDQS, UDQS#	-	10	Ω	1,2,5,7
	Delta Zpkg LDQS, LDQS#	-	10	Ω	1,3,5,7
DT <sub>dIO DQS</sub>	Delta Delay UDQS, UDQS#	-	5	ps	1,2,5,9,10
	Delta Delay LDQS, LDQS#	-	5	ps	1,3,5,9,10
Z <sub>I CTRL</sub>	Input CTRL pins Zpkg	50	90	Ω	10,11
T <sub>dI CTRL</sub>	Input CTRL pins Pkg Delay	14	42	ps	10,12
L <sub>I CTRL</sub>	Input CTRL Lpkg	-	3.4	nH	1,2,5,8,10
C <sub>I CTRL</sub>	Input CTRL Cpkg	-	0.7	pF	1,3,5,8,10
Z <sub>IADD CMD</sub>	Input- CMD ADD pins Zpkg	50	90	Ω	10,11
T <sub>dIADD_CMD</sub>	Input- CMD ADD pins Pkg Delay	14	52	ps	10,12
L <sub>I ADD CMD</sub>	Input CMD ADD Lpkg	-	3.9	nH	1,2,5,10
C <sub>I ADD CMD</sub>	Input CMD ADD Cpkg	-	0.86	pF	1,3,5,10
Z <sub>CK</sub>	CLK# Zpkg	50	90	Ω	10,11
T <sub>dCK</sub>	CLK# Pkg Delay	14	42	ps	10,12
L <sub>I CLK</sub>	Input CLK Lpkg	-	3.4	nH	1,2,5,6
C <sub>I CLK</sub>	Input CLK Cpkg	-	0.7	pF	1,3,5,6
DZ <sub>DCK</sub>	Delta Zpkg CLK#	-	10	Ω	1,2,5,10
DT <sub>dCK</sub>	Delta Delay CLK#	-	5	ps	1,3,5,10
Z <sub>OZQ</sub>	ZQ Zpkg	-	100	Ω	1,2,5,10
T <sub>dO ZQ</sub>	ZQ Delay	20	90	ps	1,3,5,10
Z <sub>O ALERT</sub>	ALERT Zpkg	40	100	Ω	1,2,4,5,10
T <sub>dO ALERT</sub>	ALERT Delay	20	55	ps	1,3,4,5,10

Note 1. This parameter is not subject to production test. It is verified by design and characterization. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with V<sub>DD</sub>, V<sub>DDQ</sub>, V<sub>SS</sub>, V<sub>SSQ</sub> shorted with all other signal pins floating. The inductance is measured with V<sub>DD</sub>, V<sub>DDQ</sub>, V<sub>SS</sub>, V<sub>SSQ</sub> shorted and all other signal pins shorted at the die side (not pin). Measurement procedure TBD.

Note 2. Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

$$Z_{pkg} \text{ (total per pin)} = \text{SQRT} (L_{pkg}/C_{pkg}).$$

Note 3. Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

$$T_{d} \text{ (total per pin)} = \text{SQRT} (L_{pkg} \times C_{pkg}).$$

Note 4. Z<sub>IO</sub> and T<sub>dIO</sub> applies to DQ, DM.

Note 5. This parameter applies to monolithic devices only.

Note 6. Absolute value of Z<sub>CK</sub>-Z<sub>CK#</sub> for impedance(Z) or absolute value of T<sub>dCK</sub>-T<sub>dCK#</sub> for delay(Td).

Note 7. Absolute value of Z<sub>IO(DQS)</sub>-Z<sub>IO(DQS#)</sub> for impedance(Z) or absolute value of T<sub>dIO(DQS)</sub>-T<sub>dIO(DQS#)</sub> for delay(Td).

Note 8. Z<sub>IADD\_CMD</sub> & T<sub>dIADD\_CMD</sub> applies to A0-A13, ACT#, BA0-BA1, BG0, RAS#/A16, CAS#/A15, WE#/A14 and PAR.

Note 9. Z<sub>I CTRL</sub> & T<sub>dI CTRL</sub> applies to ODT, CS# and CKE.

Note 10. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.

Note 11. It is assumed that Lpkg can be approximated as Lpkg = Zo x Td.

Note 12. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo.

## I<sub>DD</sub> and I<sub>DDQ</sub> Specification Parameters and Test conditions

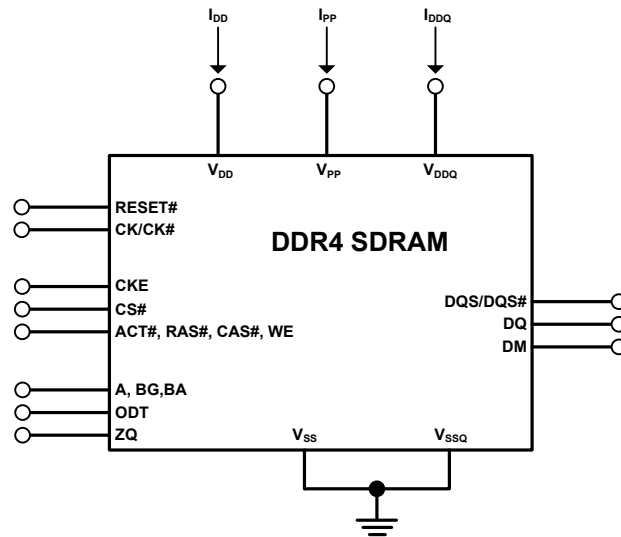
In this chapter, I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurement conditions such as test load and patterns are defined and setup and test load for I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurements are also described here.

- I<sub>DD</sub> currents (such as I<sub>DD0</sub>, I<sub>DD0A</sub>, I<sub>DD1</sub>, I<sub>DD1A</sub>, I<sub>DD2N</sub>, I<sub>DD2NA</sub>, I<sub>DD2NL</sub>, I<sub>DD2NT</sub>, I<sub>DD2P</sub>, I<sub>DD2Q</sub>, I<sub>DD3N</sub>, I<sub>DD3NA</sub>, I<sub>DD3P</sub>, I<sub>DD4R</sub>, I<sub>DD4RA</sub>, I<sub>DD4W</sub>, I<sub>DD4WA</sub>, I<sub>DD5B</sub>, I<sub>DD5F2</sub>, I<sub>DD5F4</sub>, I<sub>DD6N</sub>, I<sub>DD6E</sub>, I<sub>DD6R</sub>, I<sub>DD6A</sub>, I<sub>DD7</sub> and I<sub>DD8</sub>) are measured as time-averaged currents with all V<sub>DD</sub> balls of the DDR4 SDRAM under test tied together. Any I<sub>PP</sub> or I<sub>DDQ</sub> current is not included in I<sub>DD</sub> currents.
- I<sub>PP</sub> currents have the same definition as I<sub>DD</sub> except that the current on the V<sub>PP</sub> supply is measured.
- I<sub>DDQ</sub> currents (such as I<sub>DDQ2NT</sub> and I<sub>DDQ4R</sub>) are measured as time-averaged currents with all V<sub>DDQ</sub> balls of the DDR4 SDRAM under test tied together. Any I<sub>DD</sub> current is not included in I<sub>DDQ</sub> currents.

Attention: I<sub>DDQ</sub> values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power. In DRAM module application, I<sub>DDQ</sub> cannot be measured separately since V<sub>DD</sub> and V<sub>DDQ</sub> are using one merged-power layer in Module PCB.

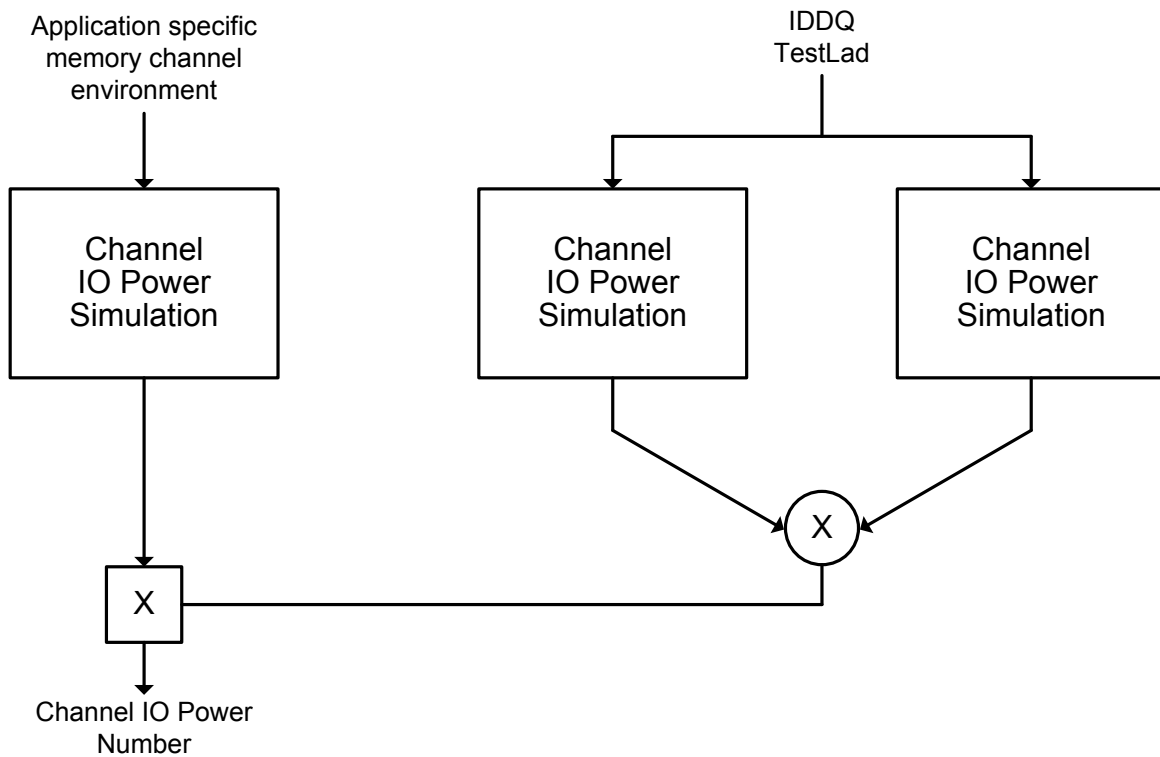
For I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurements, the following definitions apply:

- “0” and “LOW” is defined as  $V_{IN} \leq V_{ILAC(max)}$ .
- “1” and “HIGH” is defined as  $V_{IN} \geq V_{IHAC(min)}$ .
- “MID-LEVEL” is defined as inputs are  $V_{REF} = V_{DD} / 2$ .
- Timings used for I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> Measurement-Loop Patterns are described Timings used for I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> Measurement-Loop Patterns.
- Basic I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> Measurement Conditions are described in: Basic I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> Measurement Conditions.
- Detailed I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> are described in table: I<sub>DD0</sub>, I<sub>DD0A</sub> and I<sub>PP0</sub> Measurement-Loop Pattern through I<sub>DD7</sub> Measurement-Loop Pattern.
- I<sub>DD</sub> Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  - R<sub>ON</sub> = RZQ/7 (34 Ohm in MR1);
  - R<sub>TT\_NOM</sub> = RZQ/6 (40 Ohm in MR1);
  - R<sub>TT\_WR</sub> = RZQ/2 (120 Ohm in MR2);
  - R<sub>TT\_PARK</sub> = Disable;
  - Qoff = 0B (Output Buffer enabled) in MR1
  - CRC disabled in MR2;
  - CA parity feature disabled in MR5;
  - Gear down mode disabled in MR3
  - Read/Write DBI disabled in MR5;
  - DM disabled in MR5
- Attention: The I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> Measurement-Loop Patterns need to be executed at least one time before actual I<sub>DD</sub> or I<sub>DDQ</sub> measurement is started.
- Define D = {CS#, ACT#, RAS#, CAS#, WE#}:= {HIGH, LOW, LOW, LOW, LOW}; apply BG/BA changes when directed.
- Define D# = {CS#, ACT#, RAS#, CAS#, WE#}:= {HIGH, HIGH, HIGH, HIGH, HIGH}; apply invert of BG/BA changes when directed above.



NOTE 1. DIMM level Output test load condition may be different from above.

**Figure 177. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements**



**Figure 178. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement**



**Table 80. Timings used for IDD, IPP and IDDQ Measurement**

Symbol		DDR4-2400	DDR4-2666	Unit
tCK		0.833	0.75	ns
CL		17	19	nCK
CWL		16	18	nCK
nRCD		17	19	nCK
nRC		57	62	nCK
nRAS		39	43	nCK
nRP		17	19	nCK
nFAW	x4	16	16	nCK
	x8	26	28	nCK
	x16	36	40	nCK
nRRDS	x4	4	4	nCK
	x8	4	4	nCK
	x16	7	7	nCK
nRRDL	x4	6	7	nCK
	x8	6	7	nCK
	x16	8	9	nCK
tCCD_S		4	4	nCK
tCCD_L		6	7	nCK
tWTR_S		3	4	nCK
tWTR_L		9	10	nCK
nRFC 4Gb		313	347	nCK

**Table 81. Basic IDD, IPP and IDDQ Measurement Conditions**

Symbol	Description
IDD0	<b>Operating One Bank Active-Precharge Current (AL=0)</b> CKE: High; External clock: On; tCK, nRC, nRAS, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VDDQ; DM#: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IDD0A	<b>Operating One Bank Active-Precharge Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD0
IPP0	<b>Operating One Bank Active-Precharge IPP Current</b> Same condition with IDD0
IDD1	<b>Operating One Bank Active-Read-Precharge Current (AL=0)</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling according to IDD Loop table; DM#: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IDD1A	<b>Operating One Bank Active-Read-Precharge Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD1
IPP1	<b>Operating One Bank Active-Read-Precharge IPP Current</b> Same condition with IDD1
IDD2N	<b>Precharge Standby Current (AL=0)</b> CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IDD2NA	<b>Precharge Standby Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD2N
IPP2N	<b>Precharge Standby IPP Current</b> Same condition with IDD2N
IDD2NT	<b>Precharge Standby ODT Current</b> CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VSSQ; DM#: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: toggling according to IDD Loop table; Pattern Details: see to IDD Loop table
IDDQ2NT (Optional)	<b>Precharge Standby ODT IDDQ Current</b> Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	<b>Precharge Standby Current with CAL enabled</b> Same definition like for IDD2N, CAL enabled <sup>3</sup>
IDD2NG	<b>Precharge Standby Current with Gear Down mode enabled</b> Same definition like for IDD2N, Gear Down mode enabled <sup>3,5</sup>
IDD2ND	<b>Precharge Standby Current with DLL disabled</b> Same definition like for IDD2N, DLL disabled <sup>3</sup>
IDD2N_par	<b>Precharge Standby Current with CA parity enabled</b> Same definition like for IDD2N, CA parity enabled <sup>3</sup>
IDD2P	<b>Precharge Power-Down Current</b> CKE: Low; External clock: On; tCK, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0
IPP2P	<b>Precharge Power-Down IPP Current</b> Same condition with IDD2P
IDD2Q	<b>Precharge Quiet Standby Current</b> CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0
IDD3N	<b>Active Standby Current</b> CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IDD3NA	<b>Active Standby Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD3N
IPP3N	<b>Active Standby IPP Current</b> Same condition with IDD3N

IDD3P	<b>Active Power-Down Current</b> CKE: Low; External clock: On; tCK, CL: see IDD timing Table; BL: 8 <sup>1</sup> ; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0
IPP3P	<b>Active Power-Down IPP Current</b> Same condition with IDD3P
IDD4R	<b>Operating Burst Read Current</b> CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8 <sup>2</sup> ; AL: 0; CS#: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: seamless read data burst with different data between one burst and the next one according to IDD Loop table; DM#: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IDD4RA	<b>Operating Burst Read Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD4R
IDD4RB	<b>Operating Burst Read Current with Read DBI</b> Read DBI enabled <sup>3</sup> , Other conditions: see IDD4R
IPP4R	<b>Operating Burst Read IPP Current</b> Same condition with IDD4R
IDDQ4R (Optional)	<b>Operating Burst Read IDDQ Current</b> Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	<b>Operating Burst Read IDDQ Current with Read DBI</b> Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	<b>Operating Burst Write Current</b> CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: seamless write data burst with different data between one burst and the next one according to IDD Loop table; DM#: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at HIGH; Pattern Details: see IDD Loop table
IDD4WA	<b>Operating Burst Write Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD4W
IDD4WB	<b>Operating Burst Write Current with Write DBI</b> Write DBI enabled <sup>3</sup> , Other conditions: see IDD4W
IDD4WC	<b>Operating Burst Write Current with Write CRC</b> Write CRC enabled <sup>3</sup> , Other conditions: see IDD4W
IDD4W_p ar	<b>Operating Burst Write Current with CA Parity</b> CA Parity enabled <sup>3</sup> , Other conditions: see IDD4W
IPP4W	<b>Operating Burst Write IPP Current</b> Same condition with IDD4W
IDD5B	<b>Burst Refresh Current (1X REF)</b> CKE: High; External clock: On; tCK, CL, nRFC: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VDDQ; DM#: stable at 1; Bank Activity: REF command every nRFC (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IPP5B	<b>Burst Refresh Write IPP Current (1X REF)</b> Same condition with IDD5B
IDD5F2	<b>Burst Refresh Current (2X REF)</b> tRFC=tRFC_x2, Other conditions: see IDD5B
IPP5F2	<b>Burst Refresh Write IPP Current (2X REF)</b> Same condition with IDD5F2
IDD5F4	<b>Burst Refresh Current (4X REF)</b> tRFC=tRFC_x4, Other conditions: see IDD5B
IPP5F4	<b>Burst Refresh Write IPP Current (4X REF)</b> Same condition with IDD5F4
IDD6N	<b>Self Refresh Current: Normal Temperature Range</b> T <sub>CASE</sub> : 0 - 85°C; Low Power Auto Self Refresh (LP ASR) : Normal <sup>4</sup> ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM#: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
IPP6N	<b>Self Refresh IPP Current: Normal Temperature Range</b> Same condition with IDD6N

IDD6E	<b>Self-Refresh Current: Extended Temperature Range</b> $T_{CASE}$ : 0 - 95°C; Low Power Auto Self Refresh (LP ASR) : Extended <sup>4</sup> ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM#:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
IPP6E	<b>Self Refresh IPP Current: Extended Temperature Range</b> Same condition with IDD6E
IDD6R	<b>Self-Refresh Current: Reduced Temperature Range</b> $T_{CASE}$ : 0 - 45°C; Low Power Auto Self Refresh (LP ASR) : Reduced <sup>4</sup> ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM#:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
IPP6R	<b>Self Refresh IPP Current: Reduced Temperature Range</b> Same condition with IDD6R
IDD6A	<b>Auto Self-Refresh Current</b> $T_{CASE}$ : 0 - 95°C; Low Power Auto Self Refresh (LP ASR) : Auto <sup>4</sup> ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM#: stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
IPP6A	<b>Auto Self-Refresh IPP Current</b> Same condition with IDD6A
IDD7	<b>Operating Bank Interleave Read Current</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: CL-1; CS#: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: read data bursts with different data between one burst and the next one according to IDD Loop table; DM#: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see IDD Loop table; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IPP7	<b>Operating Bank Interleave Read IPP Current</b> Same condition with IDD7

Note 1. Burst Length: BL8 fixed by MRS: set MR0 A[1:0] =00.

Note 2. Output Buffer Enable:

- set MR1 A12 = 0: Qoff = Output buffer enabled
- set MR1 A [2:1] = 00: Output Driver Impedance Control = RZQ/7
- RTT\_NOM enable: set MR1 A [10:8] = 011: RTT\_NOM = RZQ/6
- RTT\_WR enable: set MR2 A [10:9] = 01: RTT\_WR = RZQ/2
- RTT\_PARK disable: set MR5 A [8:6] = 000

Note 3. CAL Enabled: set MR4 A [8:6] = 001: 1600 MT/s, 010: 1866MT/s, 2133MT/s, 011: 2400MT/s, 2666MT/s

Gear Down mode enabled: set MR3 A3 = 1:1/4 Rate

DLL disabled: set MR1 A0 = 0

CA parity enabled: set MR5 A [2:0] = 001:1600MT/s, 1866MT/s, 2133MT/s, 010: 2400MT/s, 2666MT/s

Read DBI enabled: set MR5 A12 = 1

Write DBI enabled: set: MR5 A11 = 1

Note 4. Low Power Array Self Refresh (LP ASR)

- set MR2 A [7:6] = 00: Normal
- set MR2 A [7:6] = 01: Reduced Temperature range
- set MR2 A [7:6] = 10: Extended Temperature range
- set MR2 A [7:6] = 11: Auto Self Refresh

Note 5.  $I_{DD2NG}$  should be measured after sync pulse (NOP) input.

Note 6. AL is not supported for x16 device.

**Table 82. IDD0, IDD0A and IPP0 Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 [2]	BA0-1	A12 /BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
		0	1-2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		0	3-4	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-	
		0	...	Repeat pattern 1...4 until nRAS - 1; truncate if necessary																		
		0	nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		0	...	Repeat pattern 1...4 until nRC - 1; truncate if necessary																		
		1	1×nRC	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=1 instead																		
		2	2×nRC	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead																		
		3	3×nRC	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=3 instead																		
		4	4×nRC	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead																		
		5	5×nRC	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=2 instead																		
		6	6×nRC	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead																		
		7	7×nRC	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=0 instead																		
		8	8×nRC	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead															For x4 and x8 only			
		9	9×nRC	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=1 instead																		
		10	10×nRC	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead																		
11	11×nRC	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=3 instead																				
12	12×nRC	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead																				
13	13×nRC	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=2 instead																				
14	14×nRC	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead																				
15	15×nRC	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=0 instead																				

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. DQ signals are V<sub>DDQ</sub>.

**Table 83. IDD1, IDD1A and IPP1 Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 [2]	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
		0	1-2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		0	3-4	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-	
		0	...	Repeat pattern 1...4 until nRCD-AL-1; truncate if necessary																		
		0	nRCD-AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF
		0	...	Repeat pattern 1...4 until nRAS-1; truncate if necessary																		
		0	nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		0	...	Repeat pattern 1...4 until nRC-1; truncate if necessary																		
		1	1×nRC+0	ACT	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	-
		1	1×nRC+1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	1×nRC+3,4	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-	
		1	...	Repeat pattern nRC+1...4 until 1×nRC+nRAS-1; truncate if necessary																		
		1	1×nRC +nRCD-AL	RD	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
		1	...	Repeat pattern 1...4 until nRAS-1; truncate if necessary																		
		1	1×nRAS+nRAS	PRE	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	-
			...	Repeat nRC+1...4 until 2×nRC-1; truncate if necessary																		
		2	2×nRC	Repeat sub-loop 0, use BG[1:0]=0, use BA[1:0]=2 instead																		
		3	3×nRC	Repeat sub-loop 1, use BG[1:0]=1, use BA[1:0]=3 instead																		
		4	4×nRC	Repeat sub-loop 0, use BG[1:0]=0, use BA[1:0]=1 instead																		
		5	5×nRC	Repeat sub-loop 1, use BG[1:0]=1, use BA[1:0]=2 instead																		
		6	6×nRC	Repeat sub-loop 0, use BG[1:0]=0, use BA[1:0]=3 instead																		
		8	7×nRC	Repeat sub-loop 1, use BG[1:0]=1, use BA[1:0]=0 instead																		
		9	9×nRC	Repeat sub-loop 1, use BG[1:0]=2, use BA[1:0]=0 instead																		
		10	10×nRC	Repeat sub-loop 0, use BG[1:0]=3, use BA[1:0]=1 instead																		
		11	11×nRC	Repeat sub-loop 1, use BG[1:0]=2, use BA[1:0]=2 instead																		
		12	12×nRC	Repeat sub-loop 0, use BG[1:0]=3, use BA[1:0]=3 instead																		
13	13×nRC	Repeat sub-loop 1, use BG[1:0]=2, use BA[1:0]=1 instead																				
14	14×nRC	Repeat sub-loop 0, use BG[1:0]=3, use BA[1:0]=2 instead																				
15	15×nRC	Repeat sub-loop 1, use BG[1:0]=2, use BA[1:0]=3 instead																				
16	16×nRC	Repeat sub-loop 0, use BG[1:0]=3, use BA[1:0]=0 instead																				

For x4  
and  
x8 only

Note 1. DQS, DQS# are used according to RD Commands, otherwise V<sub>DDQ</sub>.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V<sub>DDQ</sub>.

**Table 84. IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N\_par, IPP2, IDD3N, IDD3NA and IDD3P  
Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 [2]	BA0-1	A12 /BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>		
Toggling	Static High	0	0	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0	1	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	2	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	0
		0	3	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	0
		1	4-7	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=1 instead																	
		2	8-11	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead																	
		3	12-15	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=3 instead																	
		4	16-19	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead																	
		5	20-23	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=2 instead																	
		6	24-27	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead																	
		7	28-31	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=0 instead																	
		8	32-35	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead																	
		9	36-39	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=1 instead																	
		10	40-43	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead																	
		11	44-47	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=3 instead																	
12	48-51	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead																			
13	52-55	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=2 instead																			
14	56-59	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead																			
15	60-63	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=0 instead																			

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. DQ signals are V<sub>DDQ</sub>.

**Table 85. IDD2NT and IDDQ2NT Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 [2]	BA0-1	A12 /BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>		
Toggling	Static High	0	0	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		0	1	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		0	2	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-
		0	3	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-
		1	4-7	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 1 instead																	
		2	8-11	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 2 instead																	
		3	12-15	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 3 instead																	
		4	16-19	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 1 instead																	
		5	20-23	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 2 instead																	
		6	24-27	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 3 instead																	
		7	28-31	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 0 instead																	
		8	32-35	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 0 instead															For x4 and x8 only		
		9	36-39	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 1 instead																	
		10	40-43	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 2 instead																	
		11	44-47	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 3 instead																	
12	48-51	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 1 instead																			
13	52-55	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 2 instead																			
14	56-59	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 3 instead																			
15	60-63	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 0 instead																			

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. DQ signals are V<sub>DDQ</sub>.



**Table 86. IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 [2]	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>	
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF
		0	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		0	2-3	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
		1	5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	6-7	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-
		2	8-11	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead																
		3	12-15	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=3 instead																
		4	16-19	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead																
		5	20-23	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=2 instead																
		6	24-27	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead																
		7	28-31	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=0 instead																
		8	32-35	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead																
		9	36-39	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=1 instead																
		10	40-43	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead																
11	44-47	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=3 instead																		
12	48-51	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead																		
13	52-55	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=2 instead																		
14	56-59	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead																		
15	60-63	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=0 instead																		

For x4  
and  
x8 only

Note 1. DQS, DQS# are used according to RD Commands, otherwise V<sub>DDQ</sub>.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Read Command.

**Table 87. IDD4W, IDD4WA, IDD4WB and IDD4W<sub>par</sub> Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 [2]	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>		
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF	
		0	1	D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
		0	2-3	D#,D#	1	1	1	1	1	1	1	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-
		1	4	WR	0	1	1	0	0	0	1	1	1	0	0	0	7	F	0	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
		1	5	D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
		1	6-7	D#,D#	1	1	1	1	1	1	1	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-
		2	8-11	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead																	
		3	12-15	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=3 instead																	
		4	16-19	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead																	
		5	20-23	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=2 instead																	
		6	24-27	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead																	
		7	28-31	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=0 instead																	
		8	32-35	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead																	
		9	36-39	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=1 instead																	
		10	40-43	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead																	
11	44-47	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=3 instead																			
12	48-51	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead																			
13	52-55	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=2 instead																			
14	56-59	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead																			
15	60-63	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=0 instead																			

Note 1. DQS, DQS# are used according to WR Commands, otherwise V<sub>DDQ</sub>.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Write Command.

For x4  
and  
x8 only

**Table 88. IDD4WC Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 <sup>[2]</sup>	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>		
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF, D8=CRC	
		0	1-2	D,D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
		0	3-4	D#,D#	1	1	1	1	1	1	1	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-
		0	5	WR	0	1	1	0	0	0	1	1	1	0	0	0	7	F	0	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00, D8=CRC
		0	6-7	D,D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
		0	8-9	D#,D#	1	1	1	1	1	1	1	3 <sup>[2]</sup>	3	0	0	0	7	F	0	0	-
		2	10-14	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead																	
		3	15-19	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=3 instead																	
		4	20-24	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead																	
		5	25-29	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=2 instead																	
		6	30-34	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead																	
		7	35-39	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=0 instead																	
		8	40-44	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead																	
		9	45-49	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=1 instead																	
		10	50-54	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead																	
11	55-59	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=3 instead																			
12	60-64	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead																			
13	65-69	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=2 instead																			
14	70-74	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead																			
15	75-79	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=0 instead																			

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Write Command.

For x4  
and  
x8 only

**Table 89. IDD5B Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 [2]	BA0-1	A12 /BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>			
Toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		1	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	3	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	0	7	F	0	0	-
		1	4	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	0	7	F	0	0	-
		1	5-8	Repeat pattern 1...4, use BG[1:0]=1, BA[1:0]=1 instead																		
		1	9-12	Repeat pattern 1...4, use BG[1:0]=0, BA[1:0]=2 instead																		
		1	13-16	Repeat pattern 1...4, use BG[1:0]=1, BA[1:0]=3 instead																		
		1	17-20	Repeat pattern 1...4, use BG[1:0]=0, BA[1:0]=1 instead																		
		1	21-24	Repeat pattern 1...4, use BG[1:0]=1, BA[1:0]=2 instead																		
		1	25-28	Repeat pattern 1...4, use BG[1:0]=0, BA[1:0]=3 instead																		
		1	29-32	Repeat pattern 1...4, use BG[1:0]=1, BA[1:0]=0 instead																		
		1	33-36	Repeat pattern 1...4, use BG[1:0]=2, BA[1:0]=0 instead																		
		1	37-40	Repeat pattern 1...4, use BG[1:0]=3, BA[1:0]=1 instead																		
		1	41-44	Repeat pattern 1...4, use BG[1:0]=2, BA[1:0]=2 instead																		
		1	45-48	Repeat pattern 1...4, use BG[1:0]=3, BA[1:0]=3 instead																		
		1	49-52	Repeat pattern 1...4, use BG[1:0]=2, BA[1:0]=1 instead																		
		1	53-56	Repeat pattern 1...4, use BG[1:0]=3, BA[1:0]=2 instead																		
		1	57-60	Repeat pattern 1...4, use BG[1:0]=2, BA[1:0]=3 instead																		
		1	61-64	Repeat pattern 1...4, use BG[1:0]=3, BA[1:0]=0 instead																		
2	65...nRFC-1	Repeat sub-loop 1, Truncate, if necessary																				

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care for x16 device.

Note 3. DQ signals are V<sub>DDQ</sub>.

For x4  
and  
x8 only

**Table 90. IDD7 Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/ A16	CAS#/ A15	WE#/ A14	ODT	BG0-1 [2]	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
		0	1	RDA	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF	
		0	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		0	3	D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	0	7	F	0	-	
		0	...	Repeat pattern 2...3, until nRRD - 1, if nRRD > 4. Truncate if necessary																		
		1	nRRD	ACT	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	
		1	nRRD+1	RDA	0	1	1	0	1	0	1	0	1	1	0	0	1	0	0	0	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
		1	...	Repeat pattern 2...3, until 2xnRRD - 1, if nRRD > 4. Truncate if necessary																		
		2	2xnRRD	Repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																		
		3	3xnRRD	Repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead																		
		4	4xnRRD	Repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4xnRRD. Truncate if necessary																		
		5	nFAW	Repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																		
		6	nFAW+ nRRD	Repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead																		
		7	nFAW+ 2xnRRD	Repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																		
		8	nFAW+ 3xnRRD	Repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead																		
		9	nFAW+ 4xnRRD	Repeat Sub-Loop 4																		
		10	2xnFAW	Repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																		
		11	2xnFAW+ nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 1 instead																		
		12	2xnFAW+ 2xnRRD	Repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead																		
		13	2xnFAW+ 3xnRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 3 instead																		
		14	2xnFAW+ 4xnRRD	Repeat Sub-Loop 4																		
15	3xnFAW	Repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																				
16	3xnFAW+ nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 2 instead																				
17	3xnFAW+ 2xnRRD	Repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																				
18	3xnFAW+ 3xnRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 0 instead																				
19	3xnFAW+ 4xnRRD	Repeat Sub-Loop 4																				
20	4xnFAW	Repeat pattern 2 ... 3 until nRC - 1, if nRC > 4xnFAW. Truncate if necessary																				

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V<sub>DDQ</sub>.

**Table 91. IDD and IDDQ Specification Parameters and Test conditions**

Parameter	Symbol	DDR4-2400	DDR4-2666	Unit
		Max.	Max.	
Operating One Bank Active-Precharge Current (AL=0)	I <sub>DD0</sub>	86	92	mA
Operating One Bank Active-Precharge IPP Current	I <sub>PP0</sub>	8	9	mA
Operating One Bank Active-Read-Precharge Current (AL=0)	I <sub>DD1</sub>	128	142	mA
Operating One Bank Active-Read-Precharge IPP Current	I <sub>PP1</sub>	8	9	mA
Precharge Standby Current (AL=0)	I <sub>DD2N</sub>	67	74	mA
Precharge Standby IPP Current	I <sub>PP2N</sub>	6	7	mA
Precharge Standby ODT Current	I <sub>DD2NT</sub>	86	97	mA
Precharge Standby Current with CAL enabled	I <sub>DD2NL</sub>	59	63	mA
Precharge Standby Current with Gear Down mode enabled	I <sub>DD2NG</sub>	65	71	mA
Precharge Standby Current with DLL disabled	I <sub>DD2ND</sub>	49	52	mA
Precharge Standby Current with CA parity enabled	I <sub>DD2N_par</sub>	82	94	mA
Precharge Power-Down Current CKE	I <sub>DD2P</sub>	40	44	mA
Precharge Power-Down IPP Current	I <sub>PP2P</sub>	6	7	mA
Precharge Quiet Standby Current	I <sub>DD2Q</sub>	67	75	mA
Active Standby Current	I <sub>DD3N</sub>	78	86	mA
Active Standby IPP Current	I <sub>PP3N</sub>	6	7	mA
Active Power-Down Current	I <sub>DD3P</sub>	64	67	mA
Active Power-Down IPP Current	I <sub>PP3P</sub>	6	7	mA
Operating Burst Read Current	I <sub>DD4R</sub>	188	205	mA
Operating Burst Read Current with Read DBI	I <sub>DD4RB</sub>	190	206	mA
Operating Burst Read IPP Current	I <sub>PP4R</sub>	6	7	mA
Operating Burst Write Current	I <sub>DD4W</sub>	211	230	mA
Operating Burst Write Current with Write DBI	I <sub>DD4WB</sub>	199	215	mA
Operating Burst Write Current with Write CRC	I <sub>DD4WC</sub>	194	210	mA
Operating Burst Write Current with CA Parity	I <sub>DD4W_par</sub>	215	204	mA
Operating Burst Write IPP Current	I <sub>PP4W</sub>	6	7	mA
Burst Refresh Current (1X REF)	I <sub>DD5B</sub>	170	180	mA
Burst Refresh Write IPP Current (1X REF)	I <sub>PP5B</sub>	24	27	mA

Burst Refresh Current (2X REF)		I <sub>DD5F2</sub>	179	189	mA
Burst Refresh Write IPP Current (2X REF)		I <sub>PP5F2</sub>	25	29	mA
Burst Refresh Current (4X REF)		I <sub>DD5F4</sub>	147	160	mA
Burst Refresh Write IPP Current (4X REF)		I <sub>PP5F4</sub>	18	20	mA
Self Refresh Current: Normal Temperature Range	T <sub>C</sub> = -40~85°C	I <sub>DD6N</sub>	30	30	mA
Self Refresh IPP Current: Normal Temperature Range		I <sub>PP6N</sub>	6	6	mA
Self-Refresh Current: Extended Temperature Range)	T <sub>C</sub> = -40~95°C	I <sub>DD6E</sub>	36	36	mA
Self Refresh IPP Current: Extended Temperature Range		I <sub>PP6E</sub>	8	8	mA
Self-Refresh Current: Reduced Temperature Range	T <sub>C</sub> = -40~45°C	I <sub>DD6R</sub>	25	25	mA
Self Refresh IPP Current: Reduced Temperature Range		I <sub>PP6R</sub>	4	4	mA
Auto Self-Refresh Current	T <sub>C</sub> = -40~85°C	I <sub>DD6A</sub>	30	30	mA
Auto Self-Refresh IPP Current		I <sub>PP6A</sub>	6	6	mA
Operating Bank Interleave Read Current		I <sub>DD7</sub>	234	235	mA
Operating Bank Interleave Read IPP Current		I <sub>PP7</sub>	33	40	mA

**Table 92. Timing Parameters**

Symbol	Parameter	DDR4-2400		DDR4-2666		Unit			
		Min.	Max.	Min.	Max.				
tAA	Internal read command to first data	14.16	18	14.25	18	ns			
tAA_DBI	Internal read command to first data with read DBI enabled	$t_{AA(min)} + 3 t_{CK}$	$t_{AA(max)} + 3 t_{CK}$	$t_{AA(min)} + 3 t_{CK}$	$t_{AA(max)} + 3 t_{CK}$	ns			
tRCD	ACT to internal read or write delay time	14.16	-	14.25	-	ns			
tRP	PRE command period	14.16	-	14.25	-	ns			
tRAS	ACT to PRE command period	32	$9 \times t_{REFI}$	32	$9 \times t_{REFI}$	ns			
tRC	ACT to ACT or REF command period	46.16	-	46.25	-	ns			
Speed Bins		CWL	Normal	Read DBI	Min.	Max.	Min.	Max.	Unit
tCK(avg)	ACT to ACT or REF command period	9	10	12	1.5	1.6	1.5	1.6	ns
		9,11	11	13	1.25	<1.5	1.25	<1.5	ns
		9,11	12	14	1.25	<1.5	1.25	<1.5	ns
		10,12	13	15	1.071	<1.25	1.071	<1.25	ns
		10,12	14	16	1.071	<1.25	1.071	<1.25	ns
		11,14	15	18	0.937	<1.071	0.937	<1.071	ns
		11,14	16	19	0.937	<1.071	0.937	<1.071	ns
		12,16	17	20	0.833	<0.937	0.833	<0.937	ns
		12,16	18	21	-	-	0.833	<0.937	ns
14,18	19	22	-	-	0.75	<0.833	ns		
Clock Timing									
tCK (DLL_OFF)	Minimum Clock Cycle Time (DLL off mode)	8	20	8	20	8	20	ns	
tCK(avg) <sup>35,36</sup>	Average clock period	0.833	<0.937	0.750	<0.833	ns			
tCH(avg)	Average high pulse width	0.48	0.52	0.48	0.52	tCK			
tCL(avg)	Average low pulse width	0.48	0.52	0.48	0.52	tCK			
tCK(abs)	Absolute Clock Period	$t_{CK(avg)min} + t_{JIT(per)min\_tot}$	$t_{CK(avg)max} + t_{JIT(per)max\_tot}$	$t_{CK(avg)min} + t_{JIT(per)min\_tot}$	$t_{CK(avg)max} + t_{JIT(per)max\_tot}$	tCK			
tCH(abs) <sup>23</sup>	Absolute clock high pulse width	0.45	-	0.45	-	tCK			
tCL(abs) <sup>24</sup>	Absolute clock low pulse width	0.45	-	0.45	-	tCK			
JIT(per)_tot <sup>25</sup>	Clock Period Jitter- total	-42	42	-38	38	ps			
JIT(per)_dj <sup>26</sup>	Clock Period Jitterdeterministic	-21	21	-19	19	ps			
tJIT(per, lck)	Clock Period Jitter during DLL locking period	-33	33	-30	30	ps			
tJIT(cc)	Cycle to Cycle Period Jitter	-	83	-	75	ps			
tJIT(cc, lck)	Cycle to Cycle Period Jitter during DLL locking period	-	67	-	60	ps			
tJIT(duty)	Duty Cycle Jitter	TBD	TBD	TBD	TBD	ps			
tERR(2per)	Cumulative error across 2 cycles	-61	61	-55	55	ps			
tERR(3per)	Cumulative error across 3 cycles	-73	73	-66	66	ps			
tERR(4per)	Cumulative error across 4 cycles	-81	81	-73	73	ps			
tERR(5per)	Cumulative error across 5 cycles	-87	87	-78	78	ps			
tERR(6per)	Cumulative error across 6 cycles	-92	92	-83	83	ps			
tERR(7per)	Cumulative error across 7 cycles	-97	97	-87	87	ps			
tERR(8per)	Cumulative error across 8 cycles	-101	101	-91	91	ps			
tERR(9per)	Cumulative error across 9 cycles	-104	104	-94	94	ps			
tERR(10per)	Cumulative error across 10 cycles	-107	107	-96	96	ps			
tERR(11per)	Cumulative error across 11 cycles	-110	110	-99	99	ps			
tERR(12per)	Cumulative error across 12 cycles	-112	112	-101	101	ps			
tERR(13per)	Cumulative error across 13 cycles	-114	114	-103	103	ps			
tERR(14per)	Cumulative error across 14 cycles	-116	116	-104	104	ps			
tERR(15per)	Cumulative error across 15 cycles	-118	118	-106	106	ps			
tERR(16per)	Cumulative error across 16 cycles	-120	120	-108	108	ps			
tERR(17per)	Cumulative error across 17 cycles	-122	122	-110	110	ps			



tERR(18per)	Cumulative error across 18 cycles	-124	124	-112	112	ps
tERR(nper)	Cumulative error across n =13, 14 . . . 49, 50 cycles	$tERR(nper)_{min} = ((1 + 0.68 \ln(n)) \times t_{JIT(per\_total\ min)})$ $tERR(nper)_{max} = ((1 + 0.68 \ln(n)) \times t_{JIT(per\_total\ max)})$				ps
tIS(base)	Command and Address setup time to CK, CK# referenced to VIH(AC)/VIL(AC) levels	62	-	55	-	ps
tIS(VREF)	Command and Address setup time to CK, CK# referenced to VREF levels	162	-	145	-	ps
tIH(base)	Command and Address hold time to CK, CK# referenced to VIH(AC)/VIL(AC) levels	87	-	80	-	ps
tIH(VREF)	Command and Address hold time to CK, CK# referenced to VREF levels	162	-	145	-	ps
tIPW	Control and Address Input pulse width for each input	410	-	385	-	ps
<b>Command and Address Timing</b>						
tCCD_L <sup>34</sup>	CAS# to CAS# command delay for same bank group	max(5nCK, 5ns)	-	max(5nCK, 5ns)	-	tck
tCCD_S <sup>34</sup>	CAS# to CAS# command delay for different bank group	4	-	4	-	tck
tRRD_S(2K) <sup>34</sup>	Activate to Activate Command delay to different bank group for 2KB page size	max(4nCK, 5.3ns)	-	max(4nCK, 5.3ns)	-	tck
tRRD_L(2K) <sup>34</sup>	Activate to Activate Command delay to same bank group for 2KB page size	max(4nCK, 6.4ns)	-	max(4nCK, 6.4ns)	-	tck
tFAW_2K <sup>34</sup>	Four activate window for 2KB page size	max(28nCK, 30ns)	-	max(28nCK, 30ns)	-	ns
twTR_S <sup>1,2,34</sup>	Delay from start of internal write transaction to internal read command for different bank group	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	
twTR_L <sup>1,34</sup>	Delay from start of internal write transaction to internal read command for same bank group	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
tRTP <sup>34</sup>	Internal Read Command to Precharge Command delay	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
tWR <sup>1</sup>	WRITE recovery time	15	-	15	-	ns
tWR_CRC_DM <sup>1,28</sup>	Write recovery time when CRC and DM are enabled	tWR + max(5nCK, 3.75ns)	-	tWR + max(5nCK, 3.75ns)	-	ns
twTR_S_CRC_DM <sup>2,29,34</sup>	delay from start of internal write transaction to internal read command for different bank groups with both CRC and DM enabled	twTR_S + max(5nCK, 3.75ns)	-	twTR_S + max(5nCK, 3.75ns)	-	ns
twTR_L_CRC_DM <sup>3,30,34</sup>	delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	twTR_L + max(5nCK, 3.75ns)	-	twTR_L + max(5nCK, 3.75ns)	-	ns
tDLLK	DLL locking time	768	-	854	-	tck
tMRD	Mode Register Set command cycle time	8	-	8	-	tck
tMOD <sup>50</sup>	Mode Register Set command update delay	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	tck
tMPRR <sup>33</sup>	Multi-Purpose Register Recovery Time	1	-	1	-	tck
tWR_MPR	Multi Purpose Register Write Recovery Time	tMOD(min) + AL + PL	-	tMOD(min) + AL + PL	-	tck
tDAL(min)	Auto precharge write recovery + precharge time	Programmed WR + roundup (trp/ tck(avg))				tck
tPDA_S <sup>45,47</sup>	DQ0 driven to 0 setup time to first DQS rising edge	0.5	-	0.5	-	UI
tPDA_H <sup>46,47</sup>	DQ0 driven to 0 hold time from last DQS falling edge	0.5	-	0.5	-	UI
<b>CS# to Command Address Latency</b>						
tCAL	CS# to Command Address Latency	max(3nCK, 3.748ns)	-	5	-	tck
tMRD_tCAL	Mode Register Set command cycle time in CAL mode	tMOD + tCAL	-	tMOD + tCAL	-	tck
tMOD_tCAL	Mode Register Set update delay in CAL mode	tMOD + tCAL	-	tMOD + tCAL	-	tck
<b>DRAM Data Timing</b>						
tdQSQ <sup>13,18,39,49</sup>	DQS, DQS# to DQ skew, per group, per access	-	0.17	-	0.18	tck
tQH <sup>13,17,18,39,49</sup>	DQ output hold time per group, per access from DQS,DQS#	0.74	-	0.74	-	tck
tdVWd <sup>17,18,39,49</sup>	Data Valid Window per device per UI: (tQH - tdQSQ) of each UI on a given DRAM	0.64	-	TBD	-	UI
tdVWp <sup>17,18,39,49</sup>	Data Valid Window per pin per UI: (tQH - tdQSQ) each UI on a pin of a given DRAM	0.72	-	0.72	-	UI
tLZ(DQ) <sup>39</sup>	DQ low impedance time from CK, CK#	-330	175	-310	170	ps
tHZ(DQ) <sup>39</sup>	DQ high impedance time from CK, CK#	-	175	-	170	ps
<b>Data Strobe Timing</b>						
trPRE <sup>39,40,44</sup>	DQS, DQS# differential Read Preamble (1 clock preamble)	0.9	-	0.9	-	tck
trPRE2 <sup>39,41,44</sup>	DQS, DQS# differential Read Preamble (2 clock preamble)	1.8	-	1.8	-	tck
trPST <sup>39,45</sup>	DQS, DQS# differential Read Postamble	0.33	-	0.33	-	tck
tQSH <sup>21,39</sup>	DQS, DQS# differential output high time	0.4	-	0.4	-	tck

tQSL <sup>20,39</sup>	DQS, DQS# differential output low time	0.4	-	0.4	-	tck
tWPRE <sup>42</sup>	DQS, DQS# differential Write Preamble (1 clock preamble)	0.9	-	0.9	-	tck
tWPRE2 <sup>43</sup>	DQS, DQS# differential Write Preamble (2 clock preamble)	1.8	-	1.8	-	tck
tWPST	DQS, DQS# differential Write Postamble	0.33	-	0.33	-	tck
tLZ(DQS) <sup>39</sup>	DQS, DQS# low impedance time (Referenced from RL-1)	-330	175	-310	170	ps
tHZ(DQS) <sup>39</sup>	DQS, DQS# high impedance time (Referenced from RL+BL/2)	-	175	-	170	ps
tdQSL	DQS, DQS# differential input low pulse width	0.46	0.54	0.46	0.54	tck
tdQSH	DQS, DQS# differential input high pulse width	0.46	0.54	0.46	0.54	tck
tdQSS <sup>42</sup>	DQS, DQS# rising edge to CK, CK# rising edge (1 clock preamble)	-0.27	0.27	-0.27	0.27	tck
tdQSS2 <sup>43</sup>	DQS, DQS# rising edge to CK, CK# rising edge (2 clock preamble)	TBD	TBD	TBD	TBD	tck
tbSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	0.18	-	tck
tdSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	0.18	-	tck
tdQSCK(DLL On) 37,38,39	DQS, DQS# rising edge output timing location from rising CK, CK# with DLL On mode	-175	175	-170	170	ps
tdQSCKI(DLL On) 37,38,39	DQS, DQS# rising edge output variance window per DRAM	-	290	-	270	ps
<b>Calibration Timing</b>						
tzQinit	Power-up and Reset calibration time	1024	-	1024	-	tck
tzQoper	Normal operation Full calibration time	512	-	512	-	tck
tzQCS	Normal operation Short calibration time	128	-	128	-	tck
<b>Reset/Self Refresh Timing</b>						
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	tck
tXS	Exit Self Refresh to commands not requiring a locked DLL	tRFC(min) + 10ns	-	tRFC(min) + 10ns	-	tck
tXS_ABORT(min)	SRX to commands not requiring a locked DLL in Self Refresh ABORT	tRFC4(min) + 10ns	-	tRFC4(min) + 10ns	-	tck
tXS_FAST(min)	Exit Self Refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	tRFC4(min) + 10ns	-	tRFC4(min) + 10ns	-	tck
tXSDLL	Exit Self Refresh to commands requiring a locked DLL	tDLLK(min)	-	tDLLK(min)	-	tck
tCKESR	Minimum CKE low width for Self refresh entry to exit timing	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	tck
tCKESR_PAR	Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKE(min) + 1nCK + PL	-	tCKE(min) + 1nCK + PL	-	tck
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	tck
tCKSRE_PAR	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	max(5nCK, 10ns) + PL	-	max(5nCK, 10ns) + PL	-	tck
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	tck
<b>Power Down Timing</b>						
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	tck
tCKE <sup>31,32</sup>	CKE minimum pulse width	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	tck
tCPDED	Command pass disable delay	4	-	4	-	tck
tPD <sup>6</sup>	Power Down Entry to Exit Timing	tCKE(min)	9 x tREFI	tCKE(min)	9 x tREFI	tck
tACTPDEN <sup>7</sup>	Timing of ACT command to Power Down entry	2	-	2	-	tck
tPRPDEN <sup>7</sup>	Timing of PRE or PREA command to Power Down entry	2	-	2	-	tck
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL + 4 + 1	-	RL + 4 + 1	-	tck
tWRPDEN <sup>4</sup>	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	tck
tWRAPDEN <sup>5</sup>	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	tck
tWRPBC4DEN <sup>4</sup>	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	tck
tWRAPBC4DEN <sup>5</sup>	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	tck
tREFPDEN <sup>7</sup>	Timing of REF command to Power Down entry	2	-	2	-	tck
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	tMOD(min)	-	tck
<b>PDA Timing</b>						

tMRD_PDA	Mode Register Set command cycle time in PDA mode	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	ns
tMOD_PDA	Mode Register Set command update delay in PDA mode	tMOD		tMOD		ns
<b>ODT Timing</b>						
tAONAS	Asynchronous R <sub>TT</sub> turn-on delay (Power-Down with DLL frozen)	1.0	9.0	1.0	9.0	ns
tAOFAS	Asynchronous R <sub>TT</sub> turn-off delay (Power-Down with DLL frozen)	1.0	9.0	1.0	9.0	ns
tADC	R <sub>TT</sub> dynamic change skew	0.3	0.7	0.3	0.7	tCK
<b>Write Leveling Timing</b>						
tWLMRD <sup>12</sup>	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	40	-	tCK
tWLDQSEN <sup>12</sup>	DQS/DQS# delay after write leveling mode is programmed	25	-	25	-	tCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS/DQS# crossing	0.13	-	0.13	-	tCK
tWLH	Write leveling hold time from rising DQS/DQS# crossing to rising CK, CK# crossing	0.13	-	0.13	-	tCK
twLO	Write leveling output delay	0	9.5	0	9.5	ns
twLOE	Write leveling output error	0	2	0	2	ns
<b>CA Parity Timing</b>						
tPAR_UNKNOWN	Commands not guaranteed to be executed during this time	-	PL	-	PL	tCK
tPAR_ALERT_ON	Delay from errant command to ALERT# assertion	-	PL + 6ns	-	PL + 6ns	tCK
tPAR_ALERT_PW	Pulse width of ALERT# signal when asserted	72	144	80	160	tCK
tPAR_ALERT_RSP	Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	-	64	-	71	tCK
PL	Parity Latency	5				tCK
<b>CRC Error Reporting</b>						
tCRC_ALERT	CRC error to ALERT# latency	3	13	3	13	ns
tCRC_ALERT_PW	CRC ALERT# pulse width	6	10	6	10	tCK
<b>Geardown timing</b>						
tXPR_GEAR	Exit Reset from CKE High to a valid MRS Gear Down (T2/ Reset)	-	-	TBD	-	
tXS_GEAR	CKE High Assert to Gear Down Enable time(T2/CKE)	-	-	TBD	-	
tSYNC_GEAR <sup>27</sup>	MRS command to Sync pulse time(T3)	-	-	TBD	-	
tCMD_GEAR <sup>27</sup>	Sync pulse to First valid command(T4)	-	-	TBD	-	
tGEAR_setup	Geardown setup time	2	-	2	-	tCK
tGEAR_hold	Geardown hold time	2	-	2	-	tCK
<b>tREFI</b>						
tRFC1 (min) <sup>34</sup>	4Gb	260	-	260	-	ns
tRFC2 (min) <sup>34</sup>	4Gb	160	-	160	-	ns
tRFC4 (min) <sup>34</sup>	4Gb	110	-	110	-	ns
tREFI	Average periodic refresh interval	-40°C ≤ T <sub>CASE</sub> ≤ 85°C	7.8	-	7.8	μs
		85°C ≤ T <sub>CASE</sub> ≤ 95°C	3.9	-	3.9	μs

Note 1. Start of internal write transaction is defined as follows:

- For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
- For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
- For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

Note 2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.

Note 3. Commands requiring a locked DLL are: Read (and RAP) and synchronous ODT commands.

Note 4. tWR is defined in ns, for calculation of tWRP<sub>EN</sub> it is necessary to round up tWR/tCK to the next integer.

Note 5. WR in clock cycles as programmed in MR0.

Note 6. tREFI depends on T<sub>OPER</sub>.

Note 7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

Note 8. For these parameters, the DDR4 SDRAM device supports t<sub>PARAM</sub>[nCK]=RU{t<sub>PARAM</sub>[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.

Note 9. When CRC and DM are both enabled, t<sub>WR\_CRC\_DM</sub> is used in place of tWR.

Note 10. When CRC and DM are both enabled t<sub>WTR\_S\_CRC\_DM</sub> is used in place of t<sub>WTR\_S</sub>.

Note 11. When CRC and DM are both enabled t<sub>WTR\_L\_CRC\_DM</sub> is used in place of t<sub>WTR\_L</sub>.

Note 12. The max values are system dependent.

Note 13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.

Note 14. The deterministic component of the total timing. Measurement method TBD.

Note 15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.

Note 16. This parameter will be characterized and guaranteed by design.

Note 17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual t<sub>JIT(per)\_total</sub> of the input clock. (Output deratings are relative to the SDRAM input clock). Example TBD.

Note 18. DRAM DBI mode is off.

- Note 19. DRAM DBI mode is enabled.
- Note 20.  $t_{QSL}$  describes the instantaneous differential output low pulse width on DQS - DQS#, as measured from on falling edge to the next consecutive rising edge.
- Note 21.  $t_{QSH}$  describes the instantaneous differential output high pulse width on DQS - DQS#, as measured from on falling edge to the next consecutive rising edge.
- Note 22. There is no maximum cycle time limit besides the need to satisfy the refresh interval  $t_{REFI}$ .
- Note 23.  $t_{CH(ABS)}$  is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
- Note 24.  $t_{CL(ABS)}$  is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
- Note 25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
- Note 26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
- Note 27. This parameter has to be even number of clocks.
- Note 28. When CRC and DM are both enabled,  $t_{WR\_CRC\_DM}$  is used in place of  $t_{WR}$ .
- Note 29. When CRC and DM are both enabled  $t_{WR\_S\_CRC\_DM}$  is used in place of  $t_{WR\_S}$ .
- Note 30. When CRC and DM are both enabled  $t_{WR\_L\_CRC\_DM}$  is used in place of  $t_{WR\_L}$ .
- Note 31. After CKE is registered low, CKE signal level shall be maintained below  $V_{ILDc}$  for  $t_{CKE}$  specification (low pulse width).
- Note 32. After CKE is registered high, CKE signal level shall be maintained above  $V_{IHDC}$  for  $t_{CKE}$  specification (high pulse width).
- Note 33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
- Note 34. Parameters apply from  $t_{CK(avg)min}$  to  $t_{CK(avg)max}$  at all standard JEDEC clock period values as stated in the Speed-Bin tables.
- Note 35. This parameter must keep consistency with Speed-Bin tables.
- Note 36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.  $UI = t_{CK(avg).min}/2$
- Note 37. Applied when DRAM is in DLL ON mode.
- Note 38. Assume no jitter on input clock signals to the DRAM.
- Note 39. Value is only valid for  $R_{ONNOM} = 34$  ohms.
- Note 40. 1tck toggle mode with setting MR4 A[11] to 0.
- Note 41. 2tck toggle mode with setting MR4 A[11] to 1, which is valid for DDR4-2400/2666 speed grade.
- Note 42. 1tck mode with setting MR4 A[12] to 0.
- Note 43. 2tck mode with setting MR4 A[12] to 1, which is valid for DDR4-2400/2666 speed grade.
- Note 44. The maximum read preamble is bounded by  $t_{LZ(DQS)min}$  on the left side and  $t_{DQSK(max)}$  on the right side. See Clock to Data Strobe Relationship. Boundary of DQS Low-Z occur one cycle earlier in 2tck toggle mode which is illustrated in Read Preamble.
- Note 45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point.
- Note 46. Last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High.
- Note 47.  $V_{REFDQ}$  value must be set to either its midpoint or  $V_{cent\_DQ}$  (midpoint) in order to capture DQ0 low level for entering PDA mode.
- Note 48. The maximum read postamble is bound by  $t_{DQSK(min)}$  plus  $t_{QSH(min)}$  on the left side and  $t_{HZ(DQS)max}$  on the right side. See Clock to Data Strobe Relationship.
- Note 49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately  $0.7 \times V_{DDQ}$  as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to  $V_{TT} = V_{DDQ}$ .
- Note 50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

## AC and DC output Measurement levels

### Output Driver DC Electrical Characteristics

The DDR4 driver supports two different  $R_{ON}$  values. These  $R_{ON}$  values are referred as strong (low  $R_{ON}$ ) and weak mode (high  $R_{ON}$ ). A functional representation of the output buffer is shown in the figure below. Output driver impedance  $R_{ON}$  is defined as follows:

The individual pull-up and pull-down resistors ( $R_{ONPu}$  and  $R_{ONPd}$ ) are defined as follows:

$$R_{ONPu} = \frac{V_{DDQ} - V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ONPd} \text{ is off}$$

$$R_{ONPd} = \frac{V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ONPu} \text{ is off}$$

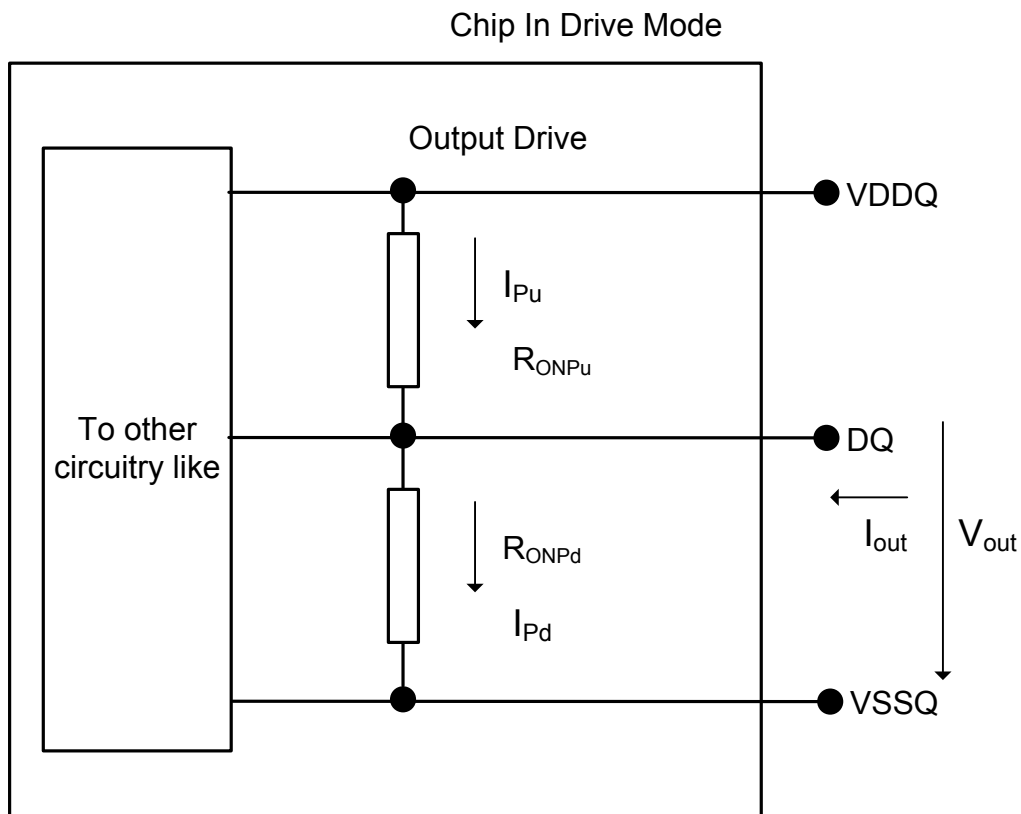


Figure 179. Output driver

**Table 93. Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration**

R <sub>ON,NOM</sub>	Resistor	V <sub>out</sub>	Min.	Nom.	Max.	Unit	Note
34Ω	R <sub>ON34Pd</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/7	1,2
		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/7	1,2
		V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/7	1,2
	R <sub>ON34Pu</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/7	1,2
		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/7	1,2
		V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/7	1,2
48Ω	R <sub>ON48Pd</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/5	1,2
		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/5	1,2
		V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/5	1,2
	R <sub>ON48Pu</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/5	1,2
		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/5	1,2
		V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	-10	-	10	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	-	-	10	%	1,2,4

Note 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity (TBD).

Note 2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 x V<sub>DDQ</sub>. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 x V<sub>DDQ</sub> and 1.1 x V<sub>DDQ</sub>.

Note 3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd: Measure R<sub>ONPu</sub> and R<sub>ONPd</sub> both at 0.8 x V<sub>DDQ</sub> separately; R<sub>ON,NOM</sub> is the nominal R<sub>ON</sub> value.

$$MMPuPd = \frac{R_{ONPu} - R_{ONPd}}{R_{TTNOM}} \times 100$$

Note 4. R<sub>ON</sub> variance range ratio to R<sub>ON</sub> Nominal value in a given component, including DQS and DQS#.

$$MMPudd = \frac{R_{ONPuMax} - R_{ONPdMin}}{R_{TTNOM}} \times 100$$

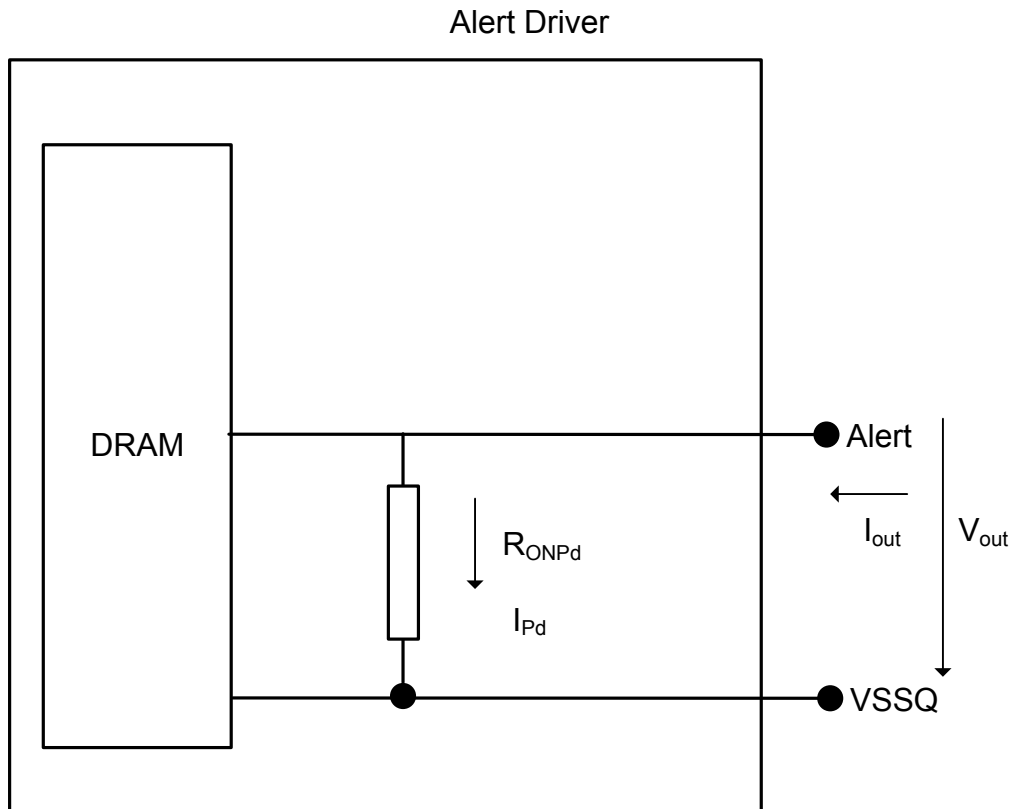
$$MMPddd = \frac{R_{ONPdMax} - R_{ONPdMin}}{R_{TTNOM}} \times 100$$

Note 5. This parameter of x16 device is specified for Upper byte and Lower byte.

### ALERT# output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance  $R_{ON}$  is defined as follows:

$$R_{ONPd} = \frac{V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ONPu} \text{ is off}$$



**Figure 180. ALERT# output Drive Characteristic**

**Table 94. ALERT Driver Voltage**

Resistor	V <sub>out</sub>	Min.	Max.	Unit	Note
$R_{ONPd}$	$V_{OLdc} = 0.1 \times V_{DDQ}$	0.3	1.2	34Ω	1
	$V_{OMdc} = 0.8 \times V_{DDQ}$	0.4	1.2	34Ω	1
	$V_{OHdc} = 1.1 \times V_{DDQ}$	0.4	1.4	34Ω	1

Note 1.  $V_{DDQ}$  voltage is at  $V_{DDQ}$  DC.  $V_{DDQ}$  DC definition is TBD.

### Output Driver Characteristic of Connectivity Test ( CT ) Mode

Following Output driver impedance  $R_{ON}$  will be applied Test Output Pin during Connectivity Test (CT) Mode. The individual pull-up and pull-down resistors ( $R_{ONPu\_CT}$  and  $R_{ONPd\_CT}$ ) are defined as follows:

$$R_{ONPu\_CT} = \frac{V_{DDQ} - V_{out}}{|I_{out}|}$$

$$R_{ONPd\_CT} = \frac{V_{out}}{|I_{out}|}$$

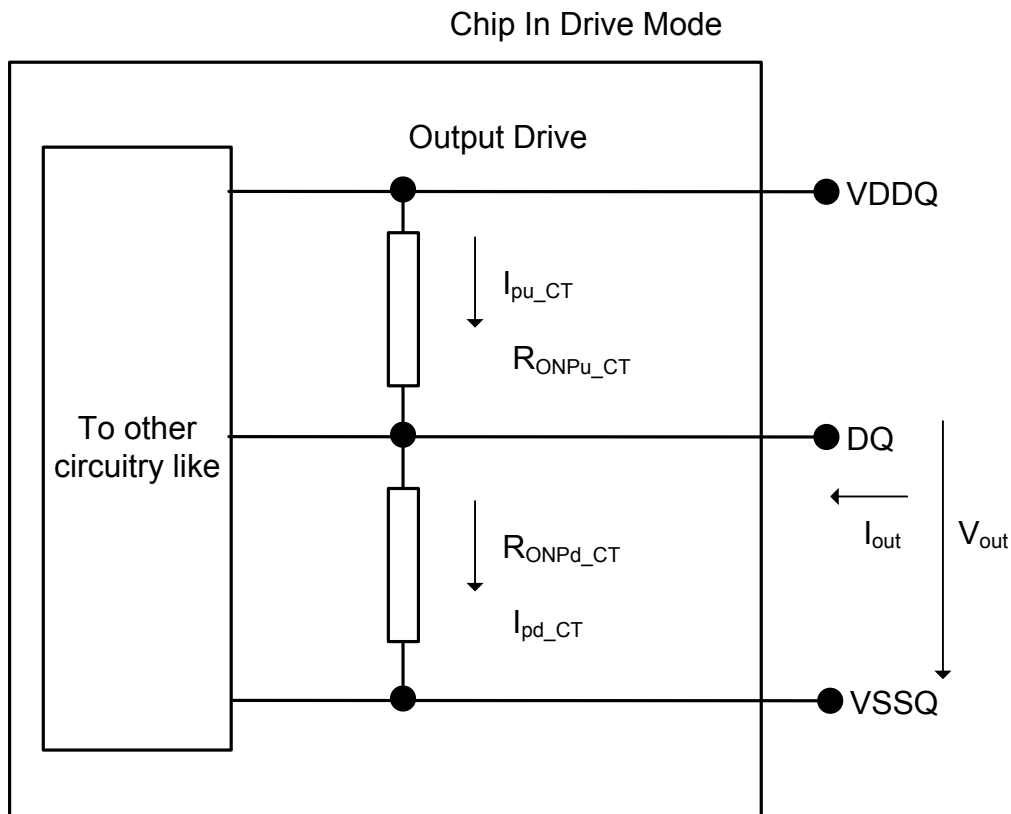


Figure 181. Output Driver Characteristic of Connectivity Test

Table 95. Output Driver Electrical Characteristics during Connectivity Test Mode

$R_{ON\_NOM}$	Resistor	$V_{out}$	Max.	Unit	Note
34Ω	$R_{ONPd\_CT}$	$V_{OBdC} = 0.2 \times V_{DDQ}$	1.9	34Ω	1
		$V_{OLdC} = 0.5 \times V_{DDQ}$	2.0	34Ω	1
		$V_{OMdC} = 0.8 \times V_{DDQ}$	2.2	34Ω	1
		$V_{OHdC} = 1.1 \times V_{DDQ}$	2.5	34Ω	1
	$R_{ONPu\_CT}$	$V_{OBdC} = 0.2 \times V_{DDQ}$	2.5	34Ω	1
		$V_{OLdC} = 0.5 \times V_{DDQ}$	2.2	34Ω	1
		$V_{OMdC} = 0.8 \times V_{DDQ}$	2.0	34Ω	1
		$V_{OHdC} = 1.1 \times V_{DDQ}$	1.9	34Ω	1

Note 1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.



## Single-ended AC & DC Output Levels

**Table 96. Single-ended AC & DC output levels**

Symbol	Parameter	DDR4-2400/2666	Unit	Note
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$(0.7 + 0.15) \times V_{DDQ}$	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	$(0.7 - 0.15) \times V_{DDQ}$	V	1

Note 1. The swing of  $\pm 0.15 \times V_{DDQ}$  is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of  $R_{ZQ}/7\Omega$  and an effective test load of  $50\Omega$  to  $V_{TT} = V_{DDQ}$ .

## Differential AC & DC Output Levels

**Table 97. Differential AC & DC output levels**

Symbol	Parameter	DDR4-2400/2666	Unit	Note
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	$+0.3 \times V_{DDQ}$	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	$-0.3 \times V_{DDQ}$	V	1

Note 1. The swing of  $\pm 0.3 \times V_{DDQ}$  is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of  $R_{ZQ}/7\Omega$  and an effective test load of  $50\Omega$  to  $V_{TT} = V_{DDQ}$  at each of the differential outputs.

## Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $V_{OL(AC)}$  and  $V_{OH(AC)}$  for single ended signals.

**Table 98. Single-ended output slew rate definition**

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TRse$
Single ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TFse$

Note 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

**Table 99. Single-ended output slew rate**

Symbol	Parameter	DDR4-2400/2666		Unit
		Min.	Max.	
SRQse	Single ended output slew rate	4	9	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For  $R_{ON} = RZQ/7$  setting

Note 1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

- **Case 1** is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

- **Case 2** is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies.

## Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $V_{OLdiff(AC)}$  and  $V_{OHdiff(AC)}$  for differential signals.

**Table 100. Differential output slew rate definition**

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TRdiff$
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TFdiff$

Note 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

**Table 101. Differential output slew rate**

Symbol	Parameter	DDR4-2400/2666		Unit
		Min.	Max.	
SRQdiff	Differential output slew rate	8	18	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For  $R_{on} = RZQ/7$  setting

## Single-ended AC and DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

**Table 102. Single-ended AC & DC output levels of Connectivity Test Mode**

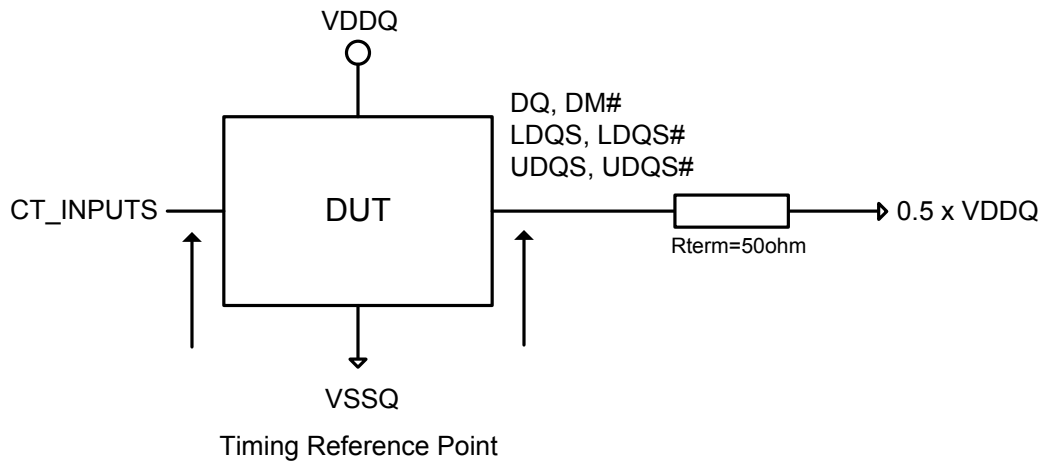
Symbol	Parameter	DDR4-2400/2666		Unit	Note
		Min.	Max.		
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$		V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$		V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$		V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$		V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$V_{TT} + (0.1 \times V_{DDQ})$		V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	$V_{TT} - (0.1 \times V_{DDQ})$		V	1

Note 1. The effective test load is  $50\Omega$  terminated by  $V_{TT} = 0.5 \times V_{DDQ}$ .

**Table 103. Single-ended output slew rate of Connectivity Test Mode**

Symbol	Parameter	DDR4-2400/2666		Unit	Note
		Min.	Max.		
TF_output_CT	Output signal Falling time	-	10	ns/V	
TR_output_CT	Output signal Rising time	-	10	ns/V	

Test Load for Connectivity Test Mode Timing



**Figure 182. Connectivity Test Mode Timing Reference Load**

## Slew Rate Definitions for Differential Input Signals (CK)

**Table 104. Differential Input Slew Rate Definition**

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK - CK#)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK - CK#)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$

Note 1. The differential signal (i.e., CK - CK#) must be linear between these thresholds.

## Differential Input Cross Point Voltage

**Table 105. Cross point voltage for differential input signals (CK)**

Symbol	Parameter	DDR4-2400/2666			
		Min.		Max.	
-	Area of $V_{SEH}$ , $V_{SEL}$	TBD	TBD	TBD	TBD
$V_{IX}(CK)$	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, CK#	TBD	TBD	TBD	TBD

## CMOS rail to rail Input Levels for RESET#

**Table 106. CMOS rail to rail Input Levels for RESET#**

Symbol	Parameter	Min.	Max.	Unit	Note
$V_{IH(AC)\_RESET}$	AC Input High Voltage	$0.8 \times V_{DDQ}$	$V_{DD}$	V	6
$V_{IH(DC)\_RESET}$	DC Input High Voltage	$0.7 \times V_{DDQ}$	$V_{DD}$	V	2
$V_{IL(DC)\_RESET}$	DC Input Low Voltage	$V_{SS}$	$0.3 \times V_{DDQ}$	V	1
$V_{IL(AC)\_RESET}$	AC Input Low Voltage	$V_{SS}$	$0.2 \times V_{DDQ}$	V	7
TR_RESET	Rising time	-	1.0	$\mu s$	4
$t_{PW\_RESET}$	RESET pulse width	1.0	-	$\mu s$	3,5

Note 1. After RESET# is registered Low, RESET# level shall be maintained below  $V_{IL(DC)\_RESET}$  during  $t_{PW\_RESET}$ , otherwise, SDRAM may not be reset.

Note 2. Once RESET# is registered High, RESET# level must be maintained above  $V_{IH(DC)\_RESET}$ , otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET# signal Low.

Note 3. RESET is destructive to data contents.

Note 4. No slope reversal (ringback) requirement during its level transition from Low to High.

Note 5. This definition is applied only "Reset Procedure at Power Stable".

Note 6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.

Note 7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

## Differential swing requirements for DQS (DQS – DQS#)

**Table 107. Differential AC and DC Input Levels for DQS**

Symbol	Parameter	DDR4-2400		DDR4-2666		Unit	Note
		Min.	Max.	Min.	Max.		
$V_{IH,DIFF,Peak}$	$V_{IH,DIFF,Peak}$ Voltage	160	-	TBD	TBD	mV	1,2
$V_{IL,DIFF,Peak}$	$V_{IL,DIFF,Peak}$ Voltage	-	-160	TBD	TBD	mV	1,2

Note 1. Used to define a differential signal slew-rate.

Note 2. These values are not defined; however, the differential signals DQS – DQS#, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

## Differential Input Cross Point Voltage

**Table 108. Cross point voltage for DQS differential input signals**

Symbol	Parameter	DDR4-2400/2666		Unit	Note
		Min.	Max.		
$V_{IX,DQS,Ratio}$	DQS and DQS# crossing relative to the midpoint of the DQS and DQS# signal swings	-	25	%	1,2
$V_{DQSmid\_to\_V_{cent}}$	$V_{DQSmid}$ offset relative to $V_{cent,DQ}$ (midpoint)	-	$\min(V_{IH,diff}, 50)$	mV	3-5

Note 1.  $V_{IX,DQS,Ratio}$  is DQS VIX crossing ( $V_{IX,DQS\_FR}$  or  $V_{IX,DQS\_RF}$ ) divided by  $V_{DQS,trans}$ .  $V_{DQS,trans}$  is the difference between the lowest horizontal tangent above  $V_{DQSmid}$  of the transitioning DQS signals and the highest horizontal tangent below  $V_{DQSmid}$  of the transitioning DQS signals.

Note 2.  $V_{DQSmid}$  will be similar to the  $V_{REFDQ}$  internal setting value obtained during  $V_{REF}$  Training if the DQS and DQs drivers and paths are matched.

Note 3. The maximum limit shall not exceed the smaller of  $V_{IH,diff}$  minimum limit or 50mV.

Note 4.  $V_{IX}$  measurements are only applicable for transitioning DQS and DQS# signals when toggling data, preamble and highz states are not applicable conditions.

Note 5. The parameter  $V_{DQSmid}$  is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

## Differential Input Cross Point Voltage

**Table 109. Differential Input Slew Rate Definition for DQS, DQS#**

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (DQS - DQS#)	$V_{ILDiff\_DQS}$	$V_{IHDiff\_DQS}$	$ V_{ILDiff\_DQS} - V_{IHDiff\_DQS}  / \Delta TR_{diff}$
Differential input slew rate for falling edge (DQS - DQS#)	$V_{IHDiff\_DQS}$	$V_{ILDiff\_DQS}$	$ V_{ILDiff\_DQS} - V_{IHDiff\_DQS}  / \Delta TF_{diff}$

**Table 110. Differential Input Level for DQS, DQS#**

Symbol	Parameter	DDR4-2400		DDR4-2666		Unit	Note
		Min.	Max.	Min.	Max.		
$V_{IHDiff\_DQS}$	Differential Input High	130	-	TBD	TBD	mV	
$V_{ILDiff\_DQS}$	Differential Input Low	-	130	TBD	TBD	mV	

**Table 111. Differential Input Slew Rate for DQS, DQS#**

Symbol	Parameter	DDR4-2400		DDR4-2666		Unit	Note
		Min.	Max.	Min.	Max.		
SR <sub>Idiff</sub>	Differential Input Slew Rate	3	18	TBD	TBD	V/ns	

## Electrical Characteristics and AC Timing

### Reference Load for AC Timing and Output Slew Rate

Reference Load for AC Timing and Output Slew Rate represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

$R_{ON}$  nominal of DQ, DQS and DQS# drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal =  $1.0 \times V_{DDQ}$ .

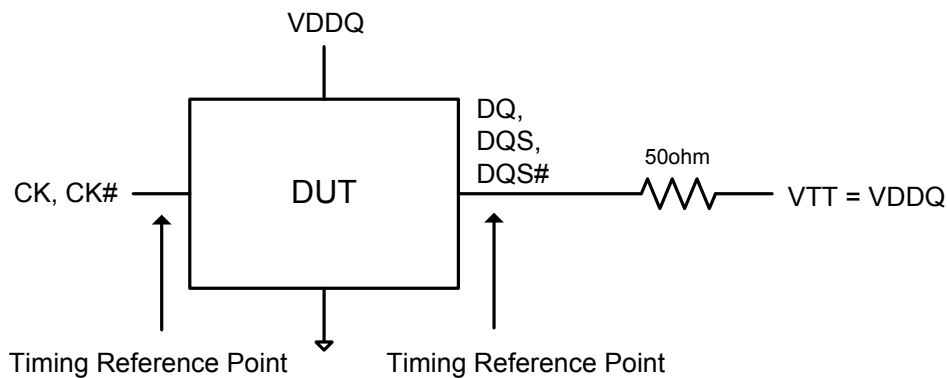
The minimum DC Low level of Output signal =  $\{ 34 / ( 34 + 50 ) \} \times V_{DDQ} = 0.4 \times V_{DDQ}$

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low =  $\{ ( 1 + 0.4 ) / 2 \} \times V_{DDQ} = 0.7 \times V_{DDQ}$

The actual reference level of Output signal might vary with driver  $R_{on}$  and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



**Figure 183. Reference Load for AC Timing and Output Slew Rate**



## Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the device.

### Definitions for $t_{CK(abs)}$ :

$t_{CK(abs)}$  is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.  $t_{CK(abs)}$  is not subject to production test.

### Definitions for $t_{CK(avg)}$ and $nCK$ :

$t_{CK(avg)}$  is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$t_{CK(avg)} = \frac{\sum_{i=1}^N t_{CK(abs)}_i}{N}$$

Where  $N=200$

### Definitions for $t_{CH(avg)}$ and $t_{CL(avg)}$ :

$t_{CH(avg)}$  is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$t_{CH(avg)} = \frac{\sum_{i=1}^N t_{CH}_i}{N} \cdot t_{CK(avg)}$$

Where  $N=200$

$t_{CL(avg)}$  is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$t_{CL(avg)} = \frac{\sum_{i=1}^N t_{CL}_i}{N} \cdot t_{CK(avg)}$$

Where  $N=200$

### Definitions for $t_{ERR(nper)}$ :

$t_{ERR}$  is defined as the cumulative error across  $n$  consecutive cycles of  $n \times t_{CK(avg)}$ .  $t_{ERR}$  is not subject to production test.

## Command, Control, and Address Setup, Hold, and Derating

The total  $t_{IS}$  (setup time) and  $t_{IH}$  (hold time) required is calculated to account for slew rate variation by adding the data sheet  $t_{IS(base)}$  values, the  $V_{IL(AC)}/V_{IH(AC)}$  points, and  $t_{IH(base)}$  values, the  $V_{IL(DC)}/V_{IH(DC)}$  points; to the  $\Delta t_{IS}$  and  $\Delta t_{IH}$  derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example:  $t_{IS}$  (total setup time) =  $t_{IS(base)} + \Delta t_{IS}$ . For a valid transition, the input signal has to remain above/below  $V_{IH(AC)}/V_{IL(AC)}$  for the time defined by  $t_{VAC}$ .

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached  $V_{IH(AC)}/V_{IL(AC)}$  at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach  $V_{IH(AC)}/V_{IL(AC)}$ . For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup ( $t_{IS}$ ) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL(DC)max}$  and the first crossing of  $V_{IH(AC)min}$  that does not ring back below  $V_{IH(DC)min}$ . Setup ( $t_{IS}$ ) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH(DC)min}$  and the first crossing of  $V_{IL(AC)max}$  that does not ring back above  $V_{IL(DC)max}$ .

Hold ( $t_{IH}$ ) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL(DC)max}$  and the first crossing of  $V_{IH(AC)min}$  that does not ring back below  $V_{IH(DC)min}$ . Hold ( $t_{IH}$ ) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH(DC)min}$  and the first crossing of  $V_{IL(AC)min}$  that does not ring back above  $V_{IL(DC)max}$ .

**Table 112. Command, Address, Control Setup and Hold Values**

Symbol	Reference	DDR4-2400	DDR4-2666	Unit
$t_{IS(base, AC100)}$	$V_{IH(AC)}/V_{IL(AC)}$	62	TBD	ps
$t_{IH(base, DC75)}$	$V_{IH(DC)}/V_{IL(DC)}$	87	TBD	ps
$t_{IS}/t_{IH}(VREF)$	-	162	TBD	ps

Note 1. Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.

Note 2. Values listed are referenced only; applicable limits are defined elsewhere.

**Table 113. Command, Address, Control Input Voltage Values**

Symbol	Reference	DDR4-2400	DDR4-2666	Unit
$V_{IH,CA(AC)min}$	$V_{IH(AC)}/V_{IL(AC)}$	100	TBD	mV
$V_{IH,CA(DC)min}$	$V_{IH(DC)}/V_{IL(DC)}$	75	TBD	mV
$V_{IL,CA(AC)max}$	$V_{IH(AC)}/V_{IL(AC)}$	-75	TBD	mV
$V_{IL,CA(DC)max}$	$V_{IH(DC)}/V_{IL(DC)}$	-100	TBD	mV

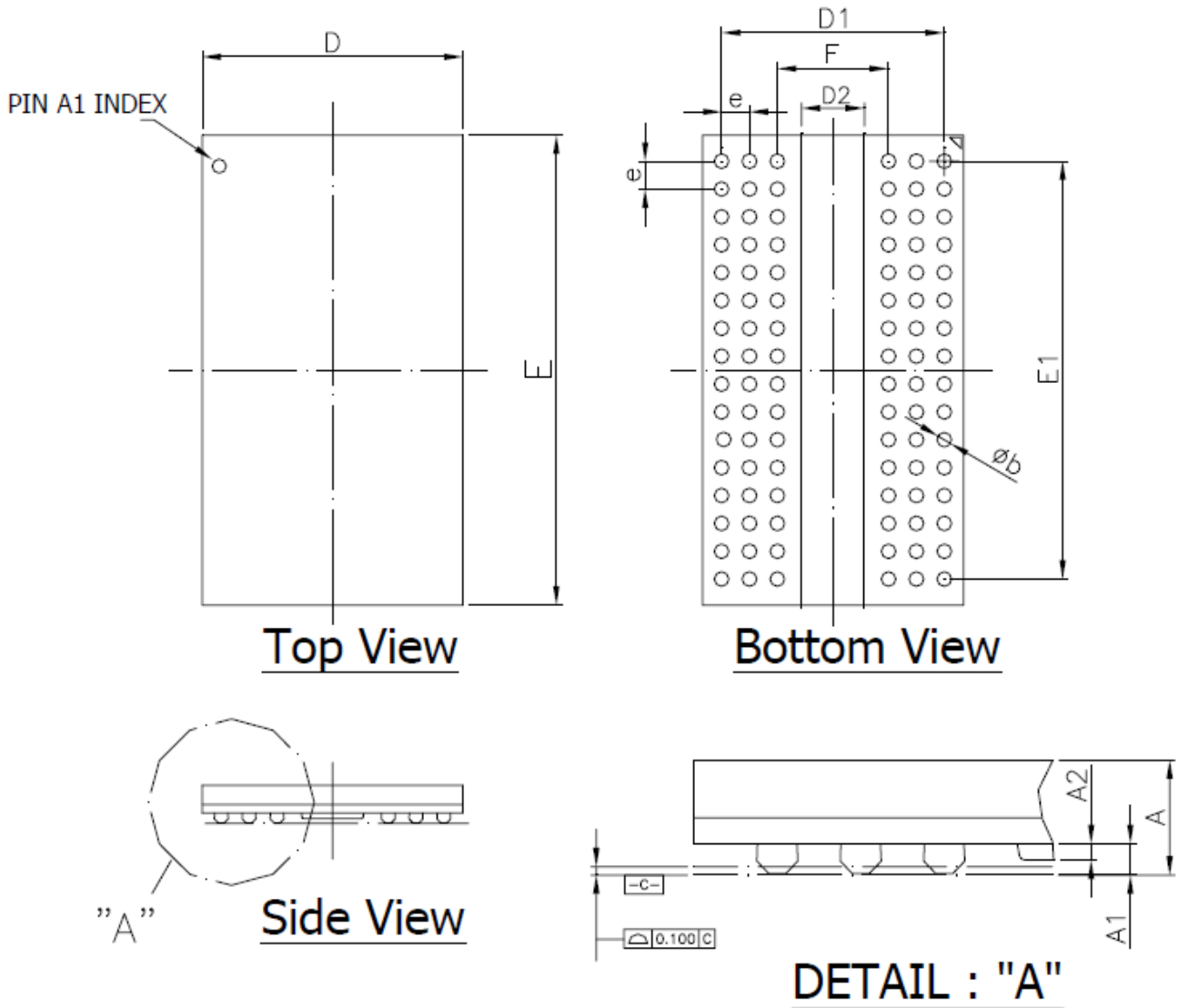
Note 1. Command, Address, Control input levels relative to  $V_{REFCA}$ .

Note 2. Values listed are referenced only; applicable limits are defined elsewhere.

**Table 114. Derating values DDR4-2400 tIS/tIH – AC/DC based**

$\Delta t_{IS}, \Delta t_{IH}$ derating in [ps] AC/DC based -- $V_{IH(AC)}/V_{IL(AC)} = \pm 100mV, V_{IH(DC)}/V_{IL(DC)} = \pm 75mV$ ; relative to $V_{REFCA}$																	
		CK, CK# Differential Slew Rate															
		10.0 V/ns		8.0 V/ns		6.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.5 V/ns		1.0 V/ns	
		$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$
CMD, ADDR, CNTL Input Slew rate V/ns	7.0	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6.0	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5.0	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4.0	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3.0	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2.0	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1.0	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
0.6	-52	-35	-51	-34	-50	-33	-48	-13	-46	-29	-42	-25	-33	-17	-17	-0	
0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13	
0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85	-48	-69	-31	

## Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.047	--	--	1.20
A1	0.010	--	0.016	0.25	--	0.40
A2	--	--	0.008	--	--	0.20
D	0.291	0.295	0.299	7.40	7.50	7.60
E	0.528	0.531	0.535	13.40	13.50	13.60
D1	--	0.252	--	--	6.40	--
E1	--	0.472	--	--	12.00	--
F	--	0.126	--	--	3.20	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
D2	--	--	0.081	--	--	2.05

Figure 184. 96-Ball FBGA Package 7.5x13.5x1.2mm(max)