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**Revision History****8Gbit DDR3L SDRAM**

8 BANKS X 64Mbit X 16 - Dual Die Package (DDP)  
96ball FBGA Package

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Feb. 2019

## Specifications

- Density : 8G bits
- Organization :
  - 64M words x 16 bits x 8 banks
- Package :
  - 96-ball FBGA
  - Two 512Mbit x 8 dies stacked (DDP)
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply : VDD, VDDQ = 1.35V (1.283V to 1.45V)
  - Backward compatible to VDD, VDDQ = 1.5V ± 0.075V
- Data rate : 1866Mbps
- 2KB page size
  - Row address: A0 to A15
  - Column address: A0 to A9
- Eight internal banks for concurrent operation
- Burst lengths (BL) : 8 and 4 with Burst Chop (BC)
- Burst type (BT) :
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- CAS Latency (CL) : 5, 6, 7, 8, 9, 10, 11, 13
- CAS Write Latency (CWL) : 5, 6, 7, 8, 9
- Precharge : auto precharge option for each burst access
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Refresh : auto-refresh, self-refresh
- Refresh cycles :
  - Average refresh period
    - 7.8 μs at -40°C ≤ Tc ≤ +85°C
    - 3.9 μs at +85°C < Tc ≤ +105°C
- Operating case temperature range
  - Commercial Tc = 0°C to +95°C
  - Industrial Tc = -40°C to +95°C
  - Automotive Tc = -40°C to +105°C

## Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipeline architecture
- Bi-directional differential data strobe (DQS and  $\overline{DQS}$ ) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and  $\overline{CK}$ )
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- RESET pin for Power-up sequence and reset function
- SRT range : Normal/extended
- Programmable Output driver impedance control

**Table 1. Ordering Information**

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C512M16D3LA-10BCN	512M x 16	Commercial 0°C to 95°C	933	96-ball FBGA
AS4C512M16D3LA-10BIN	512M x 16	Industrial -40°C to 95°C	933	96-ball FBGA
AS4C512M16D3LA-10BAN	512M x 16	Automotive -40°C to 105°C	933	96-ball FBGA

**Table 2. Speed Grade Information**

Speed Grade	Clock Frequency	CAS Latency	tRCD(ns)	tRP(ns)
DDR3-1866	933 MHz	13	13.91	13.91

## Pin Configurations

### 96-ball FBGA (x16 configuration)

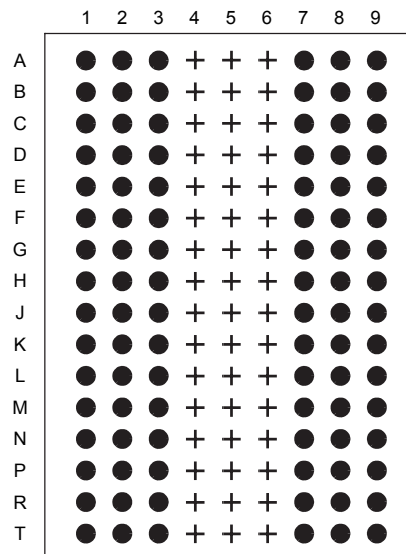
	1	2	3	4	5	6	7	8	9	
<b>A</b>	V <sub>DDQ</sub>	DQU5	DQU7				DQU4	V <sub>DDQ</sub>	V <sub>SS</sub>	<b>A</b>
<b>B</b>	V <sub>SSQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>				$\overline{\text{DQSU}}$	DQU6	V <sub>SSQ</sub>	<b>B</b>
<b>C</b>	V <sub>DDQ</sub>	DQU3	DQU1				DQSU	DQU2	V <sub>DDQ</sub>	<b>C</b>
<b>D</b>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	DMU				DQU0	V <sub>SSQ</sub>	V <sub>DD</sub>	<b>D</b>
<b>E</b>	V <sub>SS</sub>	V <sub>SSQ</sub>	DQL0				DML	V <sub>SSQ</sub>	V <sub>DDQ</sub>	<b>E</b>
<b>F</b>	V <sub>DDQ</sub>	DQL2	$\overline{\text{DQSL}}$				DQL1	DQL3	V <sub>SSQ</sub>	<b>F</b>
<b>G</b>	V <sub>SSQ</sub>	DQL6	$\overline{\text{DQSL}}$				V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SSQ</sub>	<b>G</b>
<b>H</b>	V <sub>REFDQ</sub>	V <sub>DDQ</sub>	DQL4				DQL7	DQL5	V <sub>DDQ</sub>	<b>H</b>
<b>J</b>	NC	V <sub>SS</sub>	$\overline{\text{RAS}}$				CK	V <sub>SS</sub>	NC	<b>J</b>
<b>K</b>	ODT	V <sub>DD</sub>	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	V <sub>DD</sub>	CKE	<b>K</b>
<b>L</b>	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	<b>L</b>
<b>M</b>	V <sub>SS</sub>	BA0	BA2				A15	V <sub>REFCA</sub>	V <sub>SS</sub>	<b>M</b>
<b>N</b>	V <sub>DD</sub>	A3	A0				$\overline{\text{A12/BC}}$	BA1	V <sub>DD</sub>	<b>N</b>
<b>P</b>	V <sub>SS</sub>	A5	A2				A1	A4	V <sub>SS</sub>	<b>P</b>
<b>R</b>	V <sub>DD</sub>	A7	A9				A11	A6	V <sub>DD</sub>	<b>R</b>
<b>T</b>	V <sub>SS</sub>	$\overline{\text{RESET}}$	A13				A14	A8	V <sub>SS</sub>	<b>T</b>

### Ball Locations (x16)

- Populated ball
- + Ball not populated

### Top view

(See the balls through the package)



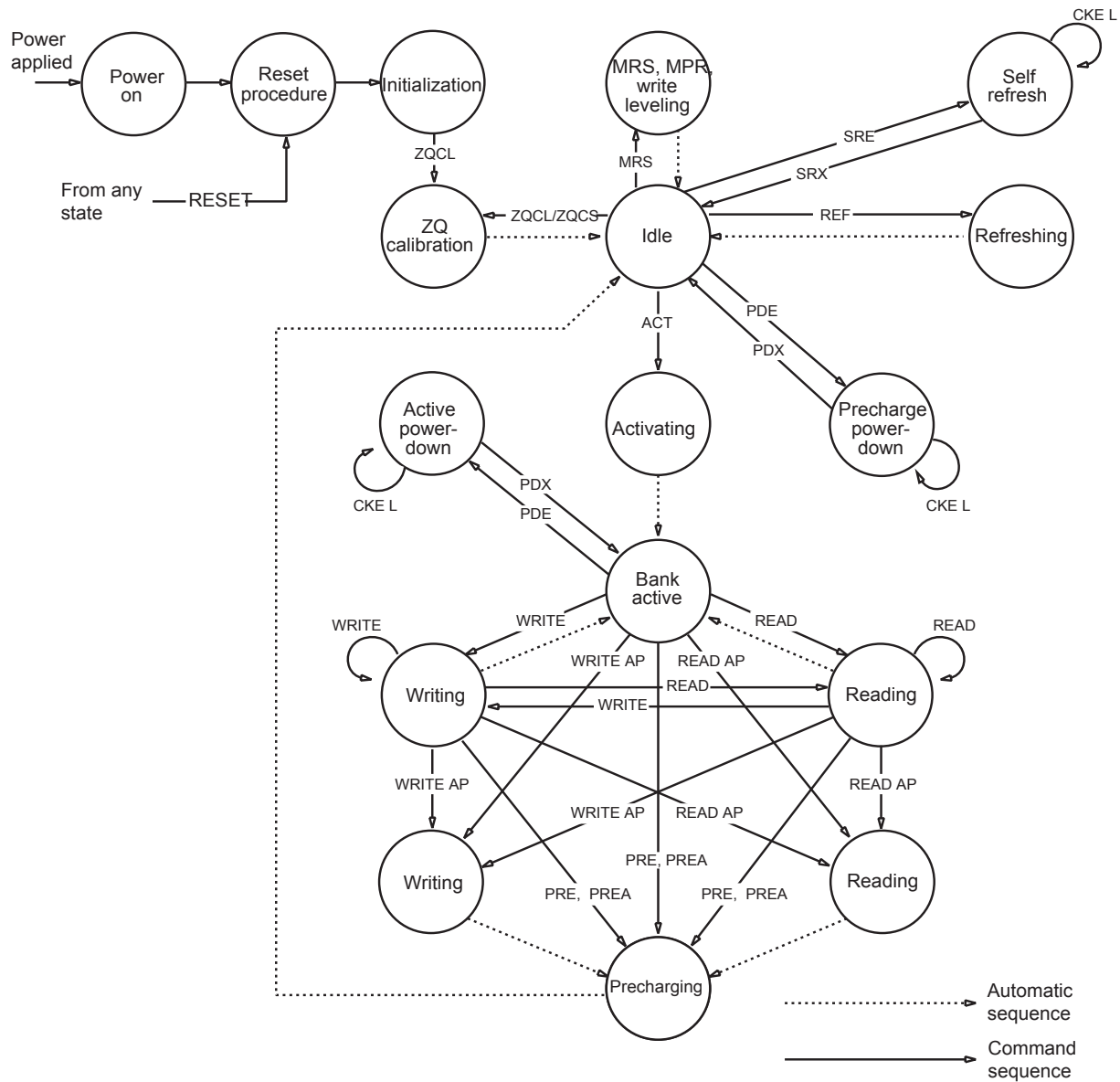
## Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	<b>Clock</b> : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$ . Output (read) data is referenced to the crossings of CK and $\overline{CK}$
CKE	Input	<b>Clock Enable</b> : CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After $V_{REFCA}$ has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS}$	Input	<b>Chip Select</b> : All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	<b>On Die Termination</b> : ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Input	<b>Command Inputs</b> : $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$ ) define the command being entered.
DM	Input	<b>Input Data Mask</b> : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	<b>Bank Address Inputs</b> : BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	<b>Address Inputs</b> : Provided the row address for Active commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/ $\overline{BC}$ have additional functions, see below) The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	<b>Autoprecharge</b> : A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge)A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	<b>Burst Chop</b> : A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be performed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details.
$\overline{RESET}$	Input	<b>Active Low Asynchronous Reset</b> : Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input/ Output	<b>Data Input/ Output</b> : Bi-directional data bus.
DQSL, $\overline{DQSL}$ DQSU, $\overline{DQSU}$	Input/ Output	<b>Data Strobe</b> : Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signals $\overline{DQS}$ , respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
NC		No Connect: No internal electrical connection is present.

Pin	Type	Function
VDDQ	Supply	DQ power supply: 1.35V ,1.283V to 1.45V operational; compatible to 1.5V +/- 0.075V operation
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.35V ,1.283V to 1.45V operational; compatible to 1.5V +/- 0.075V operation
VSS	Supply	Ground
VREFDQ	Supply	Reference Voltage for DQ
VREFCA	Supply	Reference Voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE : Input only pins ( BA0-BA2, A0-A15, RAS, CAS, WE, CS, CKE, ODT and RESET ) do not supply termination.

## Simplified State Diagram



ACT = ACTIVATE  
 MPR = Multipurpose register  
 MRS = Mode register set  
 PDE = Power-down entry  
 PDX = Power-down exit  
 PRE = PRECHARGE

PREA = PRECHARGE ALL  
 READ = RD, RDS4, RDS8  
 READ AP = RDAP, RDAPS4, RDAPS8  
 REF = REFRESH  
 RESET = START RESET PROCEDURE  
 SRE = Self refresh entry

SRX = Self refresh exit  
 WRITE = WR, WRS4, WRS8  
 WRITE AP = WRAP, WRAPS4, WRAPS8  
 ZQCL = ZQ LONG CALIBRATION  
 ZQCS = ZQ SHORT CALIBRATION

## Basic Functionality

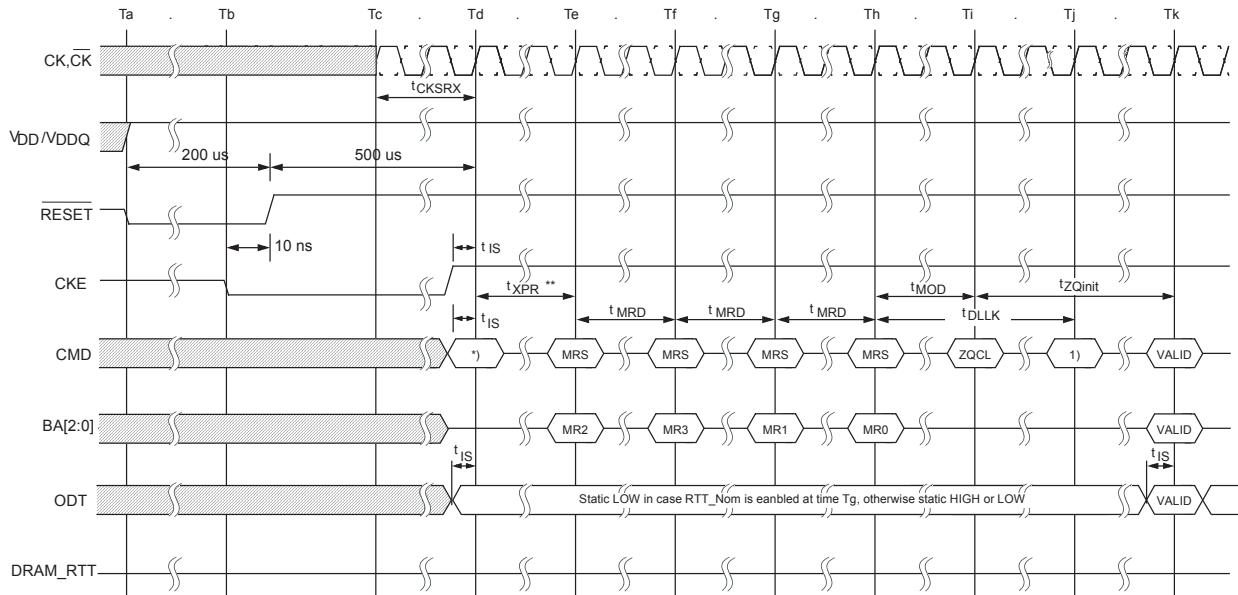
Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of four or eight in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10/AP), and the select BC4 or BL8 mode “on the fly” (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

## Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain  $\overline{\text{RESET}}$  below  $0.2 \times \text{VDD}$  (all other inputs may be undefined).  $\overline{\text{RESET}}$  needs to be maintained for minimum  $200\mu\text{s}$  with stable power.  $\text{CKE}$  is pulled “Low” anytime before  $\overline{\text{RESET}}$  being de-asserted (min. time 10ns). The power voltage ramp time between  $300\text{mV}$  to  $\text{VDD min}$  must be no longer than  $200\text{ms}$ ; and during the ramp,  $\text{VDD} > \text{VDDQ}$  and  $\text{VDD} - \text{VDDQ} < 0.3$  volts.
  - $\text{VDD}$  and  $\text{VDDQ}$  are driven from a single power converter output, AND
  - The voltage levels on all pins other than  $\text{VDD}, \text{VDDQ}, \text{VSS}, \text{VSSQ}$  must be less than or equal to  $\text{VDDQ}$  and  $\text{VDD}$  on one side and must be larger than or equal to  $\text{VSSQ}$  and  $\text{VSS}$  on the other side. In addition,  $\text{VTT}$  is limited to  $0.95\text{V}$  max once power ramp is finished, AND
  - $\text{Vref}$  tracks  $\text{VDDQ}/2$ .or
  - Apply  $\text{VDD}$  without any slope reversal before or at the same time as  $\text{VDDQ}$ .
  - Apply  $\text{VDDQ}$  without any slope reversal before or at the same time as  $\text{VTT}$  &  $\text{Vref}$ .
  - The voltage levels on all pins other than  $\text{VDD}, \text{VDDQ}, \text{VSS}, \text{VSSQ}$  must be less than or equal to  $\text{VDDQ}$  and  $\text{VDD}$  on one side and must be larger than or equal to  $\text{VSSQ}$  and  $\text{VSS}$  on the other side.
2. After  $\overline{\text{RESET}}$  is de-asserted, wait for another  $500\mu\text{s}$  until  $\text{CKE}$  becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks ( $\text{CK}$ ,  $\overline{\text{CK}}$ ) need to be started and stabilized for at least 10ns or  $5\text{tCK}$  (which is larger) before  $\text{CKE}$  goes active. Since  $\text{CKE}$  is a synchronous signal, the corresponding setup time to clock ( $\text{tIS}$ ) must be met. Also a NOP or Deselect command must be registered (with  $\text{tIS}$  set up time to clock) before  $\text{CKE}$  goes active. Once the  $\text{CKE}$  registered “High” after Reset,  $\text{CKE}$  needs to be continuously registered “High” until the initialization sequence is finished, including expiration of  $\text{tDLLK}$  and  $\text{tZQinit}$ .
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as  $\overline{\text{RESET}}$  is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after  $\overline{\text{RESET}}$  deassertion until  $\text{CKE}$  is registered HIGH. The ODT input signal may be in undefined state until  $\text{tIS}$  before  $\text{CKE}$  is registered HIGH. When  $\text{CKE}$  is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If  $\text{RTT\_NOM}$  is to be enabled in MR1 and the on-die termination is required to remain in the high impedance state, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of  $\text{tDLLK}$  and  $\text{tZQinit}$ .
5. After  $\text{CKE}$  is registered high, wait minimum of Reset CKE Exit time,  $\text{tXPR}$ , before issuing the first MRS command to load mode register. ( $\text{tXPR} = \text{Max}(\text{tXS}, 5\text{tCK})$ )
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to BA1-BA2)
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both  $\text{tDLLK}$  and  $\text{tZQ}$  init completed.
12. The DDR3 SDRAM is now ready for normal operation.

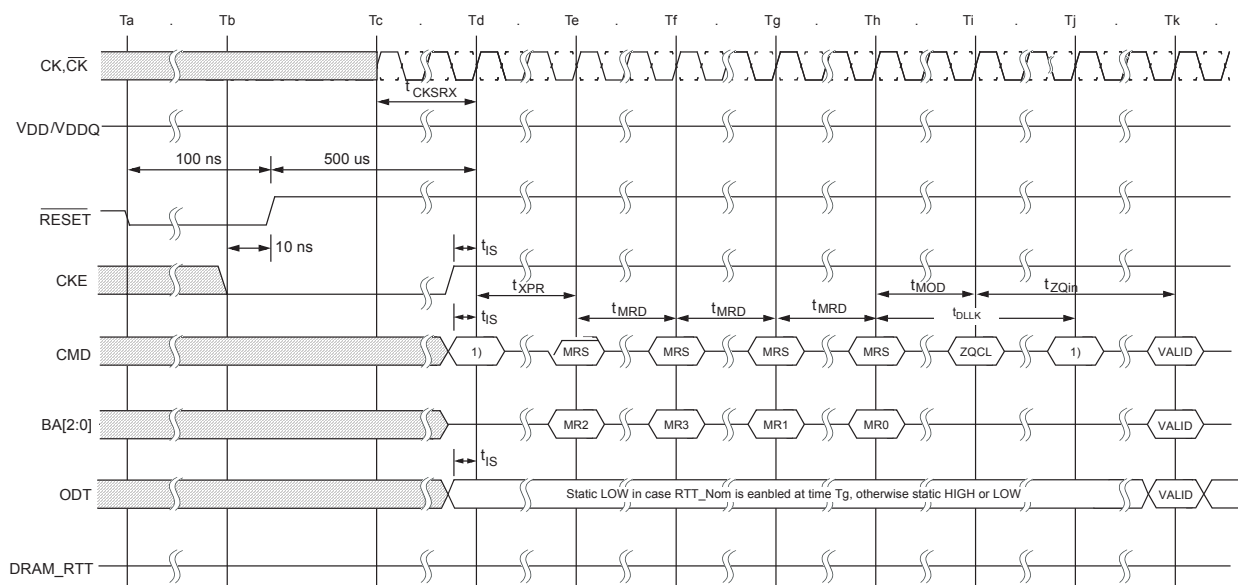


1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

## Reset and Initialization with Stable Power

The following sequence is required for /RESET at no power interruption initialization.

1. Assert /RESET below  $0.2 \times VDD$  anytime when reset is needed (all other inputs may be undefined). /RESET needs to be maintained for minimum 100ns. CKE is pulled low before /RESET being de-asserted (minimum time 10ns).
2. Follow Power-Up Initialization Sequence steps 2 to 11.
3. The reset sequence is now completed; DDR3 SDRAM is ready for normal operation.

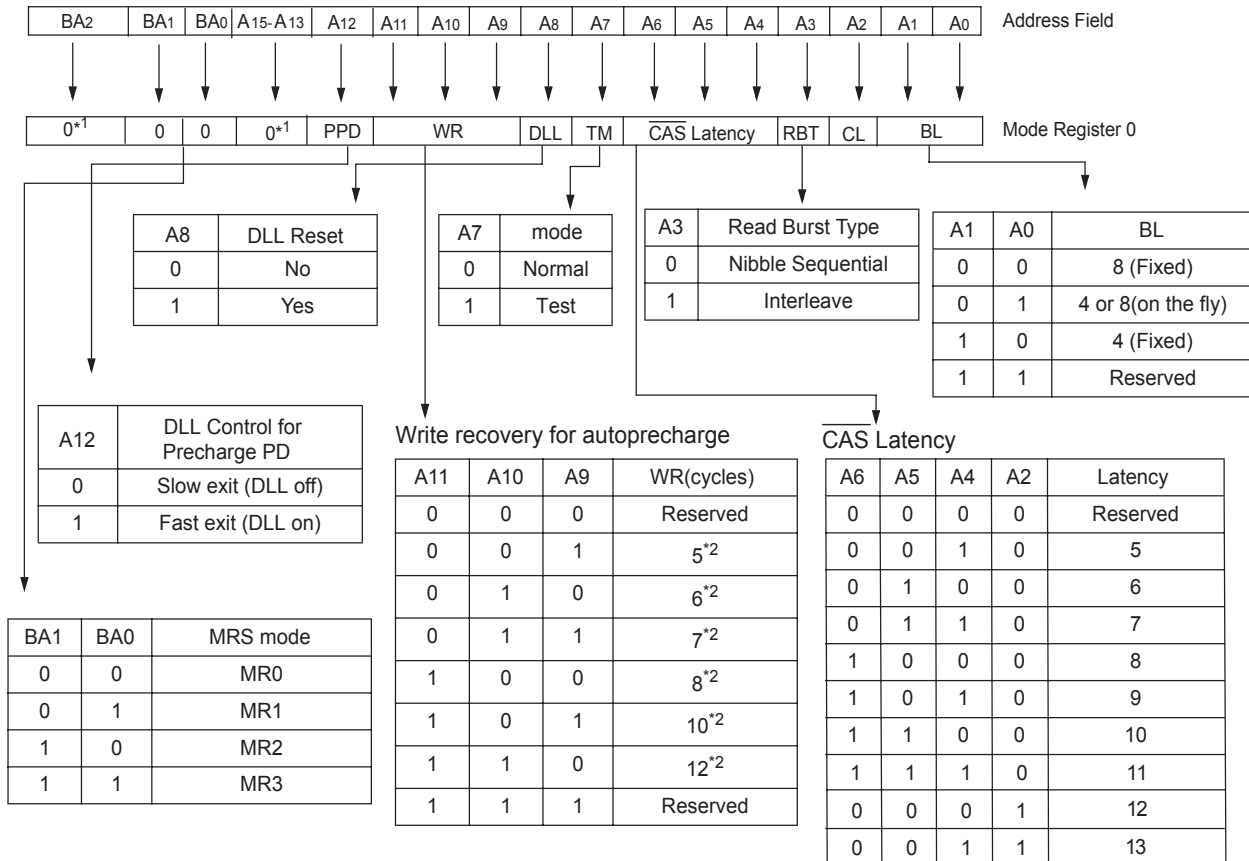


1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands



## Mode Register MR0

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS, RAS, CAS, WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.



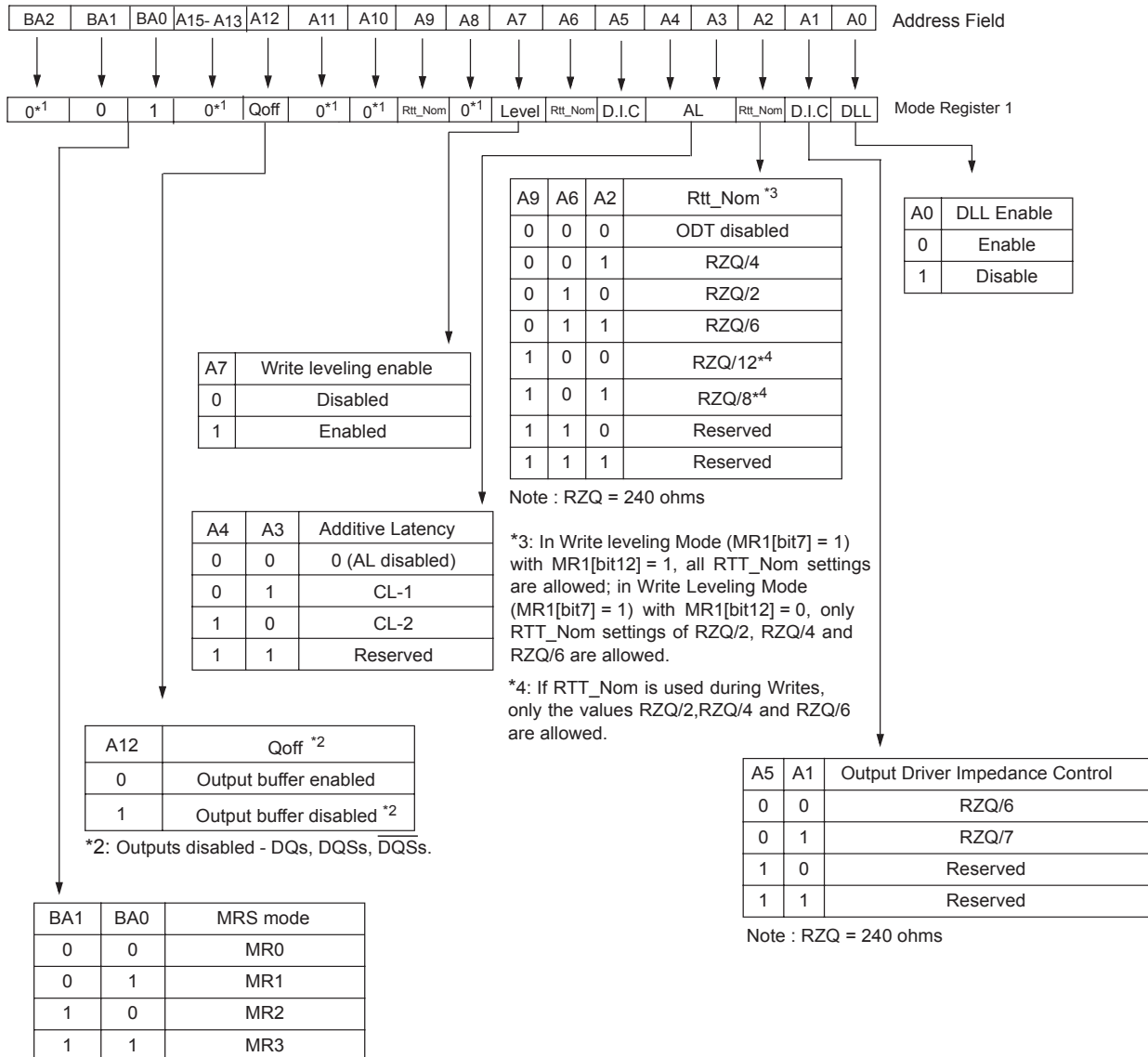
\*1 : BA2, A13, A14 and A15 are reserved for future use and must be programmed to 0 during MRS.

\*2 : WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer:  $WR_{min}[\text{cycles}] = \text{Roundup}(tWR[\text{ns}]/tCK[\text{ns}])$ . The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

## Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT\_Nom impedance, additive latency, write leveling enable and Qoff.

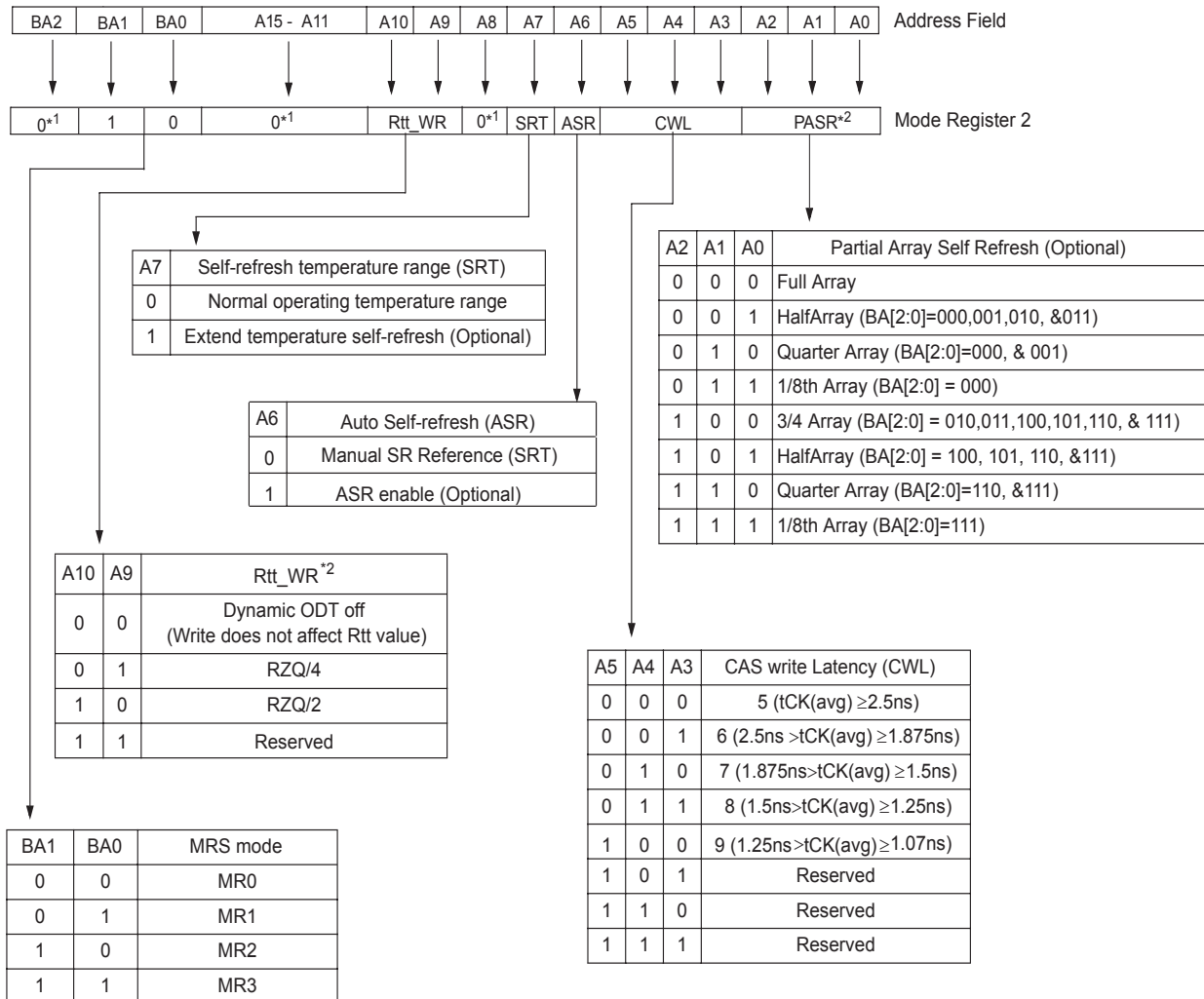
The Mode Register 1 is written by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.



\* 1 : BA2, A8, A10, A11, A13, A14 and A15 are reserved for future use (RFU) and must be programmed to 0 during MRS.

## Mode Register MR2

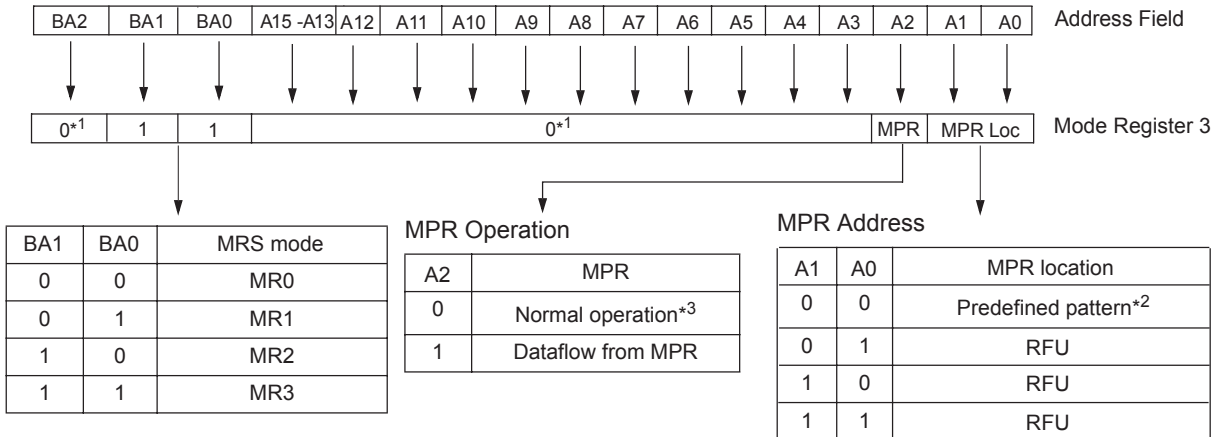
The Mode Register MR2 stores the data for controlling refresh related features, RTT\_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on CS, RAS, CAS, WE, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.



\* 1 : BA2, A8, A11 ~ A15 are RFU and must be programmed to 0 during MRS.  
 \* 2 : The Rtt\_WR value can be applied during writes even when Rtt\_Nom is disabled. During write leveling, Dynamic ODT is not available.

## Mode Register MR3

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



\* 1 : BA2, A3 - A15 are reserved for future use (RFU) and must be programmed to 0 during MRS.

\* 2 : The predefined pattern will be used for read synchronization.

\* 3 : When MPR control is set for normal operation, MR3 A[2] = 0, MR3 A[1:0] will be ignored

## Burst Length (MR0)

Read and write accesses to the DDR3 are burst oriented, with the burst length being programmable, as shown in the figure MR0 Programming. The burst length determines the maximum number of column locations that can be accessed for a given read or write command. Burst length options include fixed BC4, fixed BL8, and on the fly which allows BC4 or BL8 to be selected coincident with the registration of a read or write command Via A12 (BC). Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

## Burst Chop

In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on the fly via A12(BC), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

## Burst Type (MR0)

### [Burst Length and Sequence]

Burst length	Operation	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4 (Burst chop)	READ	000	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T
		001	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T
		010	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T
		011	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T
		100	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T
		101	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T
		110	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T
		111	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T
	WRITE	0VV	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X
		1VV	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X
8	READ	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
		010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
		011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
		100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
		110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
		111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0
	WRITE	VVV	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7

Remark: T: Output driver for data and stobes are in high impedance.

V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

X: Don't Care.

Notes: 1. Page length is a function of I/O organization and column addressing

2. 0...7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.

## Command Truth Table

(a) Note 1,2,3,4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BA=Bank Address, RA=Row Address, CA=Column Address,  $\overline{BC}$ =Burst Chop, X=Don't care, V=Valid]

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 - BA2	A13 - A15	A12 / BC	A10 / AP	A0 - A9,A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

Note :

- All DDR3 SDRAM commands are defined by states of  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$  and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant
- $\overline{RESE\overline{T}}$  is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
- Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
- "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level"
- Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
- The Power Down Mode does not perform any refresh operations.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- Self refresh exit is asynchronous.
- $V_{REF}$ (Both  $V_{REFDQ}$  and  $V_{REFCA}$ ) must be maintained during Self Refresh operation.
- The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
- The Deselect command performs the same function as a No Operation command.
- Refer to the CKE Truth Table for more detail with CKE transition

## CKE Truth Table

(a) Note 1~7 apply to the entire Command truth table

(b) CKE low is allowed only if tMRD and tMOD are satisfied

Current State <sup>2</sup>	CKE		Command (N) <sup>3</sup> <u>RAS</u> , <u>CAS</u> , <u>WE</u> , <u>CS</u>	Action (N) <sup>3</sup>	Notes
	Previous Cycle <sup>1</sup> (N-1)	Current Cycle <sup>1</sup> (N)			
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See "Command Truth Table," on previous page					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command truth table
8. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self Refresh Exit are NOP and DESELECT only.
13. Self Refresh can not be entered while Read or Write operations. See 'Self-Refresh Operation' and 'Power-Down Modes' on later section for a detailed list of restrictions.
14. The Power Down does not perform any refresh operations.
15. "X" means "don't care (including floating around V<sub>REF</sub>)" in Self Refresh and Power Down. It also applies to Address pins
16. V<sub>REF</sub> (Both V<sub>REFDQ</sub> and V<sub>REFCA</sub>) must be maintained during Self Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered
18. 'Idle state' means that all banks are closed (tRP,tDAL,etc. satisfied) and CKE is high and all timings from previous operations are satisfied (tMRD,tMOD,tRFC,tZQinit,tZQoper,tZQCS,etc)as well as all SRF exit and Power Down exit parameters are satisfied (tXS,tXP,tXPDLL,etc)

### Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.4 V ~ 1.8 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 V ~ 1.8 V	V	1,3
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to Vss	-0.4 V ~ 1.8 V	V	1
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C	1,2

NOTE :

- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

### Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
T <sub>C</sub>	Operating case temperature - Commercial	0 to +95	°C	1,2,3
T <sub>C</sub>	Operating case temperature - Industrial	-40 to +95	°C	1,2,3
T <sub>C</sub>	Operating case temperature - Automotive	-40 to +105	°C	1,2,3

NOTE :

- Operating temperature is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9μs. (This double refresh requirement may not apply for some devices.)
  - If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

### Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply voltage	1.275	1.35	1.425	V	1,2,3
VDDQ	Supply voltage for Output	1.275	1.35	1.425	V	1,2,3

NOTE :

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.



## AC and DC Input Measurement Levels

### Single-Ended AC and DC Input Levels for Command and Address(1.35V)

Symbol	Parameter	Min.	Max.	Units	Notes
VIHCA (DC90)	DC input logic high	VREF + 0.090	VDD	V	1
VILCA (DC90)	DC input logic low	VSS	VREF - 0.090	V	1
VIHCA (AC160)	AC input logic high	-	-	V	1,2
VILCA (AC160)	AC input logic low	-	-	V	1,2
VIHCA (AC135)	AC input logic high	-	-	V	1,2
VILCA (AC135)	AC input logic low	-	-	V	1,2
VIHCA (AC125)	AC input logic high	VREF + 0.125	-	V	1,2
VILCA (AC125)	AC input logic low	-	VREF - 0.125	V	1,2
VREFCA (DC)	Reference voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3,4

NOTE :

1. For input only pins except /RESET : VREF = VREFCA (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on VREF may not allow VREF to deviate from VREFCA (DC) by more than  $\pm 1\%$  VDD (for reference : approx.  $\pm 15$  mV).
4. For reference : approx.  $VDD/2 \pm 15$  mV.

## Single-Ended AC and DC Input Levels for DQ and DM(1.35V)

Symbol	Parameter	Min.	Max.	Units	Notes
VIHDQ (DC90)	DC input logic high	VREF + 0.090	VDD	V	1
VILDQ (DC90)	DC input logic low	VSS	VREF - 0.090	V	1
VIHDQ (AC160)	AC input logic high	-	-	V	1,2
VILDQ (AC160)	AC input logic low	-	-	V	1,2
VIHDQ (AC135)	AC input logic high	-	-	V	1,2
VILDQ (AC135)	AC input logic low	-	-	V	1,2
VIHDQ (AC130)	AC input logic high	VREF + 0.130	-	V	1,2
VILDQ (AC130)	AC input logic low	-	VREF - 0.130	V	1,2
VREFDQ (DC)	Reference voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3,4

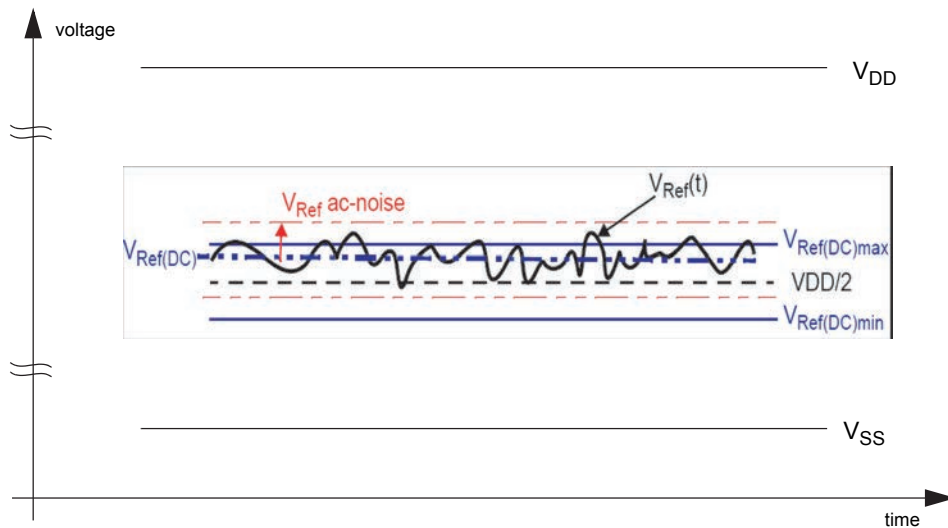
NOTE :

1. For DQ and DM : VREF = VREFDQ (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on VREF may not allow VREF to deviate from VREFDQ (DC) by more than  $\pm 1\%$  VDD (for reference: approx.  $\pm 15$  mV).
4. For reference: approx.  $VDD/2 \pm 15$  mV.

## VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrate in figure VREF(DC) tolerance and VREF AC-Noise limits. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table of "Single-Ended AC and DC Input Levels for Command and Address". Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than +/- 1% VDD.



**VREF(DC) tolerance and VREF AC-Noise limits**

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF.

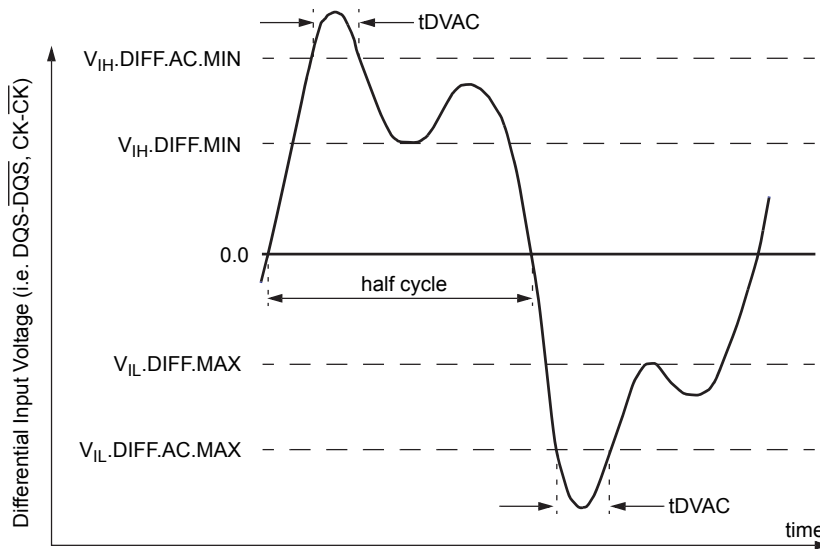
"VREF" shall be understood as VREF(DC), as defined in figure above, VREF(DC) tolerance and VREF AC-Noise limits.

This clarifies, that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (+/- 1% of VDD) are included in DRAM timings and their associated deratings.

## AC and DC Logic Input Levels for Differential Signals

### Differential signals definition



Definition of differential ac-swing and "time above ac level" tDVAC

### Differential swing requirement for clock ( $\overline{CK} - \overline{CK}$ ) and strobe ( $\overline{DQS} - \overline{DQS}$ )

#### Differential AC and DC Input Levels

Symbol	Parameter	Min.	Max.	Units	Notes
V <sub>IHdiff</sub>	Differential input high	+0.2	NOTE 3	V	1
V <sub>ILdiff</sub>	Differential input low	NOTE 3	-0.2	V	1
V <sub>IHdiff(AC)</sub>	Differential input high AC	2 x (V <sub>IH(AC)</sub> - V <sub>REF</sub> )	NOTE 3	V	2
V <sub>ILdiff(AC)</sub>	Differential input low AC	NOTE 3	2 x (V <sub>IL(AC)</sub> - V <sub>REF</sub> )	V	2

NOTE :

- Used to define a differential signal slew-rate.
- for  $\overline{CK} - \overline{CK}$  use V<sub>IH</sub>/V<sub>IL</sub>(AC) of address/command and V<sub>REFCA</sub>; for strobes ( $\overline{DQS} - \overline{DQS}$ ) use V<sub>IH</sub>/V<sub>IL</sub>(AC) of DQs and V<sub>REFDQ</sub>; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single-ended signals  $\overline{CK}$ ,  $\overline{CK}$ ,  $\overline{DQS}$ ,  $\overline{DQS}$  need to be within the respective limits (V<sub>IH</sub>(DC) max, V<sub>IL</sub>(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specification".

**Allowed time before ringback (tDVAC) for CK -  $\overline{CK}$  and DQS -  $\overline{DQS}$**

Slew Rate [V/ns]	tDVAC [ps] @  VIH/Ldiff(AC)  = 350mV		tDVAC [ps] @  VIH/Ldiff(AC)  = 300mV	
	Min.	Max.	Min.	Max.
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

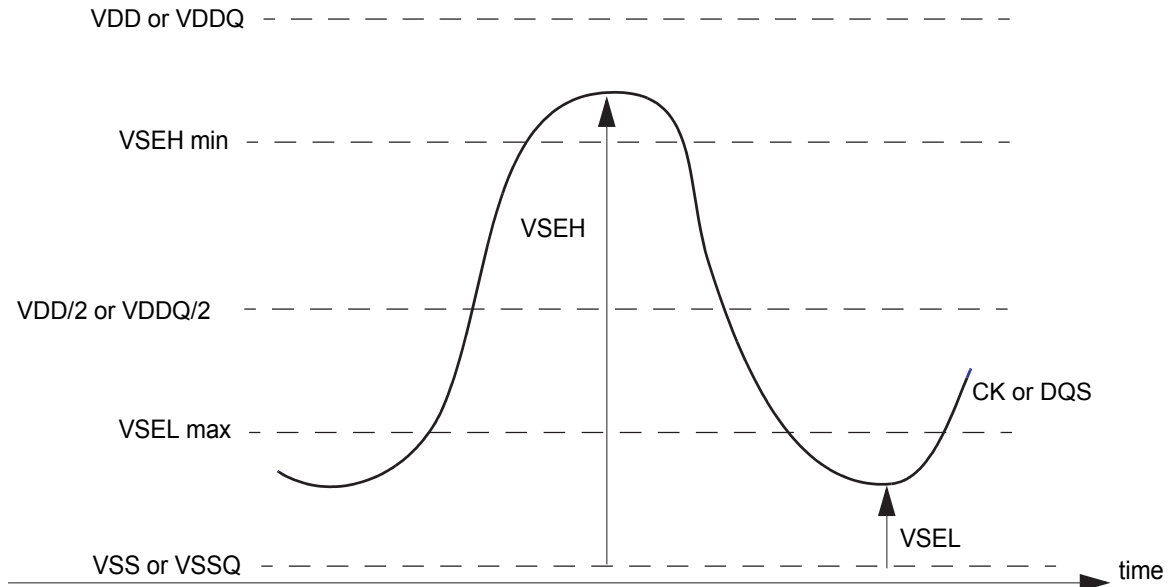
**Single-ended requirements for differential signals**

Each individual component of a differential signal (CK, DQS,  $\overline{CK}$ ,  $\overline{DQS}$ ) has also to comply with certain requirements for single-ended signals.

CK and  $\overline{CK}$  have to approximately reach VSEH min / VSEL max [ approximately equal to the AC-levels ( VIH(AC) / VIL(AC) ) for Address/command signals ] in every half-cycle.

DQS,  $\overline{DQS}$  have to reach VSEH min / VSEL max [ approximately the ac-levels ( VIH(AC) / VIL(AC) ) for DQ signals ] in every half-cycle proceeding and following a valid transition.

Note that the applicable AC-levels for Address/command and DQ's might be different per speed-bin etc. E.g. if VIH150(AC) / VIL150(AC) is used for Address/command signals, then these AC-levels apply also for the single-ended components of differential CK and  $\overline{CK}$ .



Single-ended requirement for differential signals

Note that while Address/command and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL max, VSEH min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

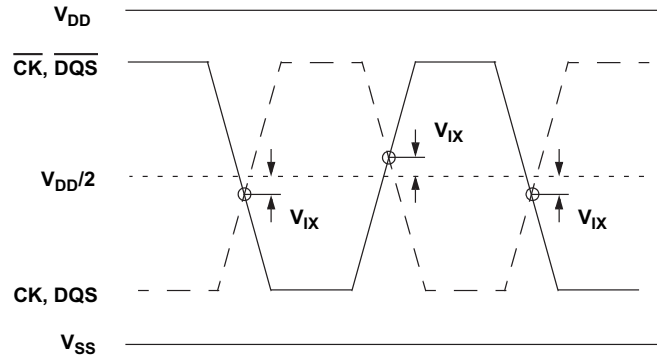
### Single-ended levels for CK, DQS, $\overline{CK}$ , $\overline{DQS}$

Symbol	Parameter	Min.	Max.	Units	Notes
VSEH	Single-ended high-level for strobes	$(VDD/2) + 0.175$	NOTE 3	V	1,2
	Single-ended high-level for CK, $\overline{CK}$	$(VDD/2) + 0.175$	NOTE 3	V	1,2
VSEL	Single-ended low-level for strobes	NOTE 3	$(VDD/2) - 0.175$	V	1,2
	Single-ended low-level for CK, $\overline{CK}$	NOTE 3	$(VDD/2) - 0.175$	V	1,2

NOTE :

- For CK,  $\overline{CK}$  use VIH/VIL(AC) of address/command; for strobes (DQS,  $\overline{DQS}$ ) use VIH/VIL(AC) of DQs.
- VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single-ended components of differential signals CK,  $\overline{CK}$ , DQS,  $\overline{DQS}$  need to be within the respective limits (VIH(DC) max, VIL(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specifications".

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK,  $\overline{\text{CK}}$  and DQS,  $\overline{\text{DQS}}$ ) must meet the requirements in below table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the mid level between of VDD and VSS.



VIX Definition

### Cross point voltage for differential input signals ( CK, DQS )

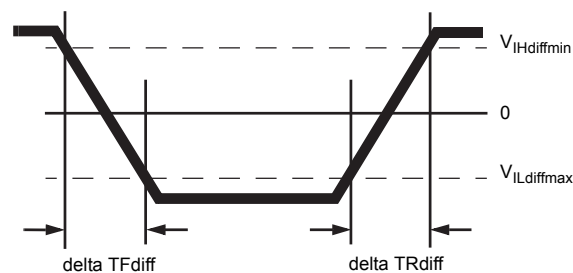
Symbol	Parameter	Min.	Max.	Units	Notes
VIX	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{\text{CK}}$	-150	150	mV	
		-175	175	mV	1
VIX	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{\text{DQS}}$	-150	150	mV	

NOTE :1. Extended range for VIX is only allowed for clock and if single-ended clock input signals CK and  $\overline{\text{CK}}$  are monotonic, have a single-ended swing VSEL / VSEH of at least VDD/2 +/- 250 mV, and the differential slew rate of CK- $\overline{\text{CK}}$  is larger than 3 V/ ns. Refer to the table of Cross point voltage for differential input signals (CK, DQS) for VSEL and VSEH standard values.

### Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge ( CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$ )	VILdiff (max)	VIHdiff (min)	$\frac{VIHdiff (min) - VILdiff (max)}{\Delta TRdiff}$
Differential input slew rate for falling edge ( CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$ )	VIHdiff (min)	VILdiff (max)	$\frac{VIHdiff (min) - VILdiff (max)}{\Delta TFdiff}$

NOTE : The differential signal (i.e. CK -  $\overline{\text{CK}}$  and DQS -  $\overline{\text{DQS}}$ ) must be linear between these thresholds.



Differential Input Slew Rate definition for DQS,  $\overline{\text{DQS}}$ , and CK,  $\overline{\text{CK}}$

## AC and DC Output Measurement Levels

### Single-ended AC & DC Output Levels

Symbol	Parameter	DDR3-1866	Units	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

NOTE : 1. The swing of +/-0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT=VDDQ/2.

### Differential AC & DC Output Levels

Symbol	Parameter	DDR3-1866	Units	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

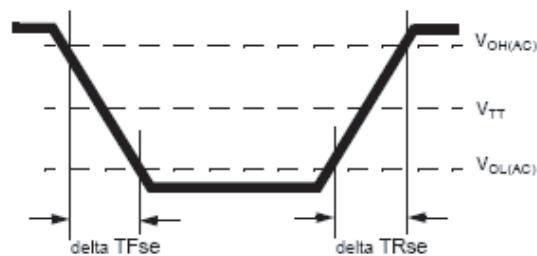
NOTE : 1. The swing of +/-0.2xVDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT=VDDQ/2 at each of the differential outputs.

### Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{\Delta TRse}$
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{VOH(AC)-VOL(AC)}{\Delta TRse}$

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.



Single-ended Output Slew Rate definition



Parameter	Symbol	DDR3-1866		Units
		Min	Max	
Single ended output slew rate	SRQse	2.5	5(1)	V/ns

Description : SR : Slew Rate

Q : Query Output (like in DQ, which stands for Data-in, Query-Output)

se : Single-ended Signals For Ron = RZQ/7 setting

NOTE : (1) In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

- Case\_1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).

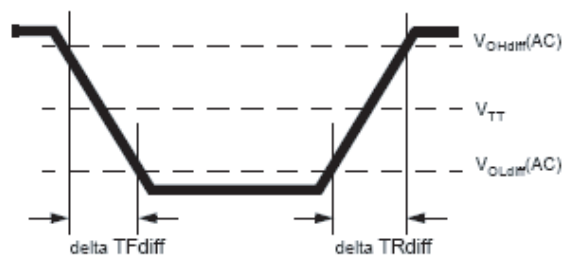
- Case\_2 is defined for a single DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

### Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals.

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	$\frac{VOHdiff(AC)-VOLdiff(AC)}{\Delta TRdiff}$
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	$\frac{VOHdiff(AC)-VOLdiff(AC)}{\Delta TFdiff}$

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate definition

Parameter	Symbol	DDR3-1866		Units
		Min	Max	
Differential output slew rate	SRQdiff	5	12	V/ns

Description : SR : Slew Rate

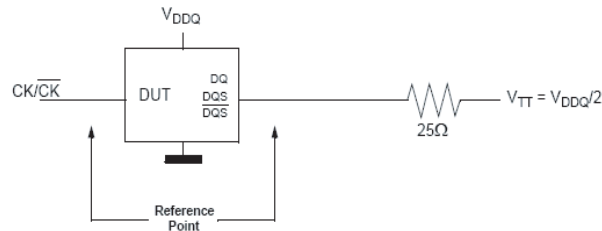
Q : Query Output (like in DQ, which stands for Data-in, Query-Output)

diff : Differential Signals

For Ron = RZQ/7 setting

## Reference Load for AC Timing and Output Slew Rate

Figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements. It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

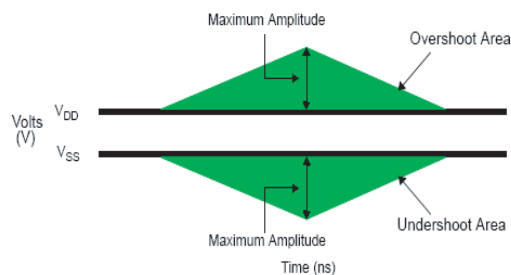


Reference Load for AC Timing and Output Slew Rate

## Overshoot/Undershoot Specification

### Address and Control Overshoot and Undershoot specifications

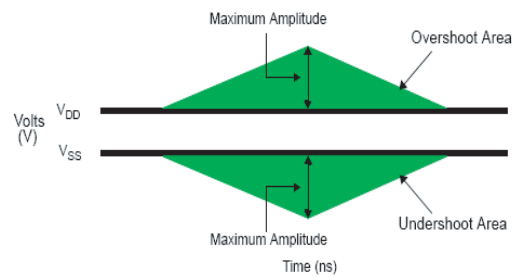
Parameter	Specification	Unit
	DDR3-1866	
Maximum peak amplitude allowed for overshoot area	0.4V	V
Maximum peak amplitude allowed for undershoot area	0.4V	V
Maximum overshoot area above VDD	0.28V-ns	V-ns
Maximum undershoot area below VSS	0.28V-ns	V-ns



Address and Control Overshoot and Undershoot Definition

### Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

Parameter	Specification	Unit
	DDR3-1866	
Maximum peak amplitude allowed for overshoot area	0.4V	V
Maximum peak amplitude allowed for undershoot area	0.4V	V
Maximum overshoot area above VDD	0.11V-ns	V-ns
Maximum undershoot area below VSS	0.11V-ns	V-ns



**Clock, Data, Strobe, Mask Overshoot and Undershoot Definition**

## IDD Specification

( VDD = 1.35V±0.075V; VDDQ =1.35V±0.075V )

Conditions	Symbol	IDD max.	Unit
<b>Operating One Bank Active-Precharge Current;</b> CKE: High; External clock: On; tCK, nRC, nRAS, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : High between ACT and PRE; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD0	96	mA
<b>Operating One Bank Active-Read-Precharge Current;</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD1	125	mA
<b>Precharge Power-Down Current Slow Exit;</b> CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit	IDD2P0	16	mA
<b>Precharge Power-Down Current Fast Exit;</b> CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	IDD2P1	30	mA
<b>Precharge Standby Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD2N	50	mA
<b>Precharge Standby ODT Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: toggling	IDD2NT	58	mA
<b>Precharge Quiet Standby Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD2Q	50	mA
<b>Active Power-Down Current;</b> CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3P	54	mA

Conditions	Symbol	IDD max.	Unit
<b>Active Standby Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3N	62	mA
<b>Operating Burst Read Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : High between RD; Command, Address: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD4R	200	mA
<b>Operating Burst Write Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	IDD4W	360	mA
<b>Burst Refresh Current;</b> CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; $\overline{CS}$ : High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD5B	477	mA
<b>Self Refresh Current: Normal Temperature Range;</b> TCASE: 0- 85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and $\overline{CK}$ : LOW; CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ , Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	IDD6	24	mA
<b>Self Refresh Current: Extended Temperature Range;</b> TCASE: 0- 95°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; External clock: Off; CK and $\overline{CK}$ : LOW; CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$ , Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	IDD6ET	32	mA
<b>Operating Bank Interleave Read Current;</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; $\overline{CS}$ : High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD7	270	mA
<b>RESET Low Current;</b> RESET: Low; External clock: off; CK and $\overline{CK}$ : LOW; CKE: FLOATING; $\overline{CS}$ , Command, Address, Data IO: FLOATING; ODT Signal: FLOATING	IDD8	20	mA

**NOTE :**

- 1) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
- 2) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT\_Nom enable: set MR1 A[9,6,2] = 011B;  
RTT\_Wr enable: set MR2 A[10,9] = 10B
- 3) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
- 4) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
- 5) Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
- 6) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM
- 7) Read Burst type : Nibble Sequential, set MR0 A[3]=0B

***Timing used for IDD and IDDQ Measured - Loop Patterns***

Speed	DDR3-1866	Unit
CL-nRCD-nRP	13-13-13	
tCKmin	1.07	ns
CL	13	nCK
tRCDmin	13	nCK
tRCmin	45	nCK
tRASmin	32	nCK
tRPmin	13	nCK
tFAW	33	nCK
tRRD	6	nCK
tRFC	328	nCK

## Input/Output Capacitance

Parameter	Symbol	DDR3-1866		Units	NOTE
		Min	Max		
Input/output capacitance (DQ, DM, DQS, DQS)	CIO	1.4	2.2	pF	1,2,3
Input capacitance (CK and CK)	CCK	0.8	1.3	pF	2,3
Input capacitance delta (CK and CK)	CDCK	0	0.15	pF	2,3,4
Input capacitance (All other input-only pins)	CI	0.75	1.2	pF	2,3,6
Input capacitance delta (DQS and DQS)	CDDQS	0	0.15	pF	2,3,5
Input capacitance delta (All control input-only pins)	CDI_CTRL	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (all ADD and CMD input-only pins)	CDI_ADD_CMD	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, DQS)	CDIO	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	CZQ	-	3	pF	2,3,12

### NOTE :

1. Although the DM pin have different function, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER( VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET and ODT as necessary). VDD=VDDQ=1.35V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of CCK-CCK
5. Absolute value of CIO(DQS)-CIO(DQS)
6. CI applies to ODT, CS, CKE, A0-A15, BA0-BA2, RAS, CAS, WE
7. CDI\_CTRL applies to ODT, CS and CKE
8. CDI\_CTRL=CI(CTRL)-0.5\*(CI(CLK)+CI(CLK))
9. CDI\_ADD\_CMD applies to A0-A15, BA0-BA2, RAS, CAS and WE
10. CDI\_ADD\_CMD=CI(ADD\_CMD) - 0.5\*(CI(CLK)+CI(CLK))
11. CDIO=CIO(DQ,DM) - 0.5\*(CIO(DQS)+CIO(DQS))
12. Maximum external load capacitance on ZQ pin: 5pF

## DDR3-1866 Speed Bins

Speed Bin			- 10 (DDR3-1866)		Unit	Notes	
CL-nRCD-nRP			13-13-13				
Parameter	Symbol		Min	Max			
Internal read command to first data	tAA		13.91 (13.125)	20	ns	11	
Active to read or write delay time	tRCD		13.91 (13.125)	-	ns	11	
Precharge command period	tRP		13.91 (13.125)	-	ns	11	
Active to active/auto-refresh command time	tRC		47.91 (47.125)	-	ns	11	
Active to precharge command period	tRAS		34	9 * tREFI	ns	9	
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,8
		CWL = 6,7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,8
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	2.5	ns	1,2,3,8
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	1,2,3,8
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	2.5	ns	1,2,3,8
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	1.875	ns	1,2,3,8
	CL = 10	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	1.875	ns	1,2,3,8
		CWL = 8	tCK(avg)	Reserved	Reserved	ns	4
	CL = 11	CWL = 5, 6,7	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 8	tCK(avg)	1.25	1.5	ns	1,2,3,8
	CL = 12	CWL = 5, 6,7,8	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 9	tCK(avg)	Reserved	Reserved	ns	4
CL = 13	CWL = 5, 6,7,8	tCK(avg)	Reserved	Reserved	ns	4	
	CWL = 9	tCK(avg)	1.07	1.25	ns	1,2,3	
Supported CL setting			5, 6, 7, 8, 9, 10,11,13		nCK		
Supported CWL setting			5, 6, 7, 8, 9		nCK		



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**Speed Bin Table Notes**

## NOTE :

1. The CL setting and CWL setting result in tCK(avg) Min and tCK(avg) Max requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg) Min limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next "Supported CL".
3. tCK(avg) Max limits: Calculate tCK(avg) = tAA Max / CL Selected and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(avg) Max corresponding to CL selected.
4. "Reserved" settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
8. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
9. tREFI depends on operating case temperature (Tc).
10. For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333(CL9) devices supporting downshift to DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600(CL11) devices supporting downshift to DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1866(CL13) devices supporting downshift to DDR3-1600(CL11) or DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600 devices supporting down binning to DDR3-1333 or DDR3-1066 should program 13.125ns in SPD byte for tAAmin (Byte 16), tRCDmin (Byte 18) and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns, (tRASmin + tRPmin = 36ns + 13.125ns) for DDR3-1333 and 48.125ns (tRASmin + tRPmin = 35ns + 13.125ns) for DDR3-1600.
11. For devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programmed to match. For example, DDR3-1866 devices supporting down binning to DDR3-1600 or DDR3-1333 or 1066 should program 13.125ns in SPD bytes for tAAmin(byte16), tRCDmin(Byte18) and tRP-min (byte20). Once tRP (Byte20) is programmed to 13.125ns, tRCmin (Byte21,23) also should be programmed accordingly. For example, 47.125ns (tRASmin + tRPmin = 34ns + 13.125ns)

( VDD = 1.35V±0.075V; VDDQ =1.35V±0.075V )

Parameter	Symbol	- 10 (DDR3-1866)		Unit	Note
		Min	Max		
Average clock cycle time	$t_{CK}(avg)$	Please refer Speed Bins		ps	
Minimum clock cycle time (DLL-off mode)	$t_{CK}$ (DLL-off)	8	-	ns	6
Average CK high level width	$t_{CH}(avg)$	0.47	0.53	$t_{CK}(avg)$	
Average CK low level width	$t_{CL}(avg)$	0.47	0.53	$t_{CK}(avg)$	
Active Bank A to Active Bank B command period	$t_{RRD}$	6	-	ns	
		4	-	nCK	
Four activate window	$t_{FAW}$	35	-	ns	
Address and Control input hold time (VIH/VIL (DC100) levels)	$t_{IH}(base)$ DC100	100	-	ps	16
Address and Control input setup time (VIH/VIL (AC125) levels)	$t_{IS}(base)$ AC125	150	-	ps	16
Address and Control input setup time (VIH/VIL (AC135) levels)	$t_{IS}(base)$ AC135	65	-	ps	16
DQ and DM input hold time (VIH/VIL (DC100) levels)	$t_{DH}(base)$ DC100	70	-	ps	17
DQ and DM input setup time (VIH/VIL (AC135) levels)	$t_{DS}(base)$ AC135	68	-	ps	17
Control and Address Input pulse width for each input	$t_{IPW}$	535	-	ps	25
DQ and DM Input pulse width for each input	$t_{DIPW}$	320	-	ps	25
DQ high impedance time	$t_{HZ}(DQ)$	-	195	ps	13,14
DQ low impedance time	$t_{LZ}(DQ)$	-390	195	ps	13,14
DQS, $\overline{DQS}$ high impedance time (RL + BL/2 reference)	$t_{HZ}(DQS)$	-	195	ps	13,14
DQS, $\overline{DQS}$ low impedance time (RL - 1 reference)	$t_{LZ}(DQS)$	-390	195	ps	13,14
DQS, $\overline{DQS}$ to DQ Skew, per group, per access	$t_{DQSQ}$	-	85	ps	12,13
$\overline{CAS}$ to $\overline{CAS}$ command delay	$t_{CCD}$	4	-	nCK	
DQ output hold time from DQS, $\overline{DQS}$	$t_{QH}$	0.38	-	$t_{CK}(avg)$	12,13
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	$t_{DQSK}$	-195	195	ps	12,13
DQS latching rising transitions to associated clock edges	$t_{DQSS}$	-0.27	0.27	$t_{CK}(avg)$	
DQS falling edge hold time from rising CK	$t_{DSH}$	0.18	-	$t_{CK}(avg)$	29
DQS falling edge setup time to rising CK	$t_{DSS}$	0.18	-	$t_{CK}(avg)$	29
DQS input high pulse width	$t_{DQSH}$	0.45	0.55	$t_{CK}(avg)$	27,28

Parameter	Symbol	-10 (DDR3-1866)		Unit	Note
		Min	Max		
DQS input low pulse width	$t_{DQSL}$	0.45	0.55	$t_{CK}(avg)$	26,28
DQS output high time	$t_{QSH}$	0.40	-	$t_{CK}(avg)$	12,13
DQS output low time	$t_{QSL}$	0.40	-	$t_{CK}(avg)$	12,13
Mode register set command cycle time	$t_{MRD}$	4	-	nCK	
Mode register set command update delay	$t_{MOD}$	15	-	ns	
		12	-	nCK	
Read preamble time	$t_{RPRE}$	0.9	-	$t_{CK}(avg)$	13,19
Read postamble time	$t_{RPST}$	0.3	-	$t_{CK}(avg)$	11,13
Write preamble time	$t_{WPRE}$	0.9	-	$t_{CK}(avg)$	1
Write postamble time	$t_{WPST}$	0.3	-	$t_{CK}(avg)$	1
Write recovery time	$t_{WR}$	15	-	ns	
Auto precharge write recovery + Precharge time	$t_{DAL}(min)$	WR + roundup [ $t_{RP} / t_{CK}(avg)$ ]		nCK	
Multi-purpose register recovery time	$t_{MPRR}$	1	-	nCK	22
Internal write to read command delay	$t_{WTR}$	7.5	-	ns	18
		4	-	nCK	18
Internal read to precharge command delay	$t_{RTP}$	7.5	-	ns	
		4	-	nCK	
Minimum CKE low width for Self-refresh entry to exit timing	$t_{CKESR}$	$t_{CKE}(min) + 1nCK$	-		
Valid clock requirement after Self-refresh entry or Power-down entry	$t_{CKSRE}$	10	-	ns	
		5	-	nCK	
Valid clock requirement before Self-refresh exit or Power-down exit	$t_{CKSRX}$	10	-	ns	
		5	-	nCK	
Exit Self-refresh to commands not requiring a locked DLL	$t_{XS}$	$t_{RFC}(min) + 10$	-	ns	
		5	-	nCK	
Exit Self-refresh to commands requiring a locked DLL	$t_{XSDLL}$	$t_{DLLK}(min)$	-	nCK	
Auto-refresh to Active/Auto-refresh command time	$t_{RFC}$	350	-	ns	
Average Periodic Refresh Interval $0^{\circ}C \leq T_c \leq +85^{\circ}C$	$t_{REFI}$	-	7.8	$\mu s$	
Average Periodic Refresh Interval $+85^{\circ}C < T_c \leq +95^{\circ}C$	$t_{REFI}$	-	3.9	$\mu s$	
CKE minimum high and low pulse width	$t_{CKE}$	5	-	ns	
		3	-	nCK	
Exit reset from CKE high to a valid command	$t_{XPR}$	$t_{RFC}(min) + 10$	-	ns	
		5	-	nCK	

Parameter	Symbol	-10 (DDR3-1866)		Unit	Note
		Min	Max		
DLL locking time	$t_{DLLK}$	512	-	nCK	
Power-down entry to exit time	$t_{PD}$	$t_{CKE}(\text{min})$	$9 \cdot t_{REFI}$		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	$t_{XPDLL}$	24	-	ns	2
		10	-	nCK	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	$t_{XP}$	6	-	ns	
		3	-	nCK	
Command pass disable delay	$t_{CPDED}$	2	-	nCK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	nCK	20
Timing of PRE command to Power-down entry	$t_{PRPDEN}$	1	-	nCK	20
Timing of RD/RDA command to Power-down entry	$t_{RDPDEN}$	RL+4+1	-	nCK	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRPDEN}$ (min)	WL + 4 + [tWR/tCK(avg)]		nCK	9
Timing of WR command to Power-down entry (BC4MRS)	$t_{WRPDEN}$ (min)	WL + 2 + [tWR/tCK(avg)]		nCK	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRAPDEN}$	WL+4 +WR+1	-	nCK	10
Timing of WRA command to Power-down entry (BC4MRS)	$t_{WRAPDEN}$	WL+2 +WR+1	-	nCK	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	nCK	20,21
Timing of MRS command to Power-down entry	$t_{MRSPDEN}$	$t_{MOD}$ (min)	-		
RTT turn-on	$t_{AON}$	-195	195	ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	$t_{AONPD}$	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	$t_{AOF}$	0.3	0.7	$t_{CK}(\text{avg})$	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	$t_{AOFPD}$	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	nCK	
RTT dynamic change skew	$t_{ADC}$	0.3	0.7	$t_{CK}(\text{avg})$	
Power-up and reset calibration time	$t_{ZQinit}$	512	-	nCK	
Normal operation full calibration time	$t_{ZQoper}$	256	-	nCK	
Normal operation short calibration time	$t_{ZQCS}$	64	-	nCK	23

Parameter	Symbol	- 10 (DDR3-1866)		Unit	Note
		Min	Max		
First DQS pulse rising edge after write leveling mode is programmed	$t_{WLMRD}$	40	-	nCK	3
DQS, $\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	nCK	3
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	$t_{WLS}$	140	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	$t_{WLH}$	140	-	ps	
Write leveling output delay	$t_{WLO}$	0	7.5	ns	
Write leveling output error	$t_{WLOE}$	0	2	ns	
Absolute clock period	$t_{CK(abs)}$	$t_{CK(avg)min} + t_{JIT(per)min}$	$t_{CK(avg)max} + t_{JIT(per)max}$	ps	
Absolute clock high pulse width	$t_{CH(abs)}$	0.43	-	$t_{CK(avg)}$	30
Absolute clock low pulse width	$t_{CL(abs)}$	0.43	-	$t_{CK(avg)}$	31
Clock period jitter	$t_{JIT(per)}$	-60	60	ps	
Clock period jitter during DLL locking period	$t_{JIT(per,lck)}$	-50	50	ps	
Cycle to cycle period jitter	$t_{JIT(cc)}$	-	120	ps	
Cycle to cycle period jitter during DLL locking period	$t_{JIT(cc,lck)}$	-	100	ps	
Cumulative error across 2 cycles	$t_{ERR(2per)}$	-88	88	ps	
Cumulative error across 3 cycles	$t_{ERR(3per)}$	-105	105	ps	
Cumulative error across 4 cycles	$t_{ERR(4per)}$	-117	117	ps	
Cumulative error across 5 cycles	$t_{ERR(5per)}$	-126	126	ps	
Cumulative error across 6 cycles	$t_{ERR(6per)}$	-133	133	ps	
Cumulative error across 7 cycles	$t_{ERR(7per)}$	-139	139	ps	
Cumulative error across 8 cycles	$t_{ERR(8per)}$	-145	145	ps	
Cumulative error across 9 cycles	$t_{ERR(9per)}$	-150	150	ps	
Cumulative error across 10 cycles	$t_{ERR(10per)}$	-154	154	ps	
Cumulative error across 11 cycles	$t_{ERR(11per)}$	-158	158	ps	
Cumulative error across 12 cycles	$t_{ERR(12per)}$	-161	161	ps	
Cumulative error across n = 13,14,...49,50 cycles	$t_{ERR(nper)}$	$t_{ERR(nper)min} = (1 + 0.68\ln(n)) * t_{JIT(per)min}$ $t_{ERR(nper)max} = (1 + 0.68\ln(n)) * t_{JIT(per)max}$		ps	32

## Notes for AC Electrical Characteristics

NOTE :

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTL<sub>on</sub>.
8. ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTL<sub>off</sub>.
9. tWR is defined in ns, for calculation of tWRP<sub>DEN</sub> it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQ<sub>SCK</sub>(min) plus tQSH(min) on the left side and tHZ(DQS)<sub>max</sub> on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.
15. tREFI depends on operating case temperature (Tc).
16. tIS(base) and tIH(base) values are for 1V/ns command/address single-ended slew rate and 2V/ns CK,  $\overline{CK}$  differential slew rate, Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Address / Command Setup, Hold and Derating section.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS,  $\overline{DQS}$  differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows ;
  - For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
  - For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
  - For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQ<sub>SCK</sub>(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFP<sub>DEN</sub>(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the "Output Driver Voltage and Temperature Sensitivity" and "ODT Voltage and Temperature Sensitivity" tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:
 
$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$
 where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.
24. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of

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derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

25. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
26. tDQSL describes the instantaneous differential input low pulse width on DQS -  $\overline{\text{DQS}}$ , as measured from one falling edge to the next consecutive rising edge.
27. tDQSH describes the instantaneous differential input high pulse width on DQS -  $\overline{\text{DQS}}$ , as measured from one rising edge to the next consecutive falling edge.
28. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
29. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
30. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
31. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
32. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

**Package Diagram (x16)**  
**96-Ball Fine Pitch Ball Grid Array Outline**

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm

