Revision History

2Gb LPDDR SDRAM AS4C64M32MD1A-5BIN - 90 ball FPBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Release	Nov. 2019

Alliance Memory Inc.12815 NE 124th St, Suite#D, Kirkland, WA 98034 USA
Tel: +1(425)898-4456 Fax +1(425)896-8628

Features

- Power Supply VDD/VDDQ = 1.8V/1.8V
- Double-data-rate architecture; two data transfers per clock cycle.
- Bidirectional data strobe (DQS).
- Four banks operation.
- Differential clock inputs (CK and CK#).
- MRS cycle with address key programs.
  - CAS Latency (3)
  - Burst Length (2, 4, 8, 16)
  - Burst Type (Sequential & Interleave)
- EMRS cycle with address key programs.
  - Partial Array Self Refresh (Full, 1/2, 1/4 Array)
  - Output Driver Strength Control (Full, 1/2, 1/4, 1/8, 3/4, 3/8, 5/8, 7/8)
- Internal Temperature Compensated Self Refresh.
- All inputs except data & DM are sampled at the positive going edge of the system clock (CK).
- Data I/O transactions on both edges of data strobe, DM for masking.
- Edge aligned data output, center aligned data input.
- No DLL; CK to DQS is not synchronized.
- DM for write masking only.
- Auto refresh duty cycle. - 7.8us for -40 to 85'C
- Clock stop capability.
- Package

  x32 : 8.0 x 13.0mm 90 Ball FPBGA
- Operating Temperature Range

  Industrial Type (-40℃ to +85℃)

Operating Frequency

Operating Conditions	DDR400
Speed @CL2 [1]	83MHz(max.)
Speed @CL3 [1]	200MHz(max.)

NOTE :
1) CAS Latency

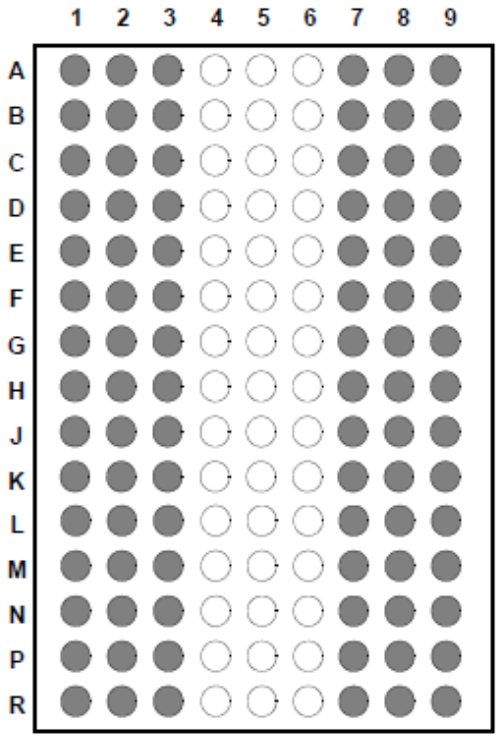
Ordering Information

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C64M32MD1A-5BIN	64M x 32	Industrial -40°C to 85°C	200 Hz	90-ball FBGA

1.0 PIN DESCRIPTION

FPBGA Assignment (x32)

Top View
(Balls seen through the package)

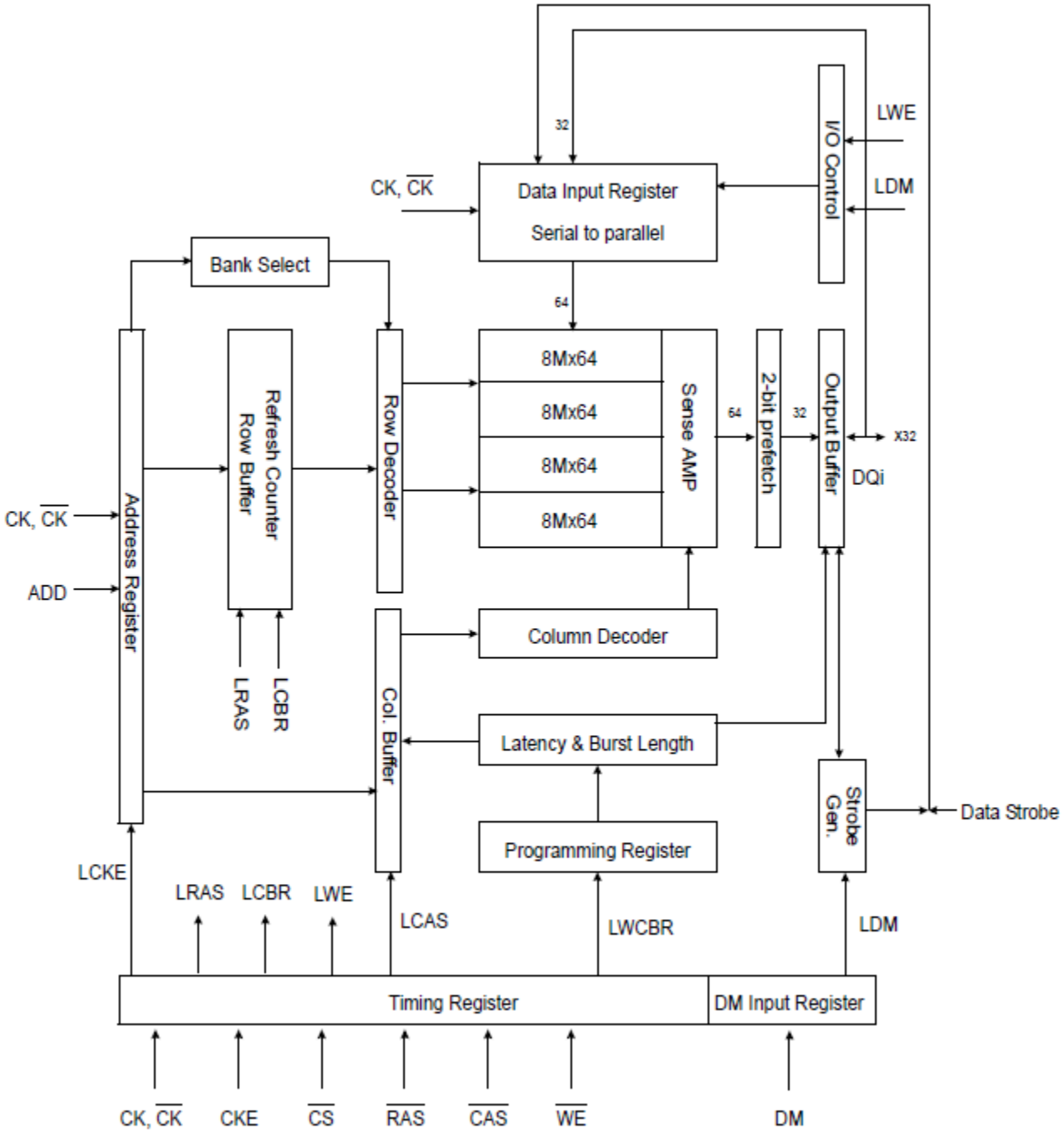


90-Ball (6x15) CSP						
	1	2	3	7	8	9
A	VSS	DQ31	VSSQ	VDDQ	DQ16	VDD
B	VDDQ	DQ29	DQ30	DQ17	DQ18	VSSQ
C	VSSQ	DQ27	DQ28	DQ19	DQ20	VDDQ
D	VDDQ	DQ25	DQ26	DQ21	DQ22	VSSQ
E	VSSQ	DQS3	DQ24	DQ23	DQS2	VDDQ
F	VDD	DM3	NC	A13	DM2	VSS
G	CKE	CK	$\overline{CK}$	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	A12	$\overline{CS}$	BA0	BA1
J	A6	A7	A8	A10/AP	A0	A1
K	A4	DM1	A5	A2	DM0	A3
L	VSSQ	DQS1	DQ8	DQ7	DQS0	VDDQ
M	VDDQ	DQ9	DQ10	DQ5	DQ6	VSSQ
N	VSSQ	DQ11	DQ12	DQ3	DQ4	VDDQ
P	VDDQ	DQ13	DQ14	DQ1	DQ2	VSSQ
R	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD

1.1 Input/Output Function Description

Symbol	Type	Description
CK, $\overline{CK}$	Input	Clock : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Internal clock signals are derived from CK / $\overline{CK}$.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any banks). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{CS}$	Input	Chip Select : $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM0,DM1, DM2,DM3	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to match the DQ and DQS loading DM0 corresponds to the data on DQ0-DQ7; DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, DM3 corresponds to the data on DQ24-DQ31
BA0, BA1	Input	Bank Address Inputs : BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the opcode during a MODE REGISTER SET command. BA0 and BA1 determines which mode register (mode register or extended mode register) is loaded during the MODE REGISTER SET command.
DQ	I/O	Data Inputs/Outputs : Data bus
DQS0,DQS1, DQS2,DQS3	I/O	Data Strobes : Output with read data, input with write data. Edge-aligned with read data, centered in write data. it is used to fetch write data. DQS0 corresponds to the data on DQ0-DQ7; DQS1 corresponds to the data on DQ8-DQ15,DQS2 corresponds to the data on DQ16-DQ23, DQS3 corresponds to the data on DQ24-DQ31
NC	-	No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply : 1.7V to 1.95V
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply : 1.7V to 1.95V
VSS	Supply	Ground.

1.2 FUNCTIONAL BLOCK DIAGRAM



2.0 FUNCTIONAL DESCRIPTION

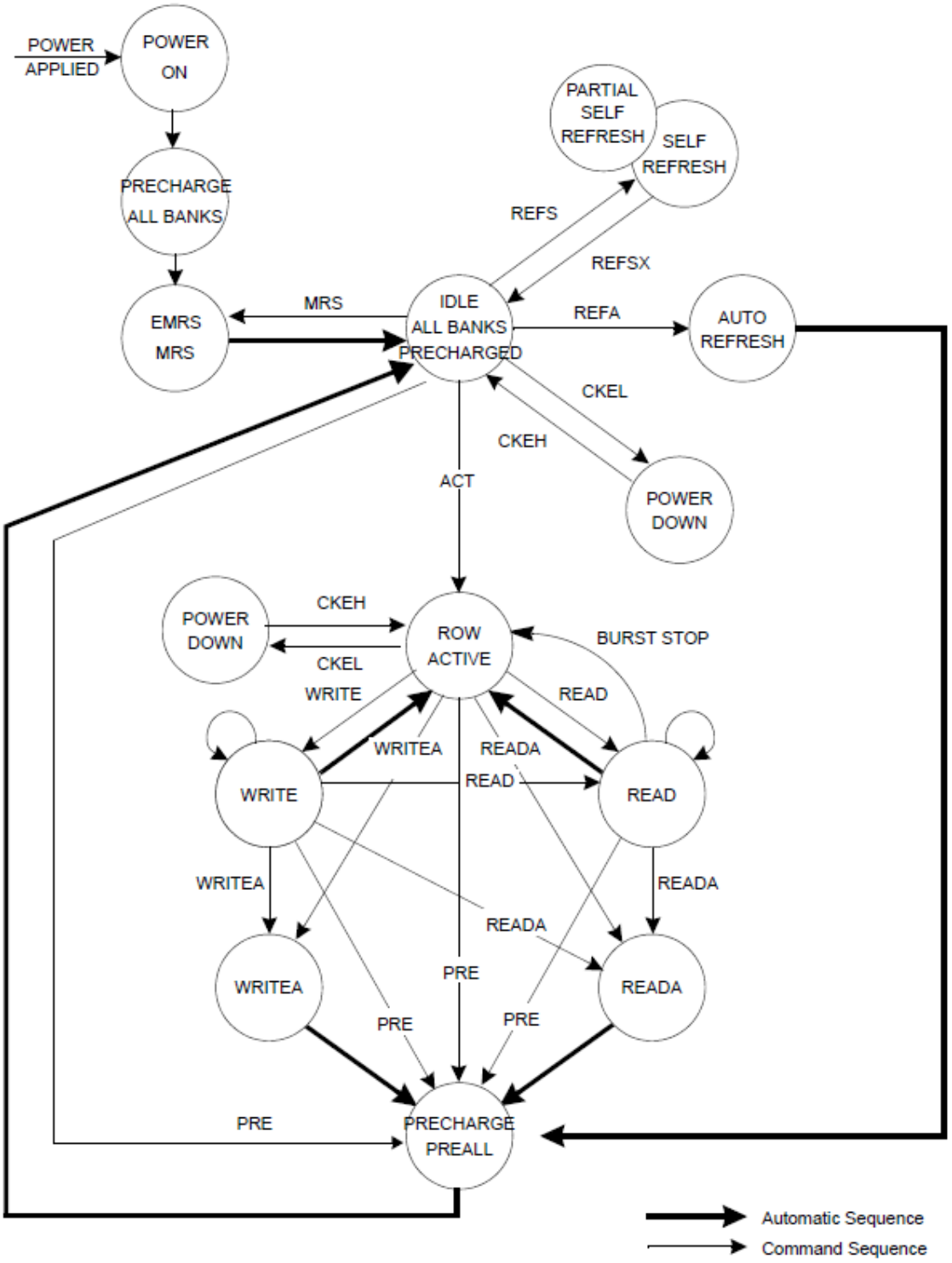


Figure 1. State diagram

3.0 MODE REGISTER DEFINITION

3.1 Mode Register Set (MRS)

The mode register is designed to support the various operating modes of Mobile DDR SDRAM. It includes CAS latency, addressing mode, burst length, test mode and vendor specific options to make Mobile DDR SDRAM useful for variety of applications. The mode register is written by asserting low on /CS,/RAS,/CAS and /WE (The Mobile DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The states of address pins A0 ~ A13 and BA0, BA1 in the same cycle as /CS, /RAS, /CAS and /WE going low are written in the mode register. Two clock cycles are required to complete the write operation in the mode register. Even if the power-up sequence is finished and some read or write operation is executed afterward, the mode register contents can be changed with the same command and two clock cycles. This command must be issued only when all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency (read latency from column address) uses A4 ~ A6, A7 ~ A13 is used for test mode. BA0 and BA1 must be set to low for proper MRS operation.

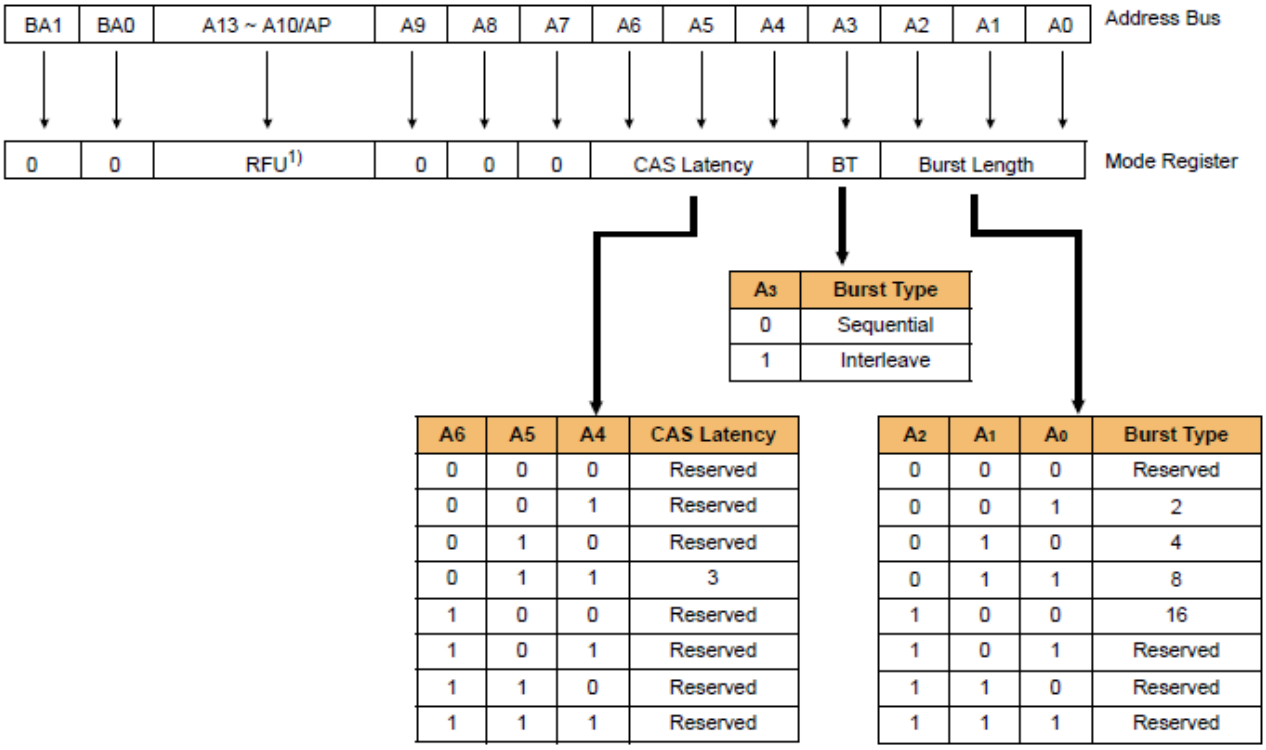


Figure 2. Mode Register Set

NOTE :

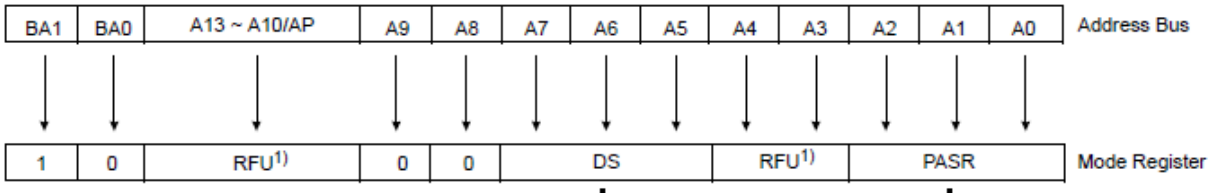
1) RFU (Reserved for future use) should stay "0" during MRS cycle

[Table 1] Burst address ordering for burst length

Burst Length	Starting Address (A3, A2, A1, A0)	Sequential Mode	Interleave Mode
2	xxx0	0, 1	0, 1
	xxx1	1, 0	1, 0
4	xx00	0, 1, 2, 3	0, 1, 2, 3
	xx01	1, 2, 3, 0	1, 0, 3, 2
	xx10	2, 3, 0, 1	2, 3, 0, 1
	xx11	3, 0, 1, 2	3, 2, 1, 0
8	x000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	x001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	x010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	x011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	x100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	x101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	x110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	x111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
16	0000	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15
	0001	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0	1, 0, 3, 2, 5, 4, 7, 6, 9, 8, 11,10,13,12,15,14
	0010	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1	2, 3, 0, 1, 6, 7, 4, 5,10,11, 8, 9, 14,15,12,13
	0011	3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4,11,10, 9, 8, 15,14,13,12
	0100	4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3,12,13,14,15, 8, 9, 10,11
	0101	5, 6, 7,8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2,13,12,15,14, 9, 8,11,10
	0110	6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1,14,15,12,13,10,11, 8, 9
	0111	7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0, 15,14,13,12,11,10, 9, 8
	1000	8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6, 7	8, 9,10,11,12,13,14,15, 0, 1, 2, 3, 4, 5, 6, 7
	1001	9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6, 7, 8	9, 8, 11,10,13,12,15,14,1, 0, 3, 2, 5, 4, 7, 6
	1010	10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9	10,11, 8, 9, 14,15,12,13, 2, 3, 0, 1, 6, 7, 4, 5
	1011	11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	11,10, 9, 8, 15,14,13,12, 3, 2, 1, 0, 7, 6, 5, 4
	1100	12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	12,13,14,15, 8, 9, 10,11, 4, 5, 6, 7, 0, 1, 2, 3
	1101	13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11,12	13,12,15,14, 9, 8,11,10, 5, 4, 7, 6, 1, 0, 3, 2
	1110	14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	14,15,12,13,10,11, 8, 9, 6, 7, 4, 5, 2, 3, 0, 1
	1111	15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	15,14,13,12,11,10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

3.2 Extended Mode Register Set (EMRS)

The extended mode register is designed to support for the desired operating modes of DDR SDRAM. The extended mode register is written by asserting low on /CS, /RAS, /CAS, /WE and high on BA1, low on BA0(The Mobile DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A13 in the same cycle as /CS, /RAS, /CAS and /WE going low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. Even if the power-up sequence is finished and some read or write operations is executed afterward, the mode register contents can be changed with the same command and two clock cycles. But this command must be issued only when all banks are in the idle state. A0 - A2 are used for partial array self refresh and A5 - A7 are used for driver strength control. "High" on BA1 and "Low" on BA0 are used for EMRS. All the other address pins except A0,A1,A2,A5,A6,A7, BA1, BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



DS			
A7	A6	A5	Driver Strength
0	0	0	Full
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	3/4
1	0	1	3/8
1	1	0	5/8
1	1	1	7/8

PASR			
A2	A1	A0	Refreshed Area
0	0	0	Full Array
0	0	1	1/2 Array
0	1	0	1/4 Array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Figure 3. Extended Mode Register Set

NOTE :
1) RFU (Reserved for future use) should stay "0" during EMRS cycle

3.3 Internal Temperature Compensated Self Refresh (TCSR)

1. In order to save power consumption, this Mobile DRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the real device temperature.

2. TCSR ranges for IDD6 shown in the table are only examples.

3. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

Temperature Range	Self Refresh Current (IDD6)			Unit
	Full Array	1/2 Array	1/4 Array	
85 °C	1700	1400	1200	uA
45 °C	400	270	200	

NOTE :
1) IDD6 85°C is guaranteed, IDD6 45°C is typical value.

3.4 Partial Array Self Refresh (PASR)

1. In order to save power consumption, Mobile DDR SDRAM includes PASR option. 2. Mobile DDR SDRAM supports three kinds of PASR in self refresh mode; Full array, 1/2 Array, 1/4 Array.

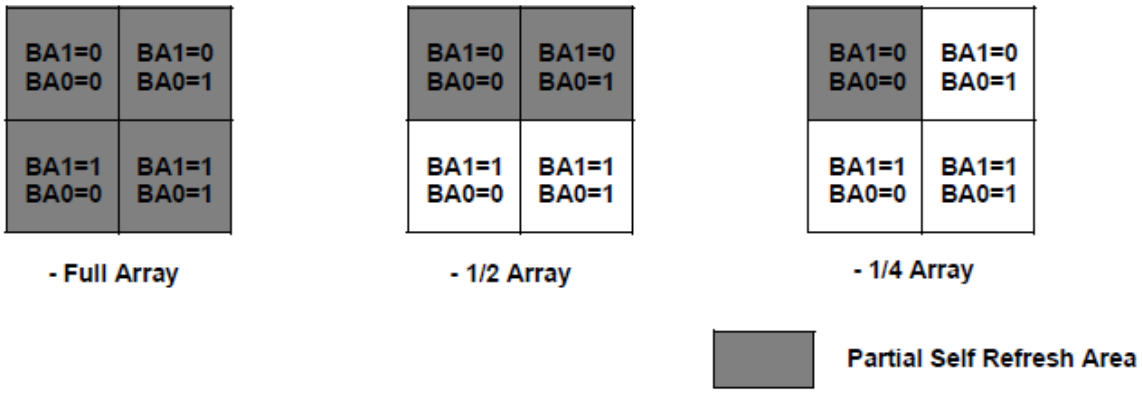


Figure 4. EMRS code and TCSR, PASR

4.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_{IN}, V_{OUT}	- 0.5 ~ 2.7	V
Voltage on VDD supply relative to VSS	VDD	- 0.5 ~ 2.7	V
Voltage on VDDQ supply relative to VSS	VDDQ	- 0.5 ~ 2.7	V
Storage temperature	T_{STG}	- 55 ~ + 150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

NOTE :

1) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
2) Functional operation should be restricted to recommend operation condition.
3) Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

5.0 DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to VSS=0V, TC = -40°C to 85°C)

Parameter		Symbol	Min	Max	Unit	Note
Supply voltage (for device with a nominal VDD of 1.8V)		VDD	1.7	1.95	V	1
I/O Supply voltage		VDDQ	1.7	1.95	V	1
Input logic high voltage	Address	V_{IH}(DC)	0.8 x VDDQ	VDDQ + 0.3	V	2
	Data		0.7 x VDDQ	VDDQ + 0.3	V	
Input logic low voltage	Address	V_{IL}(DC)	-0.3	0.2 x VDDQ	V	2
	Data		-0.3	0.3 x VDDQ	V	
Output logic high voltage		V_{OH}(DC)	0.9 x VDDQ	-	V	I_{OH} = - 0.1mA
Output logic low voltage		V_{OL}(DC)	-	0.1 x VDDQ	V	I_{OL} = 0.1mA
Input leakage current		I_I	-2	2	uA	3
Output leakage current		I_{OZ}	-5	5	uA	

NOTE :

1) Under all conditions, VDDQ must be less than or equal to VDD.
2) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
3) Any input 0V ≤ VIN ≤VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.

6.0 DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to VSS = 0V, Tc = -40 to 85°C)

Parameter	Symbol	Test Condition			DDR400	Unit	Note
Operating Current (One Bank Active)	IDD0	tRC=tRCmin; tCK=tCKmin; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE			70	mA	
Precharge Standby Current in power-down mode	IDD2P	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE			1.0	mA	
	IDD2PS	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE			1.0		
Precharge Standby Current in non power-down mode	IDD2N	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE			8	mA	
	IDD2NS	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE			4		
Active Standby Current in power-down mode	IDD3P	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE			6	mA	
	IDD3PS	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE			5		
Active Standby Current in non power-down mode (One Bank Active)	IDD3N	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE			15	mA	
	IDD3NS	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE			10		
Operating Current (Burst Mode)	IDD4R	one bank active; BL=4; CL=3; tCK = tCKmin; continuous read bursts; I_{OUT} =0 mA address inputs are SWITCHING; 50% data change each burst transfer			100	mA	
	IDD4W	one bank active; BL = 4; tCK = tCKmin; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer			90		
Refresh Current	IDD5	tRC ≥ tRFC; tCK = tCKmin; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE			250	mA	1
Self Refresh Current	IDD6	CKE is LOW; t CK = t CKmin; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	TCSR Range		Values		5
			Full Array	85°C	2000	uA	
				45°C	400		
			1/2 Array	85°C	1400	uA	
				45°C	270		
			1/4 Array	85°C	1200	uA	
				45°C	200		
Deep Power Down Current	IDD8	Deep Power Down Mode Current			10	uA	

1) IDD5 is measured in the below test condition.

Density	128Mb	256Mb	512Mb	1Gb	2Gb	Unit
^{t}RFC	80	80	110	140	140	ns

2) The IDD values need to be measured after devices are properly initialized following all sequences including MRS and EMRS in "Power Up Sequence" section in the specification.

3) Input slew rate is 1V/ns.

4) Definitions for IDD:

LOW is defined as $V_{IN} \leq 0.1 * VDDQ$;

HIGH is defined as $V_{IN} \geq 0.9 * VDDQ$;

STABLE is defined as inputs stable at a HIGH or LOW level;

SWITCHING is defined as: - address and command: inputs changing between HIGH and LOW once per two clock cycles;
- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

5) IDD6 85° C is guaranteed, IDD6 45° C is typical value.

7.0 AC OPERATING CONDITIONS & TIMMING SPECIFICATION

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, all inputs	V_{IH} (AC)	0.8 x VDDQ	VDDQ + 0.3	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL} (AC)	-0.3	0.2 x VDDQ	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	V_{IX} (AC)	0.4 x VDDQ	0.6 x VDDQ	V	2

NOTE :

1) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
2) The value of V_{IX} is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

8.0 AC TIMMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	DDR400		Unit	Note
			Min	Max		
Clock cycle time	CL=2	t_{CK}	12.0		ns	1,2
	CL=3		5			
Row cycle time		t_{RC}	55		ns	
Row active time		t_{RAS}	40	70,000	ns	
RAS to CAS delay		t_{RCD}	15		ns	
Row precharge time		t_{RP}	15		ns	
Row active to Row active delay		t_{RRD}	10		ns	
Write recovery time		t_{WR}	15		ns	
Last data in to Active delay		t_{DAL}	-		-	3
Last data in to Read command		t_{CDLR}	2		tCK	
Col. address to Col. address delay		t_{CCD}	1		tCK	
Clock high level width		t_{CH}	0.45	0.55	tCK	
Clock low level width		t_{CL}	0.45	0.55	tCK	
DQ Output data access time from CK / CK	CL=2	t_{AC}	2	6.5	ns	4
	CL=3		2	5		
DQS Output data access time from CK / CK	CL=2	t_{DQSCK}	2	6.5	ns	
	CL=3		2	5		
Data strobe edge to output data edge		t_{DQSQ}		0.4	ns	
Read Preamble	CL=2	t_{RPRE}	0.5	1.1	tCK	
	CL=3		0.9	1.1		
Read Postamble		t_{RPST}	0.4	0.6	tCK	
CK to valid DQS-in		t_{DQSS}	0.75	1.25	tCK	
DQS-in setup time		t_{WPRES}	0		ns	5
DQS-in hold time		t_{WPREH}	0.25		tCK	
DQS-in high level width		t_{DQSH}	0.4	0.6	tCK	
DQS-in low level width		t_{DQSL}	0.4	0.6	tCK	
DQS falling edge to CK setup time		t_{DSS}	0.2		tCK	
DQS falling edge hold time from CK		t_{DSH}	0.2		tCK	
DQS-in cycle time		t_{DSC}	0.9	1.1	tCK	
Address and Control Input setup time	fast slew rate	t_{IS}	0.9		ns	7
	slow slew rate		1.1			8
Address and Control Input hold time	fast slew rate	t_{IH}	0.9		ns	7
	slow slew rate		1.1			8
Address & Control input pulse width		t_{IPW}	2.2			
DQ & DM setup time to DQS	fast slew rate	t_{DS}	0.48		ns	6,7
	slow slew rate		0.58			6,8
DQ & DM hold time to DQS	fast slew rate	t_{DH}	0.48		ns	6,7
	slow slew rate		0.58			6,8
DQ & DM input pulse width		t_{DIPW}	1.2		ns	
DQ & DQS low-impedence time from CK / $\overline{CK}$		t_{LZ}	1.0		ns	
DQ & DQS high-impedence time from CK / $\overline{CK}$		t_{HZ}		5	ns	
DQS write postamble time		t_{WPST}	0.4	0.6	tCK	

Parameter	Symbol	DDR400		Unit	Note
		Min	Max		
DQS write preamble time	t_{WPRE}	0.25		tCK	
Refresh interval time	t_{REF}		64	ms	
Mode register set cycle time	t_{MRD}	2		tCK	
Power down exit time	t_{PDEX}	2		tCK	
CKE min. pulse width (high and low pulse width)	t_{CKE}	2		tCK	
Auto refresh cycle time	t_{RFC}	120		ns	9
Exit self refresh to active command	t_{XSR}	120		ns	
Data hold from DQS to earliest DQ edge	t_{QH}	t_{HP}min - t_{QHS}		ns	
Data hold skew factor	t_{QHS}		0.5	ns	
Clock half period	t_{HP}	t_{CL}min or t_{CH}min		ns	
Clock half period	t_{HP}	t_{CL}min or t_{CH}min		ns	
Minimum Deep Power Down Time	t_{DPD}	500		us	

NOTE :

1) tCK (max) value is measured at 100ns.
2) The only time that the clock Frequency is allowed to be changed is during clock stop, power-down, self-refresh modes.
3) In case of below 33MHz (tCK=30ns) condition, SEC could support tDAL (=2*tCK).
   tDAL =(tWR/tCK) + (tRP/tCK)
4) tAC (min) value is measured at the high VDD (1.95V) and cold temperature (-40°C).
   tAC (max) value is measured at the low VDD (1.7V) and hot temperature (85°C).
   tAC is measured in the device with half driver strength and under the AC output load condition (Fig.6 in next Page).
5) The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
6) I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Data Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 1.0V/ns and slew rate 2 =0.8V/ns, then the Delta Rise/Fall Rate =-0.25ns/V.

7) Input slew rate 1.0 V/ ns.
8) Input slew rate 0.5V/ns and < 1.0V/ns.
9) Maximum burst refresh cycle : 8

9.0 AC OPERATING TEST CONDITIONS (VDD = 1.7V to 1.95V, TC = -40°C to 85°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	0.8 x VDDQ / 0.2 x VDDQ	V
Input timing measurement reference level	0.5 x VDDQ	V
Input signal minimum slew rate	1.0	V/ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	See Figure 6	

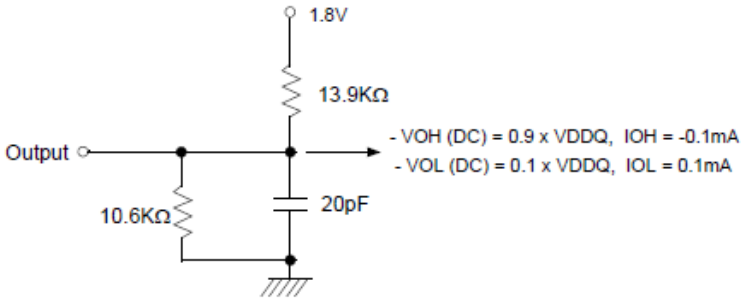


Figure 5. DC Output Load Circuit

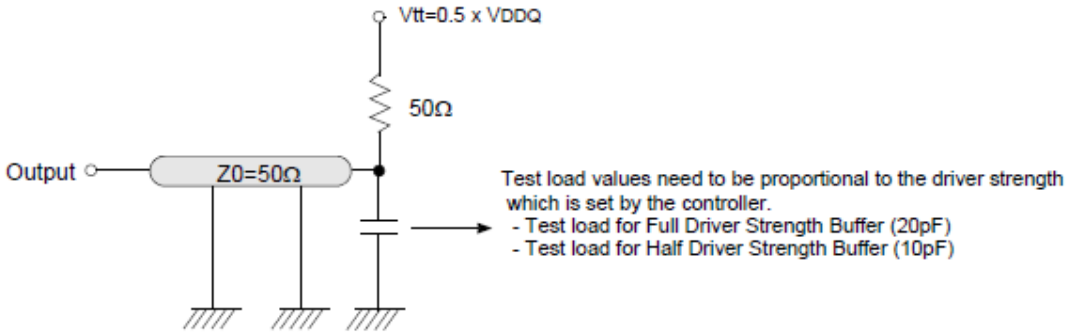


Figure 6. AC Output Load Circuit [1), 2)]

NOTE :

1) The circuit shown above represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half driver strength with a nominal 10pF load parameters t_{AC} and t_{QH} are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.

2) Based on nominal impedance at 0.5 x VDDQ.
The impedance for Half(1/2) Driver Strength is designed 55ohm. And for other Driver Strength, it is designed proportionally.

10.0 INPUT/OUTPUT CAPACITANCE(VDD=1.8, VDDQ=1.8V, TC = 25°C, f=100MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A13, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	CIN1	1.5	3.0	pF
Input capacitance (CK, $\overline{CK}$)	CIN2	1.5	3.5	pF
Data & DQS input / output capacitance	COUT	2.0	4.5	pF
Input capacitance (DM)	CIN3	2.0	4.5	pF

11.0 AC OVERSHOOT/UNDERSHOOT SPECIFICATION FOR ADDRESS & CONTROL PINS

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.9V
Maximum peak Amplitude allowed for undershoot area	0.9V
Maximum overshoot area above VDD	3V-ns
Maximum undershoot area below VSS	3V-ns

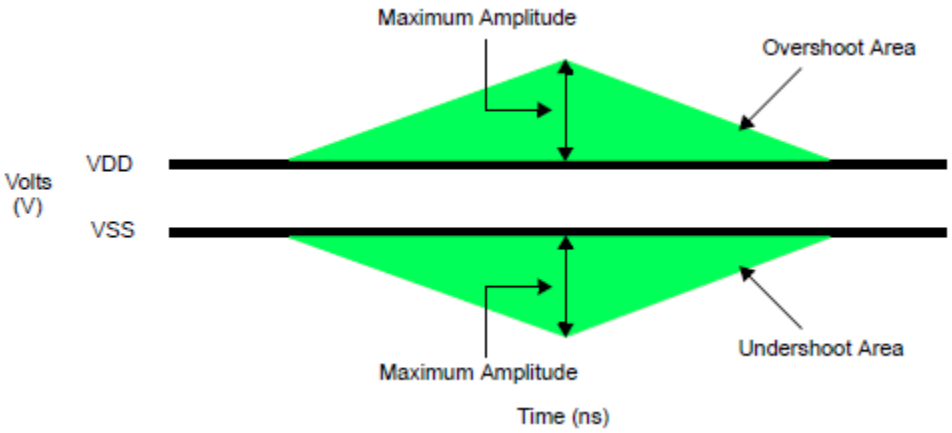


Figure 7. AC Overshoot and Undershoot Definition for Address and Control Pins

12.0 AC OVERSHOOT/UNDERSHOOT SPECIFICATION FOR CK, DQ, DQS AND DM PINS

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.9V
Maximum peak Amplitude allowed for undershoot area	0.9V
Maximum overshoot area above VDDQ	3V-ns
Maximum undershoot area below VSSQ	3V-ns

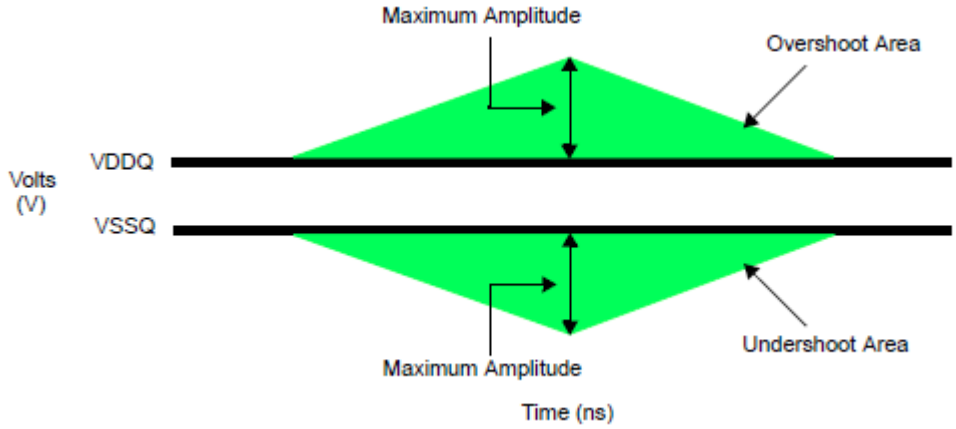


Figure 8. AC Overshoot and Undershoot Definition for CK, DQ, DQS and DM Pins

13.0 COMMAND TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A13~11, A9~A0	Note
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4, 6
Deep Power Down		Entry	H	L	L	H	H	L	X			
		Exit	L	H	H	X	X	X				
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	X	X	X	X				
Precharge Power Down		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	H	H	H				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

NOTE :

1) OP Code : Operand Code. A0 ~ A13 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2) EMRS / MRS can be issued only at all banks precharge state. A new command can be issued 2 clock cycles after EMRS or MRS.
3) Auto refresh functions are same as the CBR refresh of DRAM. The automatical precharge without row precharge command is meant by "Auto". Auto/self refresh can be issued only at all banks precharge state.
4) BA0 ~ BA1 : Bank select addresses.
5) If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6) During burst write with auto precharge, new read/write command can not be issued. Another bank read/write command can be issued after the end of burst. New row active of the associated bank can be issued at tRP after the end of burst.
7) Burst stop command is valid at every burst length.
8) DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9) This combination is not defined for any function, which means "No Operation(NOP)" in Mobile DDR SDRAM

14.0 FUNCTIONAL TRUTH TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRECHARGE STANDBY	L	H	H	L	X	Burst Stop	ILLEGAL [2]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL [2]
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL [4]
	L	L	L	H	X	Refresh	AUTO-Refresh [5]
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set [5]
ACTIVE STANDBY	L	H	H	L	X	Burst Stop	NOP
	L	H	L	H	BA, CA, A10	READ/READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	L	H	H	L	X	Burst Stop	Terminate Burst
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge [3]
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst, Precharge [10]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge [3]
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge [3]
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst With DM=High, Precharge [10]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE[6] (READA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	NOTE6
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	NOTE6
	L	L	H	L	BA, A10	PRE/PREA	NOTE6
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE with AUTO RECHARGE[7] (WRITEA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	NOTE7
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	NOTE7
	L	L	H	H	BA, RA	Active	NOTE7
	L	L	H	L	BA, A10	PRE/PREA	NOTE7
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
PRECHARGING (DURING t_{RP})	L	H	H	L	X	Burst Stop	ILLEGAL [2]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL [2]
	L	L	H	H	BA, RA	Active	ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	NOP [4] (Idle after t_{RP})
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING (FROM ROW ACTIVE TO t_{RCD})	L	H	H	L	X	Burst Stop	ILLEGAL [2]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL [2]
	L	L	H	H	BA, RA	Active	ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL [2]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING (DURING t_{WR} OR t_{CDLR})	L	H	H	L	X	Burst Stop	ILLEGAL [2]
	L	H	L	H	BA, CA, A10	READ	ILLEGAL [2]
	L	H	L	L	BA, CA, A10	WRITE	WRITE
	L	L	H	H	BA, RA	Active	ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL [2]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
RE-FRESHING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESHING [8]	L	H	H	X	X	X	X	Exit Self-Refresh
	L	H	L	H	H	H	X	Exit Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	L	H	X	X	X	X	X	Exit Power Down (Idle after t_{PDEX})
	L	L	X	X	X	X	X	NOP (Maintain Power Down)
ALL BANKS IDLE [9]	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	Enter Deep Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State = Power Down

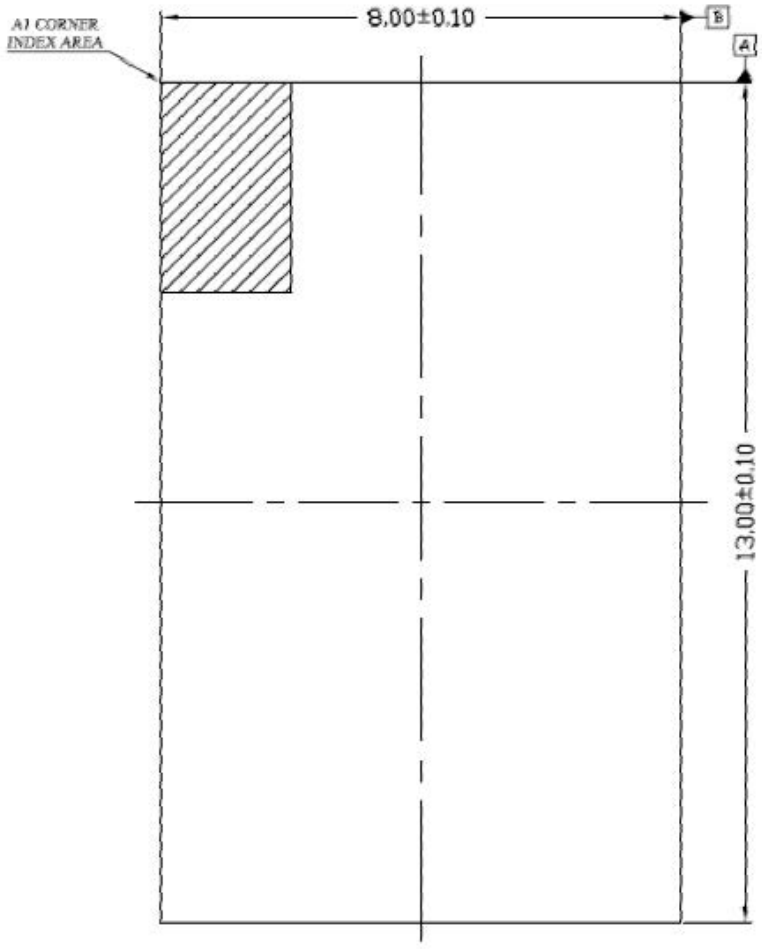
(H=High Level, L=Low level, X=Don't Care)

NOTE :

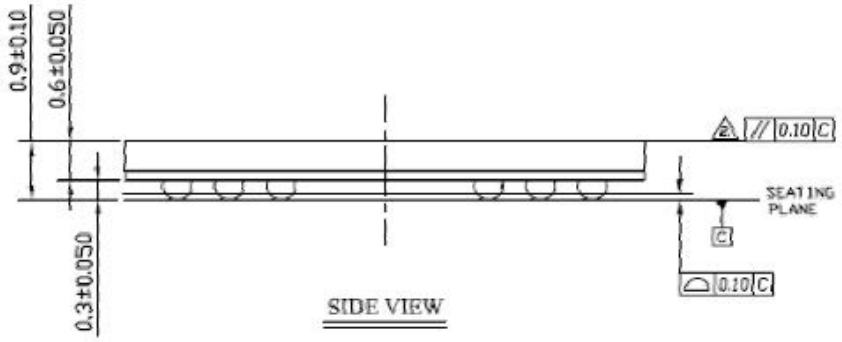
1) All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2) ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank. (ILLEGAL = Device operation and/or data integrity are not guaranteed.)
3) Must satisfy bus contention, bus turn around and write recovery requirements.
4) NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
5) ILLEGAL if any bank is not idle.
6) Refer to "Read with Auto Precharge Timing Diagram" for detailed information.
7) Refer to "Write with Auto Precharge Timing Diagram" for detailed information.
8) CKE Low to High transition will re-enable CK, CK and other inputs asynchronously. A minimum setup time must be satisfied before issuing any command other than EXIT.
9) Power-Down, Self-Refresh Mode can be entered only from All Bank Idle state.

15. PACKAGE DIMENSION

90Ball Fine Pitch BGA (1) (8.0x13.0mm)



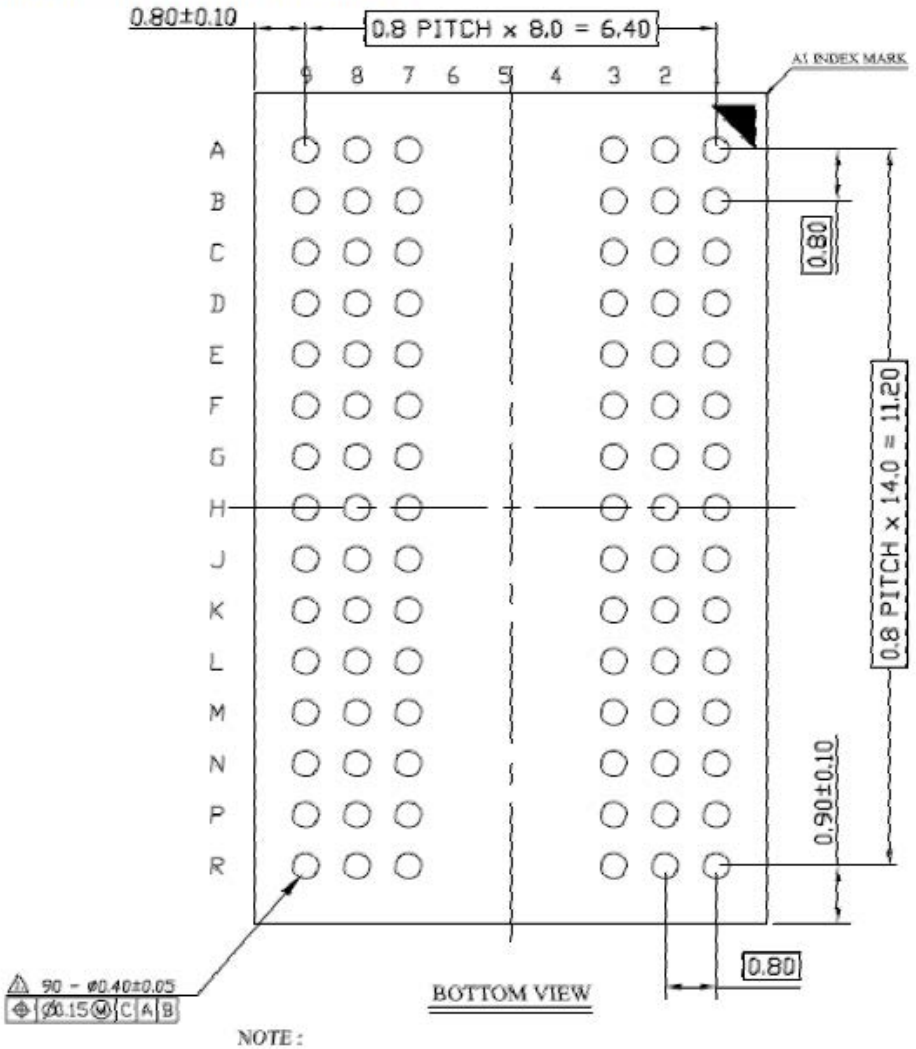
TOP VIEW



SIDE VIEW

15. PACKAGE DIMENSION

90Ball Fine Pitch BGA (2) (8.0x13.0mm)



NOTE :

1. ALL DIMENSION ARE IN MILLIMETERS.
2. ⚠ POST REFLOW SOLDER BALL DIAMETER.
   (Pre Reflow Diameter : 0.35±0.02)
3. ⚠ TOLERANCE INCLUDES WARPAGE.

Mobile DDR SDRAM Device Operation & Timing Diagram

Device Operations

1. PRECHARGE

The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses(BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, tWR(min.) must be satisfied until the precharge command can be issued. After tRP from the precharge, an active command to the same bank can be initiated.

[Table 1] Bank selection for precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

2. NO OPERATION(NOP) & DEVICE DESELECT

The device should be deselected by deactivating the /CS signal. In this mode, Mobile DDR SDRAM should ignore all the control inputs. The Mobile DDR SDRAM is put in NOP mode when /CS is activated and /RAS, /CAS and /WE are deactivated. Both Device Deselect and NOP command can not affect operation already in progress. So even if the device is deselected or NOP command is issued under operation, the operation will be completed.

3. ROW ACTIVE

The Bank Activation command is issued by holding /CAS and /WE high with /CS and /RAS low at the rising edge of the clock (/CK). The Mobile DDR SDRAM has four independent banks, so two Bank Select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of /RAS to /CAS delay time, tRCD(min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time, tRRD(min).

Any system or application incorporating random access memory products should be properly designed, tested and qualifided to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

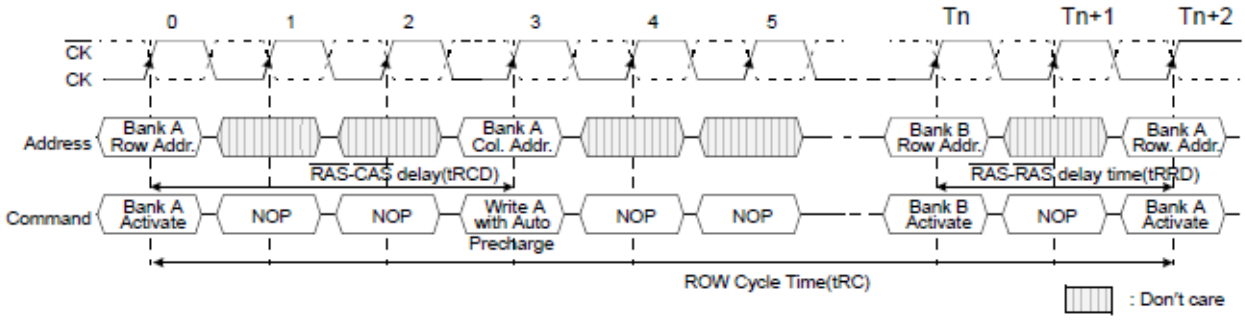


Figure 1. Bank Activation Command Cycle timing <tRCD=3CLK, tRRD=2CLK>

4. READ BANK

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating /RAS, /CS, /CAS, and /WE at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the /CAS latency time will be determined by the values programmed during the MRS cycle.

5. WRITE BANK

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating /RAS,/CS,/CAS, and /WE at the same clock sampling(rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS cycle.

6. BURST READ OPERATION

Burst Read operation in Mobile DDR SDRAM is in the same manner as the Mobile SDR SDRAM such that the Burst read command is issued by asserting /CS and /CAS low while holding /RAS and /WE high at the rising edge of the clock(CK) after tRCD from the bank activation. The address inputs determine the starting address for the Burst. The Mode Register sets type of burst (Sequential or interleave) and burst length(2, 4, 8, 16). The first output data is available with a CAS Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe (DQS) adopted by Mobile DDR SDRAM until the burst length is completed.

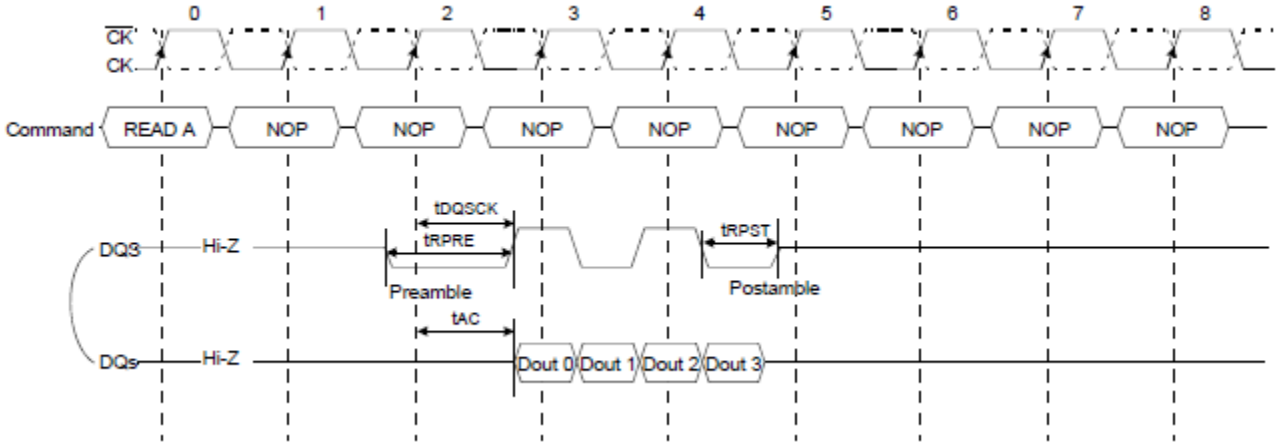


Figure 2. Burst read operation timing

NOTE :
1) Burst Length=4, /CAS Latency= 3.

7. BURST WRITE OPERATION

The Burst Write command is issued by having /CS, /CAS, and /WE low while holding /RAS high at the rising edge of the clock (CK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins tDS (Data-in setup time) prior to data strobe edge enabled after tDQSS from the rising edge of the clock (CK) that the write com-mand is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

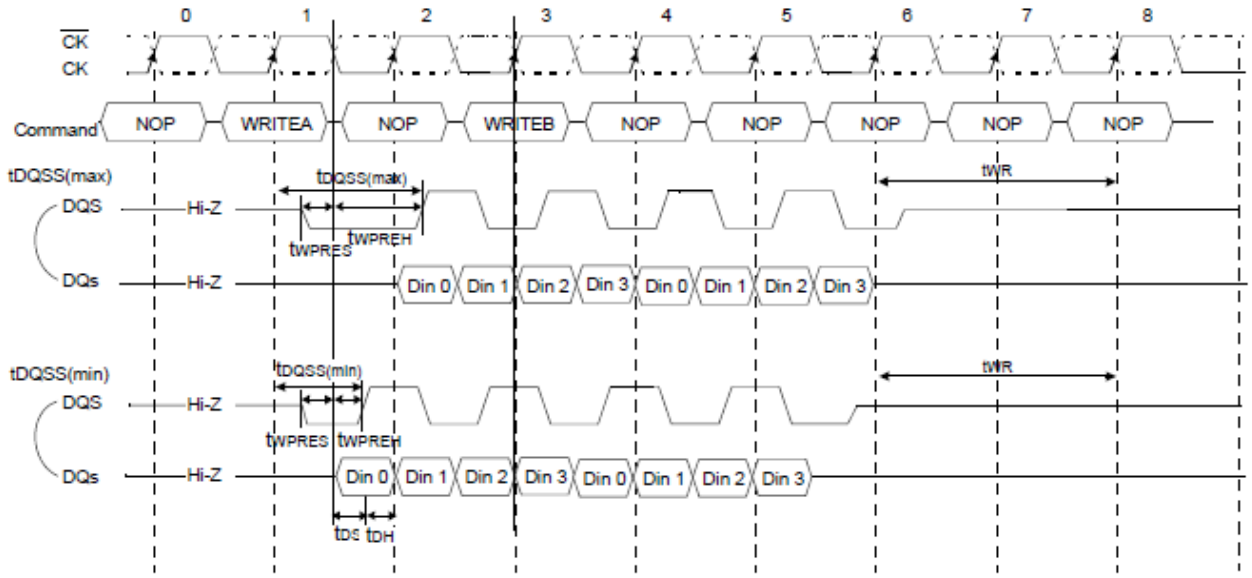


Figure 3. Burst write operation timing

NOTE :

1) Burst Length=4.

2) The specific requirement is that DQS be valid (High or Low) on or before this CK edge.
The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus.

8. READ INTERRUPTED BY A READ

A Burst Read can be interrupted by new Read command of any bank before completion of the burst. When the previous burst is interrupted, the new address with the full burst length override the remaining address. The data from the first Read command continues to appear on the outputs until the /CAS latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears. Read to Read interval is minimum 1 Clock.

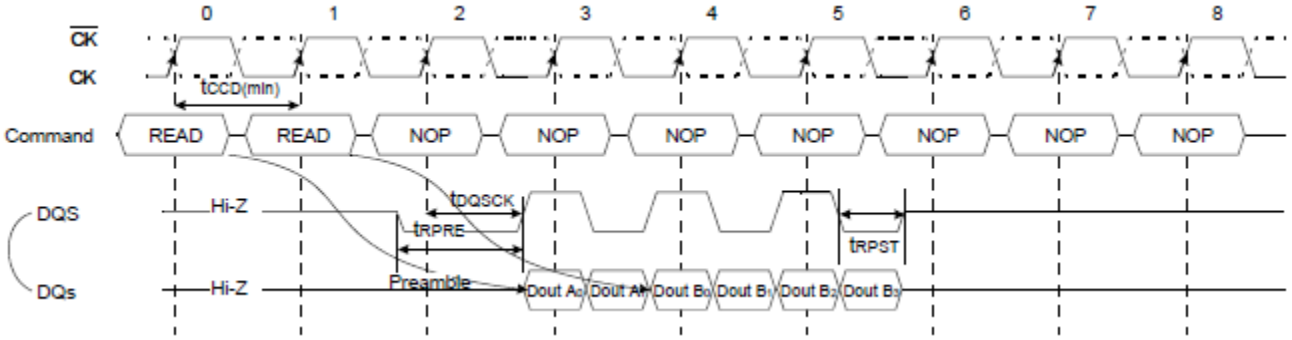


Figure 4. Read interrupted by a read timing

NOTE :
1) Burst Length=4, /CAS Latency=3

9. READ INTERRUPTED BY A WRITE & BURST STOP

To interrupt a burst read with a write command, Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQs (Output drivers) in a high impedance state.

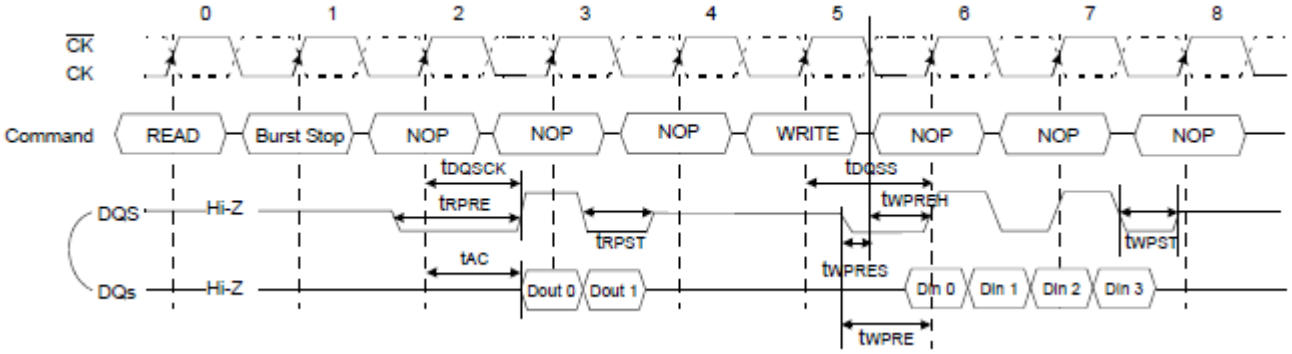


Figure 5. Read interrupted by a write and burst stop timing

NOTE :
1) Burst Length=4, /CAS Latency=3.

The following functionality establishes how a Write command may interrupt a burst Read.

1. For Write commands interrupting a burst Read, a Burst Terminate command is required to stop the burst read and tri-state the DQ bus prior to valid input write data. Burst stop command must be applied at least 2 clock cycles for CL=2 and at least 3 clock cycles for CL=3 before the Write command.

2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

10. READ INTERRUPTED BY A PRECHARGE

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. The latency from a precharge command to invalid output is equivalent to the CAS latency.

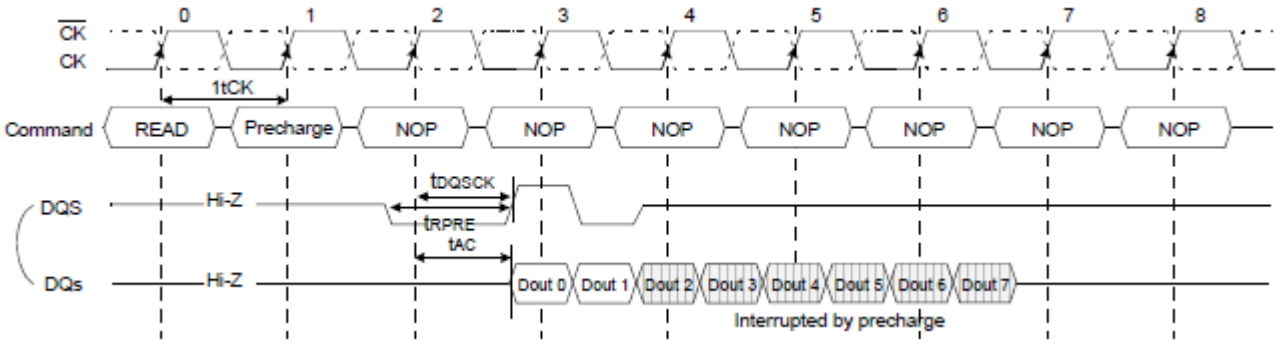


Figure 6. Read interrupted by a precharge timing

NOTE :
1) Burst Length=8, /CAS Latency=3 .

When a burst Read command is issued to a Mobile DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is completed. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a burst Read, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP (Row Precharge time).

2. When a Precharge command interrupts a burst Read operation, the Precharge command given on a rising clock edge terminates the burst with the last valid data word presented on DQ pins at CL-1(CL=CAS Latency) clock cycles after the command has been issued. Once the last data word has been output, the output buffers are tri-stated. A new Bank Activate command may be issued to the same bank after tRP.

3. For a Read with Autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP from rising clock that comes CL(CL=CAS Latency) clock cycles before the end of the Read burst. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.

4. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a rising clock edge).In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

11. WRITE INTERRUPTED BY A WRITE

A Burst Write can be interrupted by a new Write command before completion of the burst, where the interval between the successive Write commands must be at least one clock cycle(tCCD(min)). When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

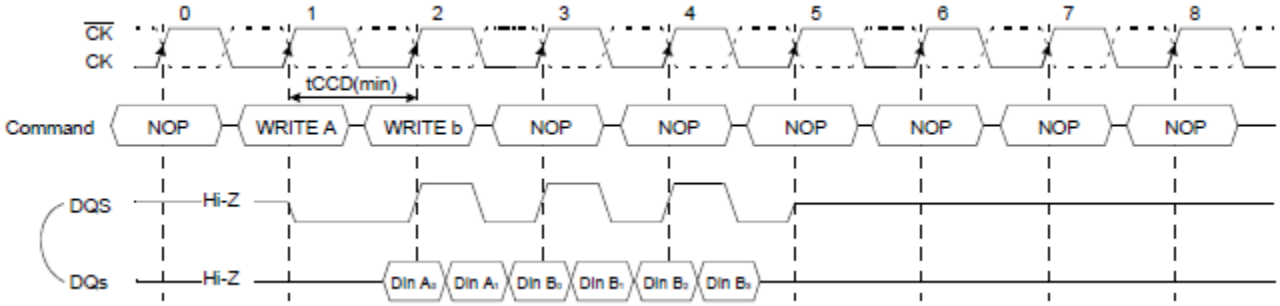


Figure 7. Write interrupted by a write timing

NOTE :
1) Burst Length=4.

12. WRITE INTERRUPTED BY A PRECHARGE & DM

A burst write operation can be interrupted by a precharge of the same bank before completion of the burst. Random column access is allowed. A write recovery time(tWR) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.

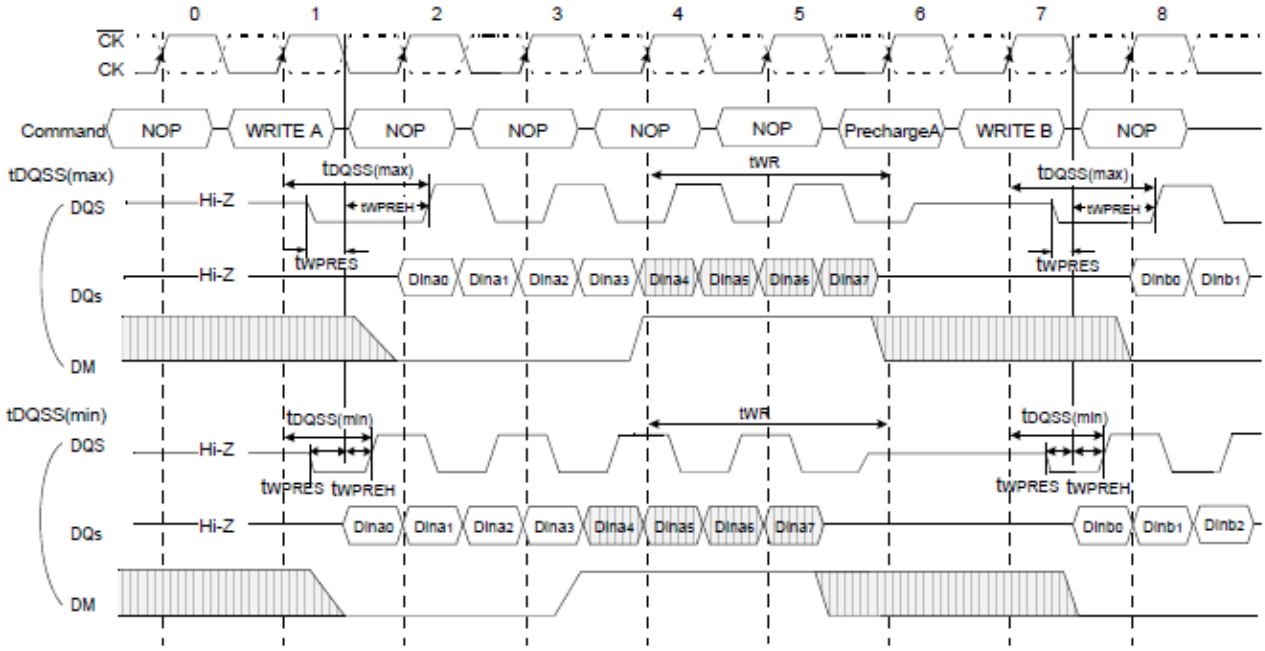


Figure 8. Write interrupted by a precharge and DM timing

NOTE :

1) Burst Length=8.

Precharge timing for Write operations in Mobile DDR SDRAM requires enough time to allow 'write recovery' which is the time required by a Mobile DDR SDRAM core to properly store a full '0' or '1' level before a Precharge operation. For Mobile DDR SDRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the Mobile DDR SDRAM, the data path is eventually synchronized with the address path by switching clock domains from the data strobe clock domain to the input clock domain. This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must make reference to only the clock domain that affects internal write operation, i.e., the input clock domain.

tWR starts on the rising clock edge after the last possible DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a burst Write without interrupting the burst, the minimum time for write recovery is defined by tWR.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge on which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by tWR.
3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after tWR+tRP where tWR+tRP starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate command. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where tRAS(min) must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.

13. WRITE INTERRUPTED BY A READ & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (tCDLR) is required to avoid the data contention Mobile DDR SDRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

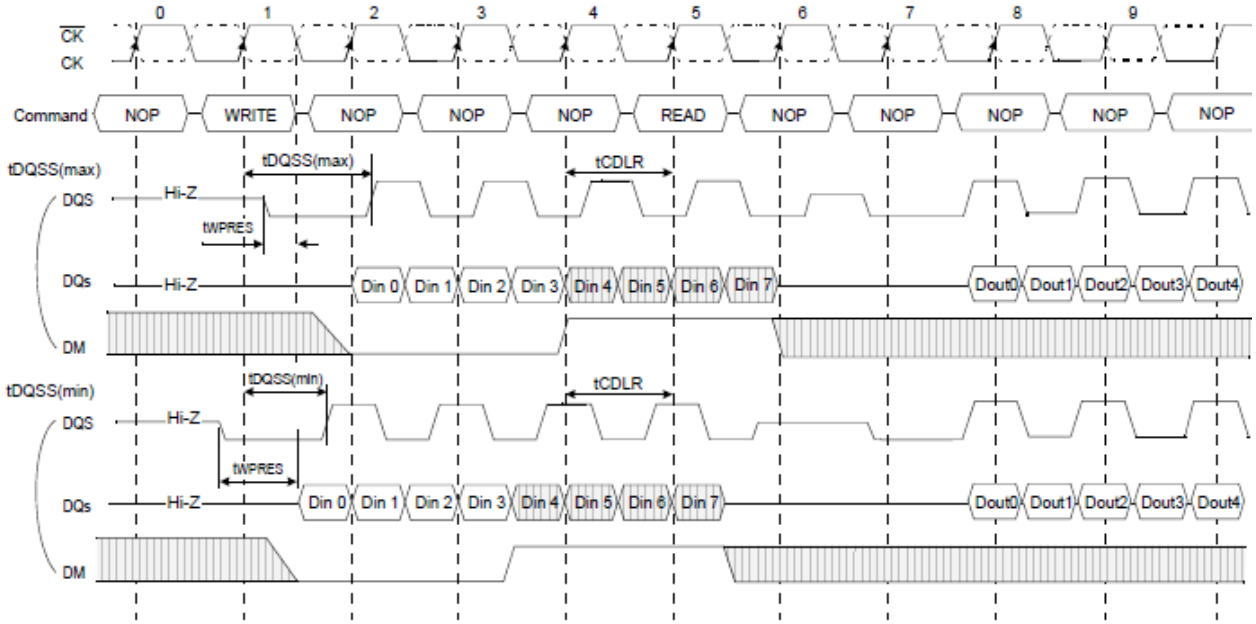


Figure 9. Write interrupted by a Read and DM timing

NOTE :
1) Burst Length=8, /CAS Latency=3.

The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a burst Write, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For Read commands interrupting a burst Write, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the Mobile DDR SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the Mobile DDR SDRAM.
5. Refer to Burst write operation.

14. BURST STOP

The burst stop command is initiated by having /RAS and /CAS high with /CS and /WE low at the rising edge of the clock(CK). The burst stop command has the fewest restrictions making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst stop command is issued during a burst read cycle, the pair of data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the CAS latency set in the mode register. However, the burst stop command is not supported during a burst write operation.

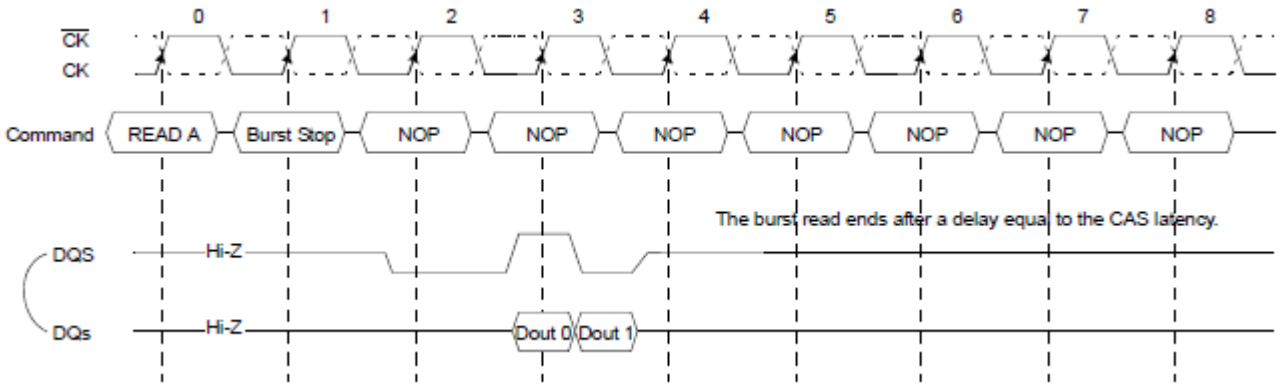


Figure 10. Burst stop timing

NOTE :
1) Burst Length=4, /CAS Latency= 3.

The Burst Stop command is a mandatory feature for Mobile DDR SDRAM. The following functionality is required:
1. The Burst Stop command may only be issued on the rising edge of the input clock, CK.
2. Burst Stop is only a valid command during Read bursts.
3. Burst Stop during a Write burst is undefined and shall not be used.
4. Burst Stop applies to all burst lengths.
5. Burst Stop is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued LBST ("BST Latency") clock cycles before the clock edge at which the output buffers are tristated, where LBST equals the CAS latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The Burst Stop command is not byte controllable and applies to all bits in the DQ data word and the(all) DQS pin(s).

15. DM MASKING

The Mobile DDR SDRAM has a data mask function that can be used in conjunction with data write cycle, not read cycle. When the data mask is activated(DM high) during write operation, Mobile DDR SDRAM does not accept the corresponding data.(DM to data-mask latency is zero). DM must be issued at the rising or falling edge of data strobe.

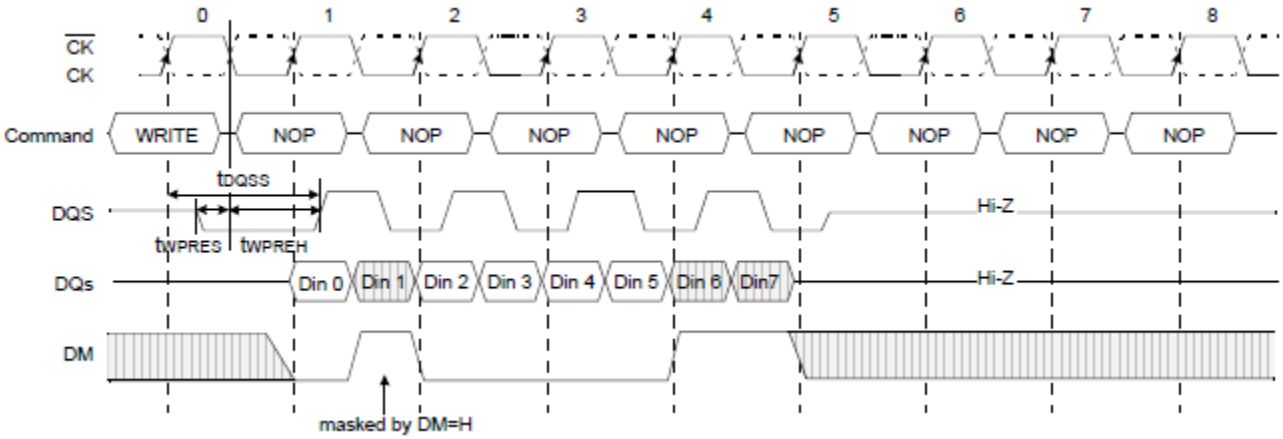


Figure 11. DM masking timing

NOTE :
1) Burst Length=8.

16. READ WITH AUTO PRECHARGE

If A10/AP is high when read command is issued, the read with auto-precharge function is performed. If a read with auto-precharge command is issued, the Mobile DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto-precharge command when tRAS(min) is satisfied. If not, the start point of precharge operation will be delayed until tRAS(min) is satisfied. Once the precharge operation has started, the bank cannot be reactivated and the new command can not be asserted until the precharge time(tRP) has been satisfied.

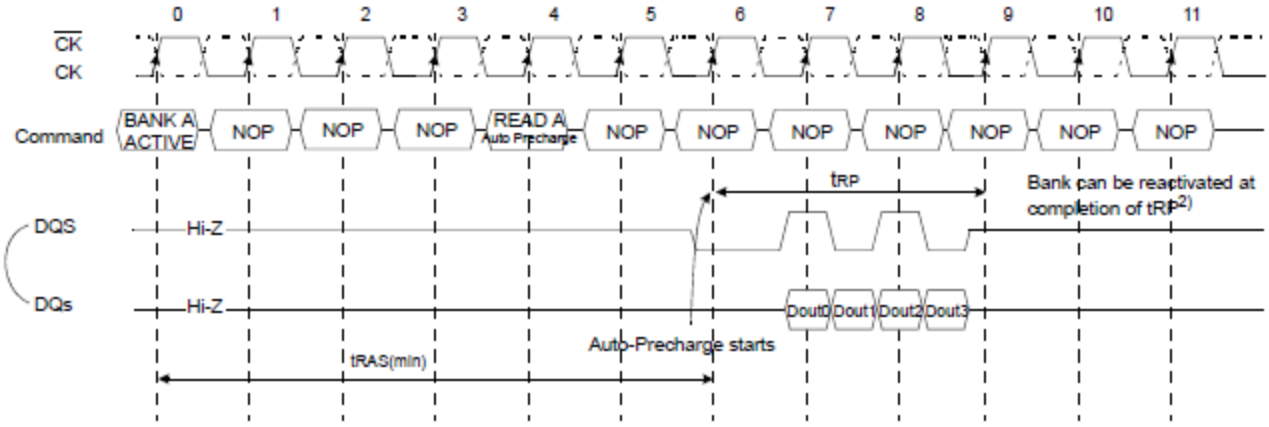


Figure 12. Read with auto precharge timing

NOTE :
1) Burst Length=4, /CAS Latency= 3.
2) The row active command of the precharge bank can be issued after tRP from this point.

Asserted command	For same Bank			For Different Bank		
	5	6	7	5	6	7
READ	READ +No AP1)	READ+No AP	Illegal	Legal	Legal	Legal
READ+AP	READ + AP	READ + AP	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

NOTE :
1) AP = Auto Precharge.

17. WRITE WITH AUTO PRECHARGE

If A10/AP is high when write command is issued, the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping tWR(min).

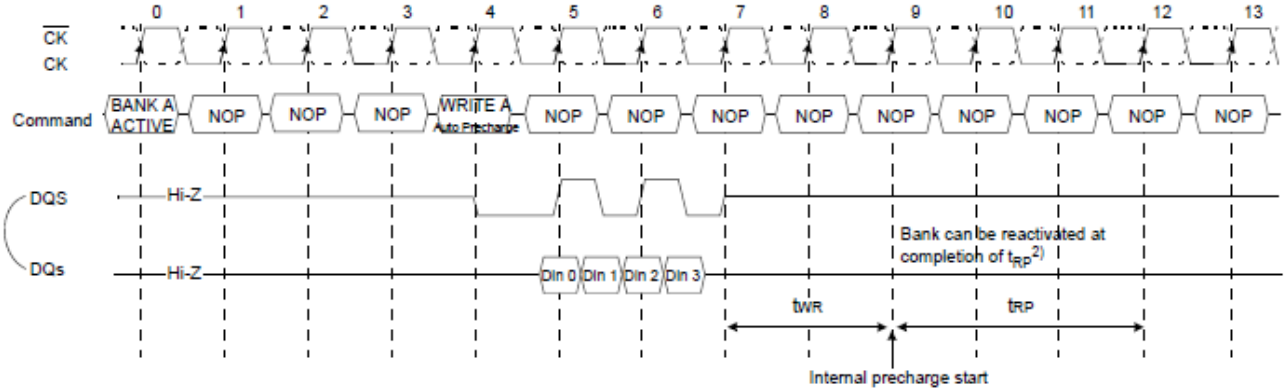


Figure 13. Write with auto precharge timing

NOTE :

1) Burst Length=4.
2) The row active command of the precharge bank can be issued after tRP from this point.

Asserted command	For same Bank						For Different Bank				
	5	6	7	8	9	10	5	6	7	8	9
WRITE	WRITE+ No AP1)	WRITE+ No AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE+ AP	WRITE+ AP	WRITE+ AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ+ NO AP+DM2)	READ+ NO AP+DM	READ+ NO AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ+AP	Illegal	READ + AP+DM	READ + AP+DM	READ + AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

NOTE :

1) AP = Auto Precharge.
2) DM : Refer to "27. *Write Interrupted by Precharge & DM* ".

18. AUTO REFRESH & SELF REFRESH

18.1. Auto Refresh

An auto refresh command is issued by having /CS, /RAS and /CAS held low with CKE and /WE high at the rising edge of the clock(CK). All banks must be precharged and idle for tRP(min) before the auto refresh command is applied. Once this cycle has been started, no control of the external address pins are required because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the tRFC(min).

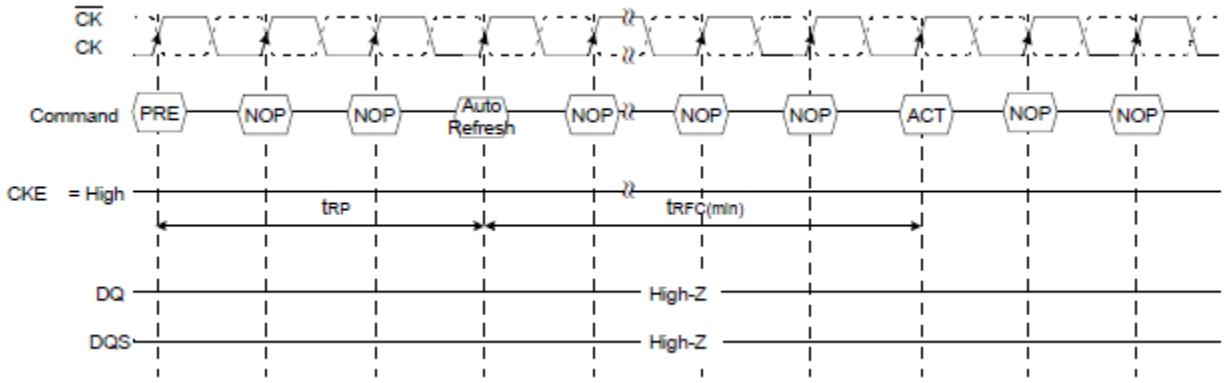


Figure 14. Auto refresh timing

NOTE :
1) tRP=3CLK
2) Device must be in the all banks idle state prior to entering Auto refresh mode.

18.2. Self Refresh

A Self Refresh command is defined by having /CS, /RAS, /CAS and CKE held low with /WE high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 1 clock cycle from the self refresh command, all of the external control signals including system clock(CK,/CK) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. Before returning CKE high to exit the Self Refresh mode, apply stable clock input signal with Deselect or NOP command asserted.

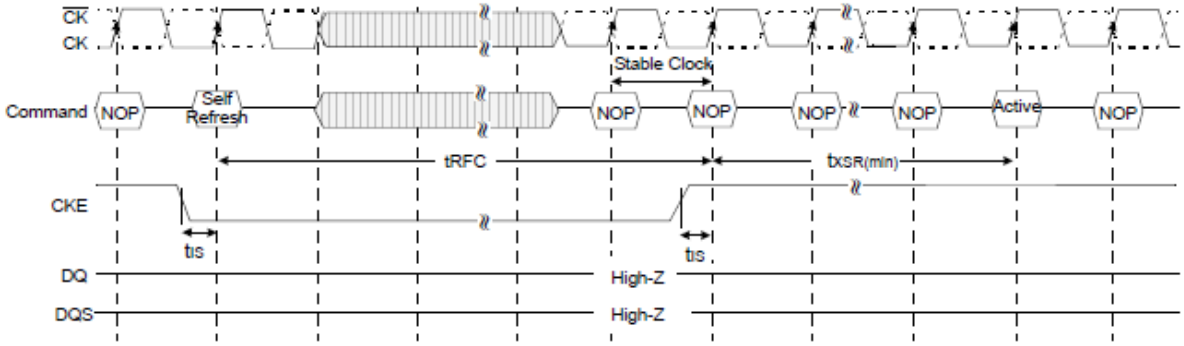


Figure 15. Self refresh timing

NOTE :
1) Device must be in the all banks idle state prior to entering Self Refresh mode.
2) The minimum time that the device must remain in Self Refresh mode is tRFC.

19. POWER DOWN

The device enters power down mode when CKE Low, and it exits when CKE High. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and CKE should be set in high for at least tPDEX prior to Row active command. Refresh operations cannot be performed during power down mode, therefore the device cannot remain in power down mode longer than the refresh period(tREF) of the device.

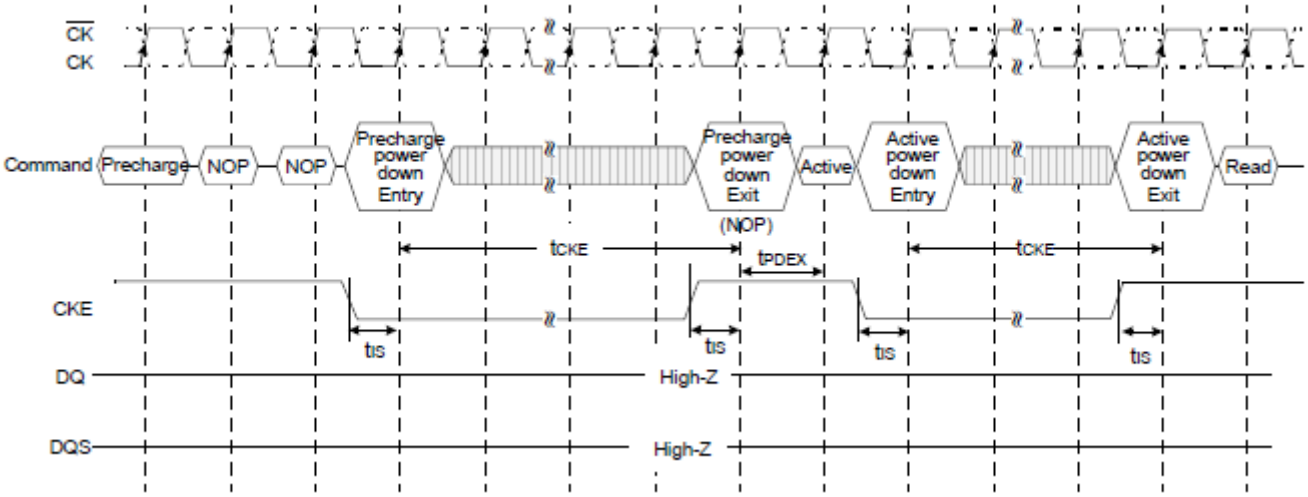


Figure 16. Power down entry and exit timing

NOTE :

1) Device must be in the all banks idle state prior to entering Power Down mode.
2) The minimum power down duration is specified by tCKE.

20. CLOCK STOP

Stopping a clock during idle periods is an effective method of reducing power consumption.

The LPDDR SDRAM supports clock stop under the following conditions :
-the last command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- the related timing conditions (tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held High

When all conditions have been met, the device is either in "idle state"or "row active state" and clock stop mode may be entered with CK held Low and CK held Hight.
Clock stop mode is exited by restarting the clock. At least one NOP command has to be issued before the next access command any be applied. Additional clock pulses might be required depending on the system characteristics.

Figure shows clock stop mode entry and exit.
-Initially the device is in clock stop mode
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs
- With T1 a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command is completed.
- Tn is the last clock pulse required by the access command latched with T1
- The clock can be stopped after Tn.

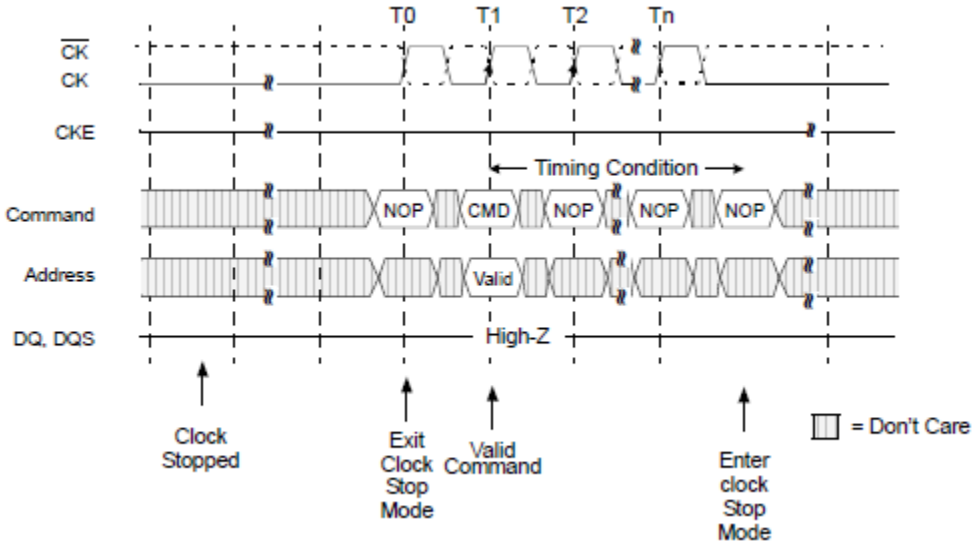


Figure 17. Clock Stop Mode Entry and Exit

Timing Diagram

1. POWER UP SEQUENCE FOR MOBILE DDR SDRAM

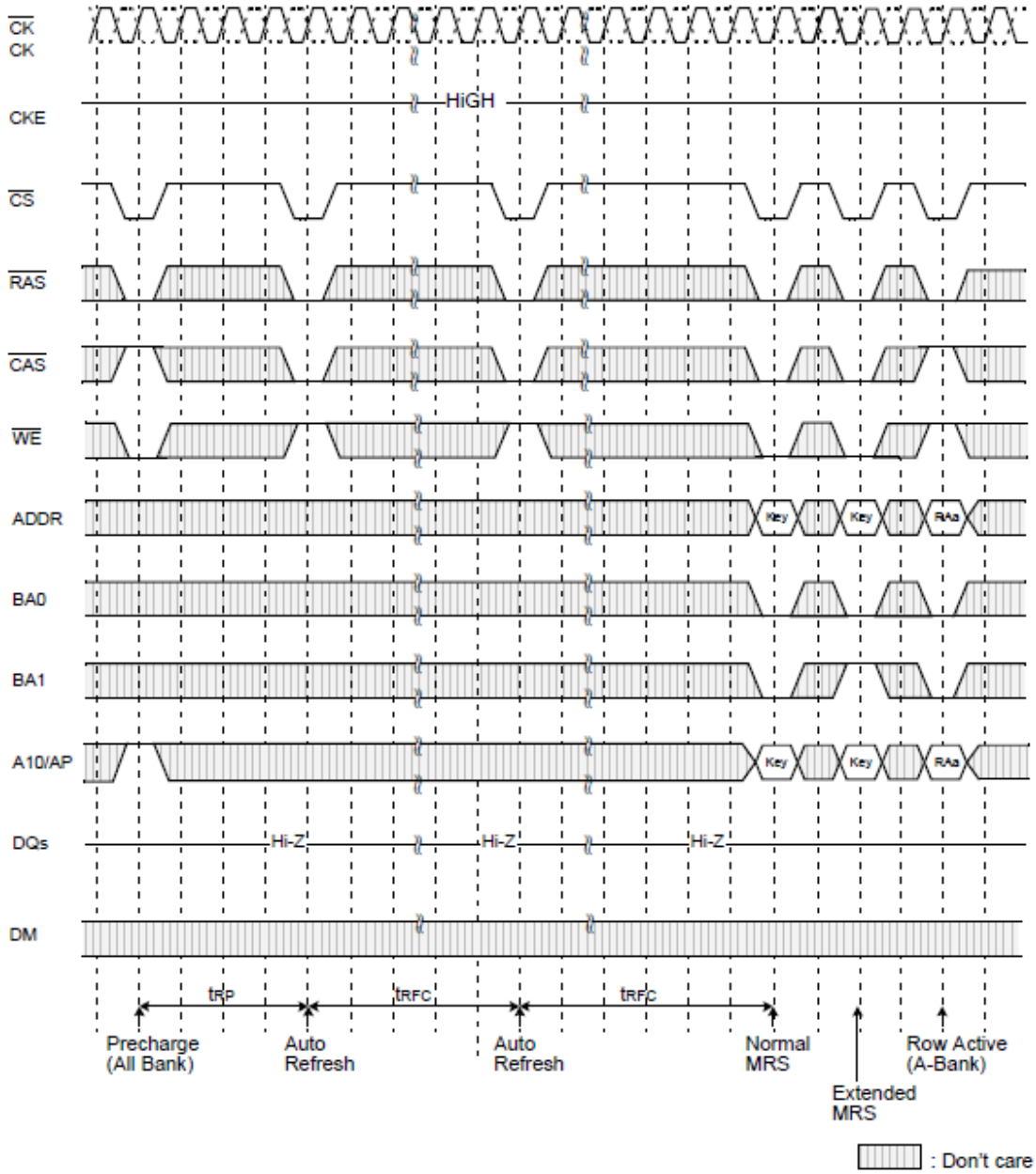


Figure 18. Power Up Sequence for Mobile DDR SDRAM

NOTE :

1) Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
- Apply VDD before or at the same time as VDDQ.

2) Maintain stable power, stable clock and NOP input condition for a minimum of 200us.

3) Issue precharge commands for all banks of the devices.

4) Issue 2 or more auto-refresh commands.

5) Issue a mode register set command to initialize the mode register.

6) Issue a extended mode register set command for the desired operating modes after normal MRS.

The Mode Register and Extended Mode Register do not have default values.
If they are not programmed during the initialization sequence, it may lead to unspecified operation.
All banks have to be in idle state prior to adjusting MRS and EMRS set.

2. BASIC TIMING

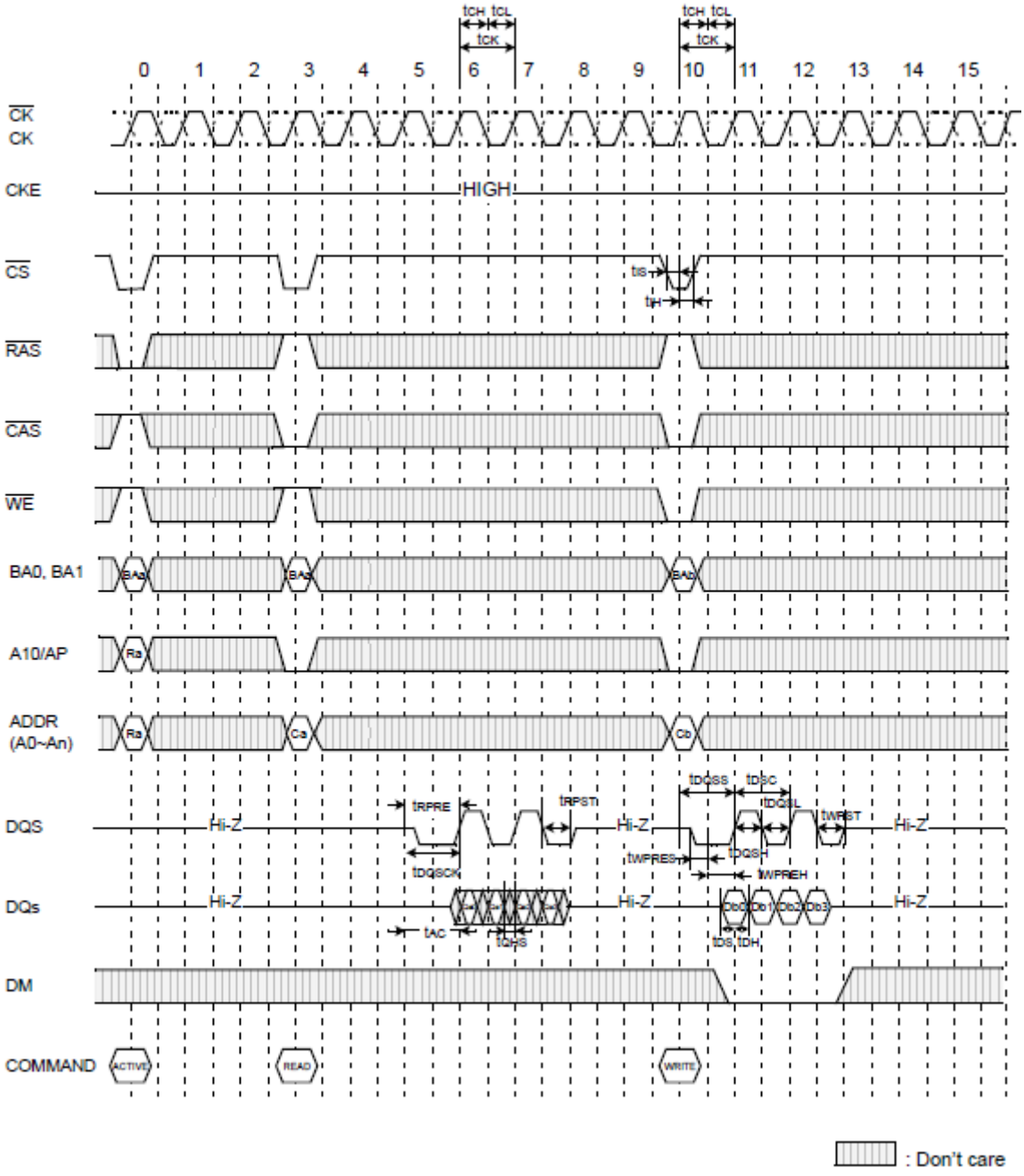


Figure 19. Basic Timing (Setup, Hold and Access Time @BL=4, CL=3)

3. MULTI BANK INTERLEAVING READ

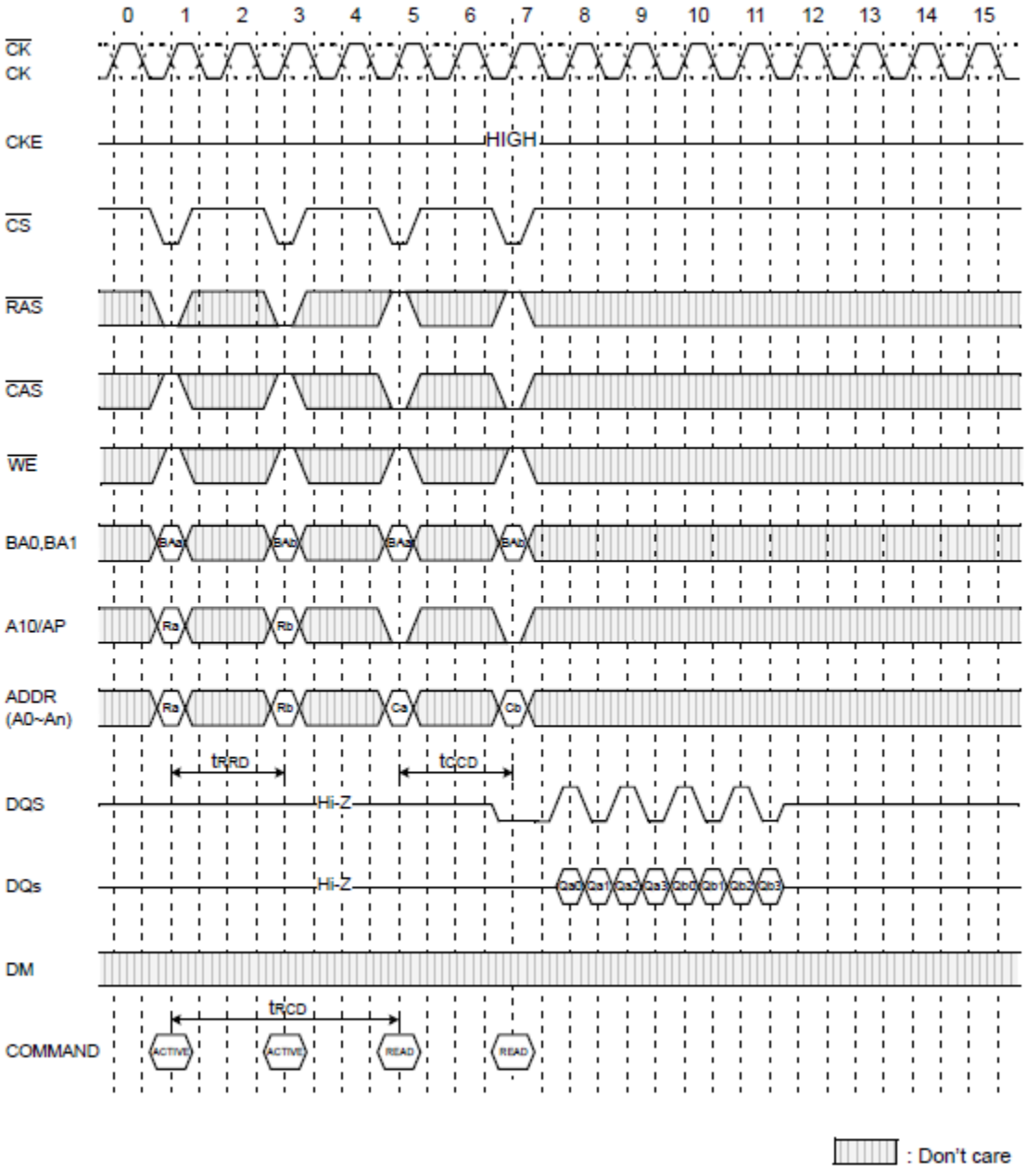


Figure 20. Multi Bank Interleaving READ (@BL=4, CL=3)

4. MULTI BANK INTERLEAVING WRITE

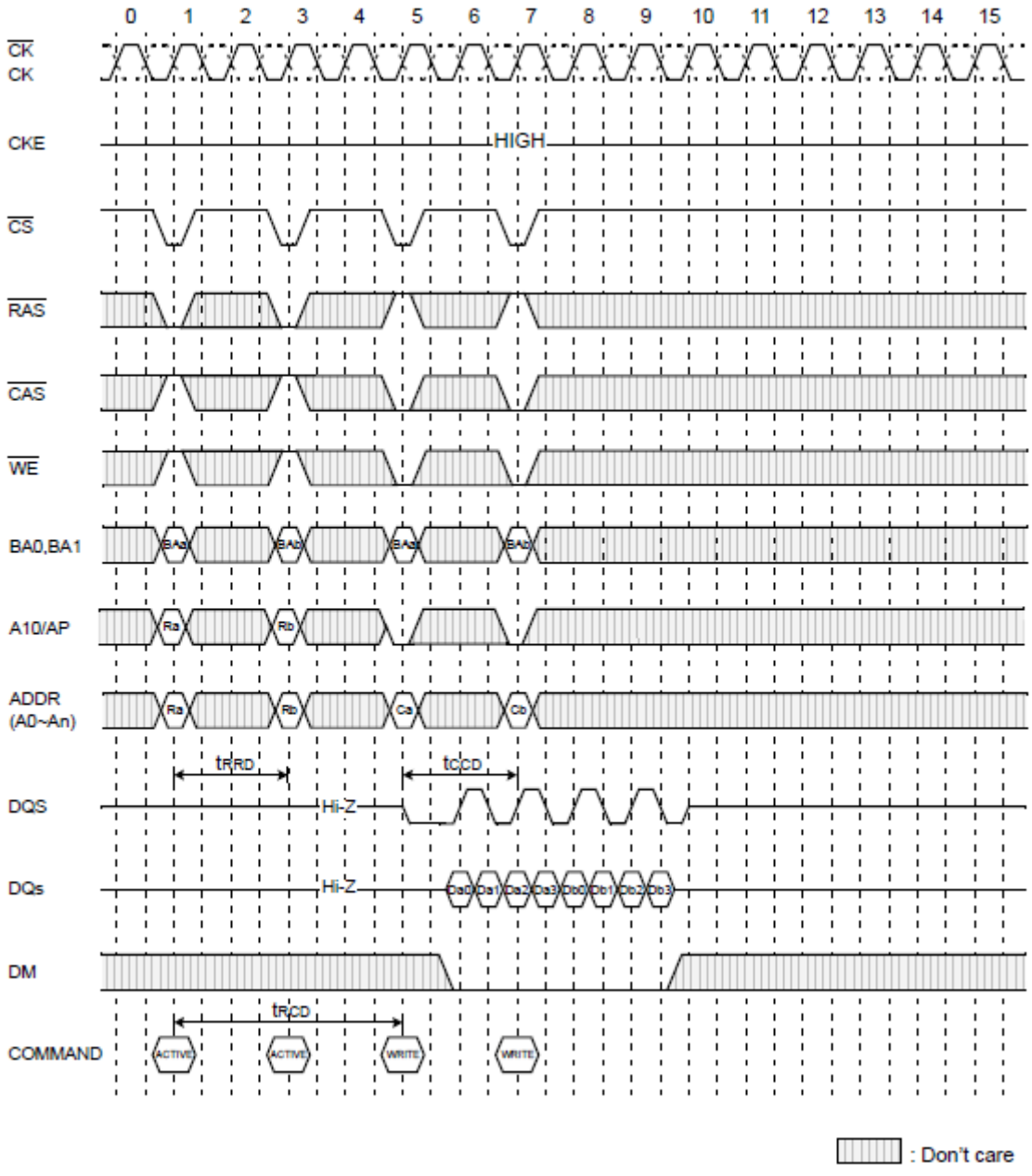


Figure 21. Multi Bank Interleaving WRITE (@BL=4)

5. READ WITH AUTO PRECHARGE

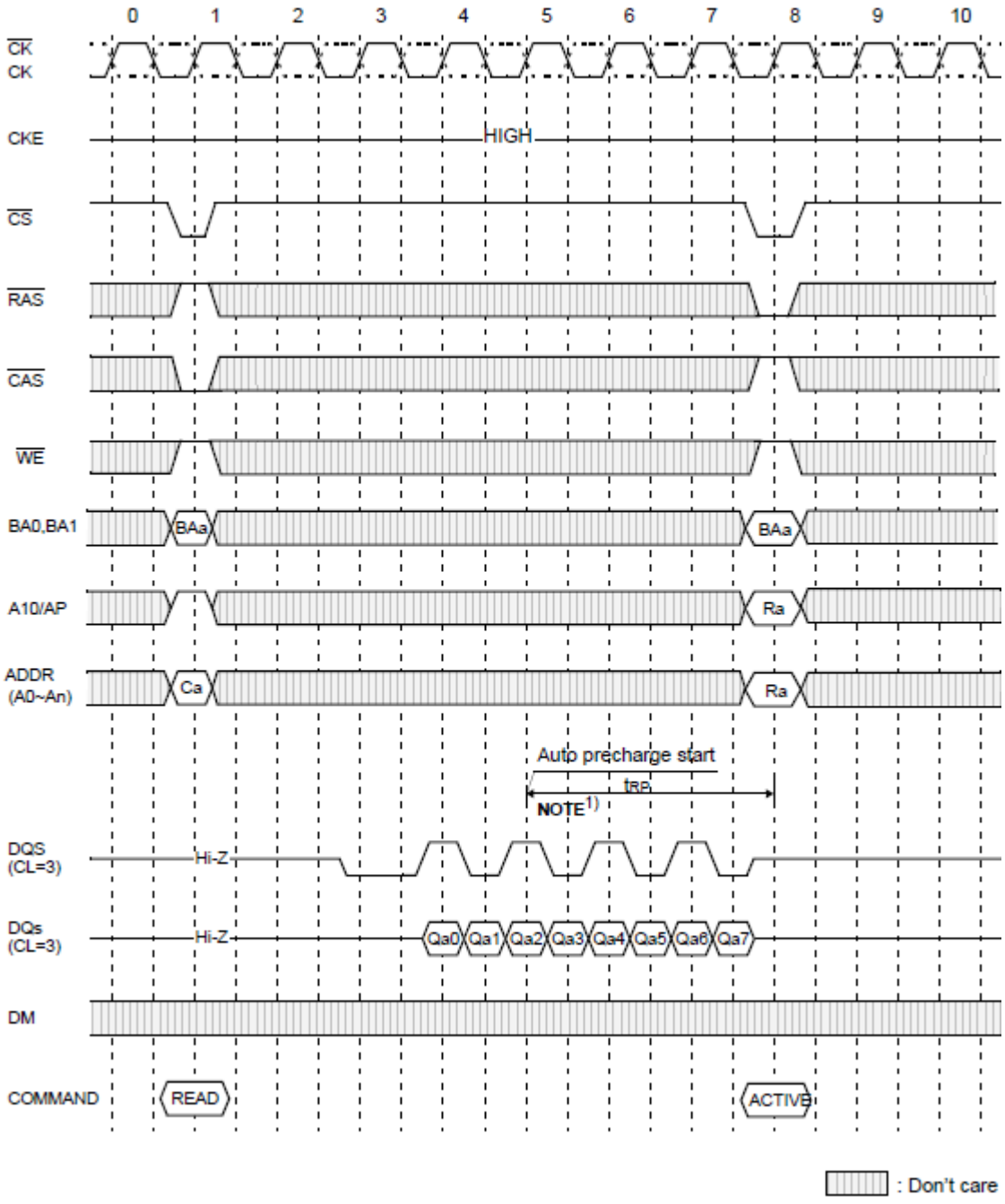


Figure 22. Read with Auto Precharge (@BL=8)

NOTE :

1) The row active command of the precharge bank can be issued after tRP from this point.

6. WRITE WITH AUTO PRECHARGE

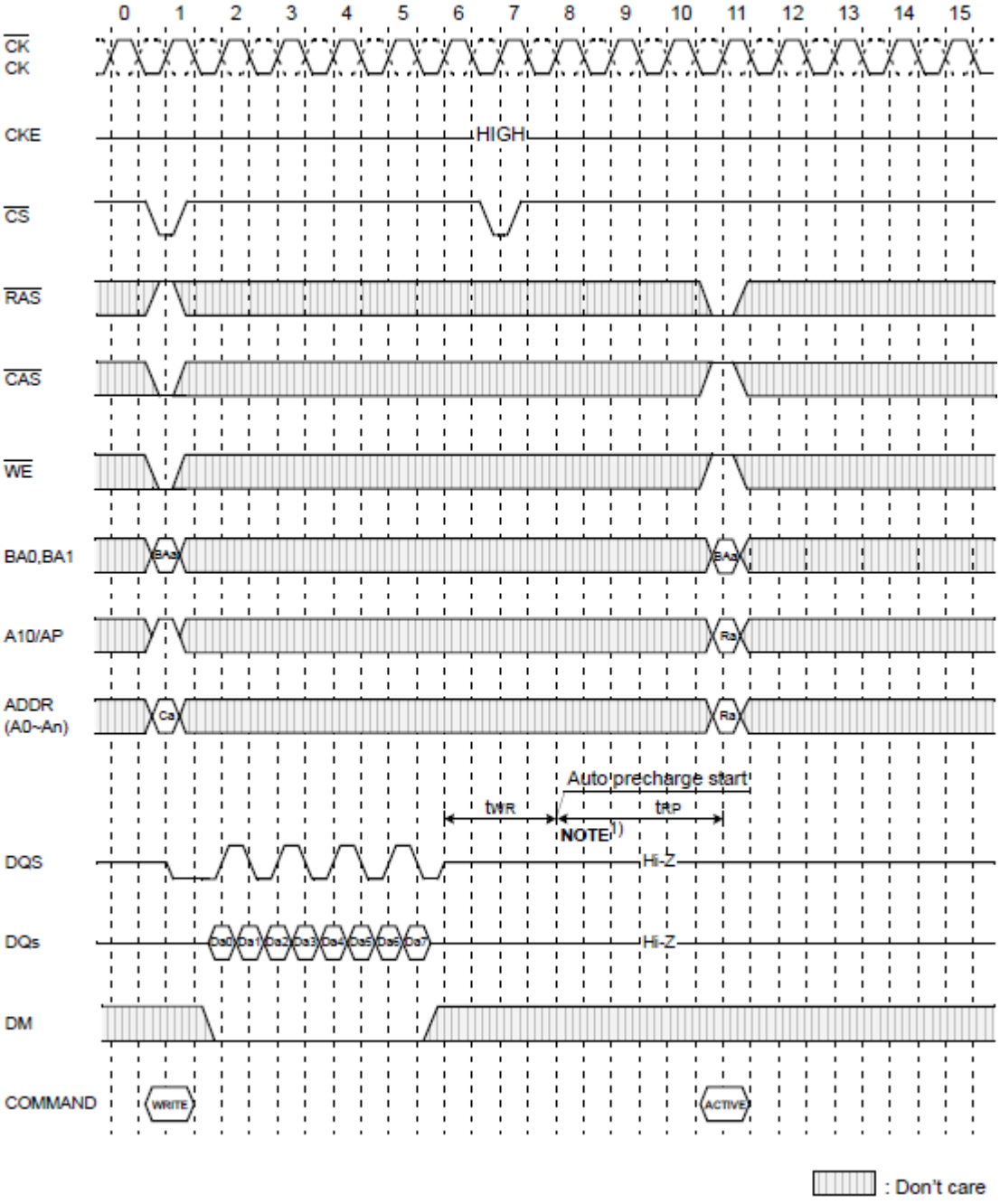


Figure 23. Write with Auto Precharge (@BL=8)

NOTE :
1) The row active command of the precharge bank can be issued after tRP from this point

7. WRITE FOLLOWED BY PRECHARGE

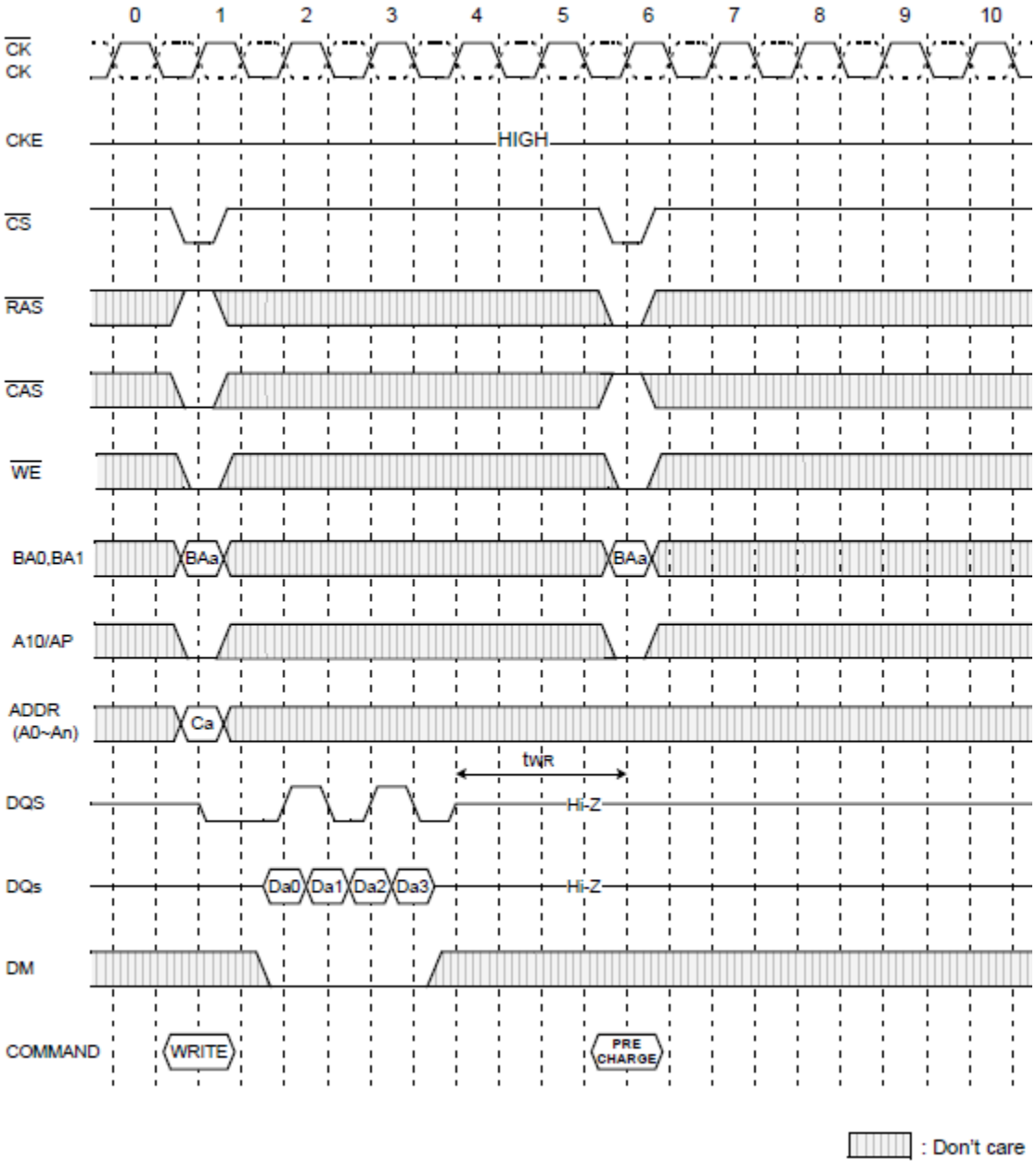


Figure 24. Write followed by Precharge (@BL=4)

8. WRITE INTERRUPTED BY PRECHARGE & DM

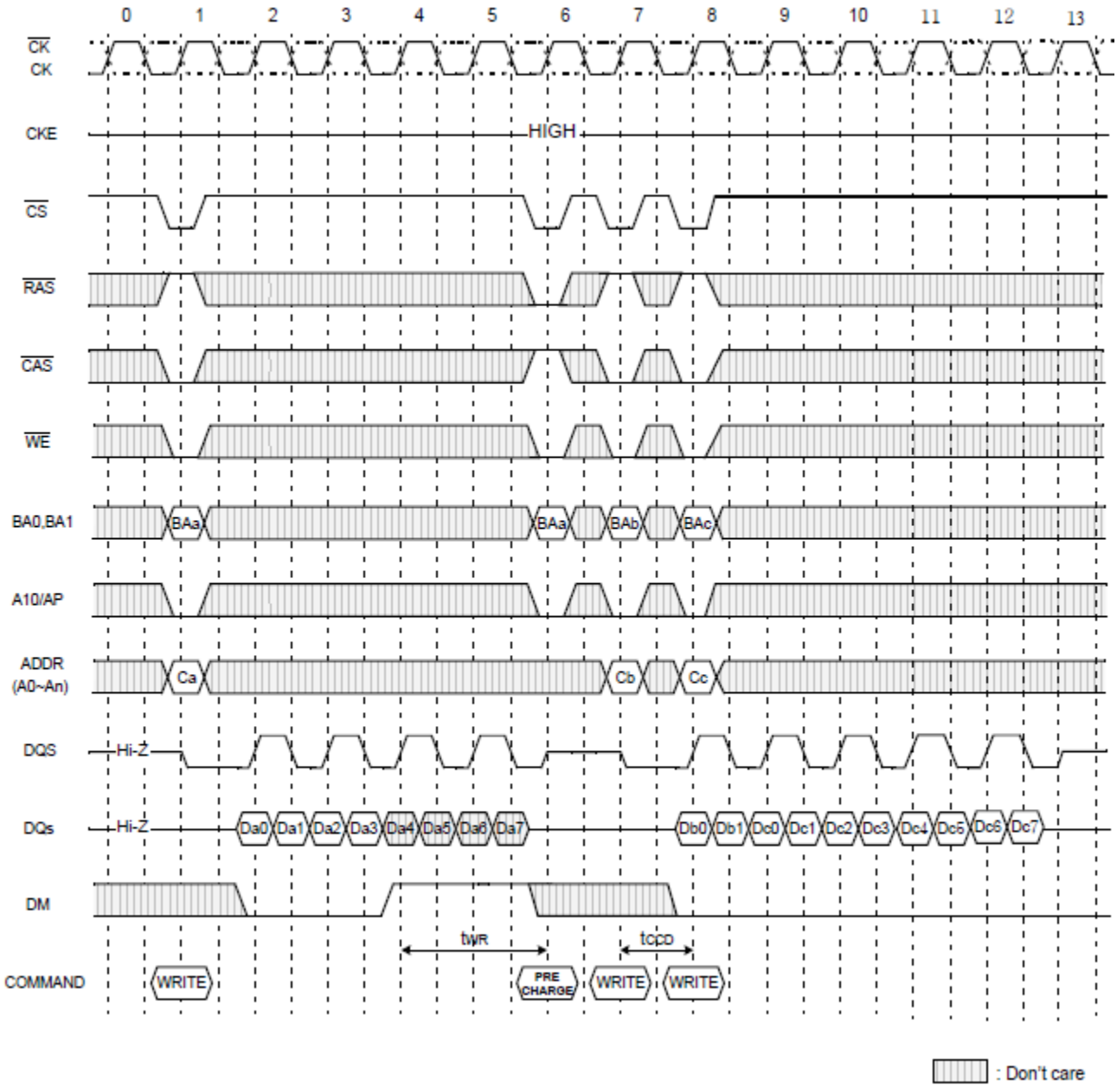


Figure 25. Write Interrupted by Precharge & DM (@BL=8)

9. WRITE INTERRUPTED BY A READ

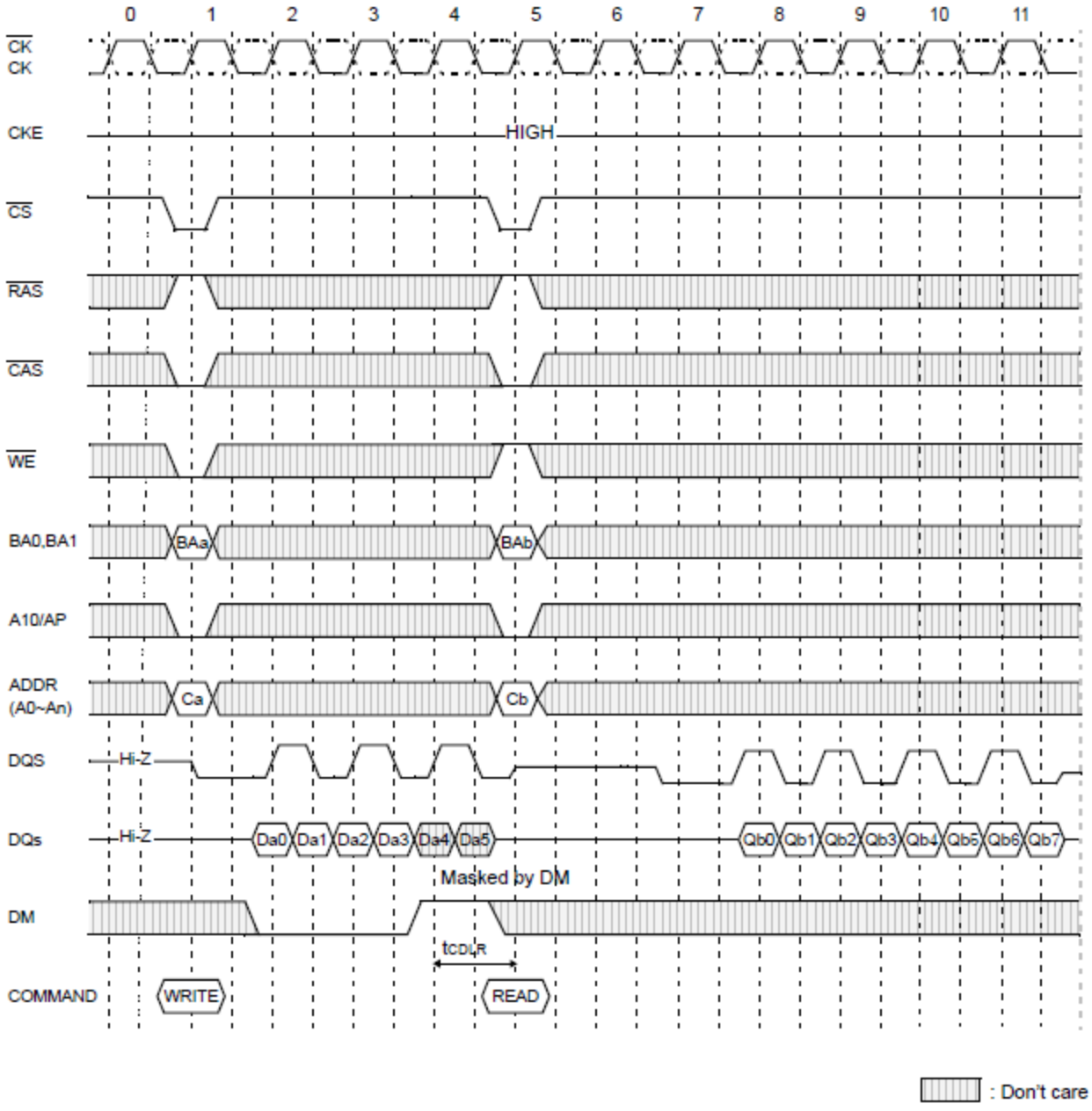


Figure 26. Write Interrupted by a Read (@BL=8, CL=3)

10. READ INTERRUPTED BY PRECHARGE

Figure 27. Read Interrupted by Precharge (@BL=8, CL=3)

11. READ INTERRUPTED BY A WRITE & BURST STOP

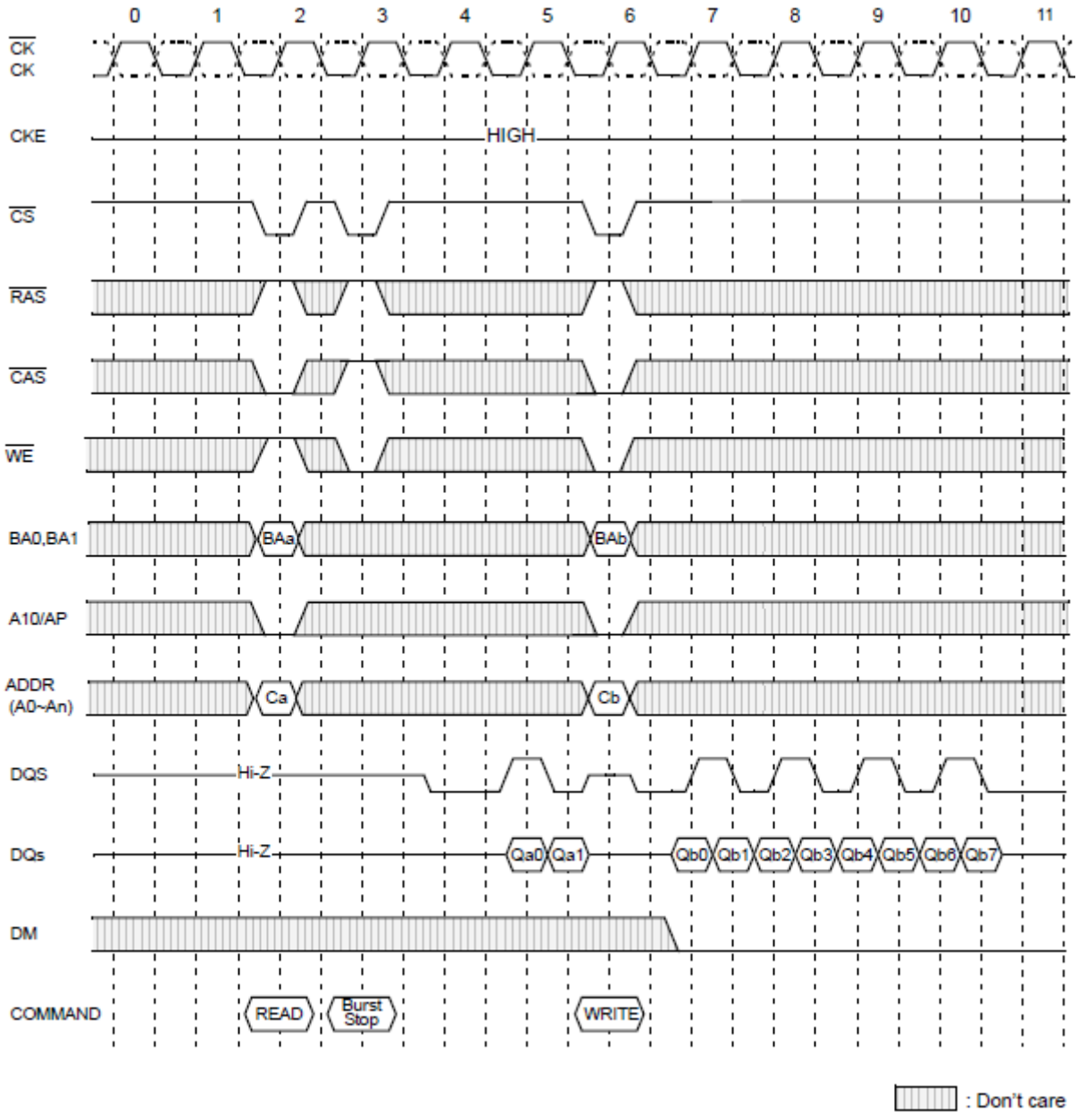


Figure 28. Read Interrupted by a Write & Burst Stop (@BL=8, CL=3)

12. READ INTERRUPTED BY A READ

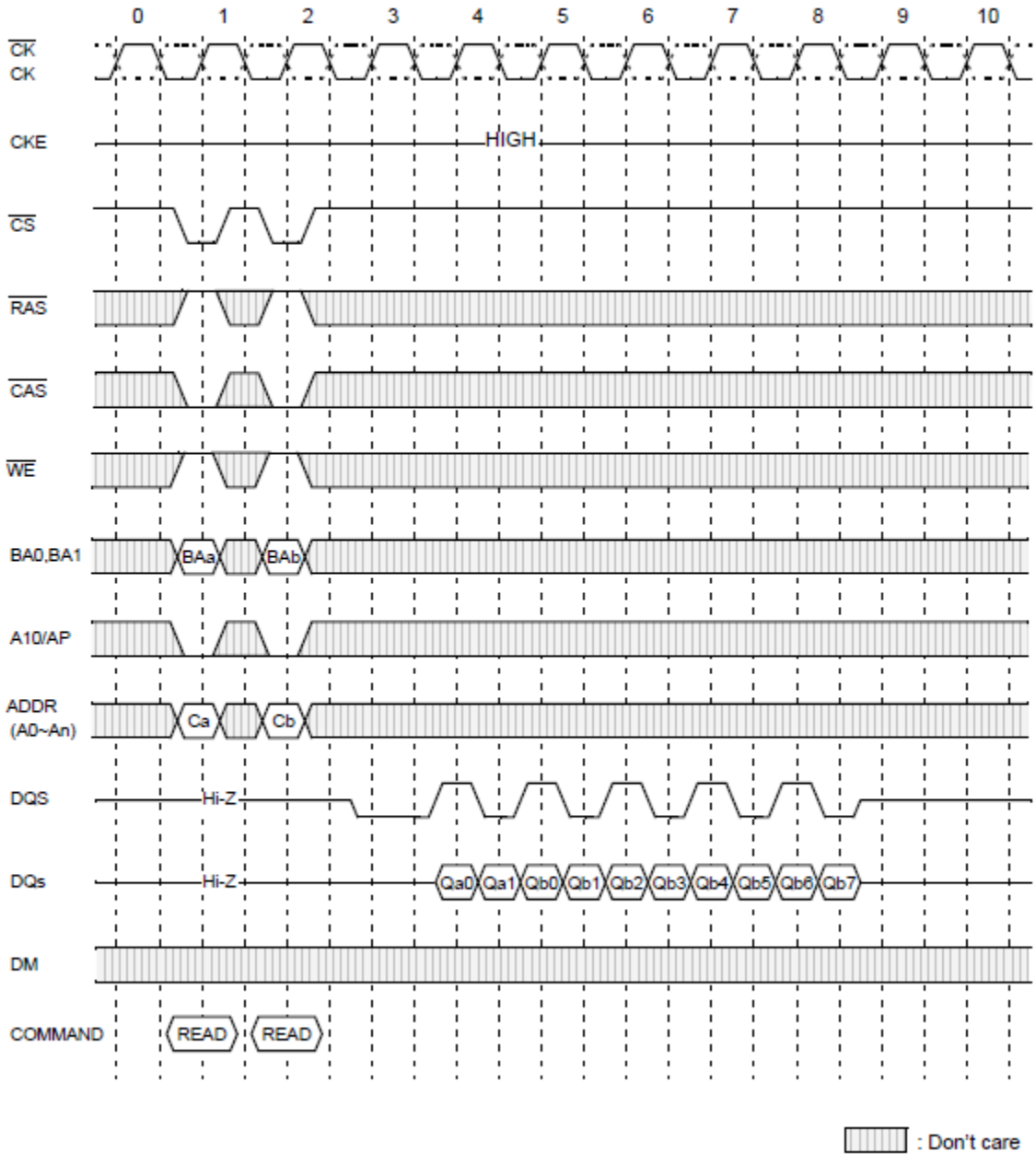


Figure 29. Read Interrupted by a Read (@BL=8, CL=3)

13. DM FUNCTION

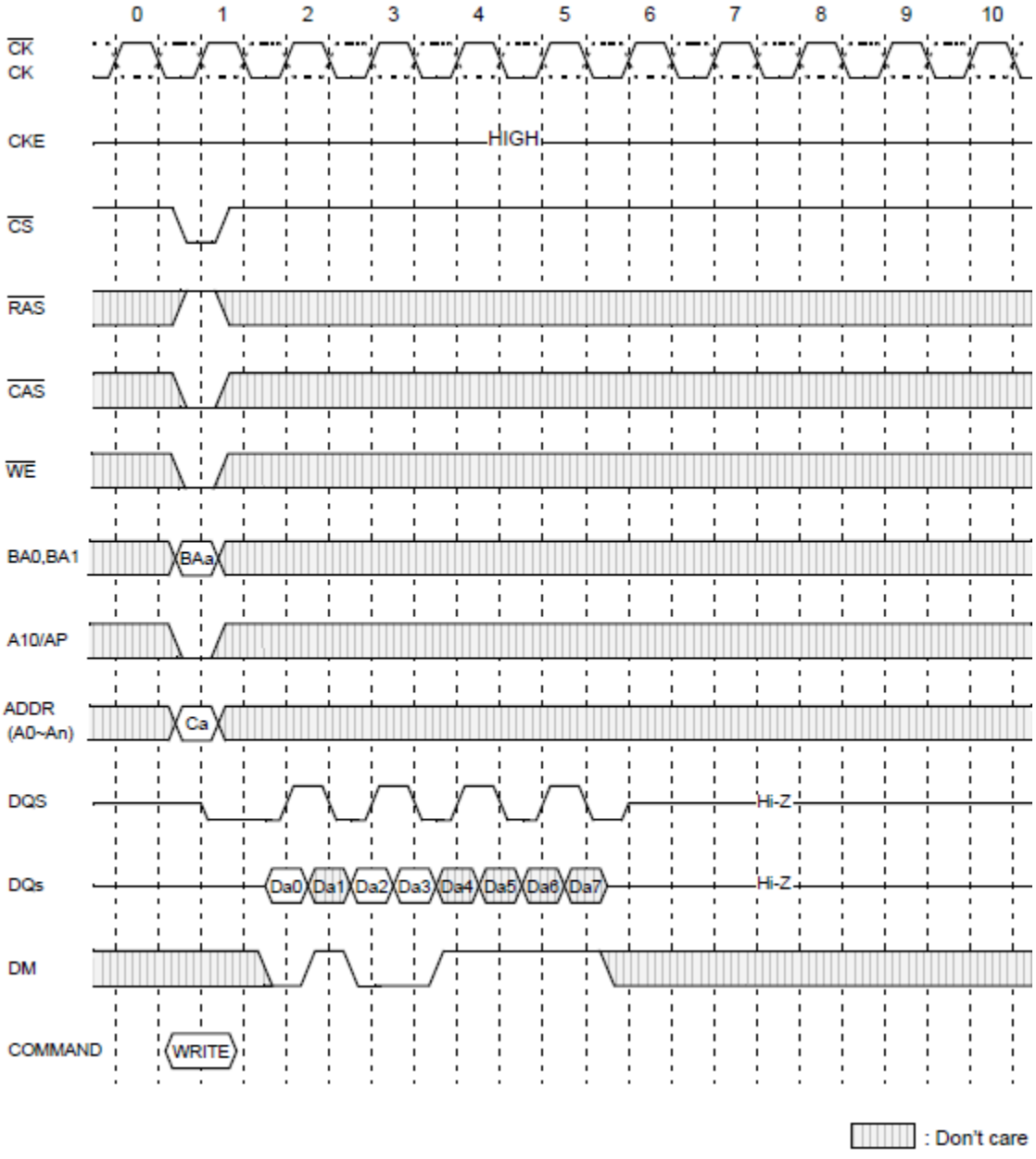


Figure 30. DM Function (@BL=8) only for write