

AS5600L

12-Bit Programmable On-Axis Magnetic Rotary Position Sensor

General Description

The AS5600L is an easy to program magnetic rotary position sensor with a high-resolution 12-bit I²C or PWM output. This contactless system measures the absolute angle of a diametric magnetized on-axis magnet. This AS5600L is designed for contactless potentiometer applications and its robust design eliminates the influence of any homogenous external stray magnetic fields.

The industry-standard I²C interface supports simple user programming of non-volatile parameters without requiring a dedicated programmer.

By default the output represents a range from 0 to 360 degrees. It is also possible to define a smaller range to the output by programming a zero angle (start position) and a maximum angle (stop position).

The AS5600L is also equipped with a smart low power mode feature to automatically reduce the power consumption.

An input pin (DIR) selects the polarity of the output with regard to rotation direction. If DIR is connected to ground, the output value increases with clockwise rotation. If DIR is connected to VDD, the output value increases with counterclockwise rotation.

The AS5600L is available in a standard SOIC-8 package and in a WL-CSP for applications requiring small-sized sensing solutions with a size of 2.07mm x 2.63mm x 0.6mm. Both variants are qualified for a temperature range from -40°C to 125°C.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5600L, 12-bit Programmable Contactless Potentiometer are listed below:

Figure 1:
Added Value of Using AS5600L

| Benefits | Features |
|--|---|
| <ul style="list-style-type: none"> Highest reliability and durability | <ul style="list-style-type: none"> Contactless magnetic angle measurement |
| <ul style="list-style-type: none"> Simple programming | <ul style="list-style-type: none"> Easy programming of start and stop positions in 3-wire mode (no programmer needed) or over the I²C interface |
| <ul style="list-style-type: none"> Multiple sensors on one I²C bus | <ul style="list-style-type: none"> User programmable I²C address |

| Benefits | Features |
|--|---|
| <ul style="list-style-type: none"> • Great flexibility on angular excursion | <ul style="list-style-type: none"> • Maximum angle programmable from 18° up to 360° |
| <ul style="list-style-type: none"> • High-resolution output signal | <ul style="list-style-type: none"> • 12-bit output resolution available on I²C and PWM output |
| <ul style="list-style-type: none"> • Low-power consumption | <ul style="list-style-type: none"> • Automatic entry into low-power mode |
| <ul style="list-style-type: none"> • Easy setup | <ul style="list-style-type: none"> • Automatic magnet detection |
| <ul style="list-style-type: none"> • Very small form factor | <ul style="list-style-type: none"> • WL-CSP (2.07mm x 2.63mm) or SOIC-8 package |
| <ul style="list-style-type: none"> • Robust environmental tolerance | <ul style="list-style-type: none"> • Wide temperature range: -40°C to 125°C |

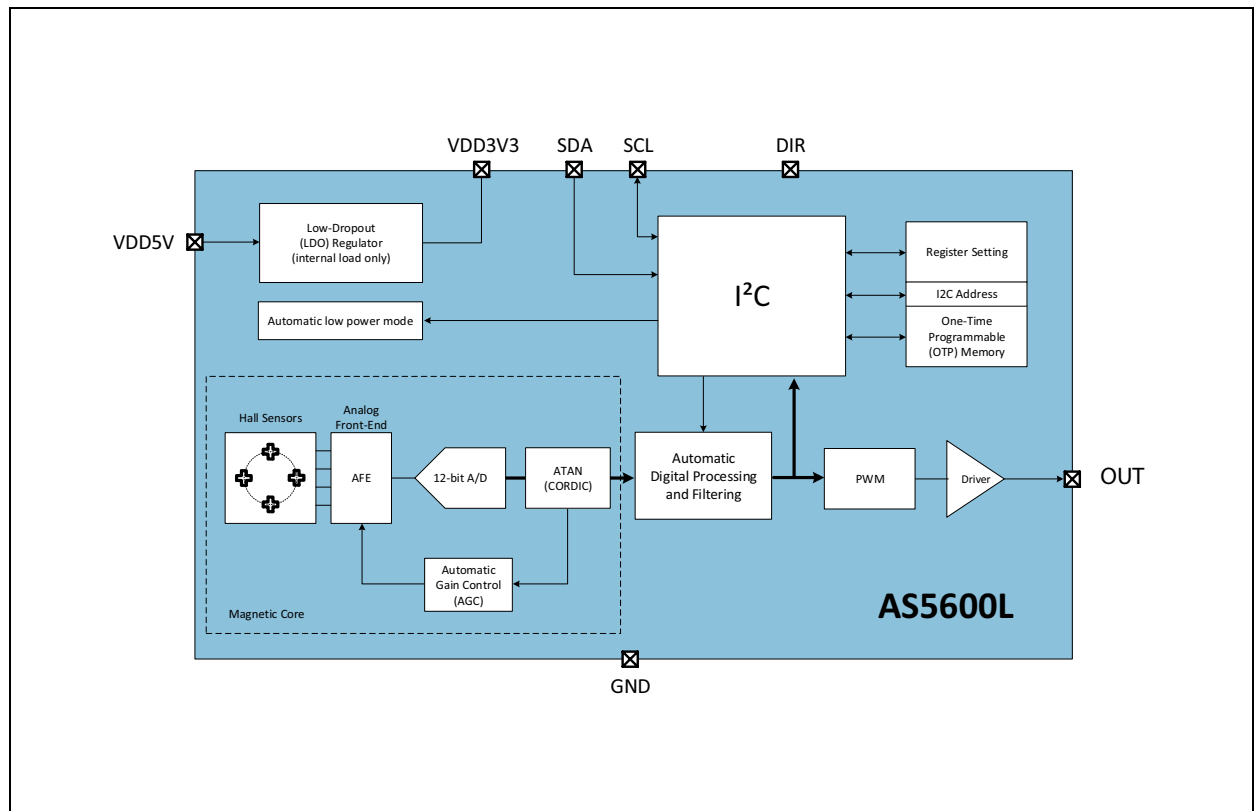
Applications

The AS5600L is ideally suited for contactless potentiometers, contactless knobs, pedals, RC servos and other angular position measurement solutions.

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS5600L



Pin Assignments

Figure 3:
SOIC-8 Pin Diagram

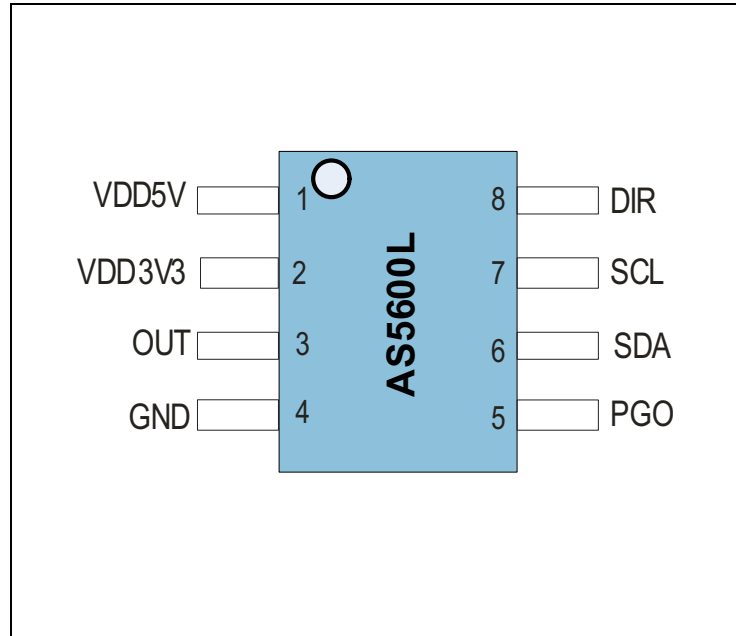


Figure 4:
SOIC-8 Pin Description

| Pin Number | Name | Type | Description |
|------------|--------|----------------------|--|
| 1 | VDD5V | Supply | Positive voltage supply in 5V mode (requires 100 nF decoupling capacitor) |
| 2 | VDD3V3 | Supply | Positive voltage supply in 3.3V mode (requires an external 1- μ F decoupling capacitor in 5V mode) |
| 3 | OUT | Digital output | PWM output. Fixed to VDD default. Enable in CONF register. |
| 4 | GND | Supply | Ground |
| 5 | PGO | Digital input | Program option (internal pull-up, connected to GND = Programming Option B) |
| 6 | SDA | Digital input/output | I ² C Data (consider external pull-up) |
| 7 | SCL | Digital input | I ² C Clock (consider external pull-up) |
| 8 | DIR | Digital input | Direction polarity (GND = values increase clockwise, VDD = values increase counterclockwise) |

Note(s):

1. In case of 5V operation the VDD3V3 output is intended for internal use only. It must not be loaded with an external load.

Figure 5:
WL-CSP Pin Diagram (Top View)

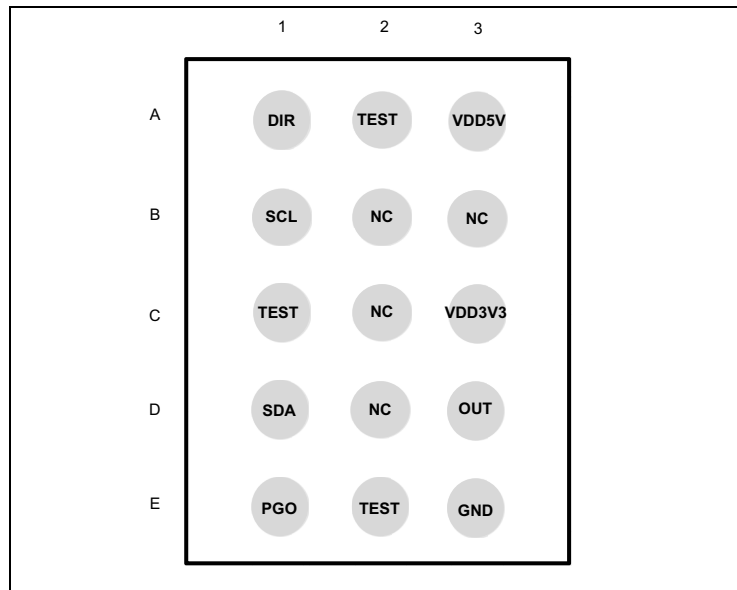


Figure 6:
WL-CSP Pin Description

| Pin Number | Name | Type | Description |
|-------------|--------|----------------------|---|
| A1 | DIR | Digital input | Direction polarity (GND = values increase clockwise, VDD = values increase counterclockwise) |
| A2 | TEST | Test pin | Connect to ground |
| A3 | VDD5V | Supply | Positive voltage supply in 5V mode (requires 100 nF decoupling capacitor) |
| B1 | SCL | Digital input | I ² C clock (consider external pull-up) |
| C1 | TEST | Test pin | Connect to ground |
| C3 | VDD3V3 | Supply | Positive voltage supply in 3.3V mode (requires an external 1 μF decoupling capacitor in 5V mode) ⁽¹⁾ |
| D1 | SDA | Digital input/output | I ² C data (consider external pull-up) |
| D3 | OUT | Digital output | PWM output. Fixed to VDD default. Enable in CONF register. |
| E1 | PGO | Digital input | Program option (internal pull-up, connected to GND = programming option B) |
| E2 | TEST | Test pin | Connect to ground |
| E3 | GND | Supply | Connect to ground |
| B2,B3,C2,D2 | NC | Not connected | Do not connect |

Note(s):

1. In case of 5V operation the VDD3V3 output is intended for internal use only. It must not be loaded with an external load.

Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Comments |
|--|---|------|---------|-------|---------------|
| Electrical Parameters | | | | | |
| VDD5V | DC supply voltage at VDD5V pin | -0.3 | 6.1 | V | |
| VDD3V3 | DC supply voltage at VDD3V3 pin | -0.3 | 4.0 | V | |
| VIO | DC supply voltage at all digital or analog pins | -0.3 | VDD+0.3 | V | |
| I _{SCR} | Input current (latch-up immunity) | -100 | 100 | mA | JESD78 |
| Continuous Power Dissipation (T_A = 70°C) | | | | | |
| P _T | Continuous power dissipation | | 50 | mW | |
| Electrostatic Discharge | | | | | |
| ESD _{HBM} | Electrostatic discharge HBM | ±1 | | kV | AEC-Q100-002E |

| Symbol | Parameter | Min | Max | Units | Comments |
|--|------------------------------------|-----|-----|-------|--|
| Temperature Ranges and Storage Conditions | | | | | |
| T _{STRG} | Storage temperature range | -55 | 125 | °C | |
| T _{BODY} | Package body temperature | | 260 | °C | SOIC-8: ICP/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn) |
| | | | | | WL-CSP: ICP/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." |
| RH _{NC} | Relative humidity (non-condensing) | 5 | 85 | % | |
| MSL | Moisture sensitivity level | 3 | | | SOIC-8: ICP/JEDEC J-STD-033 |
| | | 1 | | | WL-CSP: ICP/JEDEC J-STD-033 |

Electrical Characteristics

All limits are guaranteed. The parameters with minimum and maximum values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Operating Conditions

Figure 8:
System Electrical Characteristics and Temperature Range

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------|---|--|-----|-----|-----|-------|
| VDD5V | Positive supply voltage in 5.0V mode | 5.0V operation mode | 4.5 | 5.0 | 5.5 | V |
| | | During OTP burn procedure ⁽²⁾ | | | | |
| VDD3V3 | Positive supply voltage in 3.3V mode | 3.3V operation mode | 3.0 | 3.3 | 3.6 | V |
| | | During OTP burn procedure ⁽²⁾ | 3.3 | 3.4 | 3.5 | V |
| IDD | Supply current in NOM ⁽¹⁾ | PM = 00 Always on | | | 6.4 | mA |
| IDD_LPM1 | Supply current in LPM1 ⁽¹⁾ | PM = 01 Polling time = 5ms | | | 3.3 | mA |
| IDD_LPM2 | Supply current in LPM2 ⁽¹⁾ | PM = 10 Polling time = 20ms | | | 1.8 | mA |
| IDD_LPM3 | Supply current in LPM3 ⁽¹⁾ | PM = 11 Polling time = 100ms | | | 1.5 | mA |
| IDD_BURN | Supply current per bit for burn procedure | Initial peak, 1 μ s | | | 100 | mA |
| | | Steady burning, <30 μ s | | | 40 | mA |
| T _A | Operating temperature | | -40 | | 125 | °C |
| T _P | Programming temperature | | 20 | | 30 | °C |

Note(s):

1. For typical magnetic field (60mT) excluding current delivered to the external load and tolerance on polling times.
2. For OTP burn procedure the supply line source resistance should not exceed 10 Ω .

Digital Inputs and Outputs

Figure 9:
Digital Input and Output Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|---------------------------|------------|---------------------|-----|---------------------|---------|
| V_IH | High-level input voltage | | $0.7 \times V_{DD}$ | | | V |
| V_IL | Low-level input voltage | | | | $0.3 \times V_{DD}$ | V |
| V_OH | High-level output voltage | | $V_{DD} - 0.5$ | | | V |
| V_OL | Low-level output voltage | | | | 0.4 | V |
| I_LKG | Leakage current | | | | ± 1 | μA |

PWM Output

Figure 10:
PWM Output Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|--------------------------------|--------------|-----------|-----|------|------------|
| PWMf1 | PWM frequency ⁽¹⁾ | PWMF = 00 | | 115 | | Hz |
| PWMf2 | PWM frequency ⁽¹⁾ | PWMF = 01 | | 230 | | Hz |
| PWMf3 | PWM frequency ⁽¹⁾ | PWMF = 10 | | 460 | | Hz |
| PWMf4 | PWM frequency ⁽¹⁾ | PWMF = 11 | | 920 | | Hz |
| PWM_DC | PWM duty cycle | | 2.9 | | 97.1 | % |
| PWM_SR | PWM slew rate | Clload = 1nF | 0.5 | | 2 | V/ μs |
| I_O | Output current for PWM output | | ± 0.5 | | | mA |
| C_L | Capacitive load for PWM output | | | | 1 | nF |

Note(s):

1. Frequency is given as typical values, tolerance is $\pm 5\%$

Timing Characteristics

Figure 11:
Timing Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------|--|------------|-----|-----|-------|--------|
| T_DETWD | Watchdog detection time ⁽¹⁾ | WD = 1 | | 1 | | minute |
| T_PU | Power-up time | | | | 10 | ms |
| F_S | Sampling rate | | | | 150 | μs |
| T_SETTL1 | Settling time | SF = 00 | | | 2.2 | ms |
| T_SETTL2 | Settling time | SF = 01 | | | 1.1 | ms |
| T_SETTL3 | Settling time | SF = 10 | | | 0.55 | ms |
| T_SETTL4 | Settling time | SF = 11 | | | 0.286 | ms |

Note(s):

1. Given as typical values, tolerance is ±5%

Magnetic Characteristics

Figure 12:
Magnetic Characteristics

| Symbol | Parameter | Conditions | Min | Max | Units |
|----------|--|--|-----|-----|-------|
| Bz | Orthogonal magnetic field strength, regular output noise ON_SLOW and ON_FAST | Required orthogonal component of the magnetic field strength measured at the die's surface along a circle of 1mm | 30 | 90 | mT |
| Bz_ERROR | Minimum required orthogonal magnetic field strength, Magnet detection level | | | 8 | mT |

System Characteristics

Figure 13:
System Specifications

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------|----------------------------|---|-----|-----|-------|--------|
| RES | Resolution | | | 12 | | bit |
| INL_BL | System INL | Deviation from best line fit; 360° maximum angle, no magnet displacement, no zero-programming performed (PWM, I ² C) | | | ±1 | degree |
| ON_SLOW | RMS output noise (1 sigma) | Orthogonal component for the magnetic field within the specified range (Bz), after 2.2 ms; SF = 00 | | | 0.015 | degree |
| ON_FAST | RMS output noise (1 sigma) | Orthogonal component for the magnetic field within the specified range (Bz), after 286 μs, SF=11 | | | 0.043 | degree |

Detailed Description

The AS5600L is a Hall-based rotary magnetic position sensor using planar sensors that convert the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals coming from the Hall sensors are first amplified and filtered before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the hardwired CORDIC block (Coordinate Rotation Digital Computer) to compute the angle and magnitude of the magnetic field vector. The intensity of the magnetic field is used by the automatic gain control (AGC) to adjust the amplification level to compensate for temperature and magnetic field variations.

The angle value provided by the CORDIC algorithm is used by the output stage. The PWM output provides a digital output which represents the angle as the pulse width.

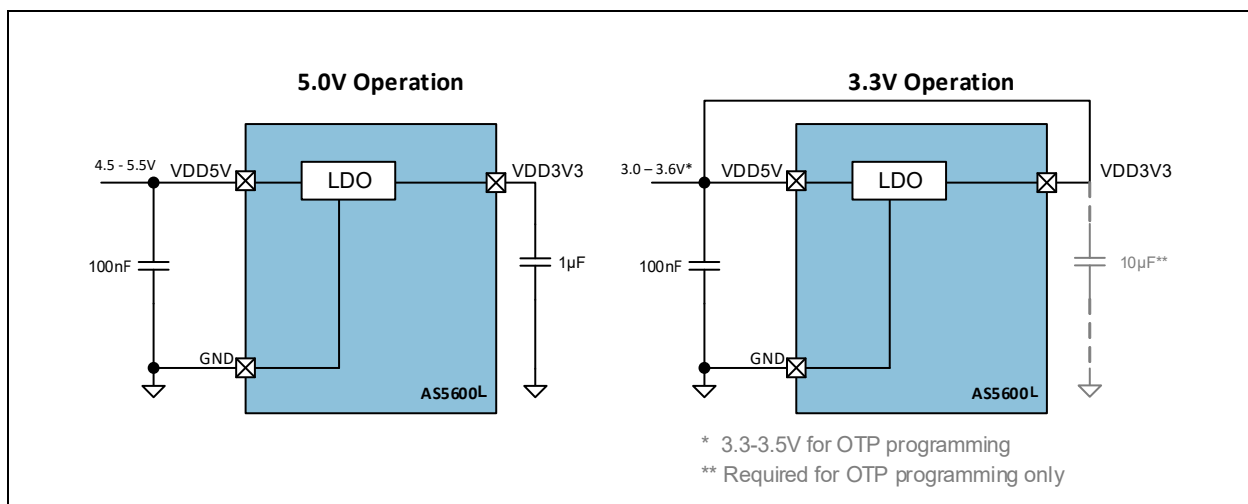
The AS5600L is programmed through an industry-standard I²C interface to write an on-chip non-volatile memory. This interface can be used to program a zero angle (start position) and a maximum angle (stop position) which maps the full resolution of the output to a subset of the entire 0 to 360 degree range.

IC Power Management

The AS5600L can be powered from a 5.0V supply using the on-chip LDO regulator, or it can be powered directly from a 3.3V supply. The internal LDO is not intended to power other external ICs and needs a 1 μ F capacitor to ground, as shown in Figure 14.

In 3.3V operation, the VDD5V and VDD3V3 pins must be tied together. VDD is the voltage level present at the VDD5V pin.

Figure 14:
5.0V and 3.3V Power Supply Options



I²C Interface

The AS5600L supports the 2-wire Fast-mode Plus I²C-slave protocol in device mode, in compliance with the NXP Semiconductors (formerly Philips Semiconductors) specification UM10204. A device that sends data onto the bus is a transmitter and a device receiving data is a receiver. The device that controls the message is called a master. The devices that are controlled by the master are called slaves. A master device generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions that control the bus. The AS5600L always operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and the input SCL. Clock stretching is not included.

The host MCU (master) initiates data transfers. The 7-bit slave address of the AS5600L is 0x40 (1000000 in binary).

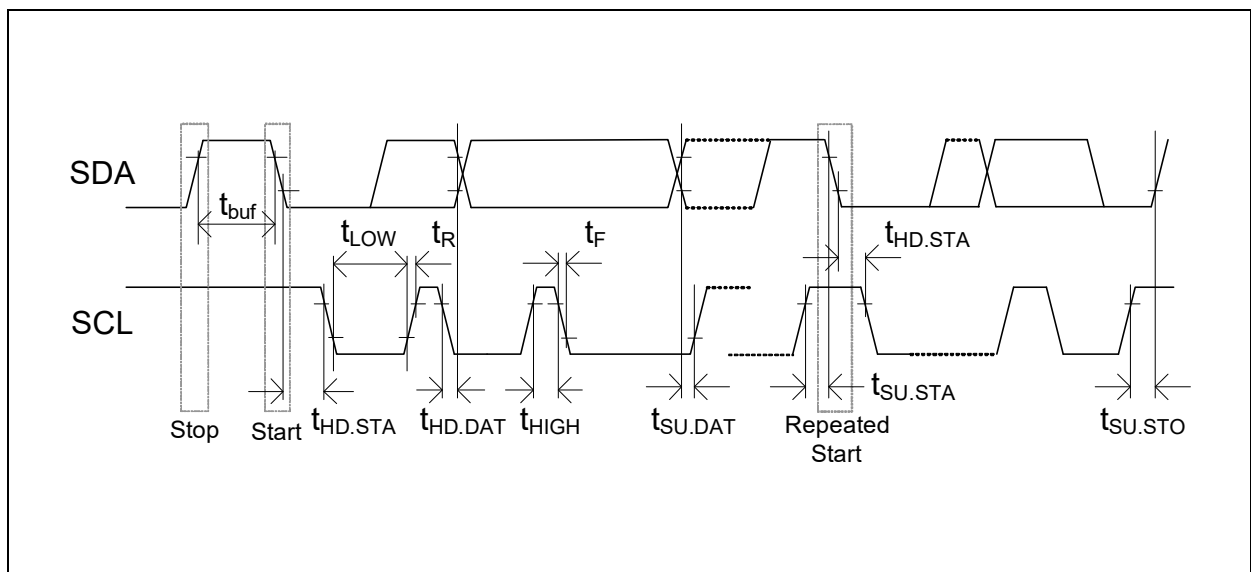
Supported Modes

- Random/Sequential read
- Byte/Page write
- Automatic increment (ANGLE register)
- Standard-mode
- Fast-mode
- Fast-mode Plus

The SDA signal is the bidirectional data line. The SCL signal is the clock generated by the I²C bus master to synchronize sampling data from SDA. The maximum SCL frequency is 1 MHz. Data is sampled on the rising edge of SCL.

I²C Interface Operation

Figure 15:
I²C Timing Diagram



I²C Electrical Specification

Figure 16:
I²C Electrical Specifications

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--|---|------------|-----|--------------------|------|
| V _{IL} | Logic low input voltage | | -0.3 | | 0.3 x VDD | V |
| V _{IH} | Logic high input voltage | | 0.7 x VDD | | VDD + 0.3 | V |
| V _{HYS} | Hysteresis of Schmitt trigger inputs | VDD > 2.5V | 0.05 x VDD | | | V |
| V _{OL} | Logic low output voltage (open-drain or open-collector) at 3 mA sink current | VDD > 2.5V | | | 0.4 | V |
| I _{OL} | Logic low output current | V _{OL} = 0.4V | 20 | | | mA |
| t _{OF} | Output fall time from V _{IHmax} to V _{ILmax} | | 10 | | 120 ⁽¹⁾ | ns |
| t _{SP} | Pulse width of spikes that must be suppressed by the input filter | | | | 50 ⁽²⁾ | ns |
| I _I | Input current at each I/O Pin | Input Voltage between 0.1 x VDD and 0.9 x VDD | -10 | | +10 ⁽³⁾ | μA |
| C _B | Total capacitive load for each bus line | | | | 550 | pF |
| C _{I/O} | I/O capacitance (SDA, SCL) ⁽⁴⁾ | | | | 10 | pF |

Note(s):

1. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing.
2. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
3. I/O pins of Fast-mode and Fast-mode Plus devices must not load or drive the SDA and SCL lines if VDD is switched OFF.
4. Special-purpose devices such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.

I²C Timing

Figure 17:
I²C Timing

| Symbol | Parameter | Min | Max | Unit |
|---------------------|--|------|--------------------|---------------|
| f_{SCLK} | SCL clock frequency | | 1.0 | MHz |
| t_{BUF} | Bus free time (time between the STOP and START conditions) | 0.5 | | μs |
| $t_{\text{HD;STA}}$ | Hold time; (Repeated) START condition ⁽¹⁾ | 0.26 | | μs |
| t_{LOW} | Low phase of SCL clock | 0.5 | | μs |
| t_{HIGH} | High phase of SCL clock | 0.26 | | μs |
| $t_{\text{SU;STA}}$ | Setup time for a Repeated START condition | 0.26 | | μs |
| $t_{\text{HD;DAT}}$ | Data hold time ⁽²⁾ | | 0.45 | μs |
| $t_{\text{SU;DAT}}$ | Data setup time ⁽³⁾ | 50 | | ns |
| t_{R} | Rise time of SDA and SCL signals | | 120 | ns |
| t_{F} | Fall time of SDA and SCL signals | 10 | 120 ⁽⁴⁾ | ns |
| $t_{\text{SU;STO}}$ | Setup time for STOP condition | 0.26 | | μs |

Note(s):

1. After this time, the first clock is generated.
2. A device must internally provide a minimum hold time of 120 ns (Fast-mode Plus) for the SDA signal (referred to the V_{IHmin} of SCL) to bridge the undefined region of the falling edge of SCL.
3. A Fast-mode device can be used in a standard-mode system, but the requirement $t_{\text{SU;DAT}} = 250$ ns must be met. This is automatically if the device does not stretch the low phase of SCL. If such a device does stretch the low phase of SCL, it must drive the next data bit on SDA ($t_{\text{Rmax}} + t_{\text{SU;DAT}} = 1000 + 250 = 1250$ ns) before SCL is released.
4. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, this has to be considered for bus timing.

I²C Modes

Invalid Addresses

There are two addresses used to access an AS5600L register. The first is the slave address used to select the AS5600L. All I²C bus transactions include a slave address. The slave address of the AS5600L is 0x40 (1000000 in binary). The second address is a word address sent in the first byte transferred in a write transaction. The word address selects a register on the AS5600L. The word address is loaded into the address pointer on the AS5600L. During subsequent read transactions and subsequent bytes in the write transaction, the address pointer provides the address of the selected register. The address pointer is incremented after each byte is transferred, except for certain read transactions to special registers.

If the user sets the address pointer to an invalid word address, the address byte is not acknowledged (the A bit is high). Nevertheless, a read or write cycle is possible. The address pointer is increased after each byte.

Reading

When reading from an invalid address, the AS5600L returns all zeros in the data bytes. The address pointer is incremented after each byte. Sequential reads over the whole address range are possible including address overflow.

Automatic Increment of the Address Pointer for ANGLE, RAW ANGLE and MAGNITUDE Registers

These are special registers which suppress the automatic increment of the address pointer on reads, so a re-read of these registers requires no I²C write command to reload the address pointer. This special treatment of the pointer is effective only if the address pointer is set to the high byte of the register.

Writing

A write to an invalid address is not acknowledged by the AS5600L, although the address pointer is incremented. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

Supported Bus Protocol

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever SCL is high. Changes in the data line while SCL is high are interpreted as START or STOP conditions.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both SDA and SCL remain high.

Start Data Transfer

A change in the state of SDA from high to low while SCL is high defines the START condition.

Stop Data Transfer

A change in the state of SDA from low to high while SCL is high defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, SDA is stable for the duration of the high phase of SCL. The data on SDA must be changed during the low phase of SCL. There is one clock period per bit of data.

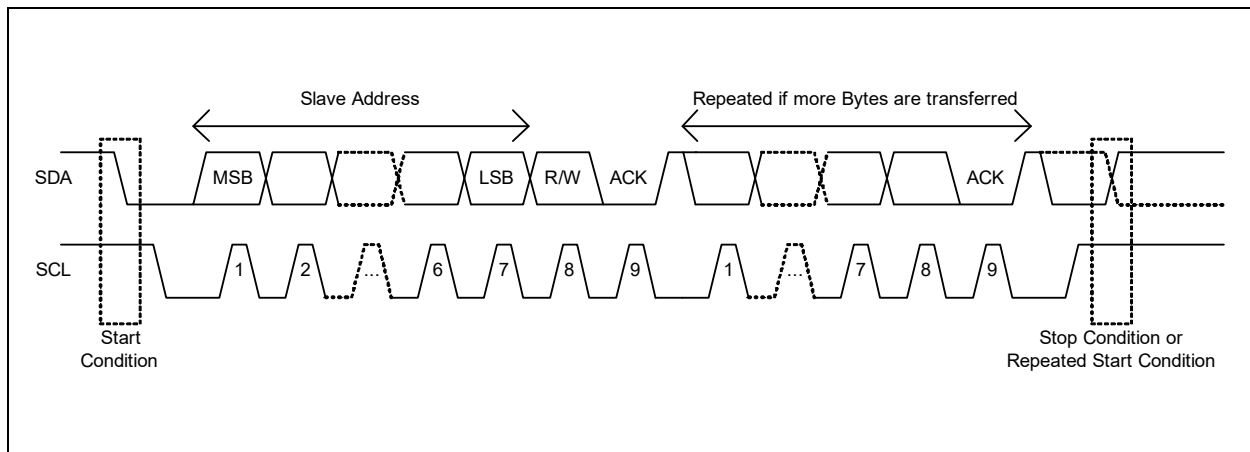
Each I²C bus transaction is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the I²C bus master. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each I²C slave device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The I²C bus master device must generate an extra clock period for this acknowledge bit.

A slave that acknowledges must pull down SDA during the acknowledge clock period in such a way that SDA is stable low during the high phase of the acknowledge clock period. Of course, setup and hold times must be taken into account. A master must signal an end of a read transaction by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave SDA high to enable the master to generate the STOP condition.

Figure 18:
Data Read



Depending on the state of the R/W bit, two types of data transfer are possible:

Data Transfer from a Master Transmitter to a Slave Receiver

The first byte transmitted by the master is the slave address, followed by R/W = 0. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. If the slave does not understand the command or data it sends a not acknowledge (NACK). Data is transferred with the most significant bit (MSB) first.

Data Transfer from a Slave Transmitter to a Master Receiver

The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a NACK is returned. The master generates all of the SCL clock periods and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Because a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

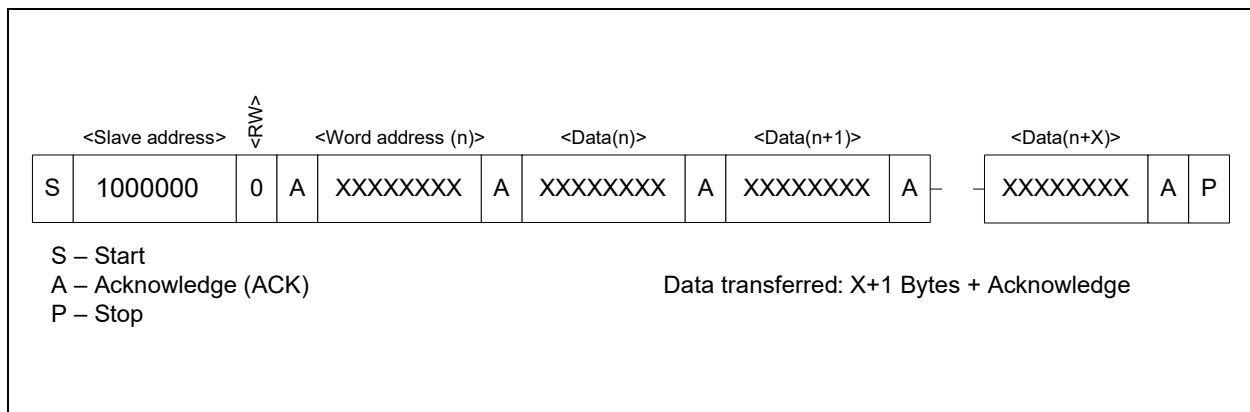
AS5600L Slave Modes

Slave Receiver Mode (Write Mode)

Serial data and clock are received through SDA and SCL. Each byte is followed by an acknowledge bit or by a not acknowledge depending on whether the address-pointer selects a valid address. START and STOP conditions are recognized as the beginning and end of a bus transaction. The slave address byte is the first byte received after the START condition. The 7-bit AS5600L address is 0x40 (1000000 in binary).

The 7-bit slave address is followed by the direction bit (R/W), which, for a write, is 0 (low). After receiving and decoding the slave address byte the slave device drives an acknowledge on SDA. After the AS5600L acknowledges the slave address and write bit, the master transmits a register address (word address) to the AS5600L. This is loaded into the address pointer on the AS5600L. If the address is a valid readable address, the AS5600L answers by sending an acknowledge (A bit low). If the address pointer selects an invalid address, a not acknowledge is sent (A bit high). The master may then transmit zero or more bytes of data. If the address pointer selects an invalid address, the received data are not stored. The address pointer will increment after each byte transferred whether or not the address is valid. If the address-pointer reaches a valid position again, the AS5600L answers with an acknowledge and stores the data. The master generates a STOP condition to terminate the write transaction.

Figure 19:
Data Write (Slave Receiver Mode)



Slave Transmitter Mode (Read Mode)

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the AS5600L will drive data on SDA. START and STOP conditions are recognized as the beginning and end of a bus transaction. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS5600L address. The 7-bit slave address is followed by the direction bit (R/W), which, for a read, is 1 (high).

After receiving and decoding the slave address byte, the slave device drives an acknowledge on the SDA line. The AS5600L then begins to transmit data starting with the register address pointed to by the address pointer. If the address pointer is not written before the initiation of a read transaction, the first address that is read is the last one stored in the address pointer. The AS5600L must receive a not acknowledge (NACK) to end a read transaction.

Figure 20:
Data Read (Slave Transmitter Mode)

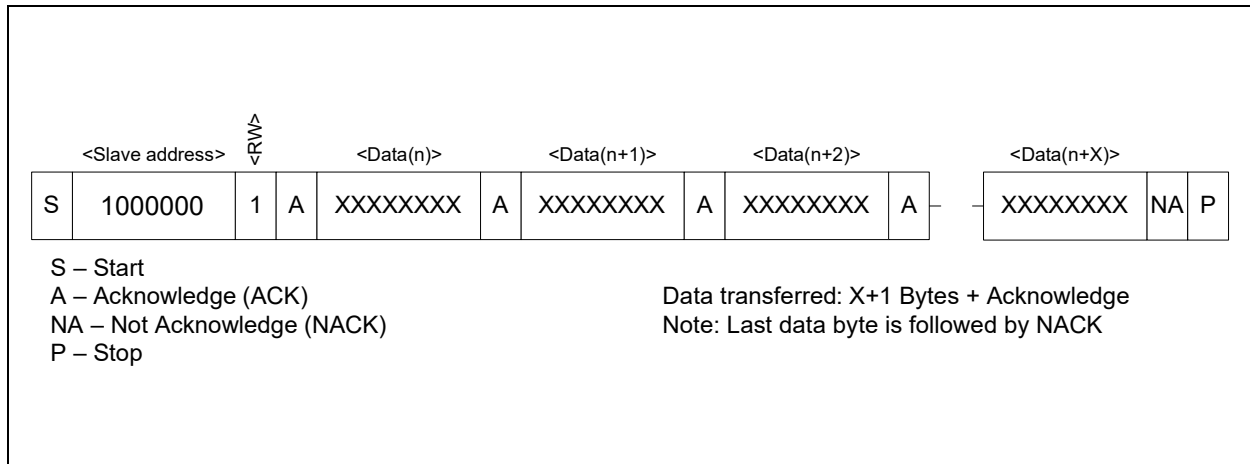
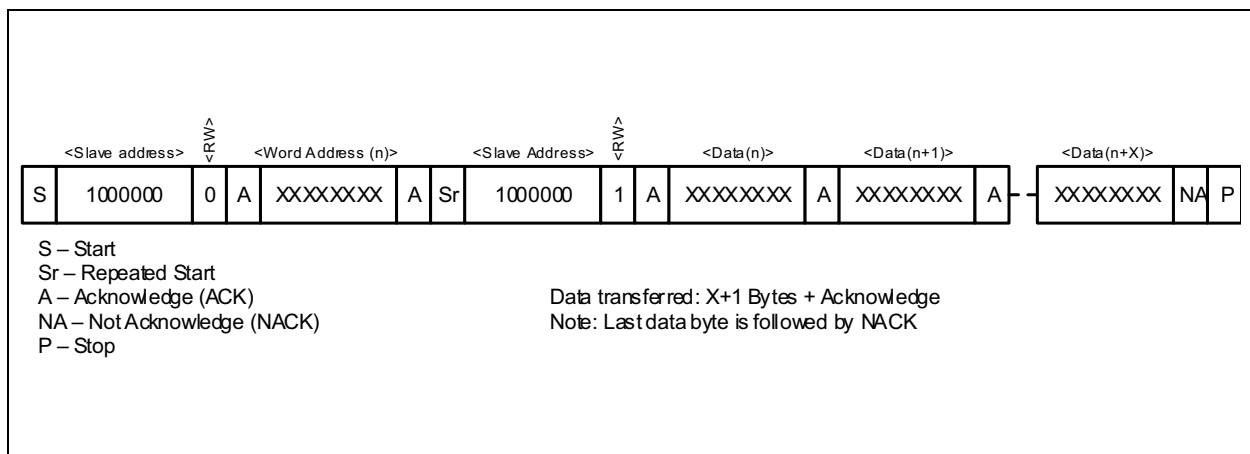


Figure 21:
Data Read with Address Pointer Reload (Slave Transmitter Mode)



SDA and SCL Input Filters

Input filters for SDA and SCL inputs are included to suppress noise spikes of less than 50ns.

Register Description

The following registers are accessible over the serial I²C interface. The 7-bit slave address of the slave is 0x40 (1000000 in binary). To permanently program a configuration, a non-volatile memory (OTP) is provided.

Figure 22:
Register Map

| Address | Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-----------|-------|-----------------------------|-----------|-----------|----------|---------|-----------------|---------|-----------|
| Configuration Registers ^{(1), (2)} | | | | | | | | | | |
| 0x00 | ZMCO | R | | | | | | | | ZMCO(1:0) |
| 0x01 | ZPOS | R/W/P | | | | | | ZPOS(11:8) | | |
| 0x02 | | | ZPOS(7:0) | | | | | | | |
| 0x03 | MPOS | R/W/P | | | | | | MPOS(11:8) | | |
| 0x04 | | | MPOS(7:0) | | | | | | | |
| 0x05 | MANG | R/W/P | | | | | | MANG(11:8) | | |
| 0x06 | | | MANG(7:0) | | | | | | | |
| 0x07 | CONF | R/W/P | | | WD | FTH(2:0) | | | SF(1:0) | |
| 0x08 | | | PWMF(1:0) | OUTS(1:0) | HYST(1:0) | | PM(1:0) | | | |
| 0x20 | I2CADDR | R/W/P | I2CADDR(6:0) ⁽³⁾ | | | | | | | |
| 0x21 | I2CUPDT | R/W | I2CSTRB(6:0) | | | | | | | |
| Output Registers | | | | | | | | | | |
| 0x0C | RAW ANGLE | R | | | | | | RAW ANGLE(11:8) | | |
| 0x0D | | R | RAW ANGLE(7:0) | | | | | | | |
| 0x0E | ANGLE | R | | | | | | ANGLE(11:8) | | |
| 0x0F | | R | ANGLE(7:0) | | | | | | | |

| Address | Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------|-----------|-----|--|-------|-------|-------|------------------|-------|-------|-------|
| Status Registers | | | | | | | | | | |
| 0x0B | STATUS | R | | | MD | ML | MH | | | |
| 0x1A | AGC | R | AGC(7:0) | | | | | | | |
| 0x1B | MAGNITUDE | R | | | | | MAGNITUDE (11:8) | | | |
| 0x1C | | R | MAGNITUDE(7:0) | | | | | | | |
| Burn Commands | | | | | | | | | | |
| 0xFF | BURN | W | Burn_Angle = 0x80; Burn_Setting = 0x40 | | | | | | | |

Note(s):

1. To change a configuration, read out the register, modify only the desired bits and write the new configuration. Blank fields may contain factory settings.
2. During power-up, configuration registers are reset to the permanently programmed value. Not programmed bits are zero.
3. The default slave address is 0x40.

ZPOS/MPOS/MANG Registers

These registers are used to configure the start position (ZPOS) and a stop position (MPOS) or size of angular range (MANG) for a narrower angular range. The angular range must be greater than 18 degrees. In case of narrowed angular range, the resolution is not scaled to narrowed range (e.g. 0°-360°(full-turn) → 4096dec; 0°-180° → 2048dec). To configure the angular range, see [Angle Programming](#).

CONF Register

The CONF register supports customizing the AS5600L. Figure 23 shows the mapping of the CONF register.

Figure 23:
CONF Register

| Name | Bit Position | Description |
|---------------|--------------|--|
| PM(1:0) | 1:0 | Power Mode 00 = NOM, 01 = LPM1, 10 = LPM2, 11 = LPM3 |
| HYST(1:0) | 3:2 | Hysteresis 00 = OFF, 01 = 1 LSB, 10 = 2 LSBs, 11 = 3 LSBs |
| OUTS(1:0) | 5:4 | Output Stage 00 = OUT set to VDD, 01 = OUT set to VDD, 10 = digital PWM |
| PWMF (1:0) | 7:6 | PWM Frequency 00 = 115 Hz; 01 = 230 Hz; 10 = 460 Hz; 11 = 920 Hz |
| SF(1:0) | 9:8 | Slow Filter 00 = 16x ⁽¹⁾ ; 01 = 8x; 10 = 4x; 11 = 2x |
| FTH(2:0) | 12:10 | Fast Filter Threshold 000 = slow filter only, 001 = 6 LSBs, 010 = 7 LSBs, 011 = 9 LSBs, 100 = 18 LSBs, 101 = 21 LSBs, 110 = 24 LSBs, 111 = 10 LSBs |
| WD | 13 | Watchdog 0 = OFF, 1 = ON |

Note(s):

1. Forced in Low Power Mode (LPM)

ANGLE/RAW ANGLE Register

The RAW ANGLE register contains the unscaled and unmodified angle. The scaled output value is available in the ANGLE register.

Note(s): If the range is configured for 360degrees (default), the ANGLE register has a 10-LSB hysteresis at the limit of the 360 degree range to avoid discontinuity points or toggling of the output within one rotation.

STATUS Register

The STATUS register provides bits that indicate the current state of the AS5600L.

Figure 24:
STATUS Register

| Name | State When Bit Is High |
|------|--|
| MH | AGC minimum gain overflow, magnet too strong |
| ML | AGC maximum gain overflow, magnet too weak |
| MD | Magnet was detected |

AGC Register

The AS5600L uses Automatic Gain Control in a closed loop to compensate for variations of the magnetic field strength due to changes of temperature, airgap between IC and magnet, and magnet degradation. The AGC register indicates the gain. For the most robust performance, the gain value should be in the center of its range. The airgap of the physical system can be adjusted to achieve this value.

In 5V operation, the AGC range is 0-255 counts. The AGC range is reduced to 0-128 counts in 3.3V mode.

MAGNITUDE Register

The MAGNITUDE register indicates the magnitude value of the internal CORDIC.

Non-Volatile Memory (OTP)

The non-volatile memory is used to permanently program the configuration. To program the non-volatile memory, the I²C interface is used ([Option A](#), [Option C](#)). Alternatively, start and stop positions can be programmed through the output pin ([Option B](#)). The programming can be either performed in the 5V supply mode or in the 3.3V operation mode but using a minimum supply voltage of 3.3V and a 10 µF capacitor at the VDD3V3 pin to ground. This 10 µF capacitor is needed only during the programming of the device. Two different commands are used to permanently program the device:

Burn_Angle Command (ZPOS, MPOS)

The host microcontroller can perform a permanent programming of ZPOS and MPOS with a BURN_ANGLE command. To perform a BURN_ANGLE command, write the value 0x80 into register 0xFF. The BURN_ANGLE command can be executed up to 2 times. ZMCO shows how many times ZPOS and MPOS have been permanently written.

This command will only be executed if the presence of the magnet is detected (MD = 1).

Burn_Setting Command (MANG, CONFIG, I2CADDR)

The host microcontroller can perform a permanent writing of MANG and CONFIG with a BURN_SETTING command. Once a bit in those registers is permanent written to 1, it stays on 1 and cannot be changed to 0 anymore. A bit which is 0 can be programmed to 1. To perform a BURN_SETTING command, write the value 0x40 into register 0xFF.

MANG can be written only if ZPOS and MPOS have never been permanently written (ZMCO = 00).

Angle Programming

For applications which do not use the full 0 to 360 degree angular range. The angular range must be greater than 18 degrees. In case of narrowed angular range, the resolution is not scaled to narrowed range. (e.g. 0°-360°(full-turn) → 4096dec; 0°-180° → 2048dec).

The range is specified by programming a start position (ZPOS) and either a stop position (MPOS) or the size of the angular range (MANG).

The BURN_ANGLE command can be executed up to 2 times.

There are three recommended methods for programming the angular range:

- **Option A:** Angle Programming Through the I²C Interface
- **Option B:** Angle Programming Through the OUT Pin
- **Option C:** Programming a Maximum Angular Range Through the I²C Interface

Figure 25:
Option A: Angle Programming Through the I²C Interface

| | |
|---|--|
| Use the correct hardware configuration shown in Figure 36 and Figure 37 . | |
| Step 1 | Power up the AS5600L. |
| Step 2 | Turn the magnet to the start position. |
| Step 3 | Read the RAW ANGLE register. Write the RAW ANGLE value into the ZPOS register. Wait at least 1 ms. |
| Step 4 | Rotate the magnet in the direction defined by the level on the DIR pin (GND for clockwise, VDD for counterclockwise) to the stop position. The amount of rotation must be greater than 18 degrees. |
| Step 5 | Read the RAW ANGLE register. Write the RAW ANGLE value into the MPOS register. Wait at least 1 ms. |
| Proceed with Step 6 to permanently program the configuration. | |
| Step 6 | Perform a BURN_ANGLE command to permanently program the device. Wait at least 1 ms. |
| Step 7 | Verify the BURN_ANGLE command: Write the commands 0x01, 0x11 and 0x10 sequentially into the register 0xFF to load the actual OTP content. Read the ZPOS and MPOS registers to verify that the BURN_ANGLE command was successful. |
| Step 8 | Read and verify the ZPOS and MPOS registers again after a new power-up cycle. |

Note(s):

1. After each register command, the new setting is effective at the output at least 1 ms later.
2. It is highly recommended to perform a functional test after this procedure.

Figure 26:
Option B: Angle Programming Through the OUT Pin

| | |
|---|--|
| Use the correct hardware configuration shown in Figure 36 and Figure 37 . The PGO pin is connected to GND and the OUT pin is pulled high by an internal resistor until the programming procedure is finished. | |
| Step 1 | Power up the AS5600L. |
| Step 2 | Position the magnet in the start position. |
| Step 3 | Pull the OUT pin to GND for at least 100 ms, then allow the pin to float. |
| Step 4 | Rotate the magnet in the same direction defined by the level on the DIR pin (GND for clockwise, VDD for counterclockwise) to the stop position. The amount of rotation must be greater than 18 degrees. |
| Step 5 | Pull the OUT pin to GND for at least 100 ms, then allow the pin to float. |
| Step 6 | Check if the OUT pin is permanently driven to GND. This indicates an error occurred during programming. If the voltage driven on the OUT pin corresponds to the magnet position, the procedure was performed successfully. |

Note(s):

1. After step 5 the new setting is effective at the output.
2. If step 3 is not followed by step 5 no permanent write will be performed.
3. It is highly recommended to perform a functional test after the procedure.
4. This procedure can be executed only one time; the zero position and maximum angle can be reprogrammed only through the I²C ([Option A](#)).
5. This procedure can be executed only if the presence of the magnet is detected (MD = 1).

Figure 27:
Option C: Programming a Maximum Angular Range Through the I²C Interface

| | |
|---|--|
| Use the correct hardware configuration shown in Figure 36 and Figure 37 . | |
| Step 1 | Power up the AS5600L. |
| Step 2 | Use the I ² C interface to write the maximum angular range into the MANG register. For example, if the maximum angular range is 90 degrees, write the MANG register with 0x400. Configure additional configuration settings by writing the CONFIG and I2CADDR register (see I²C Address Programming). Wait at least 1 ms. |
| Proceed with Step 3 to permanently program the configuration. | |
| Step 3 | Perform a BURN_SETTINGS command to permanently program the device. Wait at least 1 ms. |
| Step 4 | Verify the BURN_SETTINGS command: Write the commands 0x01, 0x11 and 0x10 sequentially into the register 0xFF to load the actual OTP content. Read and verify the MANG and CONF registers to verify that the BURN_SETTINGS command was successful. |
| Proceed with Step 5 to permanently program a zero position. If the OUT pin is used for this option, the PGO pin must be connected to GND. | |
| Step 5 | Position the magnet in the start position (zero angle). |
| Step 6 | Pull the OUT pin to GND for at least 100 ms, then allow the pin to float. Alternatively, program the zero position through the I ² C interface (Option A). Wait at least 1 ms. |
| Step 7 | Verify the permanent programming by I ² C (Option A) or check if OUT is permanently driven to GND (Option B). |
| Step 8 | Read and verify the permanently programmed registers again after a new power-up cycle. |

Note(s):

1. After each register command, the new configuration is effective at the output at least 1 ms later.
2. It is recommended to perform a functional test after this procedure.
3. Once a bit in registers MANG, CONFIG and I2CADDR is permanent written to 1, it stays on 1 and cannot be changed to 0 anymore. A bit which is 0 can be programmed to 1. Except the MSB bit of I2CADDR. Once the MSB bit of the slave address is programmed to 0, it cannot be changed to 1 again.
4. MANG can be written only if ZPOS and MPOS have never been permanently written (ZMCO = 00).

I²C Address Programming

The 7-bit I²C slave address of the AS5600L is programmable to allow communication between a MCU and multiple AS5600L position sensors on one bus. The default slave address is 40h.

There are two possibilities to change the I²C slave address:

- **Temporary Change:** Write new slave address into register [I2CADDR](#) and [I2CUPDT](#). This change of the I²C slave address is just temporary. After power-on reset the slave address is set to previous value.
- **Permanent Change:** Write the new slave address to register [I2CADDR](#), then perform BURN_SETTING command. This option is for permanently changing the I²C slave address.

Note(s): Once the MSB bit of the slave address is programmed to 0, it cannot be changed to 1 again.

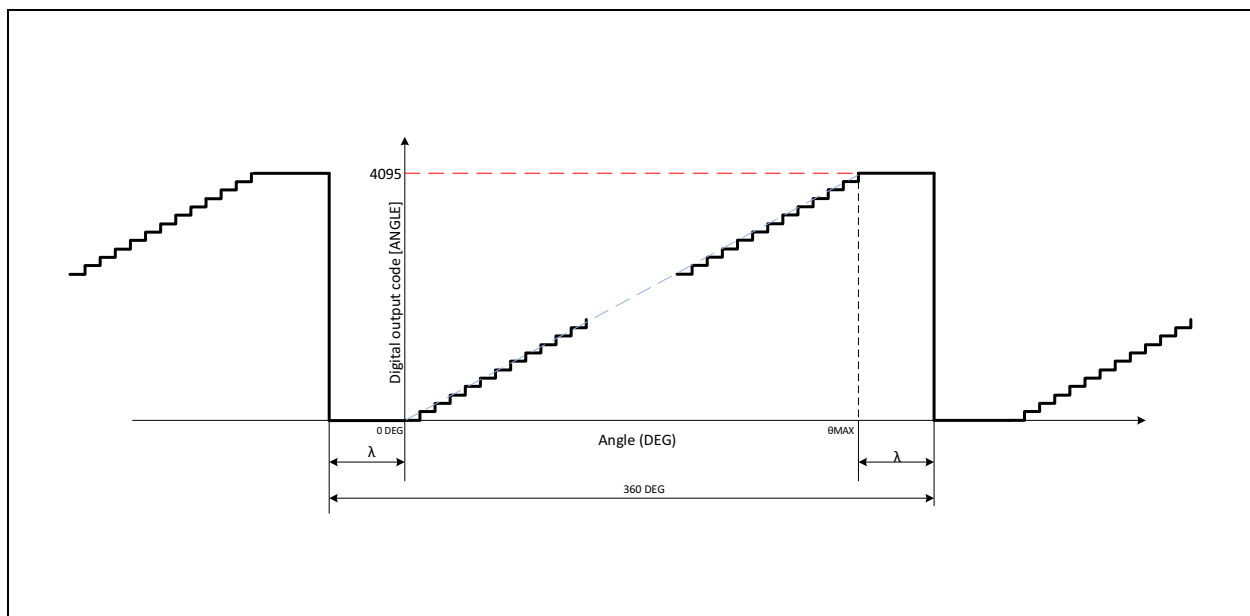
Output Stage

Without regard to the PWM output, an external unit can read the angle from the ANGLE register through I²C interface at any time. The output stage is fixed to VDD default.

Note(s): To enable the PWM output configure the OUTS bits in the CONF register.

The AS5600L supports programming both a zero angle ("0 DEG") as well as the maximum angular range (" θ_{\max} "). As shown in Figure 28, reducing the maximum angular range pushes the discontinuity points away from the edges "0 DEG" and " θ_{\max} " by λ , where $\lambda = (360 - \theta_{\max})/2$.

Figure 28:
Output Characteristic Over a Range Smaller Than 360°



If θ_{\max} is the maximum angle, the number of steps N of the output signal OUT is:

$$N = (\theta_{\max}/360) \times 4096$$

PWM Output Mode

The AS5600L output stage can be programmed in the OUTS bits of the CONF register for a PWM-encoded digital output (OUTS = 10). In this mode, the OUT pin provides a digital PWM signal. The duty cycle of each pulse is proportional to the absolute angle of the rotating magnet.

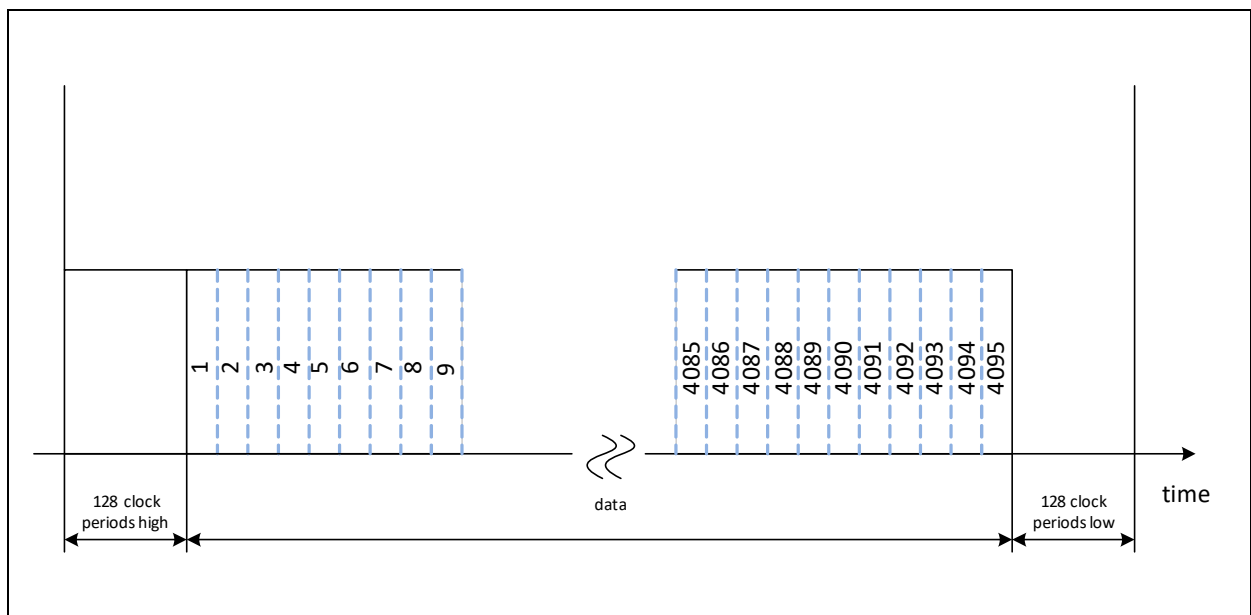
The PWM signal consists of a frame of 4351 PWM clock periods as shown in Figure 29. This PWM frame is composed of the following sections:

- 128 PWM clock periods high
- 4095 PWM clock periods data
- 128 PWM clock periods low

The angle is represented in the data part of the frame, and one PWM clock period represents one 4096th of the full angular range. The PWM frequency is programmed with the PWMF bits in the CONF register.

Note(s): If the range is 360 degrees, to avoid discontinuity points exactly at the limit of the range, a 10-LSB hysteresis is applied. This hysteresis suppresses toggling the position when the magnet is close to zero or 360 degrees.

Figure 29:
Output Characteristics in Pulse Width Modulation Mode



An angle of zero degrees is represented by 128 clock periods high and 4223 clock periods low, while a maximum angle consists of 4223 clock periods high and 128 clock periods low.

Step Response and Filter Settings

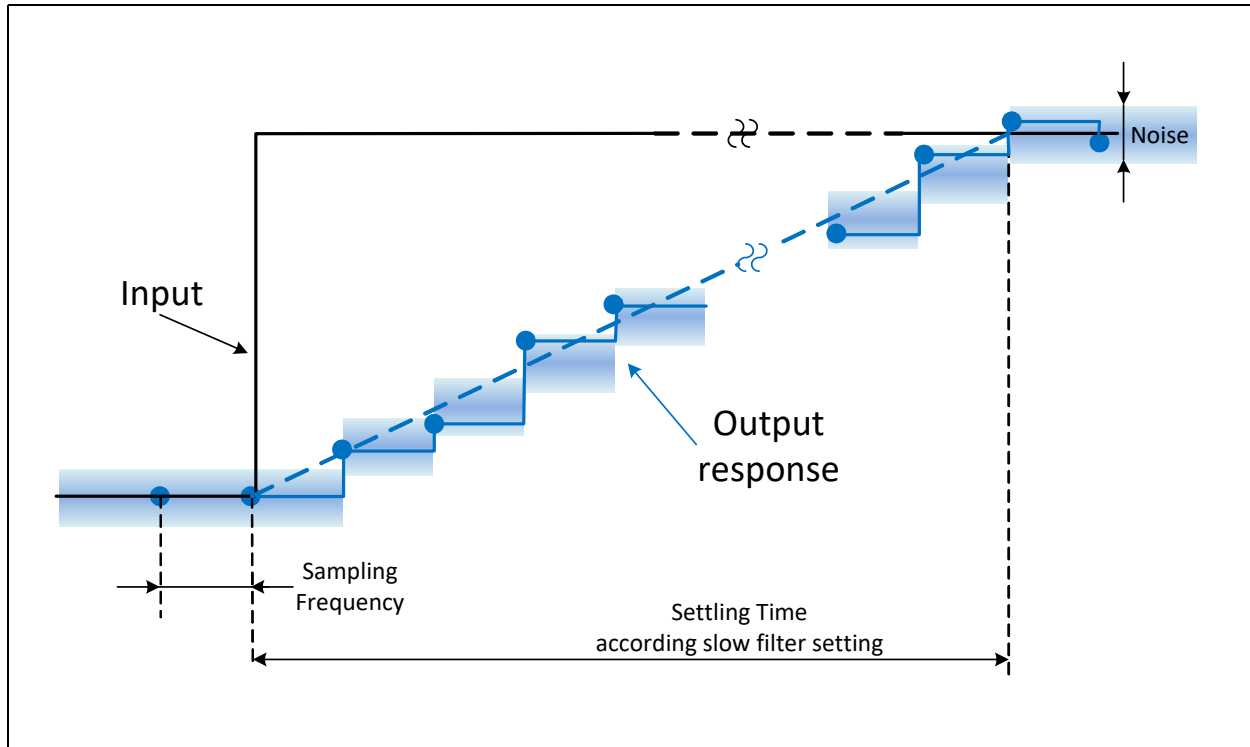
The AS5600L has a digital post-processing programmable filter which can be set in fast or slow modes. The fast filter mode can be enabled by setting a fast filter threshold in the FTH bits of the CONF register.

If the fast filter is OFF, the step output response is controlled by the slow linear filter. The step response of the slow filter is programmable with the SF bits in the CONF register. Figure 31 shows the tradeoff between delay and noise for the different SF bit settings.

Figure 30:
Step Response Delay vs. Noise Band

| SF | Step Response Delay (ms) | Max. RMS Output Noise (1 Sigma) (Degree) |
|----|--------------------------|--|
| 00 | 2.2 | 0.015 |
| 01 | 1.1 | 0.021 |
| 10 | 0.55 | 0.030 |
| 11 | 0.286 | 0.043 |

Figure 31:
Step Response (fast filter OFF)

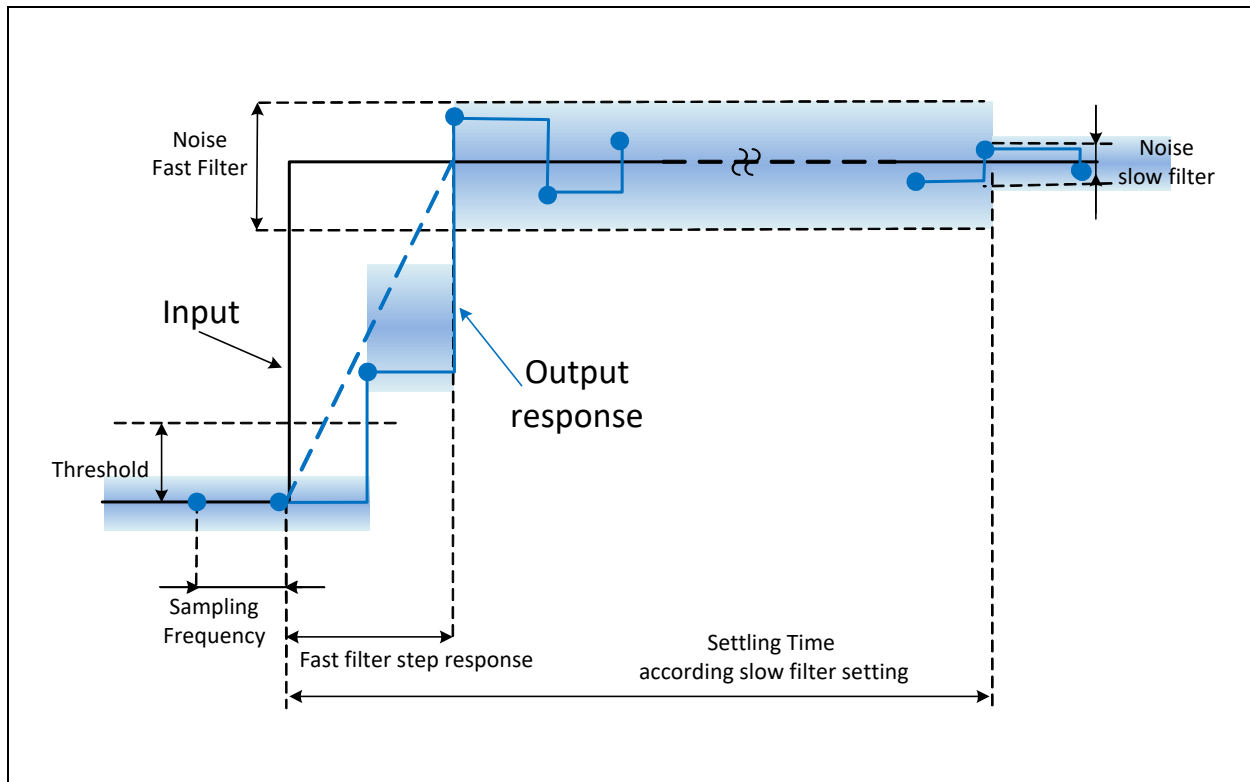


For a fast step response and low noise after settling, the fast filter can be enabled. The fast filter works only if the input variation is greater than the fast filter threshold, otherwise the output response is determined only by the slow filter. The fast filter threshold is programmed with the **FTH bits** in the **CONF Register**. As shown in **Figure 33**, the step response stays within an error band after two full sampling periods to settle to the final value determined by the slow filter.

Figure 32:
Fast Filter Threshold

| FTH | Fast Filter Threshold (LSB) | |
|-----|-----------------------------|---------------------|
| | Slow-to-fast filter | Fast-to-slow filter |
| 000 | Slow filter only | |
| 001 | 6 | 1 |
| 010 | 7 | 1 |
| 011 | 9 | 1 |
| 100 | 18 | 2 |
| 101 | 21 | 2 |
| 110 | 24 | 2 |
| 111 | 10 | 4 |

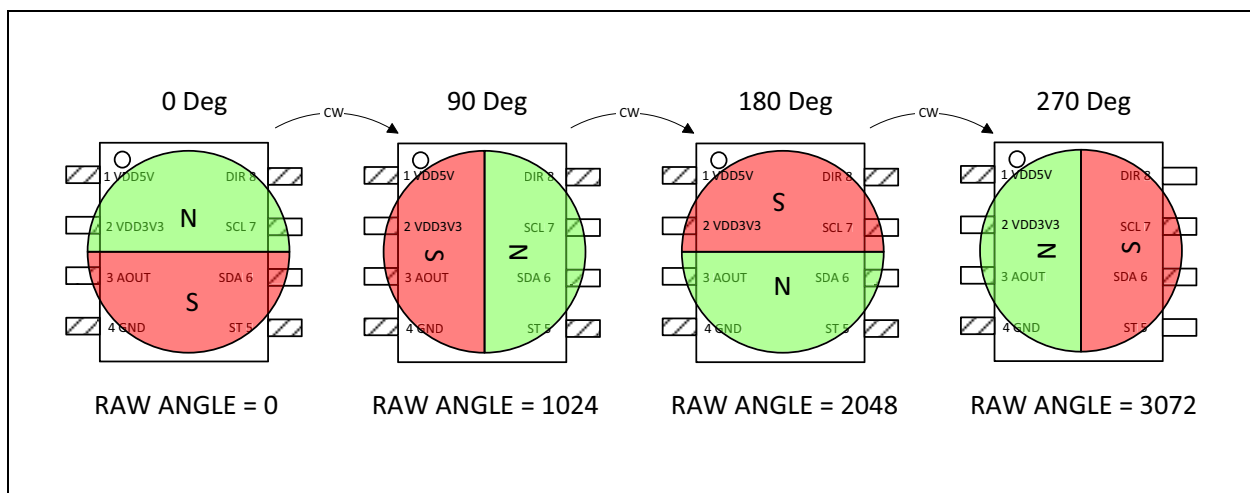
Figure 33:
Step Response (fast filter ON)



Direction (clockwise vs. counterclockwise)

The AS5600L allows controlling the direction of the magnet rotation with the DIR pin. If DIR is connected to GND (DIR = 0) a clockwise rotation viewed from the top will generate an increment of the calculated angle. If the DIR pin is connected to VDD (DIR = 1) an increment of the calculated angle will happen with counterclockwise rotation.

Figure 34:
Raw Angle in Clockwise Direction



Hysteresis

To avoid any toggling of the output when the magnet is not moving, a 1 to 3 LSB hysteresis of the 12-bit resolution can be enabled with the **HYST** bits in the **CONF** register.

Magnet Detection

As a safety and diagnostic feature, the AS5600L indicates the absence of the magnet. If the measured magnet field strength goes below the minimum specified level (**Bz_ERROR**), the output is driven low, without regard to the **MD** bit in the **STATUS** register is 0.

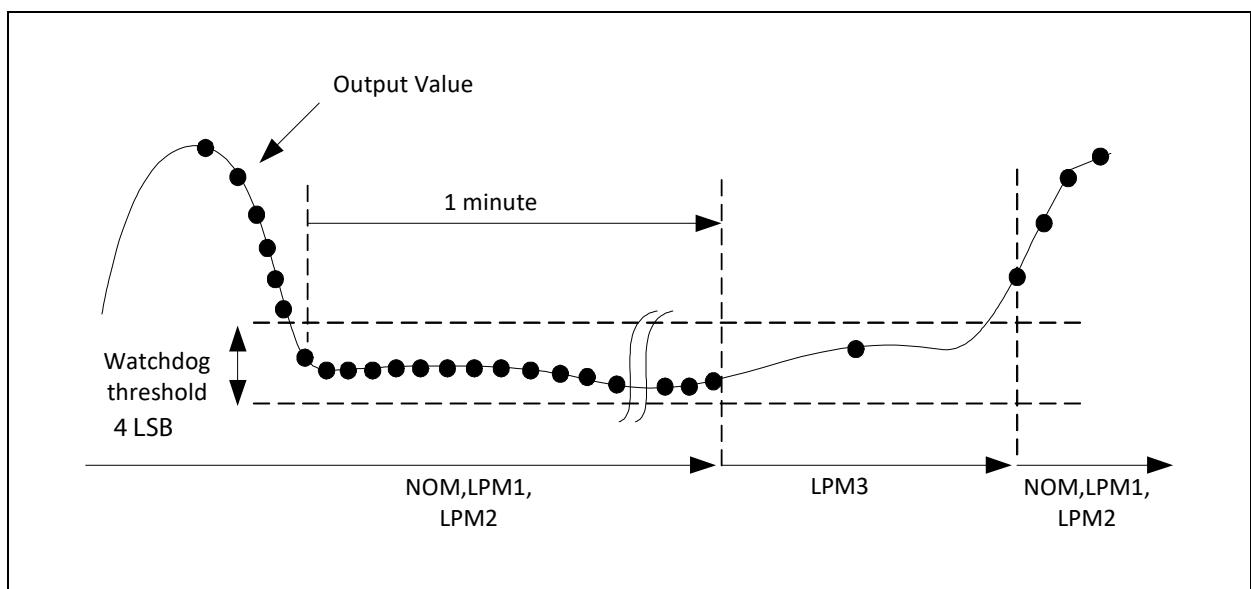
Low Power Modes

A digital state machine automatically manages the low power modes to reduce the average current consumption. Three low power modes are available and can be enabled with the **PM** bits in the **CONF** register. Current consumption and polling times are shown in [Figure 8](#).

Automatic Low Power Mode Timer

The automatic low power mode timer allows saving power by switching into LMP3 if the angle stays within the watchdog threshold of 4 LSB for at least one minute, as shown in [Figure 35](#). The watchdog function can be enabled with the **WD** bit in the **CONF** register.

Figure 35:
Automatic Low Power Mode Timer Function

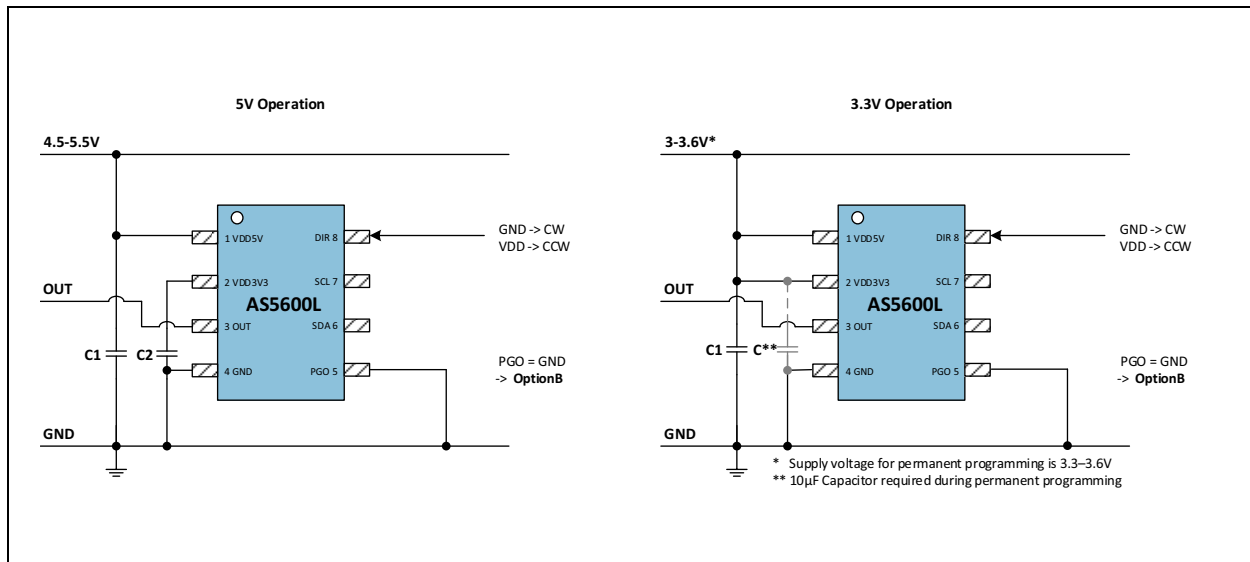


Application Information

Schematic

All required external components are shown below for the reference application diagram. To improve EMC and for remote applications, consider additional protection circuitry.

Figure 36:
Application Diagram for Angle Readout and Programming Through OUT Pin (**Option B**)



Note(s):

1. Consider that the output is driven high by an internal pull-up resistor during programming through the OUT pin. Disconnect additional external load during the programming procedure.

Figure 37:
Application Diagram for Angle Readout and Programming with I²C (**Option A and Option C**)

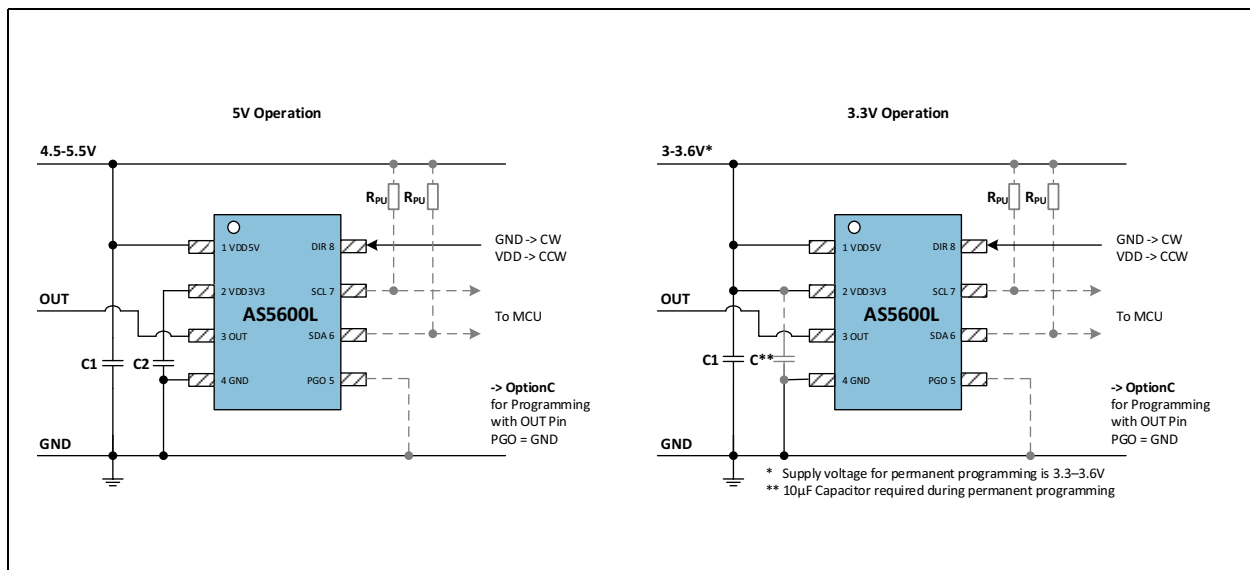


Figure 38:
Recommended External Components

| Component | Symbol | Value | Units | Notes |
|---|--------|-------|-------|--|
| VDD5V buffer capacitor | C1 | 100 | nF | 20% |
| LDO regulator capacitor | C2 | 1 | μF | 20%; < 100 mΩ; Low ESR ceramic capacitor |
| Optional pull-up for I ² C bus | RPU | 4.7 | KΩ | Refer to UM10204 for RPU sizing |

Note(s):

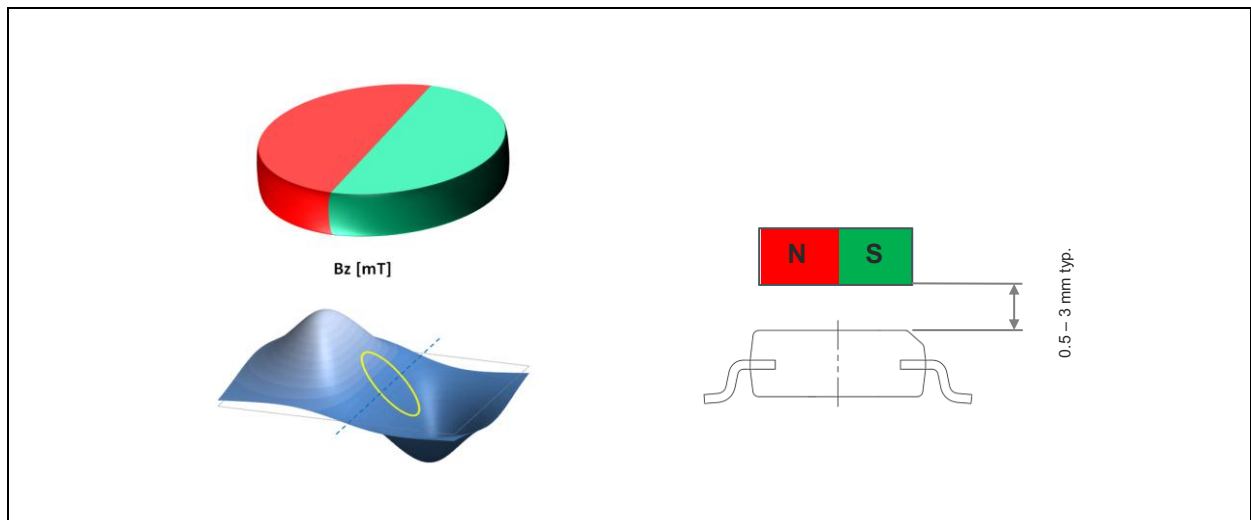
1. Given parameter characteristics have to be fulfilled over operation temperature and product lifetime

Magnetic Requirements

The AS5600L requires the magnetic field component B_z perpendicular to the sensitive area on the chip.

Along the circumference of the Hall element circle the magnetic field B_z should be sine-shaped. The magnetic field gradient of B_z along the radius of the circle should be in the linear range of the magnet to eliminate displacement error by the differential measurement principle.

Figure 39:
Magnetic Field B_z and Typical Airgap

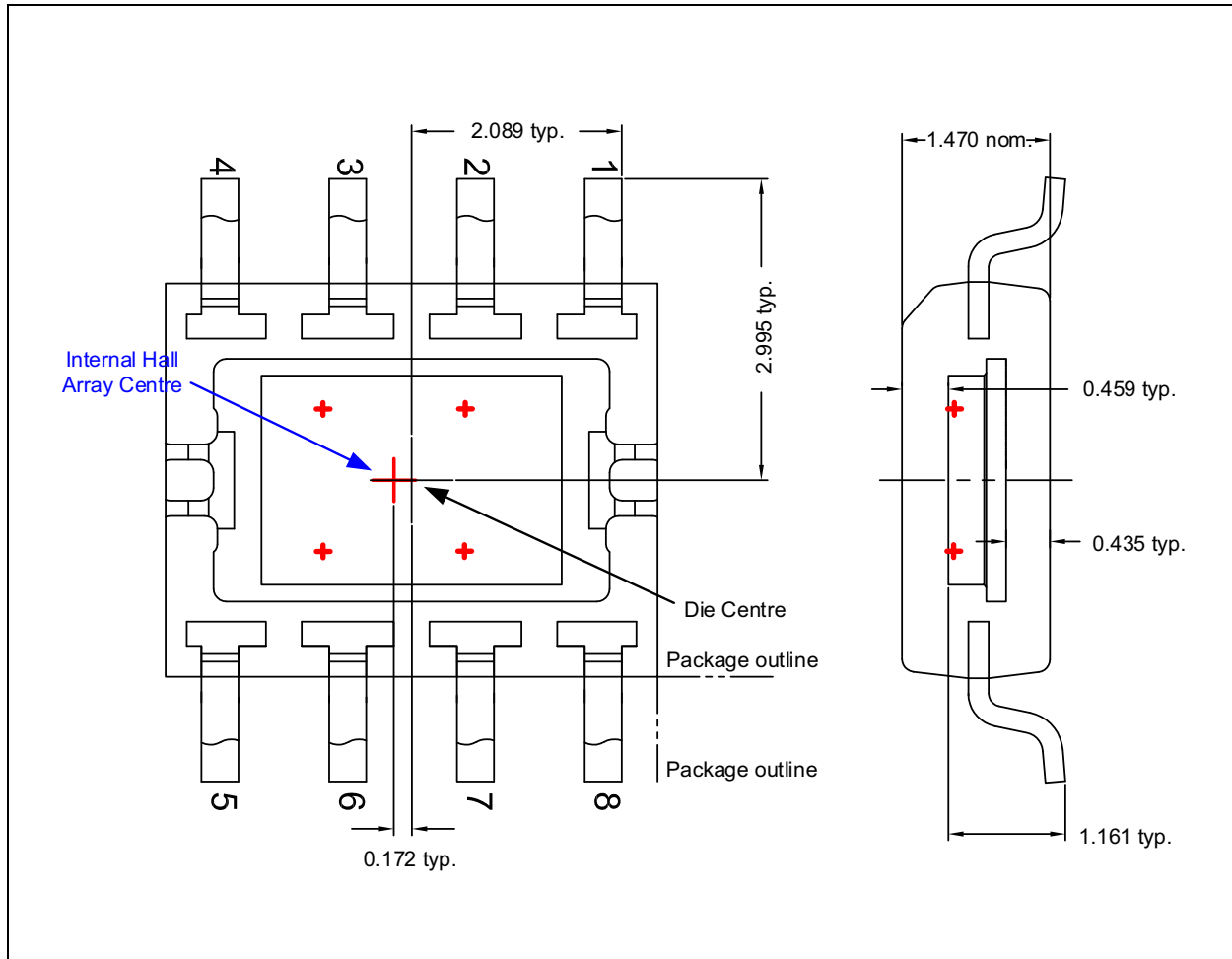


The typical airgap is between 0.5 mm and 3 mm, and it depends on the selected magnet. A larger and stronger magnet allows a larger airgap. Using the AGC value as a guide, the optimal airgap can be found by adjusting the distance between the magnet and the AS5600L so that the AGC value is in the center of its range. The maximum allowed displacement of the rotational axis of the reference magnet from the center of the package is 0.25 mm when using a magnet with a diameter of 6mm.

Mechanical Data

The internal Hall elements are placed on a radius of 1 mm. The center of the internal Hall array is NOT in the center of the package as shown below in Figure 40. The center of the magnet must be placed over the center of the Hall sensor array.

Figure 40:
Hall Element Positions (SOIC-8)

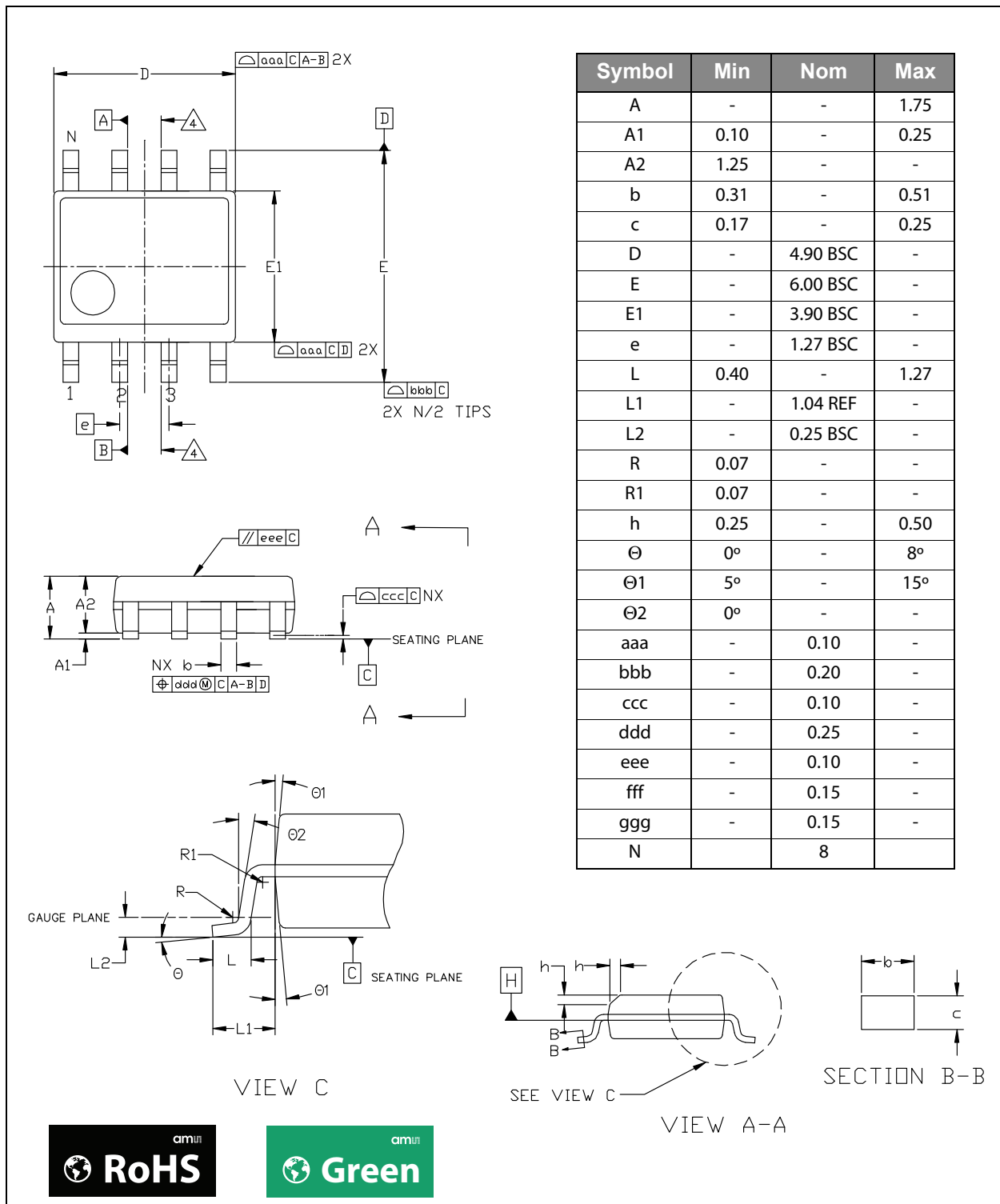


Note(s):

1. All dimensions in mm.

Package Drawings & Markings

Figure 41:
SOIC-8 Package Outline Drawing

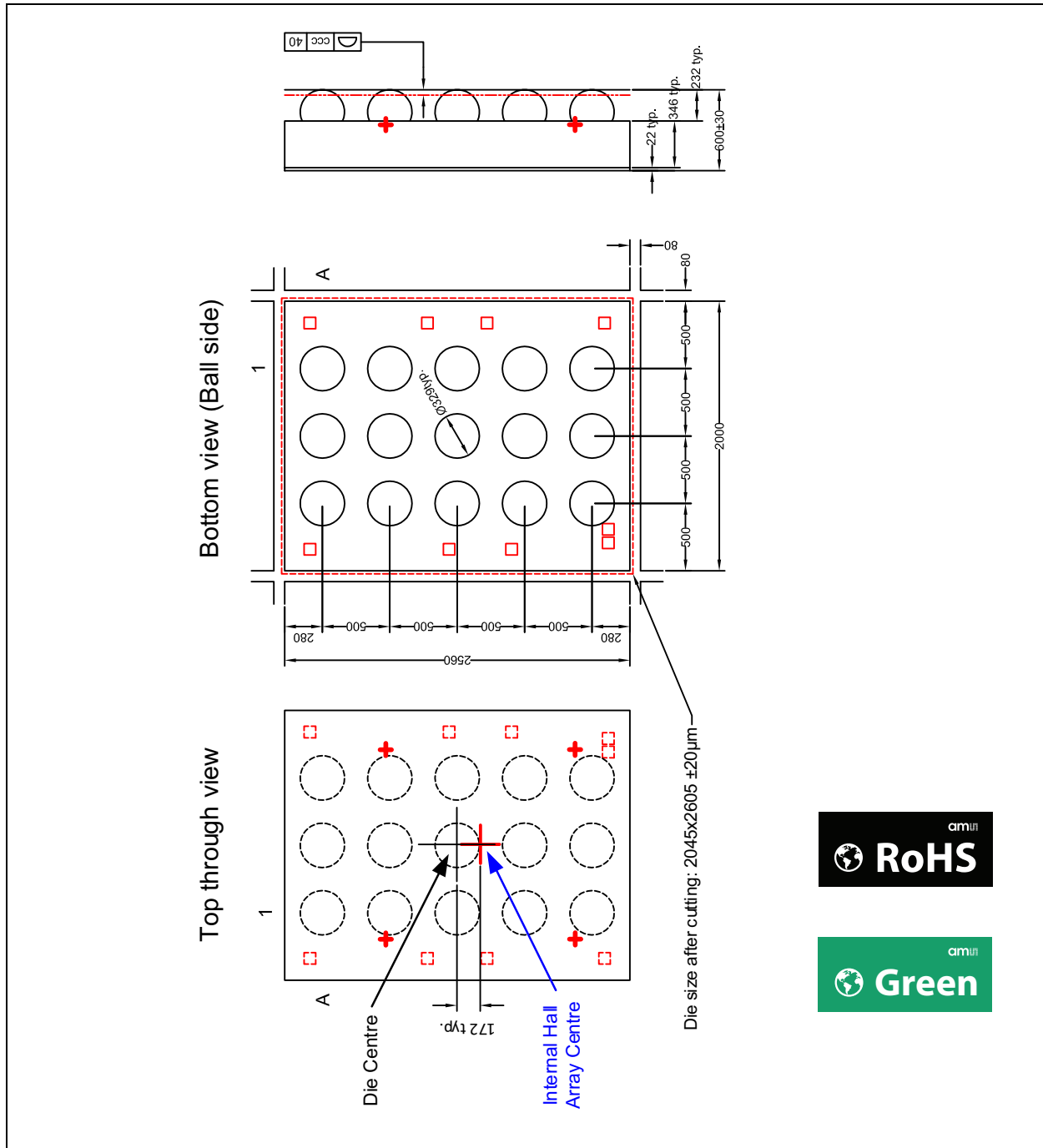


Note(s):

1. Dimensioning & tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. N is the total number of terminals.
4. DATUMS A & B to be determined at DATUM H.

The Wafer Level Chip Scale Package has a dimension of 2.07mm x 2.63mm. Ball pitch is 500µm. The internal Hall elements are placed on a radius of 1 mm. The center of the internal Hall array is NOT in the center of the package as shown in the figure below. The center of the magnet must be placed over the center of the Hall sensor array.

Figure 42:
WL-CSP Package Outline Drawing



Note(s):

1. Pin1=A1
2. ccc coplanarity
3. All dimensions are in µm

The Hall Array center is placed 172.5µm below the center of the chip (with above bonding diagram as reference).

Figure 43:
SOIC-8 Package Marking

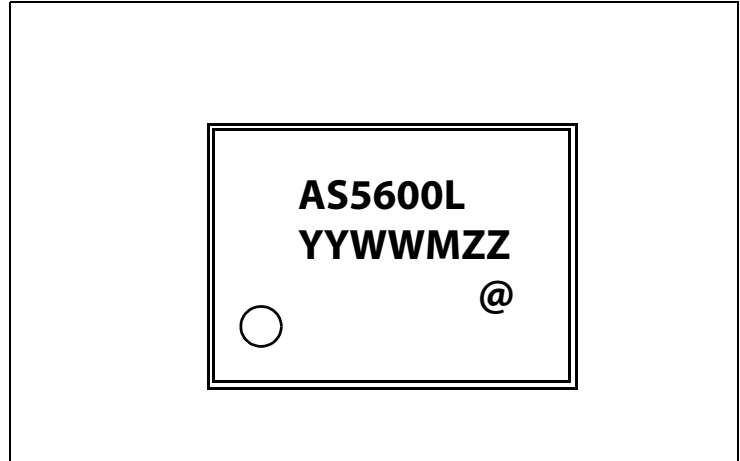


Figure 44:
SOIC-8 Packaging Code

| YY | WW | M | ZZ | @ |
|---|--------------------|------------------|-------------------------------|-------------------|
| Last two digits of the manufacturing year | Manufacturing week | Plant identifier | Free choice/traceability code | Sublot identifier |

Figure 45:
WL-CSP Package Marking

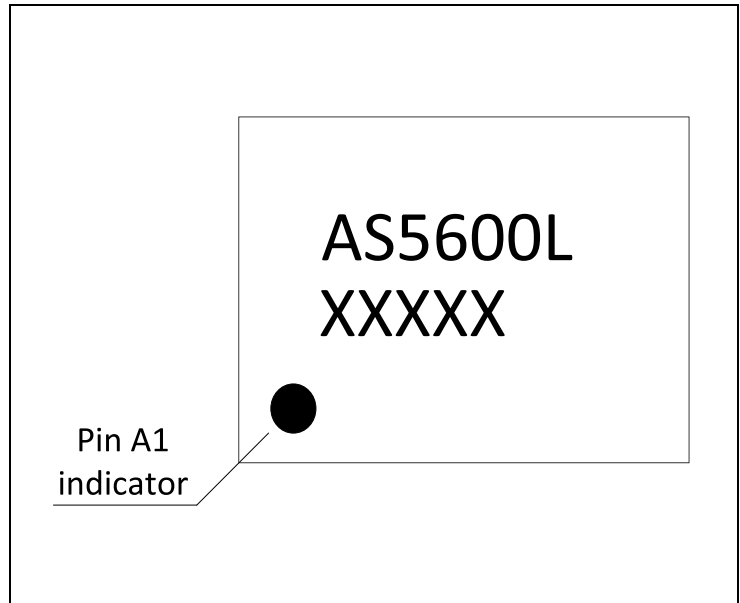


Figure 46:
WL-CSP Packaging Code

| |
|-----------|
| XXXXX |
| Tracecode |

Ordering & Contact Information

Figure 47:
Ordering Information

| Ordering Code | Package | Marking | Delivery Form | Delivery Quantity |
|---------------|---------|---------|-----------------------------|-------------------|
| AS5600L-ASOP | SOIC-8 | AS5600L | 13" Tape & Reel in dry pack | 2500 pcs/reel |
| AS5600L-ASOM | SOIC-8 | AS5600L | 7" Tape & Reel in dry pack | 500 pcs/reel |
| AS5600L-AWLT | WL-CSP | AS5600L | 13" Tape & Reel in dry pack | 6500 pcs/reel |
| AS5600L-AWLM | WL-CSP | AS5600L | 7" Tape & Reel in dry pack | 1000 pcs/reel |

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Document Status

| Document Status | Product Status | Definition |
|--------------------------|-----------------|--|
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Revision Information

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Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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