User Guide

UG000439

AS585X

Standard Board

AS585X-CB-EK-ST

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Content Guide

1 Introduction

The AS585X product family (AS5850, AS5851 and AS5852) is a 16-bit, 256-channel low-noise charge-to-digital converter designed for digital X-ray systems. It enables a wide range of applications for digital X-ray including static and dynamic flat panel detectors (FPDs) used in radiographic imaging, digital mammography and high-speed fluoroscopy.

Each of the devices consists of 256 analog charge sensitive amplifiers (CSA) with a programmable full-scale range, a correlated double sampler (CDS) for offset compensation with programmable time constant and 128 multiplexed analog-to-digital converters (ADC) for the digital readout of each pixel. The device can be configured for electron and hole polarity and includes a voltage reference and a temperature sensor. Built-in diagnostic modes enable error detection in the signal chain.

The converted channels are output on a single LVDS interface with a data rate up to 320 Mbps for optimized line time. The serial SPI interface allows the configuration of the analog frontend including timing and different power modes for low stand-by power consumptions and fast startup times.

AS5850 is a high-speed design, optimized for line times down to 19 µs for dynamic flat panel detectors in fluoroscopy applications. The AS5851 and AS5852, optimized for line times down to 38 µs, 76 µs respectively, are its low-power versions for static, portable, and battery supplied flat panels with minimum power dissipations down to 1.4 mW per channel.

All devices are delivered per default on a Chip on Flex package to minimize sidewall distances and allow direct assembly on the X-ray panel. The Flex design can be customized according to customer requirements. Alternatively, all devices can be delivered as dice on foil.

1.1 AS585X Eval Kit

The AS585X Eval Kit (Eval Kit) is a stand-alone system, which allows the AS585X complete configuration, the measurement of all the relevant parameter (like noise and input linearity) and the connection to an X-Ray photodetector panel.

Two different AS585X samples are included in the Eval Kit in order to perform the complete evaluation:

1. AS585X Chip-on-Board (COB) sample: The AS585X die is directly bonded to the AS585X sample board, which is equipped with the signal generator circuitry. Such circuitry allows the generation of the input signals that emulate the photodetector as on the final application.
2. AS585X Chip-on-Flex (COF) sample: The default package type of the AS585X, where the die is bonded on a flex substrate. Such package allows the direct connection to an X-Ray photodetector panel.

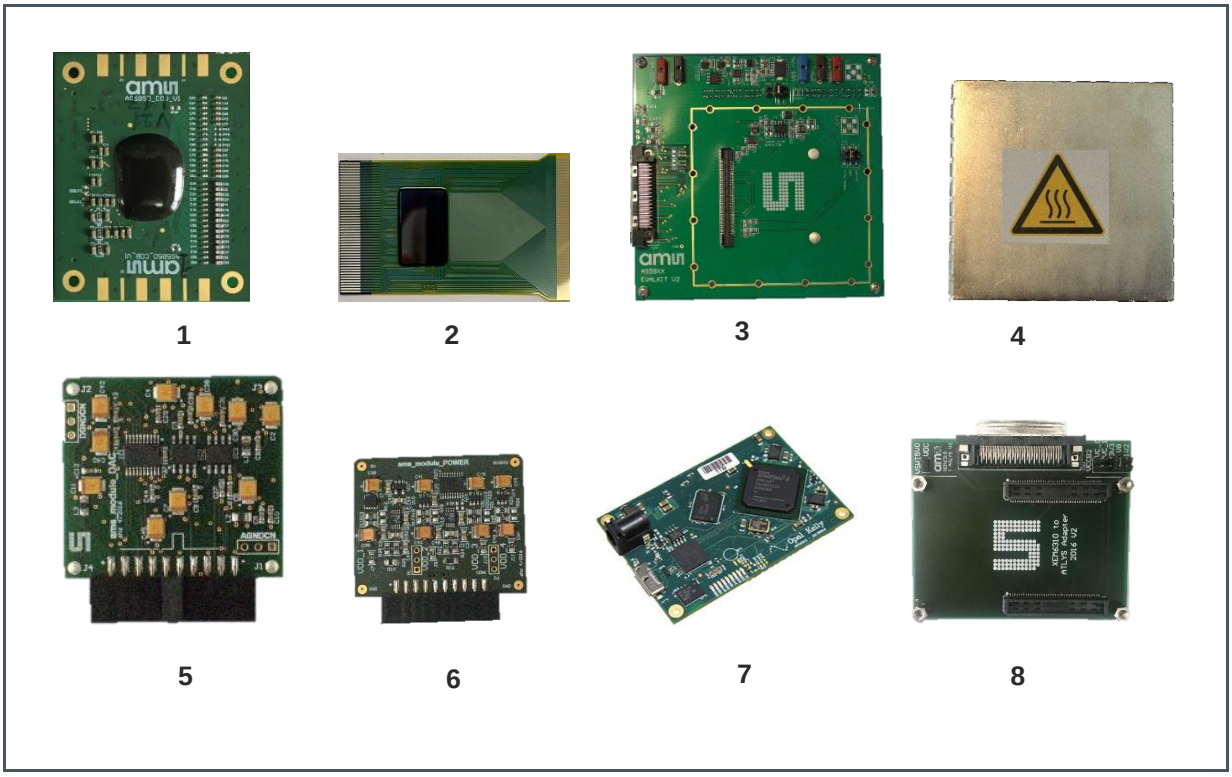
In order to connect the COF to the Base Board, an adapter board is included with the COF pre-assembled.

In the COF the signal generator circuitry is not implemented, therefore it is not possible to stimulate the input channels externally.

An FPGA Module controls the AS585X SPI interface to read and write register values, the AS585X Low-Voltage Differential Signaling (LVDS) interface to transfer the data off-chip, as well as the Eval Kit input signal generator. The FPGA Module is controlled through the AS585X Eval Kit software.

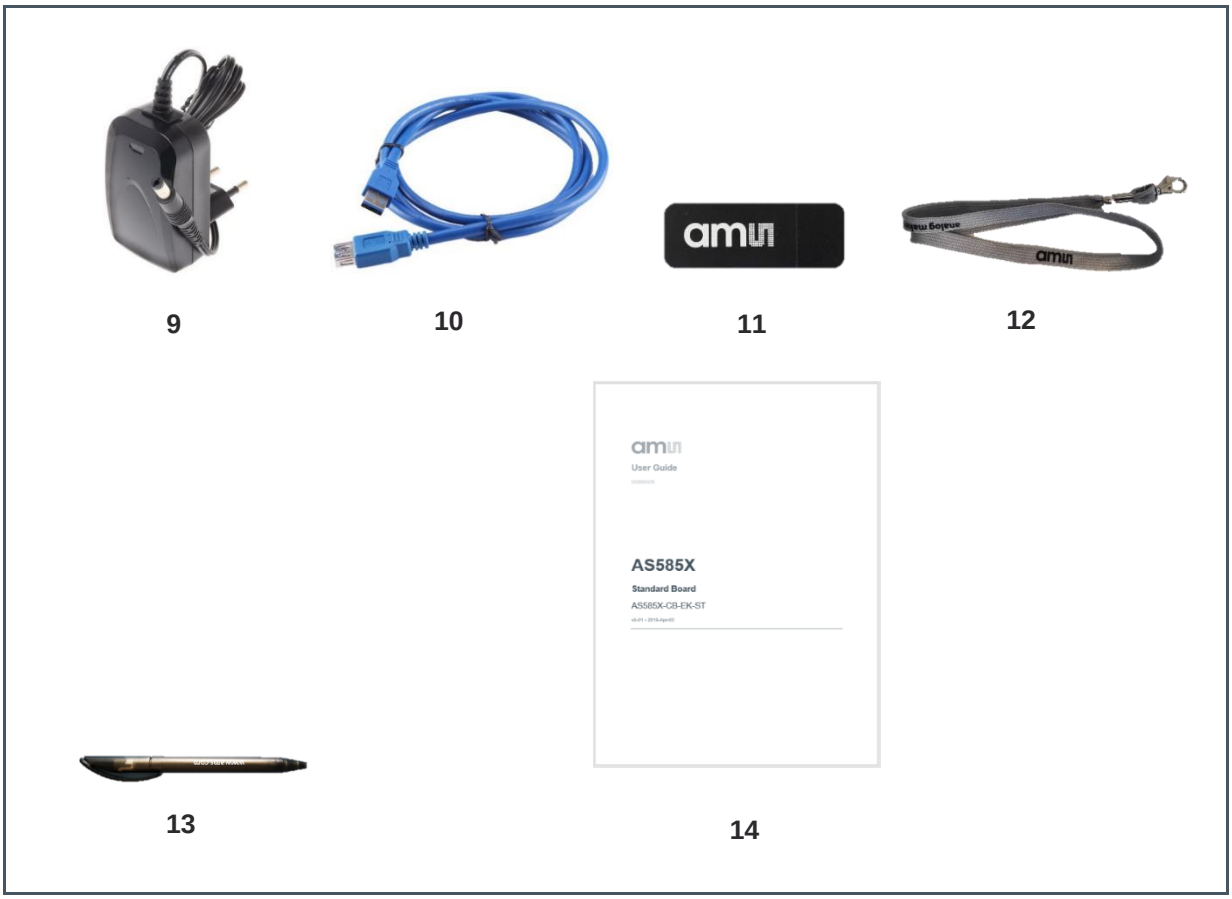
1.2 Eval Kit Content

Figure 1:
Included Components (part 1)



1	1x AS585X Chip-on-Board (COB) Sample Board	**5**	DAC Module
2	1x AS585X Chip-on-Flex (COF) Sample with adapter board	**6**	Power Module
3	AS585X Eval Kit Base Board	**7**	FPGA Board
4	Metallic shield cover	**8**	1x FPGA Adaptor Board

Figure 2:
Included Components (part 2)



9	1x FPGA Power Supply	**12**	1x **ams** neckband
10	1x USB 3.0 Cable	**13**	1x **ams** pen
11	1x USB memory stick with AS585X Eval Kit Software	**14**	1x Eval Kit User Guide

1.3 Ordering Information

Ordering Code	Description
AS585X-CB-EK-ST	AS585X Standard Board

2 Getting Started

2.1 System Requirement

The AS585X Eval Kit software requires Windows 7 SP1 or later and a port USB 3.0.

2.2 Eval Kit Assembly

Attach the Base Board to the FPGA Adapter Board. The FPGA Module is already pre-mounted on the FGPA Adapter Board. The AS585X COB Sample Board is already pre-mounted on the AS585X Eval Kit underneath the shield box. The AS585X COF Sample can be exchanged to the COB one according to the type of measurement to be performed.

Connect the FPGA Module to its 5 V power supply and to a USB 3.0 port with the supplied cable.

The Eval Kit baseboard requires a voltage supply of +5 V provided to the connector “VDD +5 V” as well as a voltage of +8 V and -8 V provided to the connectors “VSS -7 V”, “VDD +7 V”, as shown in Figure 3.

The ±8 V must be provided by an external power supply, while the +5 V voltage can be provided either from an external power supply leaving the jumper on the FPGA adapter open as shown in Figure 3, or directly from the FPGA power supply by simply closing the jumper, as shown in Figure 4. It is important to set the jumper correctly to avoid damages to the Eval Kit.

Figure 3:
Eval Kit Powered by +5 V and ±8 V External Power Supplies

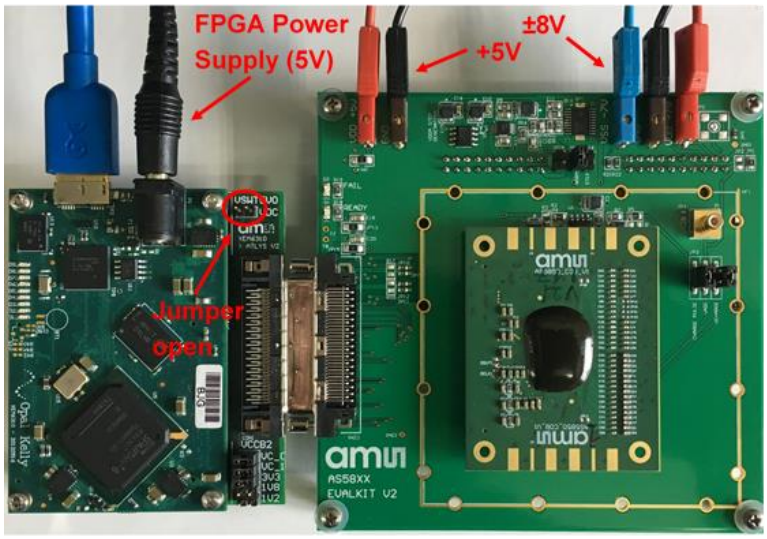
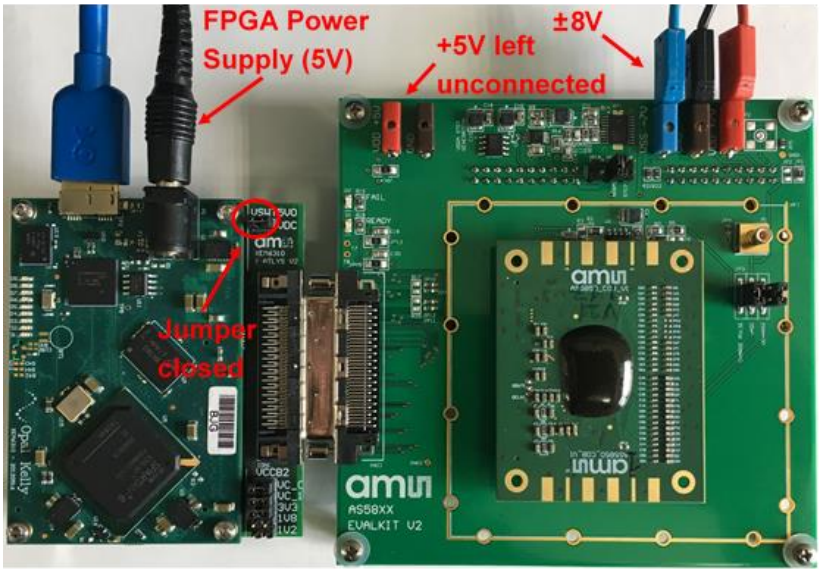


Figure 4:
Eval Kit Powered by ±8 V External Power Supplies and 5 V FPGA Power Supply



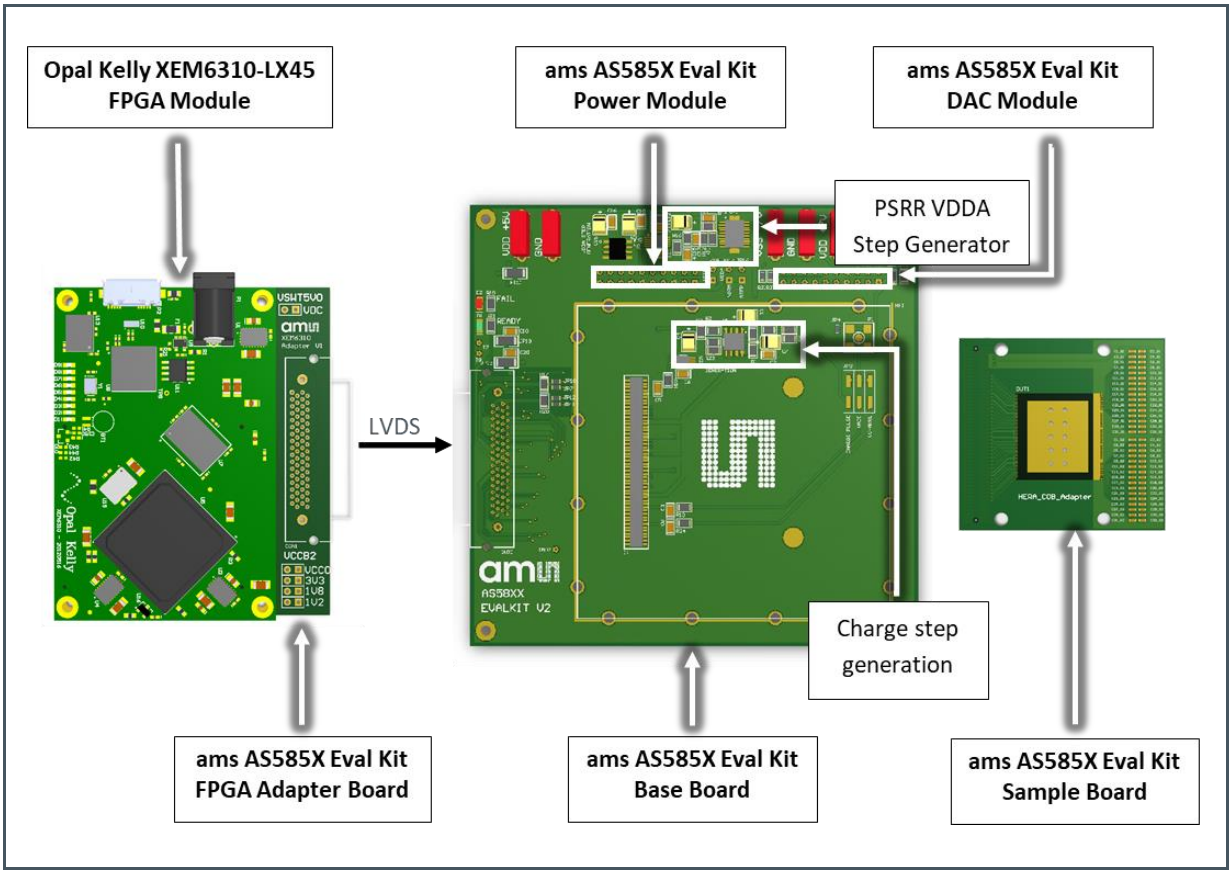
The Eval Kit is shipped with the jumper configured to supply the +5 V from the FPGA Adapter Board. In the default case, where the Eval Kit power is supplied from the FPGA power supply, the connectors VDD +5 V and its correspondent GND must be left unconnected as shown in Figure 4.

Supply the Eval Kit with +5 V (optional), +8 V and -8 V on the 2 mm banana connectors. Use a current limit of 800 mA and switch on all supplies at the same time. Under normal conditions +5 V consumes around 220 mA, +8 V around 70 mA and -8 V around 20 mA.

3 Hardware Description

The Eval Kit is composed of five boards: The Base Board on which an AS585X sample is mounted, an FPGA board and its adapter, a Power Module and a DAC Module.

Figure 5:
AS585X Eval Kit Hardware



3.1 AS585X Eval Kit Base Board

Figure 6:
AS585X Eval Kit Base Board

The Base Board is an interface between the Power Module, DAC Module, the FPGA Module and the Sample Board. It features a VDDA Step Generator and a Charge Pulse Generator circuit, which are used to generate the input signal for the different evaluation modes. Please refer to the detailed description in chapter 6 Evaluation Modes.

3.2 AS585X Eval Kit Power Module

Figure 7:
AS585X Eval Kit Power Module

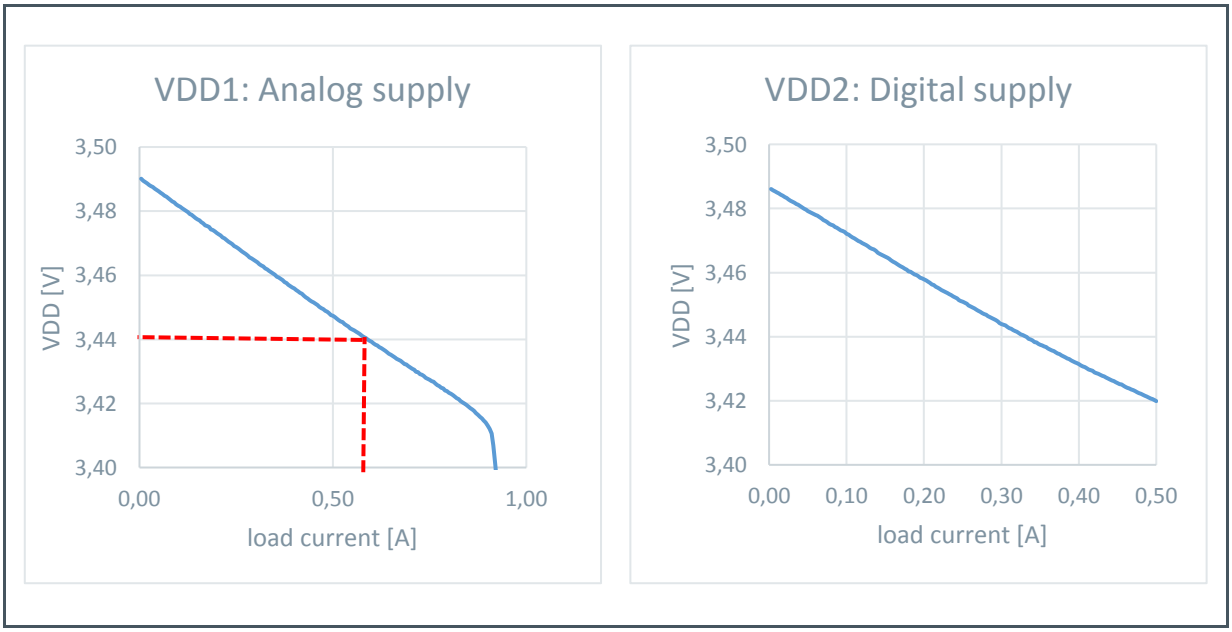
The Power Module is an adjustable voltage power module with 4 outputs, namely VDD1, VDD2, VDD3 and VDD4. VDD1 is used to supply power to the analog AS585X circuitry while VDD2 is used to supply the digital one. VDD1 delivers 1A of load current while other outputs are limited to 0.5 A of load current.

Two on-board shunt resistors are used to measure the VDD1 and VDD2 current consumption of the Power Module, using 16-bit ΔΣ ADCs. The current consumption values in the Eval Kit Software are acquired from the Power Module during power offset calibration and power measurements.

The module performances (voltage drop versus load current, measured at the Power Module output) are shown on the graphs below on a module where both output voltages are trimmed to 3.5 V. The noticeable voltage drop is due to the on-board shunt resistor for the measurement of the current consumption and to the connection to the Base Board, which adds further series resistance.

When the AS585X device is used at maximum power mode (load current = 600 mA), this implies a 50 mV analog voltage supply drop, please refer to the example of the AS585X working point in Figure 8 shown below (red line).

Figure 8:
AS585X Eval Kit Power Module Output Dynamic



3.3 AS585X Eval Kit DAC Module

Figure 9:
AS585X Eval Kit DAC Module

The DAC module is used to generate the input signals for the evaluation of the AS585X.

The DAC Module uses a 20-bit DAC, with an output non-linearity verified to be below ±15 µV over its entire 0 to 5 V range. The non-linearity of the DAC itself is not taken into account and not corrected during the linearity measurement of the AS585X.

3.4 AS585X Eval Kit COB Sample Board

Figure 10:
AS585X Eval Kit COB Sample Board

The AS585X Sample Board is a chip carrier where an AS585X die is bonded.

In the sample board, the channels "41-48, 73-80, 187-194, 219-226" are bonded to 30 pF line capacitors and 3 pF charge capacitors for external charge injection.

In the sample board, the channels “116-123, 148-155” are bonded to 30 pF line capacitors.

The channels "0-40, 49-72, 81-115, 124-147, 156-186, 195-218, 227-255" are not bonded.

A detailed description of the charge generation is explained in chapter 6.4 External Charge Generation (holes)

Figure 11:
AS585X Eval Kit Sample Board Detector Input Schematic Example with Line Capacitor Only (channel 116)

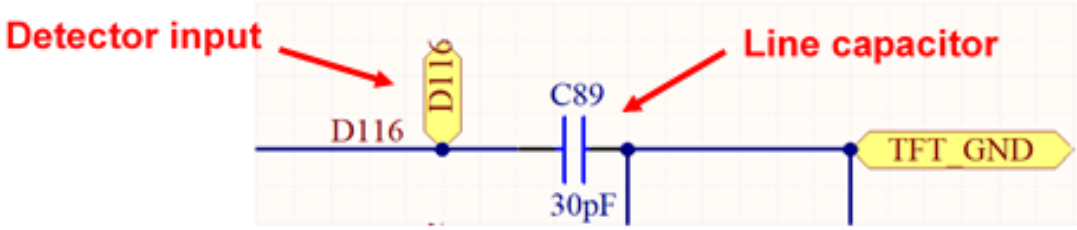
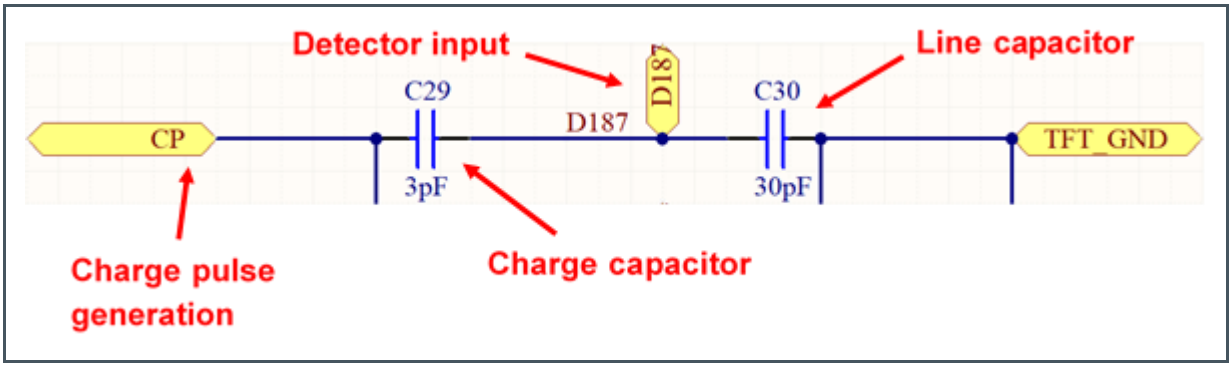


Figure 12:
AS585X Eval Kit Sample Board Detector Input Schematic Example with Both Line Capacitor and Charge Capacitor for Charge Injection (channel 187)



3.5 AS585X Eval Kit COF Sample Board

Figure 13:
AS585X Eval Kit COF Sample with Adapter Board

The Chip-on-Flex is the default package type of the AS585X, where the die is bonded on a flex substrate. Such package allows the direct connection to an X-Ray photodetector panel.

The input channels of the COF package are unconnected; therefore, the external charge generation cannot be performed on this package.

Only the measurement in no charge conditions or with internal charge generation can be performed. Detailed descriptions of such measurements are explained in chapters 6.1 No Charge Generation, 6.2 Internal Charge Generation (holes) and 6.3 Internal Charge Generation (electrons)

3.6 FPGA Board

Figure 14:
OpalKelly XEM6310-LX45

The FPGA used in the AS585X Eval Kit is an Opal Kelly XEM6310-LX45. The AS585X software loads into the FPGA a dedicated firmware, through which the FPGA manages the AS585X digital signals (SPI interface, the LVDS readout, clock generation) and the baseboard circuitry (DAC, Charge Step Generator, PSRR VDDA Step Generation)

4 Software Description

4.1 Software Download

The main software package is distributed upon request from your **ams** representative.

Please contact your **ams** representative and once downloaded the software package, the "AS5850_Eval_SW_v1-0-0.exe" setup wizard needs to be executed.

4.2 Software Installation

Follow the instructions of the wizard to unpack and install the user interface and all required software packages to run the Eval Kit.

The software does not run if no AS585X Eval Kit hardware is connected.

4.3 Getting Started

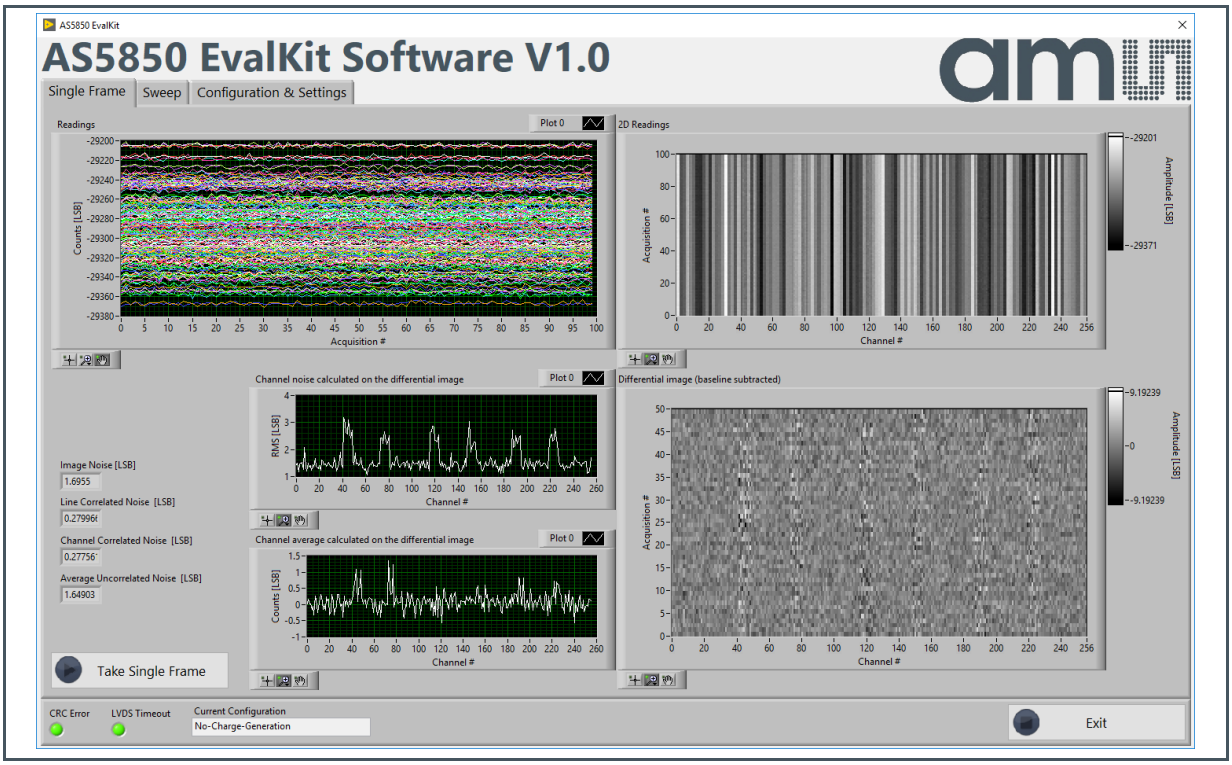
Start the AS585X Eval Kit software using the shortcut ( ) on the desktop. The software should be started with administrator privileges in order to save configuration settings. The windows firewall message can be canceled, as the software does not need access to the internet.

The FPGA's firmware upload starts automatically.

Figure 15:
Start-Up Window

By default, the configuration "No-Charge-Generation_XX_us" is loaded into the device. To check if the software is running correctly press the Take Single Frame button and the following images and plot should be shown on the GUI.

Figure 16:
AS585X Eval Kit Software GUI



4.4 GUI Description

The AS585X GUI is composed of one information panel at the bottom and three tabs at the top:

1. “Single Frame” tab: Is used to acquire images (or single frames) and to evaluate its related noise level.
2. “Sweep” tab: Is used to perform linearity and uniformity measurement. During the sweep measurement, the input signal is swept to evaluate a certain AS585X input range.
3. “Configuration & Setting” tab: Is used to set the measurements parameters, of both “Single Frame” and “Sweep”, and configure the AS585X register map.

4.4.1 Information Panel

The information panel is located at the bottom of the GUI and contains information about the LVDS reading status, the configuration loaded on the AS585X and the exit button.

Figure 17:
Information Panel

Figure 18:
Description of the Information Panel

Control/Indicator	Description
CRC Error	Indicates when a CRC error is detected during an LVDS reading. It is usually green; it becomes red only when CRC error is detected.
LVDS Timeout	Indicates if LVDS reading fails. It is usually green; it becomes red only when the LVDS reading fails.
Current Configuration	Indicates the configuration stored on the AS585X.
Exit	Stop button

4.4.2 "Single Frame" Tab

Figure 19:
Single Frame Tab

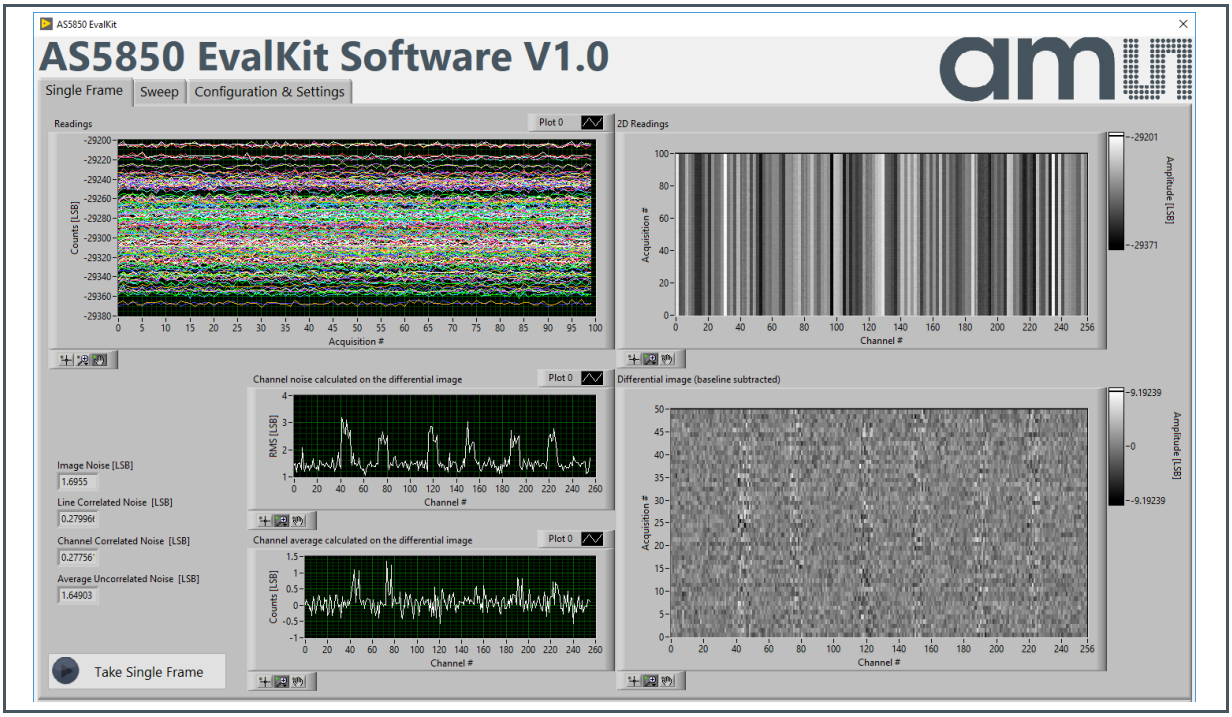


Figure 20:
Description of the Single Frame Tab

Control/Indicator	Description
Take Single Frame	Capture an image
Readings	AS585X LVDS output (counts) in LSB vs. number of samples (consecutive) for all selected channels.
2D Reading	AS585X LVDS output (counts) in LSB represented as intensity (grey scale) for all selected channels (x-axis) and acquired samples (y-axis).
Differential Image	AS585X LVDS output (counts) with baseline subtracted represented as intensity (grey scale) for all selected channels (x-axis) and acquired samples (y-axis). The baseline is subtracted by dividing the acquisition in two halves (split the image in 2 images, first half of the lines and second half the lines) and then the first half is subtracted to the second (first image subtracted to the second image), as described in Equation 1. Without the baseline, the resulting image gives an indication on the correlated noise between the different channels and different lines.
Channel noise calculated on the differential image	Noise in LSB vs. channel number represented by the standard deviation of each channel calculated on the lines of the differential image
Channel average calculated on the differential image	Mean value in LSB vs. channel number represented of each channel calculated on the lines of the differential image
Image Noise [LSB]	Image noise in LSB represented by the standard deviation of the pixels of the differential image
Line Correlated Noise [LSB]	Line correlated noise in LSB represented by the standard deviation on each line of the differential image
Channel Correlated Noise [LSB]	Channel correlated noise in LSB represented by the standard deviation on each channel of the differential image
Average Uncorrelated Noise [LSB]	Square root of the square difference of the Image Noise, Line Correlated Noise, Channel Correlated Noise as described in Equation 2.

Equation 1:

$$Differential\ image = Image\ 1 - Image\ 2$$

Equation 2:

$$Average\ uncorrelated\ noise = \sqrt{Image\ noise^2 - Line\ cor.noise^2 - Channel\ cor.\ noise^2}$$

4.4.3 Sweep Tab

Figure 21:
Sweep Tab

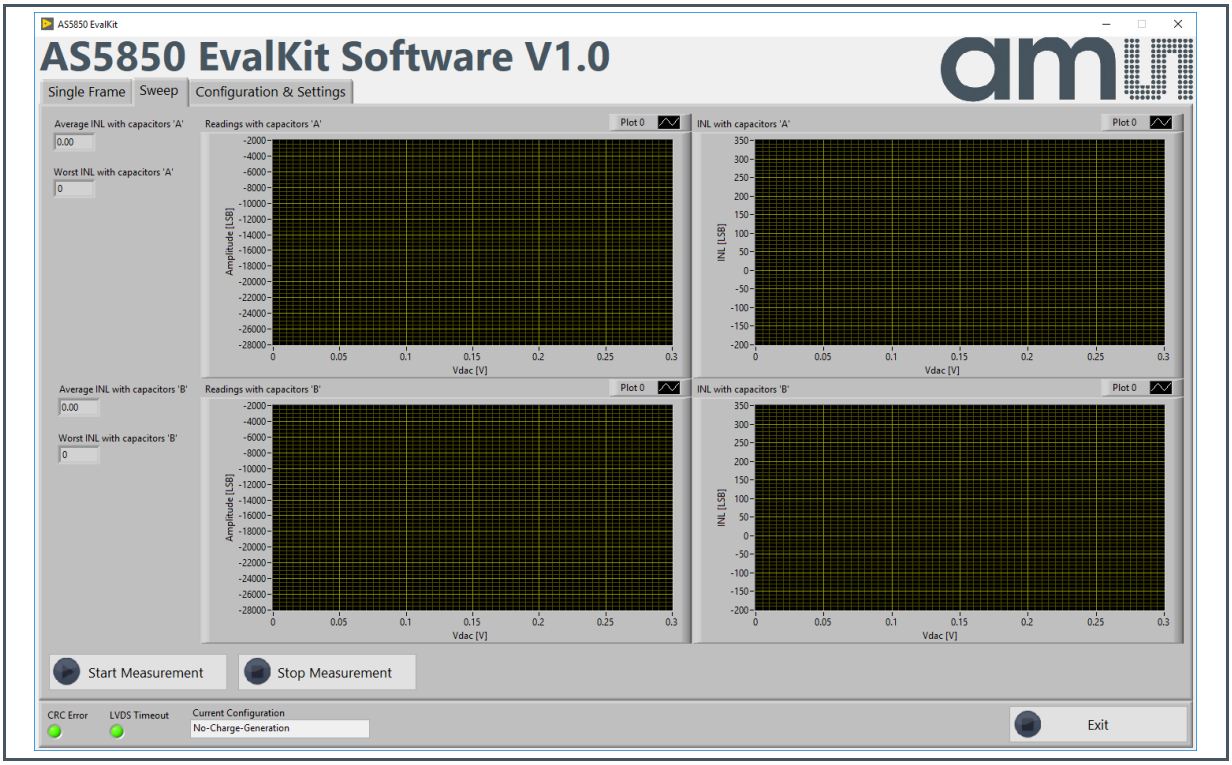


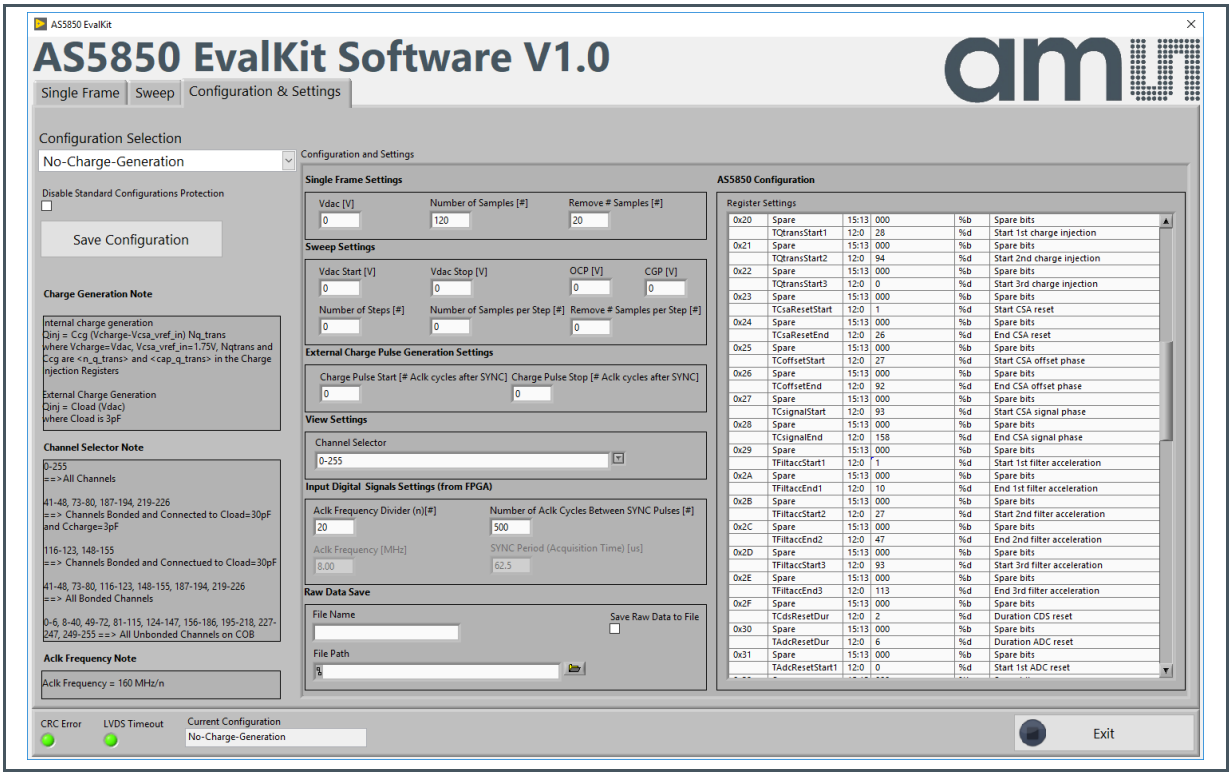
Figure 22:
Description of the Sweep Tab

Control/Indicator	Description/Note
Start Measurement	Start a sweep as defined in the measurement settings.
Stop Measurement	Stop an ongoing sweep.
Readings with capacitors 'A'	AS585X LVDS output from “capacitors A” in LSB vs. DAC voltage. Related input charge can be calculated as described in chapter 5.2 CSA Operation Overview and chapter 6 Evaluation Modes
INL with capacitors 'A'	INL of AS585X for output from “capacitors A” in LSB calculated with fixed point method
Average INL with capacitors 'A'	Maximum INL averaged over selected channels from “capacitors A”
Worst INL with capacitors 'A'	Maximum INL of worst channel from “capacitors A”
Readings with capacitors 'B'	AS585X LVDS output from “capacitors B” in LSB vs. DAC voltage. Related input charge can be calculated as described in chapter 5.2 CSA Operation Overview and chapter 6 Evaluation Modes

Control/Indicator	Description/Note
INL with capacitors 'B'	INL of AS585X for output from “capacitors B” in LSB calculated with fixed point method
Average INL with capacitors 'B'	Maximum INL averaged over selected channels from “capacitors B”
Worst INL with capacitors 'B'	Maximum INL of worst channel from “capacitors B”

4.4.4 Configuration & Setting

Figure 23:
Advanced Settings Window



Configuration Selection

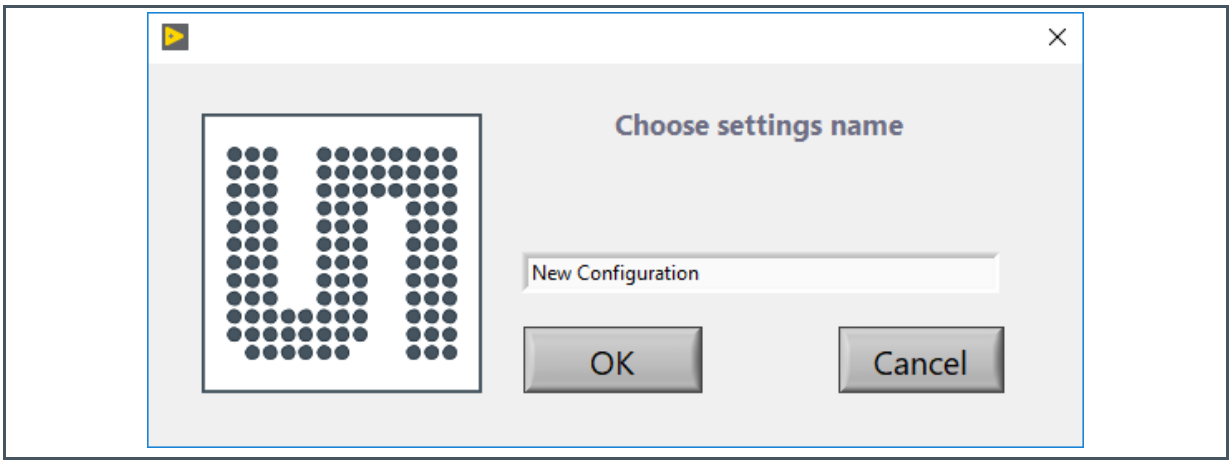
From the “Configuration selection”, it is possible to select the saved configuration. As soon as the configuration is selected, the register map gets loaded on the AS585X.

All the fields on the measurement setting as well as the AS585X register map can be edited.

Save Configuration

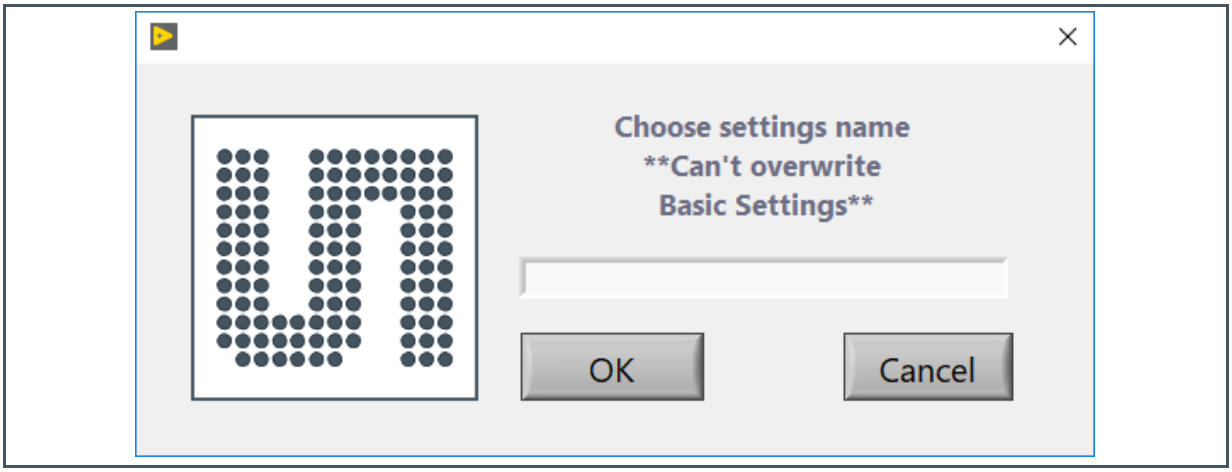
If needed, it is possible to save changes into a new configuration, by pressing on the “Save configuration” button. A window will pop up, asking to type the name of the new configuration

Figure 24:
Configuration Saving Window



In order to prevent the overwriting of the preinstalled configuration, a default configuration protection is enabled; therefore, it is required to choose a configuration name different from the preinstalled configuration ones.

Figure 25:
Preinstalled Protection Window



Disable Standard Configuration Protection

If it is required to edit the preinstalled configurations, it is possible to disable this function by ticking the option “Disable Standard Configuration Protection”, and then typing the same name of the configuration to be edited.

Charge Generation Notes, Channel Selection Notes and ACLK Frequency Note

In this section, some quick explanation notes about the setting can be found.

Single Frame Settings

In this section, settings related to the single frame measurement are located.

Figure 26:
Description of the Single Frame Settings

Function/Control	Description
Vdac [V]	DAC voltage
Number of Samples [#]	Number of samples to acquire in the single frame
Remove # Samples [#]	Number of samples to be ignored before the image acquisition

Sweep Settings

In this section, settings related to the single frame measurement are located.

Figure 27:
Description of the Sweep Settings

Function/Control	Description
Vdac Start [V]	DAC voltage sweep starting value
Vdac Stop [V]	DAC voltage sweep stop value
OCP [V]	Offset correction point for INL calculation with fixed point method
CGP [V]	Gain correction point for INL calculation with fixed point method
Number of Steps [#]	Sweep number of steps
Number of Samples per Step [#]	Number of samples per step
Remove # Samples per Step [#]	Number of samples to be discarded before the acquisition per each step

External Charge Pulse Generation Settings

In this section, settings related to the External Charge Pulse Generation are located.

Figure 28:
Description of the Single Frame Settings

Function/Control	Description
Charge Pulse Start [# ACLK cycles after SYNC]	Number of clock cycles after which the charge step starts, with respect to the start of acquisition (Sync pulse)
Charge Pulse Stop [# ACLK cycles after SYNC]	Number of clock cycles after which the charge step ends, with respect to the start of acquisition (Sync pulse)

View Settings

In this section, settings related to the “Channel Selector” are located. Refer to the note section on the GUI left hand side or to the schematic for a detailed description about the AS585X Sample channels.

Input Digital Signals Settings (from FPGA)

In this section, settings related to the Input Digital Signals Settings (from FPGA) are located.

Figure 29:
Description of the Input Digital Signals Settings (from FPGA)

Function/Control	Description
ACLK Frequency Divider (n)[#]	The FPGA has an internal clock generator at 160 MHz. In order to generate an appropriate ACLK for the AS585X, the FPGA clock frequency is divided. To have an ACLK frequency of 8 MHz, a division factor of 20 is used.
ACLK Frequency [MHz]	ACLK frequency indicator, this value is related to the ACLK Frequency Divider
Number of ACLK Cycles Between SYNC Pulses [#]	Defines the SYNC period. The default value is 500 ACLK cycles, which gives an acquisition time of 62.5 µs at 8 MHz ACLK frequency. The SYNC period must be not less than the acquisition time defined in the AS585X TIME Registers 0x33. Refer to 5.3 Timing section for the complete explanation.
SYNC Period (Acquisition Time) [µs]	Sync frequency indicator, this value is related to the ACLK Frequency Divider and to Number of ACLK Cycles Between SYNC Pulses

AS585X Configuration

In this section, settings related to the “AS585X Configuration” are located, where it is possible to edit the AS585X register map. Refer to Chapter 8 Register Description of the datasheet for the complete description.

Raw Data Save

In this section, settings related to the Raw Data Saving are located. Raw data can be saved in CSV format.

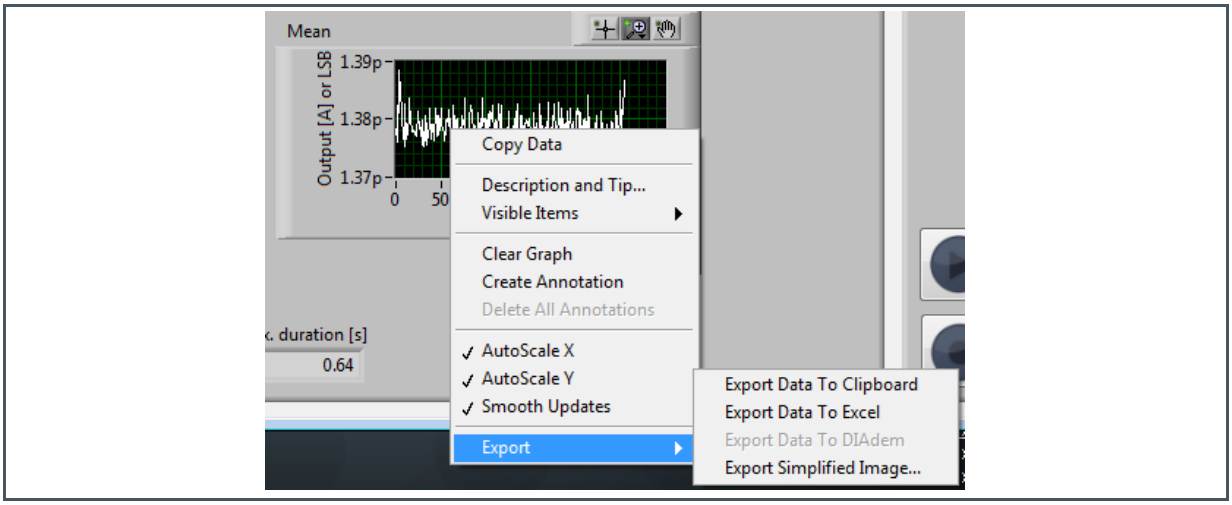
Figure 30:
Description of the Raw Data Save

Function/Control	Description
File Name	Output file name; set the Save Raw Data to File first
File Path	Output file path; set the Save Raw Data to File first
Save Raw Data to File	It enables the data save

As an alternative to the function in the Advanced Setting Window, measurement data can be exported from all of the Eval Kit’s interface graphs to the clipboard and/or to MS Excel.

Right click on a graph, and then select Clipboard or Excel from the Export menu.

Figure 31:
Export Graphs



5 AS585X Operation

5.1 Introduction

In order to evaluate the AS585X performance figures, with the Eval Kit it is possible to emulate the operating condition of the device as if it was connected to an X-ray flat panel detector.

The charge signal from an X-ray flat panel detector can be emulated by generating charge on capacitors connected to AS585X inputs. A charge is generated on a capacitor by applying a voltage step to the capacitor itself.

The charge generated on a capacitor is then transferred to the AS585X and converted into a digital output. Being the charge generated externally to the AS585X, it is called external charge generation (or injection).

The circuitry for the external charge implementation is implemented only in the COB sample.

As described in the Chapter 7.6 Low-Noise Charge-Sensitive Amplifier (CSA) in the datasheet, additional charge can be generated on the internal charge capacitors by the voltages applied to Vcharge and VchargeAux and injected on the CSA. Being the charge generated internally to the AS585X, it is called internal charge generation (or injection).

Internal charge injection is used for:

1. Injecting charge during the offset phase in order to exploit the full input range of AS585X
2. Generating test charge to evaluate the performance of the AS585X in the same way as with the external charge, but without unwanted contributions from external components.

In the Eval Kit, the pin Vcharge is connected to the DAC voltage and the pin VchargeAux is connected to GND.

5.2 CSA Operation Overview

The CSA operation is divided in 3 main phases, namely the reset phase, the offset phase and the signal phase:

1. Reset phase: During this phase, the output voltage of the CSA has the same value as on the CSA_VREF_IN pin (typically 1.75V).
2. Offset phase: A charge (with opposite polarity with respect to the charge which is intended to be converted during the signal phase) is injected at the CSA input to generate a suitable offset voltage for an optimal use of the CSA dynamic range with both charge polarities
3. Signal phase: In this phase, the signal charge is injected to be converted.

Refer to the Chapter 7.6 Low-Noise Charge-Sensitive Amplifier (CSA) in the datasheet for a more complete description.

5.2.1 CSA Dynamic Range

The CSA dynamic input range is defined by

Equation 3:

$$|Q_{SIGNAL}| < \frac{Q_{FULL\_SCALE}}{2} + |Q_{OFFSET}|$$

If no charge is injected during the offset phase, only half of the dynamic range can be exploited. That is the reason why a suitable charge needs to be internally generated and injected during this phase.

The CSA voltage decreases when a positive charge (holes) is injected and vice versa, it increases when a negative charge (electrons) is injected.

Information

In order to have a correct offset correction the polarity of the offset charge must be opposite with respect to the signal one.

5.2.2 Internal Charge Injection

The charge injection from the internal charge generation circuit 1 is described in Equation 4 the same equation applies for the charge generation 2 and 3 as well.

Equation 4:

$$Q_{INJ1} = C_{CG1} \cdot \left(V_{Vcharge\ or\ VchargeAux} - V_{CSA\_VREF\_IN}\right) \cdot N_{Q\_TRANS1}$$

Where

- Q_{INJ1} is the charge injected
- C_{CG1} are the capacitors used for the charge injection and defined in the Charge Injection Register A (Address 0x06) cap_q_trans1
- $V_{VchargeAux}$ or $V_{VchargeAux}$ are the voltages on pins Vcharge or VchargeAux. Charge can be injected from one or the other pin and it is defined in Charge Injection Register A (Address 0x06) pol_q_trans1
- $V_{CSA\_VREF\_IN}$ is 1.75V
- $N_{QTRANS1}$ is the number of charge pulses and it is defined in the Charge Injection Register A (Address 0x06) n_q_trans1

5.2.3 CSA Output Voltage Offset Phase

The CSA output voltage during the offset phase is described in:

Equation 5:

$$V_{CSA\_OFFSET} = V_{CSA\_VREF\_IN} - \left(\frac{Q_{OFFSET}}{C_{FB}}\right)$$

Where

- $V_{CSA\_VREF\_IN}$ is 1.75 V
- C_{FB} is the Feedback capacitance of the CSA and it is defined in the Control Register A (Address 0x02) csa_gain
- Q_{OFFEST} is the charge injected during the offset phase, which is internally generated, (from charge generation 1) therefore

$$Q_{OFFSET} = Q_{INJ1}$$

During the offset phase, only half of the full range charge can be injected as described in Equation 6. A frontend saturation will result if a higher charge is injected.

Equation 6:

$$|Q_{OFFSET}| < \frac{Q_{FULL\_SCALE}}{2}$$

5.2.4 CSA Output Voltage Signal Phase

The CSA output voltage during the signal phase is described in:

Equation 7:

$$V_{CSA\_SIGNAL} = V_{CSA\_OFFSET} - \left(\frac{Q_{SIGNAL}}{C_{FB}}\right)$$

Where

- V_{CSA_OFFSET} the CSA output voltage during the offset phase
- C_{FB} is the Feedback capacitance of the CSA and defined in the Control Register A (Address 0x02) csa_gain
- Q_{SIGNAL} is the charge injected during the signal phase, which can be internally or externally generated

During the signal phase, the charge that can be injected is described in Equation 8.

A frontend saturation will result if a higher charge is injected.

Equation 8:

$$|Q_{SIGNAL}| < \frac{Q_{FULL\_SCALE}}{2} + |Q_{OFFSET}|$$

5.2.5 ADC Digital Output

The charge is now integrated and converted into digital signal as defined in:

Equation 9:

$$Output\ Counts = baseline + \left(\frac{V_{CSA\_OFFSET} - V_{CSA\_SIGNAL}}{ADC\ resolution}\right) \cdot CSA\ Polarity$$

Where

- V_{CSA_SIGNAL} is the CSA output voltage during the signal phase
- V_{CSA_OFFSET} is the CSA output voltage during the offset phase
- baseline is ~-29300 LSB
- ADC resolution is ~40µV/LSB
- CSA Polarity is the polarity selection (electrons or holes) and defined in the Control Register B (Address 0x03) csa_pol. It is +1 for positive charge (holes) and -1 for negative charge:
  - csa_pol=0: Positive charge (holes) → CSA Polarity= +1
  - csa_pol=1: Negative charge (electrons) → CSA Polarity= -1

5.3 Timing

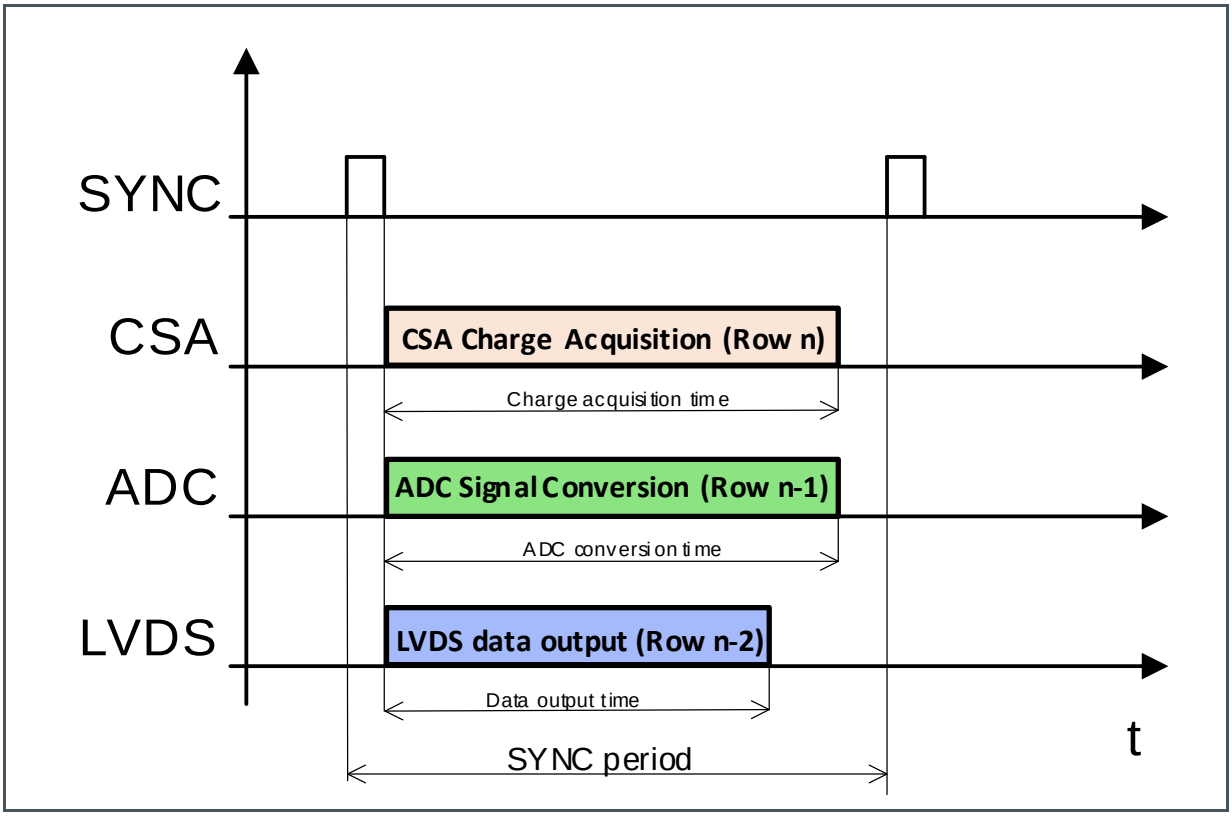
As described in Chapter 7.10.4 Readout Mode 4 – All Parallel of the datasheet, in the AS585X the CSA charge acquisition of row n, the ADC signal conversion of the previous row n-1 and LVDS data output of row n-2 are done in parallel. The user needs to make sure that the LVDS readout of row n- 2 is completed before the ADC conversion of row n-1 is finished.

As the block times (the charge acquisition time, the ADC conversion time and the data output time) may be all different form each other; it is important for a correct operation that the time between SYNC pulses is greater than the slowest AS585X block time.

Equation 10:

$$SYNC\ period \geq Max\ [charge\ acquisition\ time, ADC\ conversion\ time, data\ output\ time]$$

Figure 32:
AS585X Timing Diagram



5.3.1 Charge Acquisition Time and the ADC Conversion Time

The Charge Acquisition Time and the ADC Conversion Time can be chosen according to time and power requirements of the application from the

- Control Register A (Address 0x02) csa_pwr
- Control Register A (Address 0x02) adc_pwr
- Control Register A (Address 0x02) adc_osr

as summarized in Figure 33

Figure 33:
AS585X Minimum Charge Acquisition Time and Minimum ADC Conversion Time

AS585X Version	CSA Power Option <csa_pwr>	Minimum Charge Acquisition Time	ADC Power Option <adc_pwr>	OSR <adc_osr>	Minimum ADC Conversion Time
AS5852	00	76 µs	0	0	38 µs
	00	76 µs	0	1	45 µs
AS5851	00	76 µs	0	0	38 µs
	00	76 µs	0	1	45 µs
	01	38 µs	0	0	38 µs
	01	38 µs	0	1	45 µs
AS5850	00	76 µs	0	0	38 µs
	00	76 µs	0	1	45 µs
	01	38 µs	0	0	38 µs
	01	38 µs	0	1	45 µs
	10	28.5 µs	1	0	19 µs
	10	28.5 µs	1	1	22.5 µs
	11	19 µs	1	0	19 µs
	11	19 µs	1	1	22.5 µs

Information

In this document only the AS5850 and AS5851 time settings are covered.

The AS5852 time register settings can be calculated by doubling the values of the AS5851 ones.

5.3.2 Data Output Time

The Data Output Time depends only on the input LVDS clock frequency and it can be chosen according to time and power requirements of the application.

The maximum allowed LVDS clock frequency is 160 MHz.

Since the minimum value of the Charge Acquisition Time and the ADC Conversion Time is 19 µs at an ACLK frequency of 8 MHz, an LVDS frequency of 115 MHz is sufficient in all possible configuration.

Equation 11:

$$Data\ Output\ Time = \frac{4144}{2 \cdot LVDS\ Clock\ frequency}$$

Where

- 4144 = 259 words (start word + temperature word +256 channels + end word) * 16-bit per word
- Factor 2 because of the dual data rate

Figure 34:
AS585X Data Output Time

LVDS Clock Frequency	Data Output Time
160 MHz	12.95 µs
140 MHz	14.8 µs
115 MHz	18.1 µs
80 MHz	25.9 µs

5.3.3 AS585X TIME Registers (Address 0x20 – 0x33)

The timing management on the AS585X is defined in the Time Registers.

The content of such registers is expressed in number of ACLK cycles after the SYNC.

Information

When the ADC is in low power mode (<adc_pwr>=0), only even values are allowed in the time registers!

Figure 35:
AS585X Allowed Time Registers Values

AS585X Version	ADC Power Option <adc_pwr>	Minimum ADC Conversion Time	Allowed Time Register Values
AS5851 and AS5852	0	38 µs	Even
AS5850	1	19 µs	Odd and Even

Figure 36:
Example: TIME Registers (Address 0x20 – 0x33) Content of the Configuration "Internal-Charge-Generation-Holes_20_us"

Address	Name	Bit	Value	Format	Description
0x20	Spare	15:13	000	%b	Spare bits
	TQtransStart1	12:0	28	%d	Start 1st charge injection
0x21	Spare	15:13	000	%b	Spare bits
	TQtransStart2	12:0	94	%d	Start 2nd charge injection
0x22	Spare	15:13	000	%b	Spare bits
	TQtransStart3	12:0	0	%d	Start 3rd charge injection
0x23	Spare	15:13	000	%b	Spare bits
	TCsaResetStart	12:0	1	%d	Start CSA reset
0x24	Spare	15:13	000	%b	Spare bits
	TCsaResetEnd	12:0	26	%d	End CSA reset
0x25	Spare	15:13	000	%b	Spare bits
	TCoffsetStart	12:0	27	%d	Start CSA offset phase
0x26	Spare	15:13	000	%b	Spare bits
	TCoffsetEnd	12:0	92	%d	End CSA offset phase
0x27	Spare	15:13	000	%b	Spare bits
	TCsignalStart	12:0	93	%d	Start CSA signal phase
0x28	Spare	15:13	000	%b	Spare bits
	TCsignalEnd	12:0	158	%d	End CSA signal phase
0x29	Spare	15:13	000	%b	Spare bits
	TFiltaccStart1	12:0	1	%d	Start 1st filter acceleration
0x2A	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd1	12:0	10	%d	End 1st filter acceleration
0x2B	Spare	15:13	000	%b	Spare bits
	TFiltaccStart2	12:0	27	%d	Start 2nd filter acceleration
0x2C	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd2	12:0	47	%d	End 2nd filter acceleration
0x2D	Spare	15:13	000	%b	Spare bits
	TFiltaccStart3	12:0	93	%d	Start 3rd filter acceleration
0x2E	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd3	12:0	113	%d	End 3rd filter acceleration
0x2F	Spare	15:13	000	%b	Spare bits
	TCdsResetDur	12:0	2	%d	Duration CDS reset
0x30	Spare	15:13	000	%b	Spare bits
	TAdcResetDur	12:0	6	%d	Duration ADC reset
0x31	Spare	15:13	000	%b	Spare bits
	TAdcResetStart1	12:0	0	%d	Start 1st ADC reset
0x32	Spare	15:13	000	%b	Spare bits
	TAdcResetStart2	12:0	80	%d	Start 2nd ADC reset
0x33	Spare	15:13	000	%b	Spare bits
	Tacq	12:0	160	%d	End line acquisition (line time)

Acquisition Time

Information

The minimum acquisition time is to be considered an absolute minimum and it is not recommended to be used as typical case, unless explicitly required by the application.

When possible it is recommended to use typical timing setting.

By using typical timing settings an AS5850 configuration is optimized for 20 µs line time and it is used as use case for this document.

A detailed description of the acquisition time setting is described in “Minimum Acquisition Time” and “Recommended Acquisition Time” in page 42.

The acquisition time or line time is defined in

- Time Register A (Address 0x33) t_acquisition

The minimum line time of 19 µs at an ACLK frequency of 8 MHz, which corresponds to 152 ACLK cycles, which can only be achieved when both CSA and ADC are configured in high power mode (<csa_pwr>=11, <adc_pwr>=1).

In general, the acquisition time needs to fulfil the following condition

Equation 12:

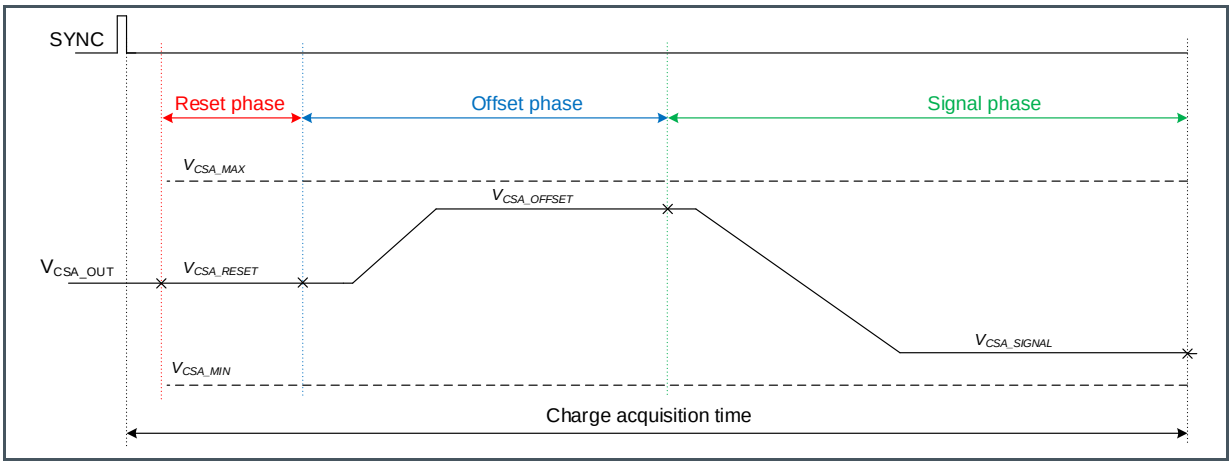
$$Acquisition\ time \geq Max\ [Charge\ acquisition\ time, ADC\ conversion\ time]$$

Figure 37:
AS585X Acquisition Time

AS585x Version	ADC Power Option <adc_pwr>	Minimum ADC Conversion Time	Min Acquisition Time	Typ Acquisition Time	Max Acquisition Time
AS5851	0	38 µs	304 ACLK cycles	320 ACLK cycles	
AS5850	1	19 µs	152 ACLK cycles	160 ACLK cycles	

Main CSA Phases

Figure 38:
AS585X CSA Phases



The timings of the 3 main CSA phases are defined in

- Time Register D (Address 0x23) t_csareset_start
- Time Register E (Address 0x24) t_csareset_end
- Time Register F (Address 0x25) t_offset_start
- Time Register G (Address 0x26) t_offset_end
- Time Register H (Address 0x27) t_signal_start
- Time Register I (Address 0x28) t_signal_end

It is important that the CSA reset start at least after 1 ACLK cycle and to leave 1 ACLK cycle between each phase when the ADC is in high power mode (<adc_pwr>=1). These values must be doubled when the ADC is in low power mode (<adc_pwr>=0).

Figure 39:
AS585X CSA Reset Start

AS585X Version	ADC Power Option <adc_pwr>	Minimum ADC Conversion Time	Min CSA Reset Start	Typ CSA Reset Start	Max CSA Reset Start
AS5851	0	38 µs	2 ACLK cycles	2 ACLK cycles	2 ACLK cycles
AS5850	1	19 µs	1 ACLK cycles	1 ACLK cycles	1 ACLK cycles

Figure 40:
AS585X Time Between CSA Phases

AS585X Version	ADC Power Option <adc_pwr>	Minimum ADC Conversion Time	Min Time Between Phases	Typ Time Between Phases	Max Time Between Phases
AS5851	0	38 µs	2 ACLK cycles	2 ACLK cycles	2 ACLK cycles
AS5850	1	19 µs	1 ACLK cycles	1 ACLK cycles	1 ACLK cycles

Figure 41:
Example: Register Map of the Configuration "Internal-Charge-Generation-Holes_20_us"

Parameter	Register	Value
Start CSA reset	t_csareset_start	1 ACLK Cycles
End CSA reset	t_csareset_end	26 ACLK Cycles
Start CSA offset phase	t_offset_start	27 ACLK Cycles
End CSA offset phase	t_offset_end	92 ACLK Cycles
Start CSA signal phase	t_signal_start	93 ACLK Cycles
End CSA signal phase	t_signal_end	158 ACLK Cycles

Internal Charge Injection

The charge injection timings of the 3 circuits are defined in

- Time Register A (Address 0x20) t_qtrans_start1
- Time Register B (Address 0x21) t_qtrans_start2
- Time Register C (Address 0x22) t_qtrans_start3

It is recommended to inject the charge 1 ACLK cycle after the start of the phase where the charge is intended to be injected when the ADC is in high power mode (<adc_pwr>=1). These values must be doubled when the ADC is in low power mode (<adc_pwr>=0).

In the example below, the Charge Injection A is used on the offset phase, the Charge Injection B is used on the signal phase and the Charge Injection C is not used.

Figure 42:
AS585X CSA Phases with Internal Charge Injection

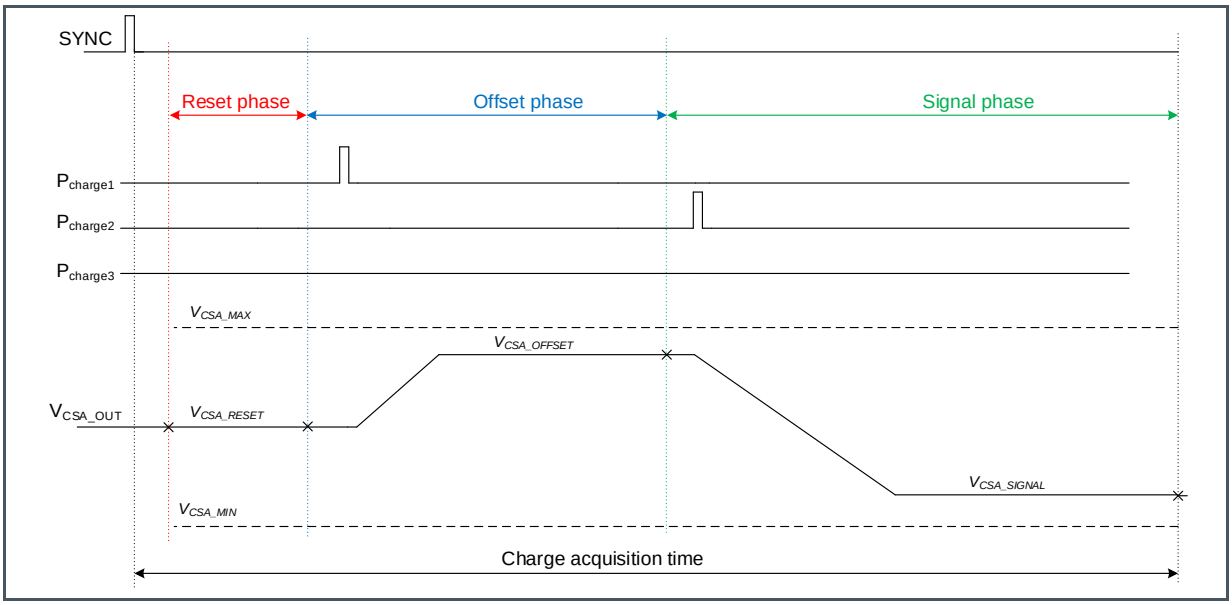
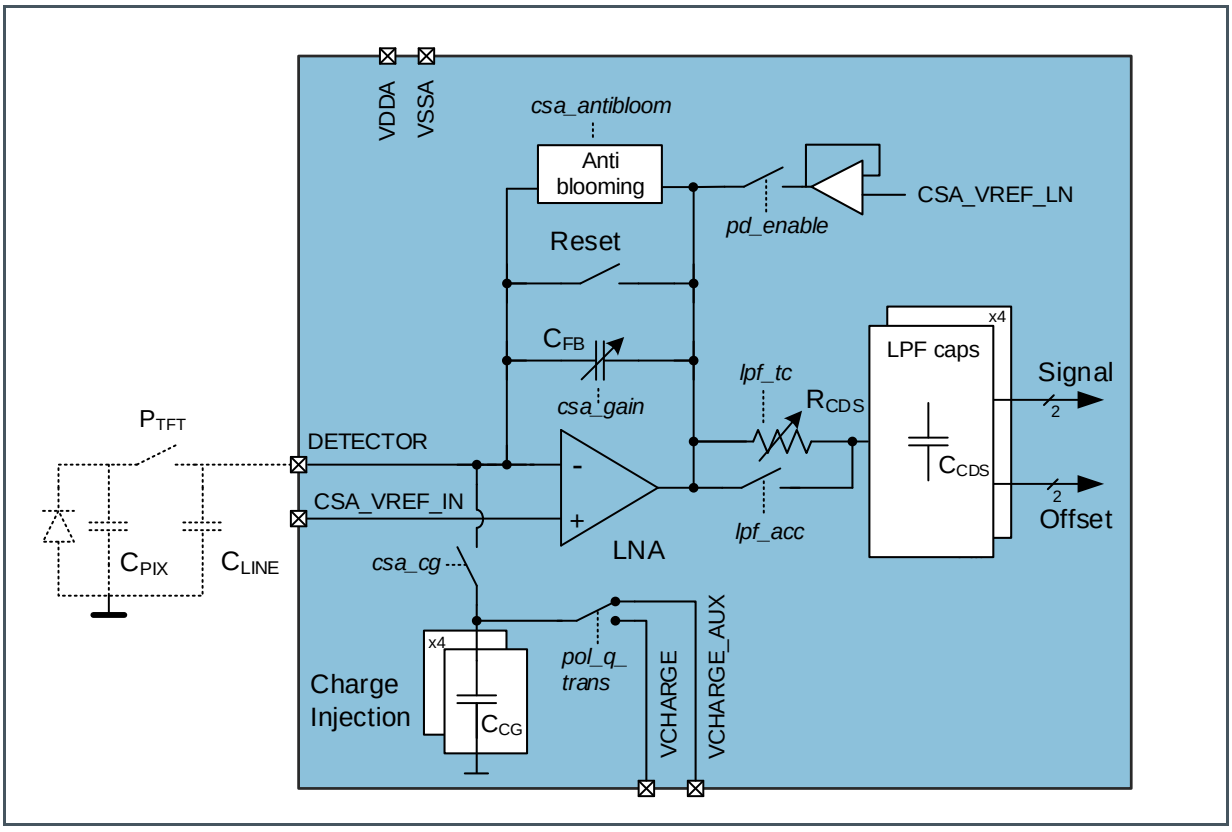


Figure 43:
Example: Register Map of the Configuration "Internal-Charge-Generation-Holes_20_us"

Parameter	Register	Value
Start 1st charge injection	t_qtrans_start1	28 ACLK Cycles
Start 2nd charge injection	t_qtrans_start2	94 ACLK Cycles
Start 3rd charge injection	t_qtrans_start3	0 ACLK Cycles

Filter Acceleration

Figure 44:
AS585X Functional Diagram



In the AS585X, the CSA output is fed into the low-pass filter. The filter time constant can be configured by changing the resistor value on bits <lpf_tc>. For fast settling, a filter acceleration circuit, which shortens the resistor by setting <lpf_acc> to logic 1 is implemented.

The filter acceleration circuit can be activated 3 times; one for each of the main CSA phases, and it is defined in

- Time Register J (Address 0x29) t_filtacc_start1
- Time Register K (Address 0x2A) t_filtacc_end1
- Time Register L (Address 0x2B) t_filtacc_start2
- Time Register M (Address 0x2C) t_filtacc_end2
- Time Register N (Address 0x2D) t_filtacc_start3
- Time Register O (Address 0x2E) t_filtacc_end3

It is recommended to start the filter acceleration simultaneously with the corresponding phase and let it last around 10-20 ACLK cycles, when the ADC is in high power mode (<adc_pwr>=1). These values must be doubled when the ADC is in low power mode (<adc_pwr>=0).

In case of longer acceleration phases, it is anyhow recommended to leave several ACLK cycles between the end of the acceleration and the end of its correspondent phase.

Figure 45:
AS585X Delay between CSA Phase Start and Filter Acceleration

AS585X Version	ADC Power Option <adc_pwr>	Min Delay Between CSA Phase Start and Filter Acceleration	Typ Delay Between CSA Phase Start and Filter Acceleration	Max Delay Between CSA Phase Start and Filter Acceleration
AS5851	0	0 ACLK cycles	0 ACLK cycles	0 ACLK cycles
AS5850	1	0 ACLK cycles	0 ACLK cycles	0 ACLK cycles

Figure 46:
AS585X Filter Acceleration Duration

AS585X Version	ADC Power Option <adc_pwr>	Min Filter Acceleration Duration	Typ Filter Acceleration Duration	Max Filter Acceleration Duration
AS5851	0		20-40 ACLK cycles	
AS5850	1		10-20 ACLK cycles	

Figure 47:
Example: Register Map of the Configuration “Internal-Charge-Generation-Holes_20_us”

Parameter	Register	Value
Start 1st filter acceleration	t_filtacc_start1	1 ACLK Cycle
Stop 1st filter acceleration	t_filtacc_end1	10 ACLK Cycles
Start 2nd filter acceleration	t_filtacc_start2	27 ACLK Cycles
Stop 2nd filter acceleration	t_filtacc_end2	47 ACLK Cycles
Start 3rd filter acceleration	t_filtacc_start1	93 ACLK Cycles
Stop 3rd filter acceleration	t_filtacc_end1	113 ACLK Cycles

CDS Reset Duration

The CDS reset duration is defined in

- Time Register P (Address 0x2F) t_adcreset_dur

The absolute minimum duration is 1 ACLK cycle but 2 ACLK cycles are recommended when the ADC is in high power mode (<adc_pwr>=1). These values must be doubled when the ADC is in low power mode (<adc_pwr>=0).

The CDS reset phases start at the same time as the ADC reset phases, as defined in

- Time Register R (Address 0x31) t_adcreset_start1
- Time Register S (Address 0x32) t_adcreset_start2

As described in paragraph 5.3.3 ADC/CDS Reset Start and Stop.

Figure 48:
AS585X CDS Reset Duration

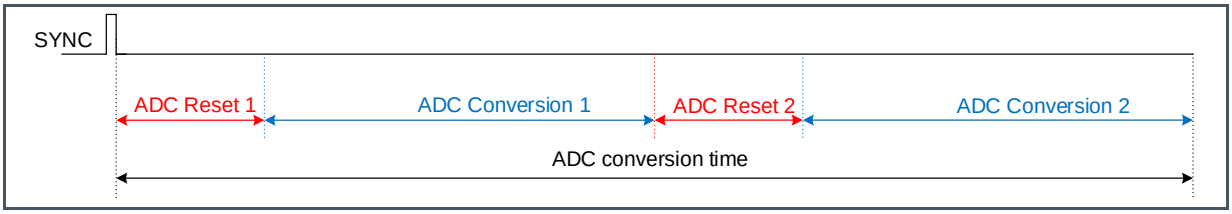
AS585X Version	ADC Power Option <adc_pwr>	Min CDS Reset Duration	Typ CDS Reset Duration	Max CDS Reset Duration
AS5851	0	2 ACLK cycles	4 ACLK cycles	
AS5850	1	1 ACLK cycles	2 ACLK cycles	

Figure 49:
Example: Register Map of the Configuration “Internal-Charge-Generation-Holes_20_us”

Parameter	Register	Value
CDS reset duration	t_adcreset_dur	2 ACLK Cycle

ADC Reset and Conversion

Figure 50:
AS585X ADC Phases



Each AS585X ADC does the sequential acquisition of two channels; therefore, during the conversion time two reset phases and two conversion phases take place.

As described in the Chapter 7.8 Analog to Digital Converter (ADC) of the datasheet, the ADC conversion phase is defined by the oversampling ratio (OSR) in:

- Control Register A (Address 0x02) adc_osr

and it can be chosen between two discrete values, 74 and 88. This corresponds to 74 or 88 ACLK cycles when <adc_pwr>=1 and 148 or 176 ACLK cycles respectively when <adc_pwr>=0.

Figure 51:
AS585X ADC Conversion Time

AS585x Version	ADC Power Option <adc_pwr>	OSR <adc_osr>	ADC Conversion
AS585X	0	0	148 ACLK cycles
AS585X	0	1	176 ACLK cycles
AS5850	1	0	74 ACLK cycles
AS5850	1	1	88 ACLK cycles

Concerning the ADC reset phase, when the ADC is in high power mode (<adc_pwr>=1) its absolute minimum duration is at least 1 ACLK cycle longer than CDS reset duration. The recommended duration is 6 ACLK cycles. These values must be doubled when the ADC is in low power mode (<adc_pwr>=0).

Equation 13:

$$ADC\ reset\ duration \geq CDS\ reset\ duration + 1$$

Figure 52:
AS585X ADC Reset Duration

AS585x Version	ADC Power Option <adc_pwr>	Min ADC Reset Duration	Typ ADC Reset Duration	Max ADC Reset Duration
AS585X	0	4 ACLK cycles	12 ACLK cycles	
AS5850	1	2 ACLK cycles	6 ACLK cycles	

ADC/CDS Reset Start and Stop

The ADC reset phases start are defined in

- Time Register R (Address 0x31) t_adcreset_start1
- Time Register S (Address 0x32) t_adcreset_start2

These registers control the CDS reset start as well.

The ADC reset 1 should start at the beginning of the acquisition and the ADC reset 2 should start right after the first conversion is finished

Equation 14:

$ADC\ reset\ start\ 2 \geq ADC\ reset\ start\ 1 + ADC\ reset\ duration + ADC\ conversion$ (From Figure 51)

Figure 53:
Example: Register Map of the Configuration "Internal-Charge-Generation-Holes_20_us"

Parameter	Register	Value
ADC reset duration	t_adcreset_dur	6 ACLK Cycle
ADC reset start 1	t_adcreset_start1	0 ACLK Cycle
ADC reset start 2	t_adcreset_start2	80 ACLK Cycle

Minimum Acquisition Time

If the minimum line time is desired, the ADC reset duration needs to be set at its minimum of 2 ACLK cycles and the OSR at 74 ACLK cycle (<adc_osr>=0).

In this case the ADC conversion time is

Equation 15:

$$Minimum\ ADC\ conversion\ time = 2 \cdot \frac{OSR + ADC\ reset\ duration}{ACLK\ frequency} = \frac{152\ ACLK\ cycles}{8MHz} = 19\mu s$$

In this case, the ADC reset phases 1 and 2 start as soon as possible, which means

- Time Register R (Address 0x31) t_adcreset_start1=0
- Time Register S (Address 0x32) t_adcreset_start2=76

Moreover, also the CDS reset duration must be set to its minimum value of 1 ACLK cycle, in order to fulfil the condition in Equation 13:

$$ADC\ reset\ duration \geq CDS\ reset\ duration + 1$$

Recommended Acquisition Time

In the recommended line time condition, the ADC reset duration should be set to 6 ACLK cycles. With an OSR of 74 ACLK cycles (<adc_osr>=0), the ADC conversion time is

Equation 16:

$$Recommended\ ADC\ conversion\ time = 2 \cdot \frac{OSR + reset\ duration}{ACLK\ frequency} = \frac{160\ ACLK\ cycles}{8MHz} = 20\mu s$$

In this case, it is important that the ADC reset phases 1 and 2 start as soon as possible, which means

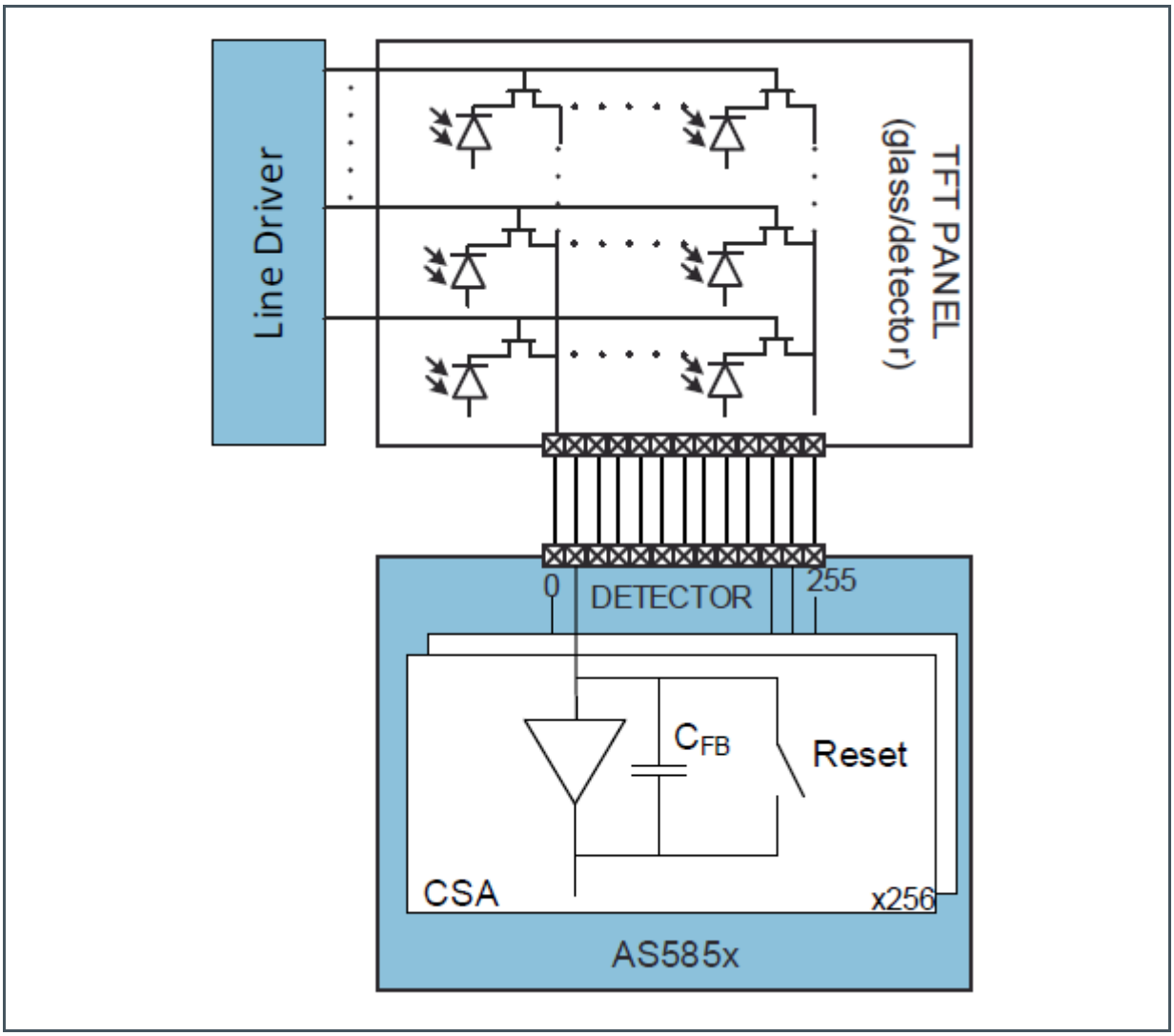
- Time Register R (Address 0x31) t_adcreset_start1=0
- Time Register S (Address 0x32) t_adcreset_start2=80

The recommended CDS reset duration is 2 ACLK cycles, which fulfils the condition in Equation 13:

$$ADC\ reset\ duration \geq CDS\ reset\ duration + 1$$

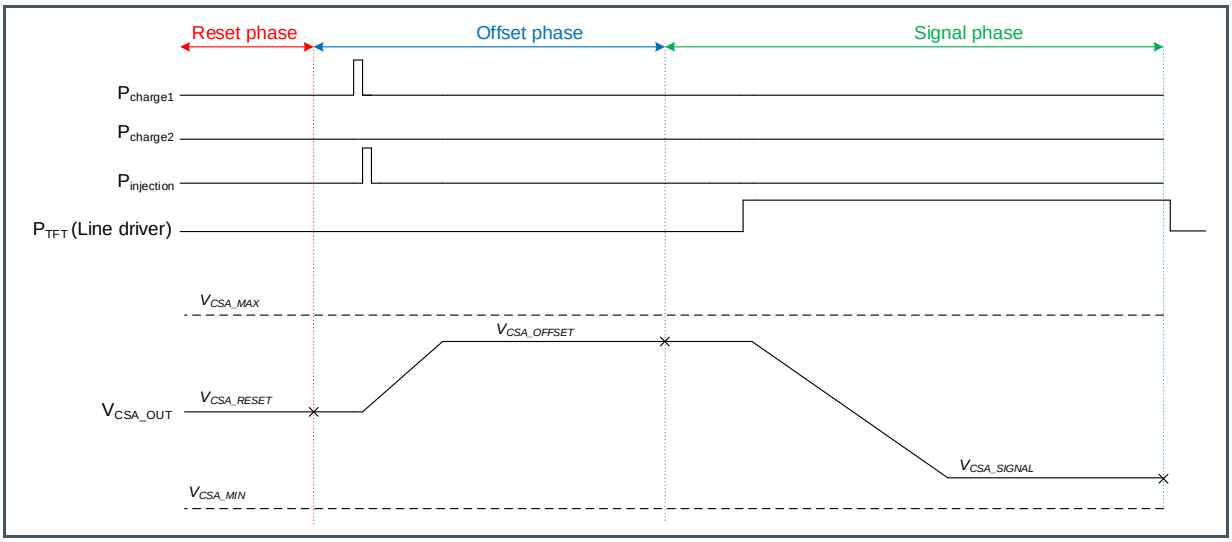
Line Driver Timing

Figure 54:
Functional Diagram of Flat Panel and AS585X Front-End



In the AS585X operation, the CSA receive charge from a TFT panel and the timing is controlled by a line driver. Refer to Chapter 7.3 of the datasheet for the complete description.

Figure 55:
Main CSA Phases During AS585X Operation



As shown in Figure 55, the line driver needs to close slightly after the signal phase starts and needs to open slightly after the signal phase ends.

6 Evaluation Modes

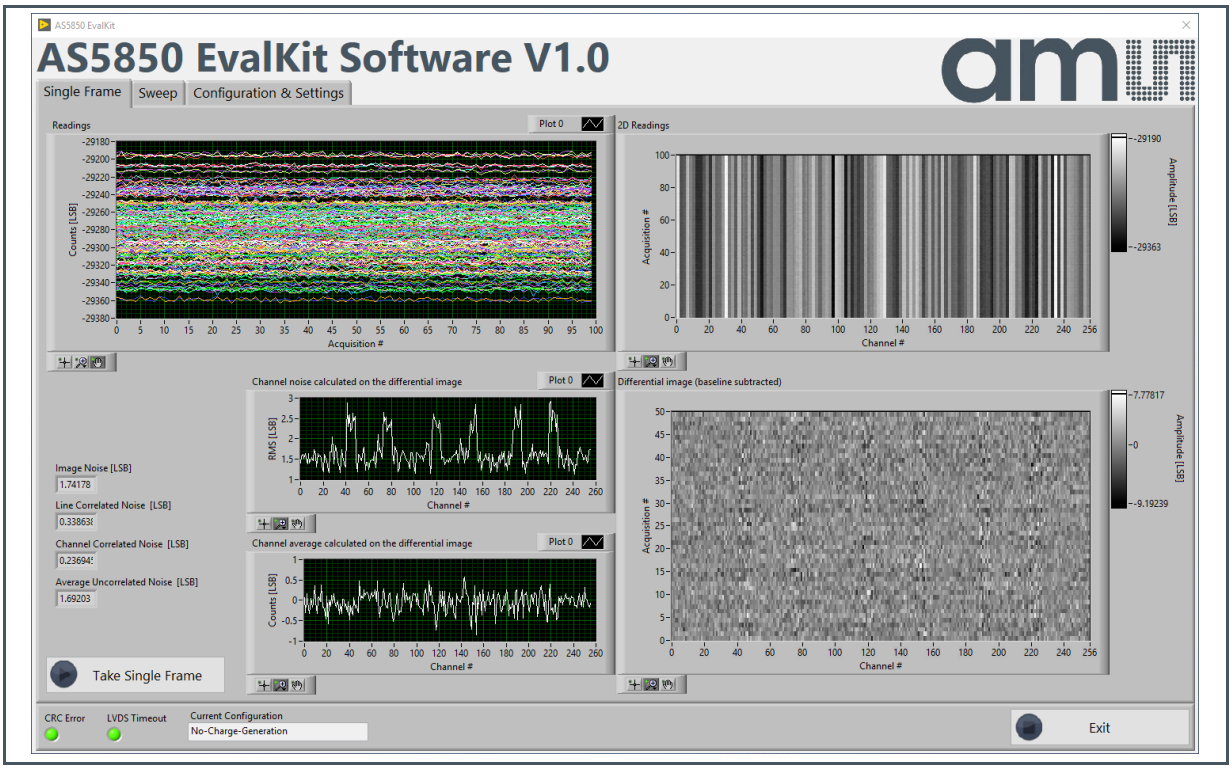
6.1 No Charge Generation

In “No charge generation” mode, no charge is injected on the AS585X. Therefore, it is possible to evaluate the AS585X noise and the output in no signal condition (baseline).

It can be evaluated with both the COB and COF samples.

A typical “Single Frame” taken in this mode is shown in Figure 56

Figure 56:
Typical No Charge Generation Single Frame



The baseline counts is ~ -29300 LSB.

6.2 Internal Charge Generation (holes)

In the “Internal-Charge-Generation-Holes” mode, negative charge (electrons) is injected during the offset phase for CSA voltage offset adjustment and a positive charge (holes) is injected during the signal phase. The offset charge is injected from the pin VchargeAux that is connected to GND while the signal charge is injected from the pin Vcharge that is driven by the DAC.

It can be evaluated with both the COB and COF samples.

Figure 57:
AS585X Eval Kit Hardware Architecture

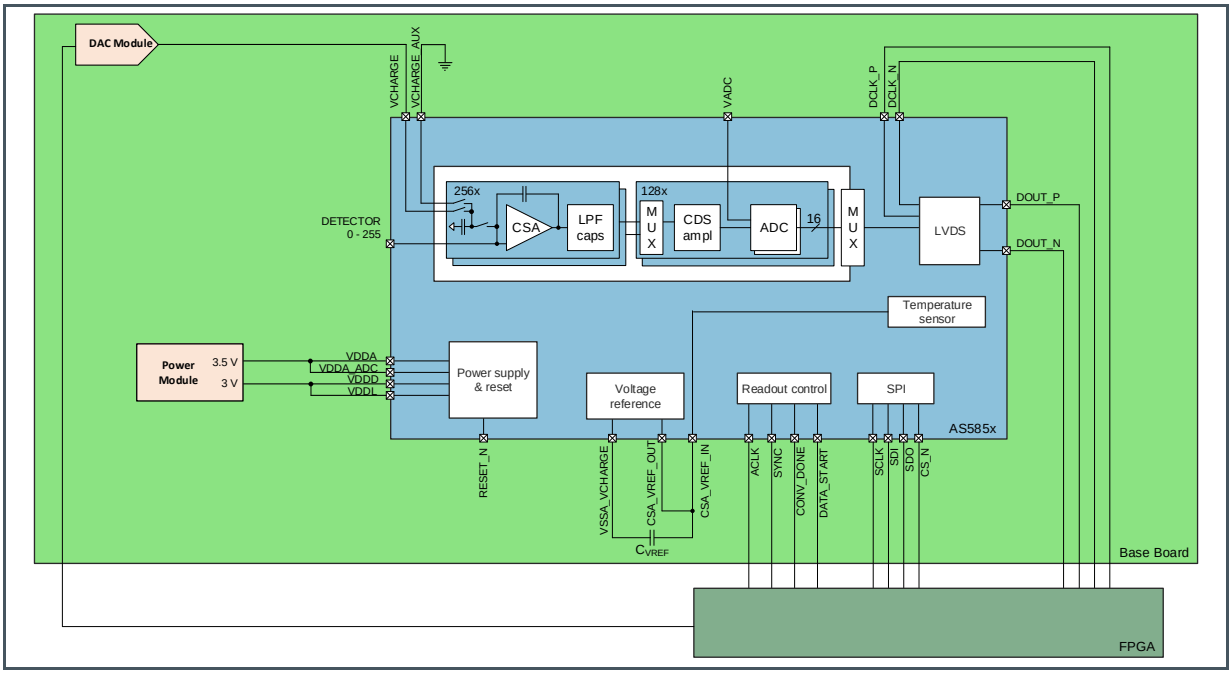


Figure 58:
Control Register A (Address 0x02) and B (Address 0x03) Content of the Configuration "Internal-Charge-Generation-Holes_20_us"

Address	Name	Bit	Value	Format	Description
0x02	PdEnable	15	0	%b	Enable power-down mode
	OutMode	14:13	11	%b	Readout mode
	AdcOsr	12	0	%b	ADC oversampling ratio
	AdcPwr	11	1	%b	ADC power setting(3)
	LpfAcc	10	0	%b	Low-pass filter acceleration (bypass)
	LpfTc	9:7	010	%b	Low-pass filter (LPF) time constant
	CsaGain	6:2	00011	%b	Feedback capacitance selection of CSA
	CsaPwr	1:0	11	%b	CSA power mode selection
0x03	TestModes	15	0	%b	CSA and ADC ams internal test modes
	TestModes	14	1	%b	CSA and ADC ams internal test modes
	TestModes	13	0	%b	CSA and ADC ams internal test modes
	TestModes	12:11	11	%b	CSA and ADC ams internal test modes
	TestModes	10:9	00	%b	CSA and ADC ams internal test modes
	TestModes	8	0	%b	CSA and ADC ams internal test modes
	TestModes	7	0	%b	CSA and ADC ams internal test modes
	CsaCg	6:5	11	%b	Charge injection
	CsaPol	4	0	%b	Polarity selection
	CsaAntiBloom	3:2	00	%b	CSA anti-blooming
	CsaVrefShortRes	1	0	%b	Low-pass resistor for the reference
	ChBin	0	0	%b	Channel binning

Figure 59:
Charge Injection Register A (Address 0x06), B (Address 0x07) and C (Address 0x08) Content of the Configuration "Internal-Charge-Generation-Holes_20_us"

Address	Name	Bit	Value	Format	Description
0x06	Spare	15:9	0000000	%b	Spare bits
	PolQtrans1	8	0	%b	Polarity of 1st charge injection
	CapQtrans1	7:4	0010	%b	Capacitors used for 1st charge injection
	NQtrans1	3:0	0001	%b	Number of charge "pluses," 1st charge
0x07	Spare	15:9	0000000	%b	Spare bits
	PolQtrans2	8	1	%b	Polarity of 2st charge injection
	CapQtrans2	7:4	1000	%b	Capacitors used for 2st charge injection
	NQtrans2	3:0	0001	%b	Number of charge "pluses," 2st charge
0x08	Spare	15:9	0000000	%b	Spare bits
	PolQtrans3	8	0	%b	Polarity of charge 3rd injection
	CapQtrans3	7:4	0000	%b	Capacitors used for 3rd charge injection
	NQtrans3	3:0	0000	%b	Number of charge "pluses," 3rd charge

Figure 60:
TIME Registers (Address 0x20 – 0x33) Content of the Configuration "Internal-Charge-Generation-Holes_20_us"

Address	Name	Bit	Value	Format	Description
0x20	Spare	15:13	000	%b	Spare bits
	TQtransStart1	12:0	28	%d	Start 1st charge injection
0x21	Spare	15:13	000	%b	Spare bits
	TQtransStart2	12:0	94	%d	Start 2nd charge injection
0x22	Spare	15:13	000	%b	Spare bits
	TQtransStart3	12:0	0	%d	Start 3rd charge injection
0x23	Spare	15:13	000	%b	Spare bits
	TCsaResetStart	12:0	1	%d	Start CSA reset
0x24	Spare	15:13	000	%b	Spare bits
	TCsaResetEnd	12:0	26	%d	End CSA reset
0x25	Spare	15:13	000	%b	Spare bits
	TCoffsetStart	12:0	27	%d	Start CSA offset phase
0x26	Spare	15:13	000	%b	Spare bits
	TCoffsetEnd	12:0	92	%d	End CSA offset phase
0x27	Spare	15:13	000	%b	Spare bits
	TCsignalStart	12:0	93	%d	Start CSA signal phase
0x28	Spare	15:13	000	%b	Spare bits
	TCsignalEnd	12:0	158	%d	End CSA signal phase
0x29	Spare	15:13	000	%b	Spare bits
	TFiltaccStart1	12:0	1	%d	Start 1st filter acceleration
0x2A	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd1	12:0	10	%d	End 1st filter acceleration
0x2B	Spare	15:13	000	%b	Spare bits
	TFiltaccStart2	12:0	27	%d	Start 2nd filter acceleration
0x2C	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd2	12:0	47	%d	End 2nd filter acceleration
0x2D	Spare	15:13	000	%b	Spare bits
	TFiltaccStart3	12:0	93	%d	Start 3rd filter acceleration
0x2E	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd3	12:0	113	%d	End 3rd filter acceleration
0x2F	Spare	15:13	000	%b	Spare bits
	TCdsResetDur	12:0	2	%d	Duration CDS reset
0x30	Spare	15:13	000	%b	Spare bits
	TAdcResetDur	12:0	6	%d	Duration ADC reset
0x31	Spare	15:13	000	%b	Spare bits
	TAdcResetStart1	12:0	0	%d	Start 1st ADC reset
0x32	Spare	15:13	000	%b	Spare bits
	TAdcResetStart2	12:0	80	%d	Start 2nd ADC reset
0x33	Spare	15:13	000	%b	Spare bits
	Tacq	12:0	160	%d	End line acquisition (line time)

6.2.1 Electrons Internal Charge Injection during the Offset Phase from VchargeAux

As shown in the “Internal-Charge-Generation-Holes_20_us” register map, the offset phase starts at 27 and ends at 92 as

- TIME Registers (Address 0x25) t_offset_start=27
- TIME Registers (Address 0x26) t_offset_end=92

The offset charge is generated by the internal charge generation circuit 1. The charge is injected during the offset phase as

- TIME Registers (Address 0x20) t_qtrans_start1=28

The offset charge is injected from the pin VchargeAux as

- Charge Injection Register A (Address 0x06) pol_q_trans1=0

The amount of charge injected from VchargeAux is calculated as:

Equation 17:

$$Q_{OFFSET} = C_{CG1} \cdot \left(V_{VchargeAux} - V_{CSA\_VREF\_IN}\right) \cdot N_{Q\_TRANS1}$$

Since the pin VchargeAux is connected to GND in the Eval Kit, the equation becomes

$$Q_{OFFSET} = C_{CG1} \cdot \left(-V_{CSA\_VREF\_IN}\right) \cdot N_{Q\_TRANS1}$$

Where

- $V_{CSA\_VREF\_IN}$=1.75 V
- Charge Injection Register A (Address 0x06) cap_q_trans1=0010: C_{CG1}=200 fF
- Charge Injection Register A (Address 0x06) n_q_trans1=1: $N_{QTRANS1}$=1

Substituting the values, the equation becomes

$$Q_{OFFSET} = 200fF \cdot (-1.75V) \cdot 1 = -0.35pC$$

As the CSA full scale range is defined in the

- Control Register A (Address 0x02) csa_gain= 00011
  - C_{FB}=0.84pF
  - Full scale range=2pC

The condition in Equation 6:

$$|Q_{OFFSET}| < \frac{Q_{FULL\_SCALE}}{2}$$

is fulfilled.

If a positive charge is to be injected during the signal phase, a negative charge is required during the offset phase in order to exploit the full input range.

The Eval Kit does not allow control on the voltage applied to the pin VchargeAux (shorted to GND), therefore only discrete values of negative charge can be injected, according to the available combinations allowed by cap_q_trans1 and n_q_trans1.

6.2.2 CSA Output Voltage Offset Phase

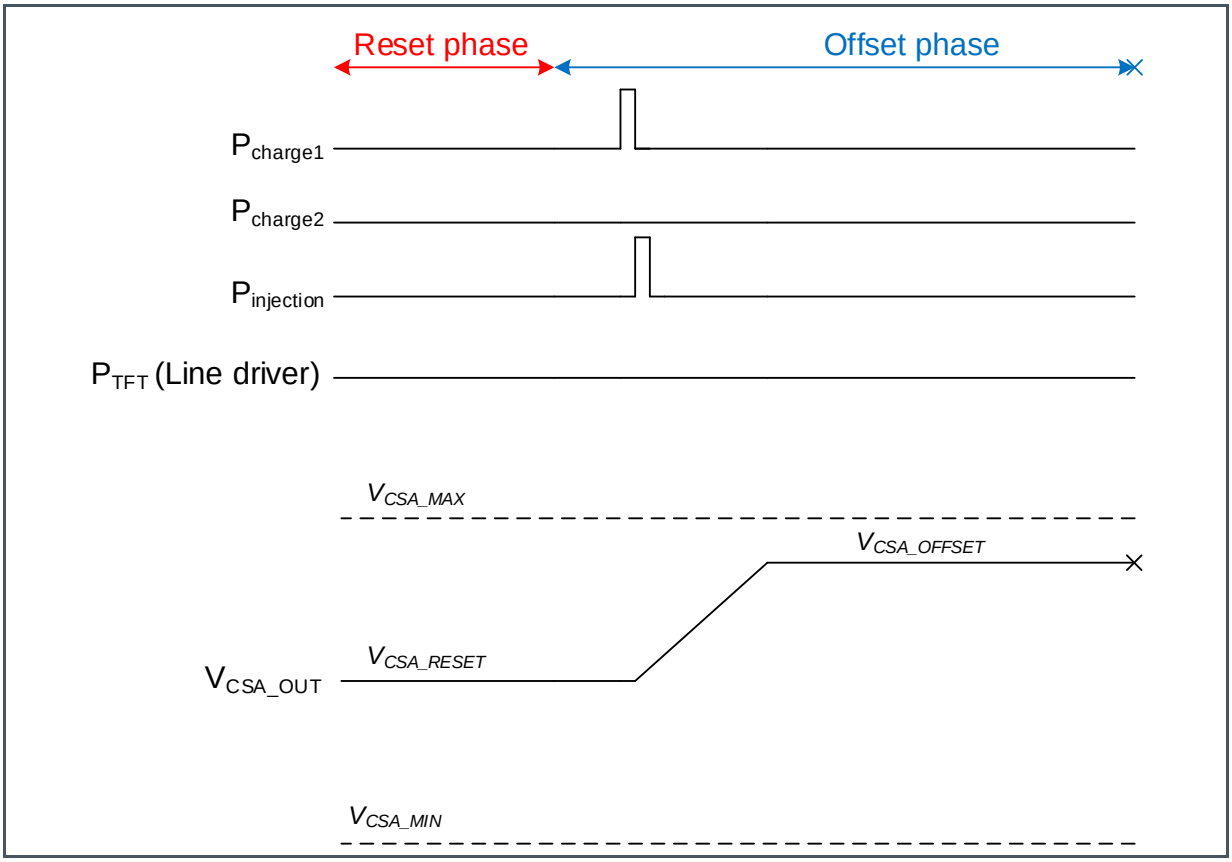
The CSA output voltage at the end of the offset phase is:

$$V_{CSA\_OFFSET} = V_{CSA\_VREF\_IN} - \left(\frac{Q_{OFFSET}}{C_{FB}}\right) = 1.75V - \left(\frac{-0.35pC}{0.84pF}\right) = 2.17V$$

Where C_{FB} is the CSA feedback capacitance defined in

- Control Register A (Address 0x02) csa_gain= 00011: C_{FB}=0.84 pF

Figure 61:
Charge Injection Timing Diagram During the Offset Phase(1)



(1) After the negative offset internal charge injection of -0.35 pC, the CSA output voltage Increases

6.2.3 Holes Internal Charge Injection During the Signal Phase from Vcharge

As shown in the “Internal-Charge-Generation-Holes_20_us” register map, the signal phase starts at 93 and ends at 158

- TIME Registers (Address 0x27) t_signal_start=93
- TIME Registers (Address 0x28) t_signal_end=158

The signal charge is generated by the internal charge generation circuit 2, as the charge is injected during the signal phase as

- TIME Registers (Address 0x21) t_qtrans_start2=94

The signal charge is injected from the pin Vcharge as

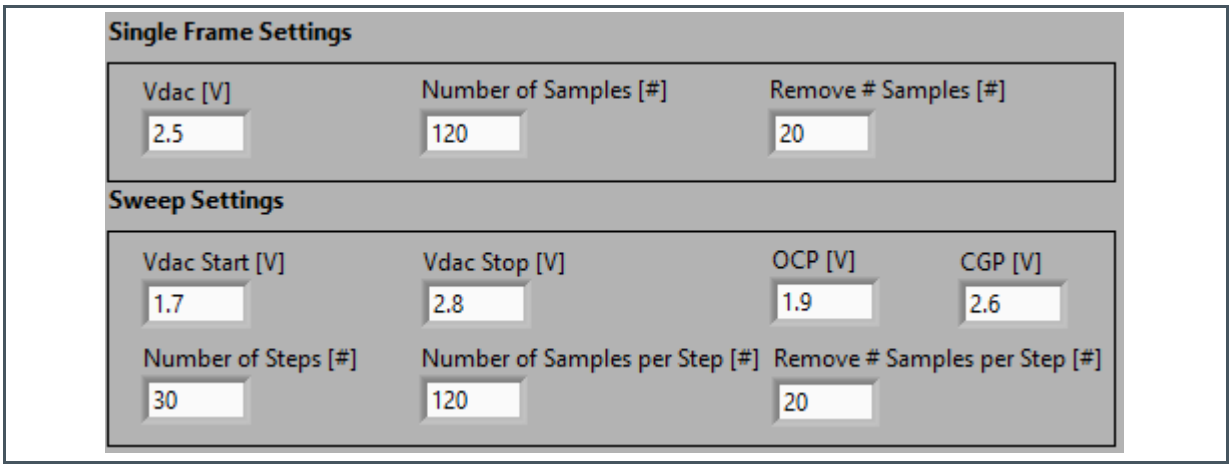
- Charge Injection Register B (Address 0x06) pol_q_trans2=1

The amount of charge injected from Vcharge is calculated as:

$$Q_{SIGNAL} = C_{CG2} \cdot \left(V_{Vcharge} - V_{CSA\_VREF\_IN}\right) \cdot N_{Q\_TRANS2}$$

Where $V_{Vcharge}$ is driven by the DAC and its voltage can be adjusted from the “Configuration and Settings” tab in the Eval Kit software

Figure 62:
Measurement Settings



Substituting the values

- Charge Injection Register B (Address 0x07) cap_q_trans2=1000: C_{CG2}=800fF
- Charge Injection Register B (Address 0x07) n_q_trans2=1: $N_{QTRANS2}$=1

It becomes

$$Q_{SIGNAL} = 800fF \cdot (2.5 - 1.75V) \cdot 1 = 0.6pC$$

With an offset charge of -0.35 pC, the condition described in Equation 8 is fulfilled

$$|Q_{SIGNAL}| < \frac{Q_{FULL_{SCALE}}}{2} + |Q_{OFFSET}| \rightarrow 0.6pC < \frac{2pC}{2} + 0.35pC$$

6.2.4 CSA Output Voltage Signal Phase

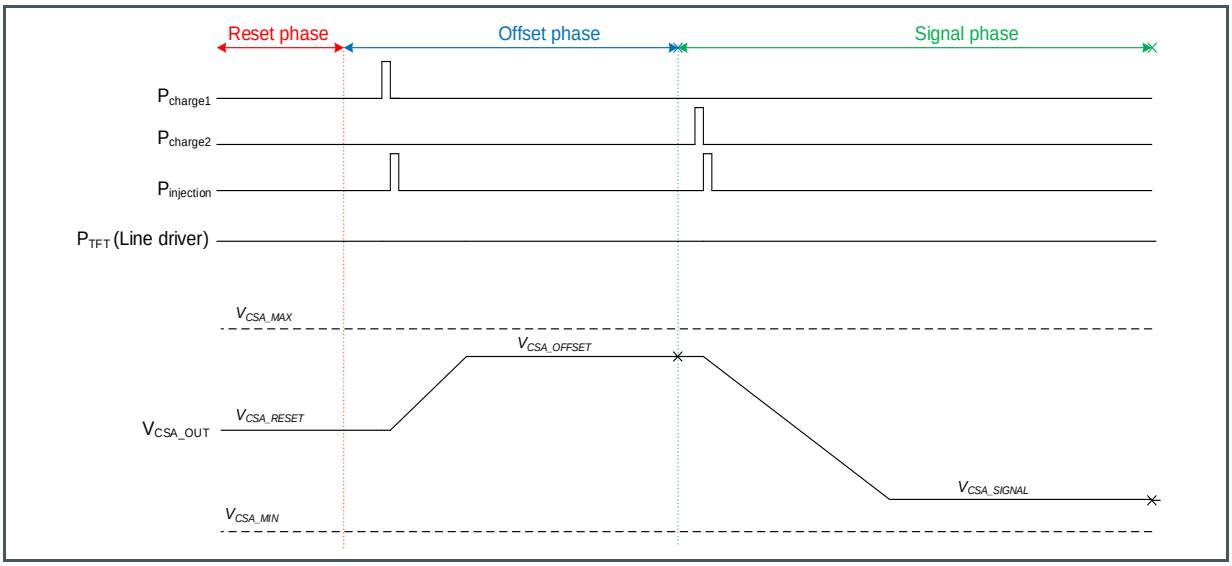
The CSA output voltage at the end of the signal phase is:

$$V_{CSA\_SIGNAL} = V_{CSA\_OFFSET} - \left(\frac{Q_{SIGNAL}}{C_{FB}}\right) = 2.17V - \left(\frac{0.6pC}{0.84pF}\right) = 1.46V$$

Where C_{FB} is the CSA feedback capacitance, defined as

- Control Register A (Address 0x02) csa_gain= 00011: C_{FB}=0.84pF

Figure 63:
Charge Injection Timing Diagram During the 3 CSA Phases.



6.2.5 ADC Digital Output

The expected ADC output is calculated as

Equation 18:

$$Output = baseline + \left(\frac{V_{CSA\_OFFSET} - V_{CSA\_SIGNAL}}{ADC\ resolution}\right) \cdot CSA\ Polarity$$

Where

- V_{CSA_SIGNAL} is the CSA output voltage during the signal phase

- V_{CSA_OFFSET} is the CSA output voltage during the offset phase
- baseline is ~-29300 LSB
- ADC resolution is ~40µV/LSB
- CSA Polarity is the polarity selection (electrons or holes) and defined in the Control Register B (Address 0x03) csa_pol=0: Positive charge (holes) → CSA Polarity= +1

Therefore:

$$Output = -29300 + \left(\frac{2.17 - 1.46}{40 \cdot 10^{-6}}\right) \cdot +1 = \ -11550\ LSB$$

Figure 64:
Typical Internal-Charge-Generation-Holes Single Frame

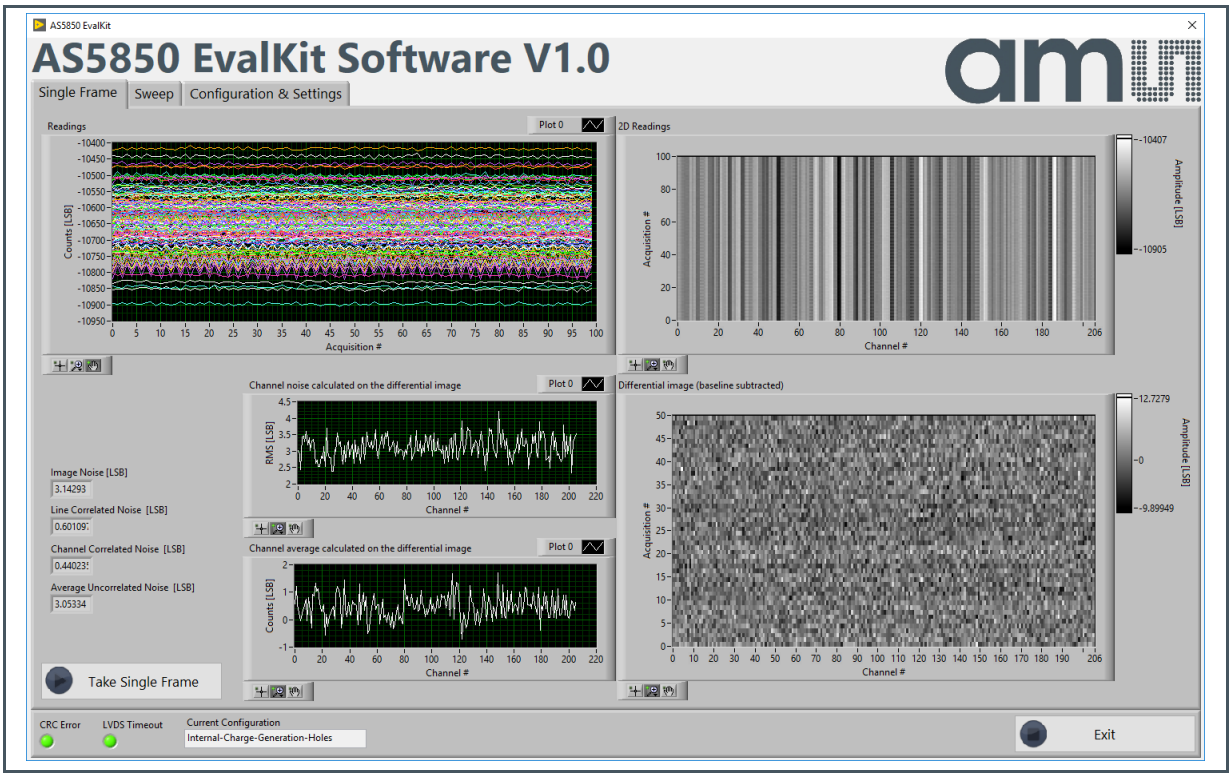


Figure 64 shows an example of a single frame acquired in the “Internal-Charge-Generation-Holes_20_us” configuration. From the “Readings” plot, it is possible to see that the output is very stable over many consecutive measurements and from the “Differential Image” no correlated noise is visible.

The measurement output is very close to calculated values. The user needs anyhow to calibrate the system with detector (offset and gain calibration).

6.3 Internal Charge Generation (electrons)

In the “Internal-Charge-Generation-Electrons” mode, a negative charge (electrons) is injected during the signal phase from the pin Vcharge that is driven by the DAC.

In this mode, a positive charge should be injected during the offset phase for CSA voltage offset adjustment, but due to the limited capabilities of the setup, it is not possible. Therefore, the offset adjustment is skipped allowing the exploitation of only half of the input range.

More precisely, the injection of a positive charge from the pin VchargeAux would require a voltage higher than 1.75V on such pin. Being the VchargeAux pin tied to GND and not being able to be driven to an arbitrary voltage, this operation is not possible.

It can be evaluated with both the COB and COF samples.

Figure 65:
AS585X Eval Kit Hardware Architecture

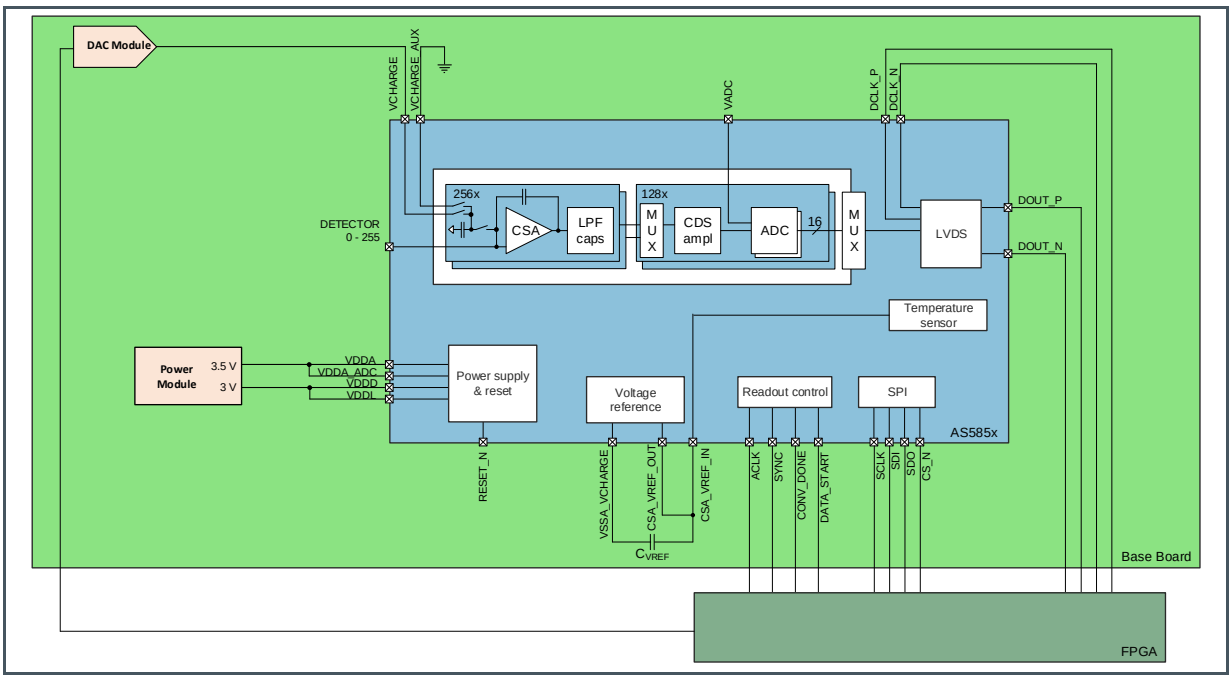


Figure 66:
Control Register A (Address 0x02) and B (Address 0x03) Content of the Configuration "Internal-Charge-Generation-Electrons_20_us"

Address	Name	Bit	Value	Format	Description
0x02	PdEnable	15	0	%b	Enable power-down mode
	OutMode	14:13	11	%b	Readout mode
	AdcOsr	12	0	%b	ADC oversampling ratio
	AdcPwr	11	1	%b	ADC power setting(3)
	LpfAcc	10	0	%b	Low-pass filter acceleration (bypass)
	LpfTc	9:7	010	%b	Low-pass filter (LPF) time constant
	CsaGain	6:2	00011	%b	Feedback capacitance selection of CSA
	CsaPwr	1:0	11	%b	CSA power mode selection
0x03	TestModes	15	0	%b	CSA and ADC ams internal test modes
	TestModes	14	1	%b	CSA and ADC ams internal test modes
	TestModes	13	0	%b	CSA and ADC ams internal test modes
	TestModes	12:11	11	%b	CSA and ADC ams internal test modes
	TestModes	10:9	00	%b	CSA and ADC ams internal test modes
	TestModes	8	0	%b	CSA and ADC ams internal test modes
	TestModes	7	0	%b	CSA and ADC ams internal test modes
	CsaCg	6:5	11	%b	Charge injection
	CsaPol	4	0	%b	Polarity selection
	CsaAntiBloom	3:2	00	%b	CSA anti-blooming
	CsaVrefShortRes	1	0	%b	Low-pass resistor for the reference
	ChBin	0	0	%b	Channel binning

Figure 67:
Charge Injection Register A (Address 0x06), B (Address 0x07) and C (Address 0x08) Content of the Configuration "Internal-Charge-Generation-Electrons_20_us"

Address	Name	Bit	Value	Format	Description
0x06	Spare	15:9	0000000	%b	Spare bits
	PolQtrans1	8	0	%b	Polarity of 1st charge injection
	CapQtrans1	7:4	0000	%b	Capacitors used for 1st charge injection
	NQtrans1	3:0	0000	%b	Number of charge "pluses," 1st charge
0x07	Spare	15:9	0000000	%b	Spare bits
	PolQtrans2	8	1	%b	Polarity of 2st charge injection
	CapQtrans2	7:4	1000	%b	Capacitors used for 2st charge injection
	NQtrans2	3:0	0001	%b	Number of charge "pluses," 2st charge
0x08	Spare	15:9	0000000	%b	Spare bits
	PolQtrans3	8	0	%b	Polarity of charge 3rd injection
	CapQtrans3	7:4	0000	%b	Capacitors used for 3rd charge injection
	NQtrans3	3:0	0000	%b	Number of charge "pluses," 3rd charge

Figure 68:
TIME Registers (Address 0x20 – 0x33) Content of the Configuration "Internal-Charge-Generation-Electrons_20_us"

Address	Name	Bit	Value	Format	Description
0x20	Spare	15:13	000	%b	Spare bits
	TQtransStart1	12:0	0	%d	Start 1st charge injection
0x21	Spare	15:13	000	%b	Spare bits
	TQtransStart2	12:0	94	%d	Start 2nd charge injection
0x22	Spare	15:13	000	%b	Spare bits
	TQtransStart3	12:0	0	%d	Start 3rd charge injection
0x23	Spare	15:13	000	%b	Spare bits
	TCsaResetStart	12:0	1	%d	Start CSA reset
0x24	Spare	15:13	000	%b	Spare bits
	TCsaResetEnd	12:0	26	%d	End CSA reset
0x25	Spare	15:13	000	%b	Spare bits
	TCoffsetStart	12:0	27	%d	Start CSA offset phase
0x26	Spare	15:13	000	%b	Spare bits
	TCoffsetEnd	12:0	92	%d	End CSA offset phase
0x27	Spare	15:13	000	%b	Spare bits
	TCsignalStart	12:0	93	%d	Start CSA signal phase
0x28	Spare	15:13	000	%b	Spare bits
	TCsignalEnd	12:0	158	%d	End CSA signal phase
0x29	Spare	15:13	000	%b	Spare bits
	TFiltaccStart1	12:0	1	%d	Start 1st filter acceleration
0x2A	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd1	12:0	10	%d	End 1st filter acceleration
0x2B	Spare	15:13	000	%b	Spare bits
	TFiltaccStart2	12:0	27	%d	Start 2nd filter acceleration
0x2C	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd2	12:0	47	%d	End 2nd filter acceleration
0x2D	Spare	15:13	000	%b	Spare bits
	TFiltaccStart3	12:0	93	%d	Start 3rd filter acceleration
0x2E	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd3	12:0	113	%d	End 3rd filter acceleration
0x2F	Spare	15:13	000	%b	Spare bits
	TCdsResetDur	12:0	2	%d	Duration CDS reset
0x30	Spare	15:13	000	%b	Spare bits
	TAdcResetDur	12:0	6	%d	Duration ADC reset
0x31	Spare	15:13	000	%b	Spare bits
	TAdcResetStart1	12:0	0	%d	Start 1st ADC reset
0x32	Spare	15:13	000	%b	Spare bits
	TAdcResetStart2	12:0	80	%d	Start 2nd ADC reset
0x33	Spare	15:13	000	%b	Spare bits
	Tacq	12:0	160	%d	End line acquisition (line time)

6.3.1 No Charge Injection during the Offset Phase from VchargeAux

As it is not possible to inject a suitable positive charge during the offset phase for CSA voltage offset adjustment, the internal charge generation circuit 1 is disabled

- TIME Register (Address 0x20) t_qtrans_start1=0
- Charge Injection Register A (Address 0x06) cap_q_trans1=0000
- Charge Injection Register A (Address 0x06) n_q_trans1=0

Therefore

$$Q_{OFFSET} = 0pC$$

And the voltage at the end of the offset phase is:

$$V_{CSA\_OFFSET} = V_{CSA\_VREF\_IN} = 1.75V$$

6.3.2 Electrons Internal Charge Injection during the Signal Phase from Vcharge

As shown in the “Internal-Charge-Generation-Electrons_20_us” register table, the signal phase starts at 93 and ends at 158

- TIME Register (Address 0x27) t_signal_start=93
- TIME Register (Address 0x28) t_signal_end=158

The signal charge is generated by the internal charge generation circuit 2, as the charge is injected during the signal phase as

- TIME Register (Address 0x21) t_qtrans_start1=94

The signal charge is injected from the pin Vcharge as

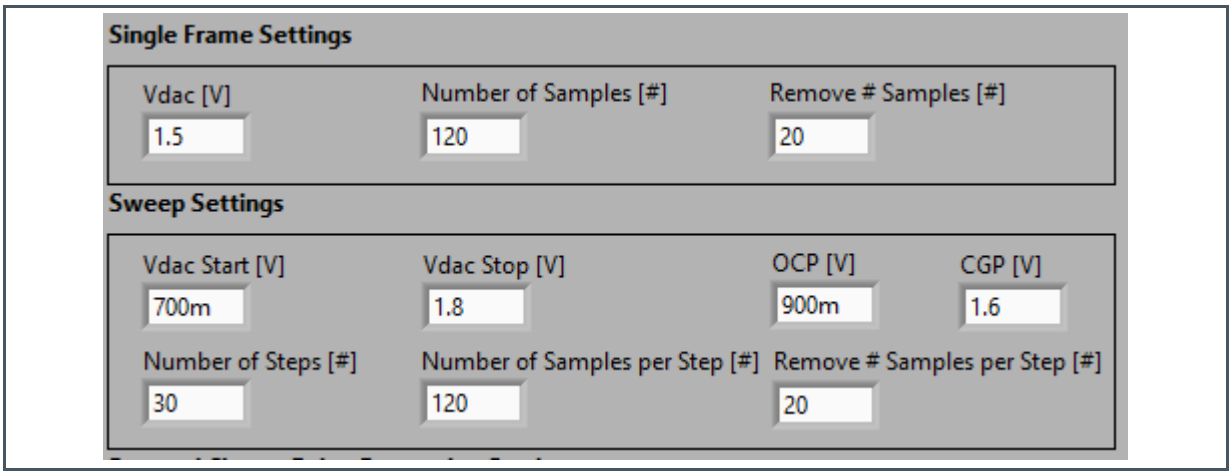
- Charge Injection Register B (Address 0x06) pol_q_trans2=1

The amount of charge injected from Vcharge is described as:

$$Q_{SIGNAL} = C_{CG2} \cdot \left(V_{Vcharge} - V_{CSA\_VREF\_IN}\right) \cdot N_{Q\_TRANS2}$$

Where $V_{Vcharge}$ is driven by the DAC, and its voltage can be adjusted from the “Configuration and Settings” tab in the Eval Kit software

Figure 69:
Measurement Settings



Substituting the values

- Charge Injection Register B (Address 0x07) cap_q_trans2=1000: C_{CG2}=800fF
- Charge Injection Register B (Address 0x07) n_q_trans2=1: $N_{QTRANS2}$=1

It becomes

$$Q_{SIGNAL} = 800fF \cdot (1.5 - 1.75V) \cdot 1 = -0.2pC$$

Without an offset charge, only half of the full-scale charge can be injected during the signal phase.

The condition described in Equation 8: is fulfilled

$$|Q_{SIGNAL}| < \frac{Q_{FULL_{SCALE}}}{2} - |Q_{OFFSET}| \rightarrow 0.2pC < \frac{2pC}{2} + 0pC$$

6.3.3 CSA Output Voltage Signal Phase

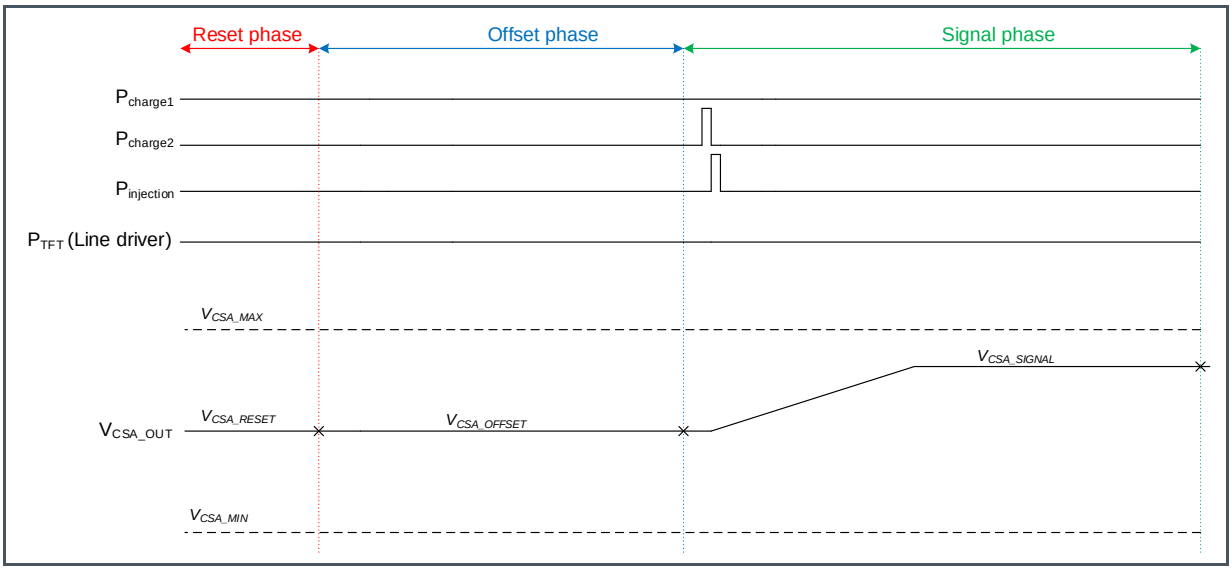
The CSA output voltage at the end of the signal phase is:

$$V_{CSA\_SIGNAL} = V_{CSA\_OFFSET} - \left(\frac{Q_{SIGNAL}}{C_{FB}}\right) = 1.75V - \left(\frac{-0.2pC}{0.84pF}\right) = 1.99V$$

As C_{FB} is Feedback capacitance of CSA and defined in the

- Control Register A (Address 0x02) csa_gain= 00011: C_{FB}=0.84pF

Figure 70:
Charge Injection Timing Diagram During the 3 CSA Phases



6.3.4 ADC Digital Output

The expected ADC output is calculated as

Equation 19:

$$Output = baseline + \left(\frac{V_{CSA\_OFFSET} - V_{CSA\_SIGNAL}}{ADC\ resolution}\right) \cdot CSA\ Polarity$$

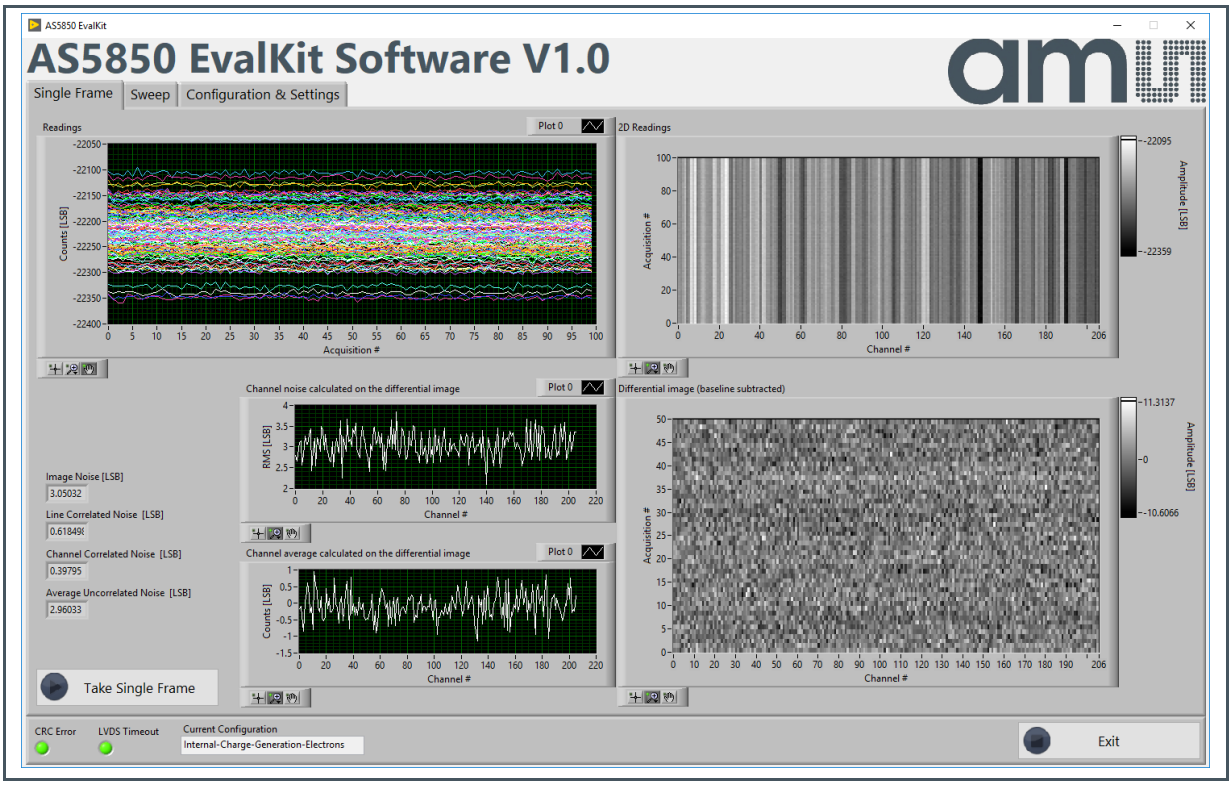
Where

- V_{CSA_SIGNAL} is the CSA output voltage during the signal phase
- V_{CSA_OFFSET} is the CSA output voltage during the offset phase
- baseline is ~-29300 LSB
- ADC resolution is ~40 µV/LSB
- CSA Polarity is the polarity selection (electrons or holes) and defined in the Control Register B (Address 0x03) csa_pol=1: Negative charge (electrons) → CSA Polarity= -1

Therefore:

$$Output\ Counts = -29300 + \left(\frac{1.75 - 1.99}{40 \cdot 10^{-6}}\right) \cdot -1 = \ -23300\ LSB$$

Figure 71:
Typical Internal-Charge-Generation-Electrons Single Frame



6.4 External Charge Generation (holes)

In the “External Charge Generation-XX” mode, the charge signal is generated externally by applying a voltage step to a set of capacitors connected to the AS585X frontend inputs, thus emulating the charge signal from an X-ray flat panel detector.

It can be evaluated only with the COB sample.

The required voltage step is generated by the charge pulse generator, which generates a signal that toggles between the DAC voltage and GND. Such signal is applied to the charge capacitor, thus generating the charge, which is then transferred to the AS585X frontend.

The step timing is controlled by the FPGA.

For the linearity evaluation, the DAC voltage can be swept in order to exploit a certain input charge range of the AS585X.

The amount of charge, which is injected in the front-end, is expressed in Equation 15:

Equation 20:

$$Q_{EXT} = C_{CHARGE} \cdot \left(V_{STEP_{HIGH}} - V_{STEP_{LOW}}\right) = C_{CHARGE} \cdot (V_{DAC} - 0)$$

In the “External Charge Generation-Holes” mode, negative charge (electrons) is injected during the offsef phase for CSA voltage offset adjustment and a positive charge (holes) is injected during the signal phase. The offset charge is injected from the pin VchargeAux that is connected to GND while the signal charge is injected in the frontend from the charge pulse generator.

Figure 72:
AS585X Eval Kit Hardware Architecture

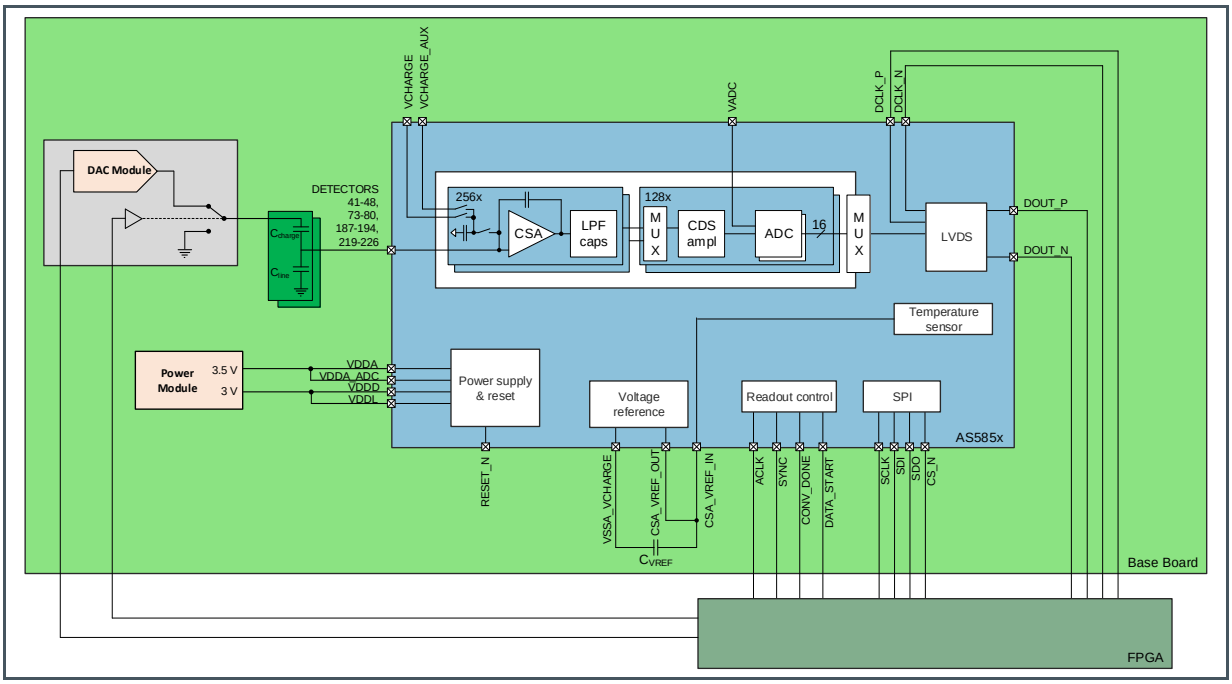


Figure 73:
Control Register A (Address 0x02) and B (Address 0x03) Content of the Configuration "External-Charge-Generation-Holes_20_us"

Address	Name	Bit	Value	Format	Description
0x02	PdEnable	15	0	%b	Enable power-down mode
	OutMode	14:13	11	%b	Readout mode
	AdcOsr	12	0	%b	ADC oversampling ratio
	AdcPwr	11	1	%b	ADC power setting(3)
	LpfAcc	10	0	%b	Low-pass filter acceleration (bypass)
	LpfTc	9:7	010	%b	Low-pass filter (LPF) time constant
	CsaGain	6:2	00011	%b	Feedback capacitance selection of CSA
	CsaPwr	1:0	11	%b	CSA power mode selection
0x03	TestModes	15	0	%b	CSA and ADC ams internal test modes
	TestModes	14	1	%b	CSA and ADC ams internal test modes
	TestModes	13	0	%b	CSA and ADC ams internal test modes
	TestModes	12:11	11	%b	CSA and ADC ams internal test modes
	TestModes	10:9	00	%b	CSA and ADC ams internal test modes
	TestModes	8	0	%b	CSA and ADC ams internal test modes
	TestModes	7	0	%b	CSA and ADC ams internal test modes
	CsaCg	6:5	11	%b	Charge injection
	CsaPol	4	0	%b	Polarity selection
	CsaAntiBloom	3:2	00	%b	CSA anti-blooming
	CsaVrefShortRes	1	0	%b	Low-pass resistor for the reference
	ChBin	0	0	%b	Channel binning

Figure 74:
Charge Injection Register A (Address 0x06), B (Address 0x07) and C (Address 0x08) Content of the Configuration "External-Charge-Generation-Holes_20_us"

Address	Name	Bit	Value	Format	Description
0x06	Spare	15:9	0000000	%b	Spare bits
	PolQtrans1	8	0	%b	Polarity of 1st charge injection
	CapQtrans1	7:4	0010	%b	Capacitors used for 1st charge injection
	NQtrans1	3:0	0001	%b	Number of charge "pluses," 1st charge
0x07	Spare	15:9	0000000	%b	Spare bits
	PolQtrans2	8	0	%b	Polarity of 2st charge injection
	CapQtrans2	7:4	0000	%b	Capacitors used for 2st charge injection
	NQtrans2	3:0	0000	%b	Number of charge "pluses," 2st charge
0x08	Spare	15:9	0000000	%b	Spare bits
	PolQtrans3	8	0	%b	Polarity of charge 3rd injection
	CapQtrans3	7:4	0000	%b	Capacitors used for 3rd charge injection
	NQtrans3	3:0	0000	%b	Number of charge "pluses," 3rd charge

Figure 75:
TIME Registers (Address 0x20 – 0x33) Content of the Configuration "External-Charge-Generation-Holes_20_us"

Address	Name	Bit	Value	Format	Description
	TQtransStart1	12:0	28	%d	Start 1st charge injection
0x21	Spare	15:13	000	%b	Spare bits
	TQtransStart2	12:0	0	%d	Start 2nd charge injection
0x22	Spare	15:13	000	%b	Spare bits
	TQtransStart3	12:0	0	%d	Start 3rd charge injection
0x23	Spare	15:13	000	%b	Spare bits
	TCsaResetStart	12:0	1	%d	Start CSA reset
0x24	Spare	15:13	000	%b	Spare bits
	TCsaResetEnd	12:0	26	%d	End CSA reset
0x25	Spare	15:13	000	%b	Spare bits
	TCoffsetStart	12:0	27	%d	Start CSA offset phase
0x26	Spare	15:13	000	%b	Spare bits
	TCoffsetEnd	12:0	92	%d	End CSA offset phase
0x27	Spare	15:13	000	%b	Spare bits
	TCsignalStart	12:0	93	%d	Start CSA signal phase
0x28	Spare	15:13	000	%b	Spare bits
	TCsignalEnd	12:0	158	%d	End CSA signal phase
0x29	Spare	15:13	000	%b	Spare bits
	TFiltaccStart1	12:0	1	%d	Start 1st filter acceleration
0x2A	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd1	12:0	10	%d	End 1st filter acceleration
0x2B	Spare	15:13	000	%b	Spare bits
	TFiltaccStart2	12:0	27	%d	Start 2nd filter acceleration
0x2C	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd2	12:0	47	%d	End 2nd filter acceleration
0x2D	Spare	15:13	000	%b	Spare bits
	TFiltaccStart3	12:0	93	%d	Start 3rd filter acceleration
0x2E	Spare	15:13	000	%b	Spare bits
	TFiltaccEnd3	12:0	113	%d	End 3rd filter acceleration
0x2F	Spare	15:13	000	%b	Spare bits
	TCdsResetDur	12:0	2	%d	Duration CDS reset
0x30	Spare	15:13	000	%b	Spare bits
	TAdcResetDur	12:0	6	%d	Duration ADC reset
0x31	Spare	15:13	000	%b	Spare bits
	TAdcResetStart1	12:0	0	%d	Start 1st ADC reset
0x32	Spare	15:13	000	%b	Spare bits
	TAdcResetStart2	12:0	80	%d	Start 2nd ADC reset
0x33	Spare	15:13	000	%b	Spare bits
	Tacq	12:0	160	%d	End line acquisition (line time)

6.4.1 Electrons Internal Charge Injection during the Offset Phase from VchargeAux

As in “Internal-Charge-Generation-Holes_20_us”, an offset charge of 0.35 pC is injected for CSA voltage adjustment

$$Q_{OFFSET} = 200fF \cdot (-1.75V) \cdot 1 = -0.35pC$$

Therefore, the CSA output voltage at the end of the offset phase is:

Equation 21:

$$V_{CSA\_OFFSET} = V_{CSA\_VREF\_IN} - \left(\frac{Q_{OFFSET}}{C_{FB}}\right) = 1.75V - \left(\frac{-0.35pC}{0.84pF}\right) = 2.17V$$

6.4.2 Holes External Charge Injection during the Signal Phase

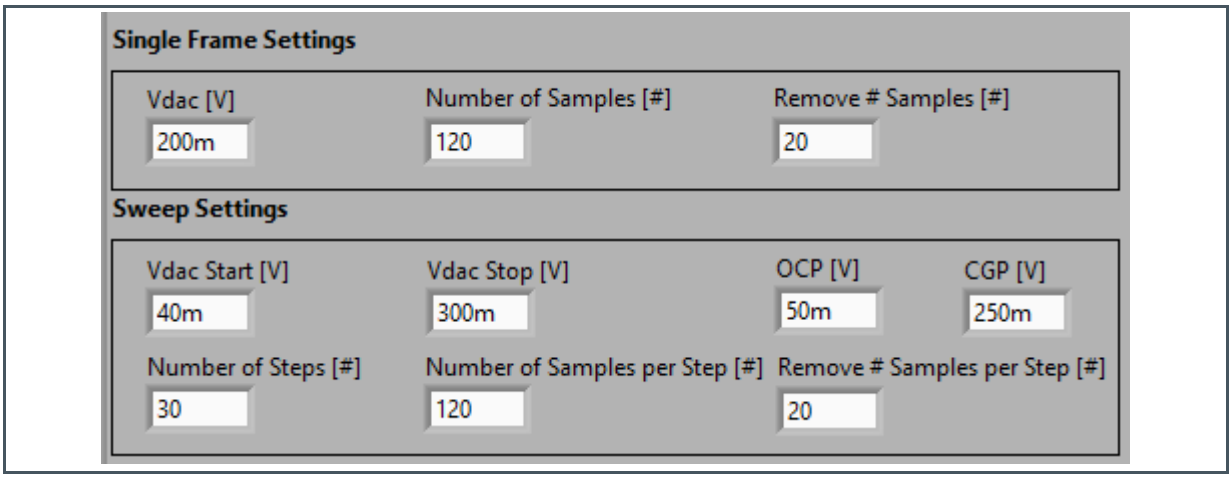
As described in Equation 15: the external charge generation is defined as

$$Q_{SIGNAL} = C_{CHARGE} \cdot (V_{DAC} - 0)$$

Where:

- C_{CHARGE} is 3 pF
- V_{DAC} is defined from the “Configuration and Settings” tab in the Eval Kit software

Figure 76:
Measurement Settings



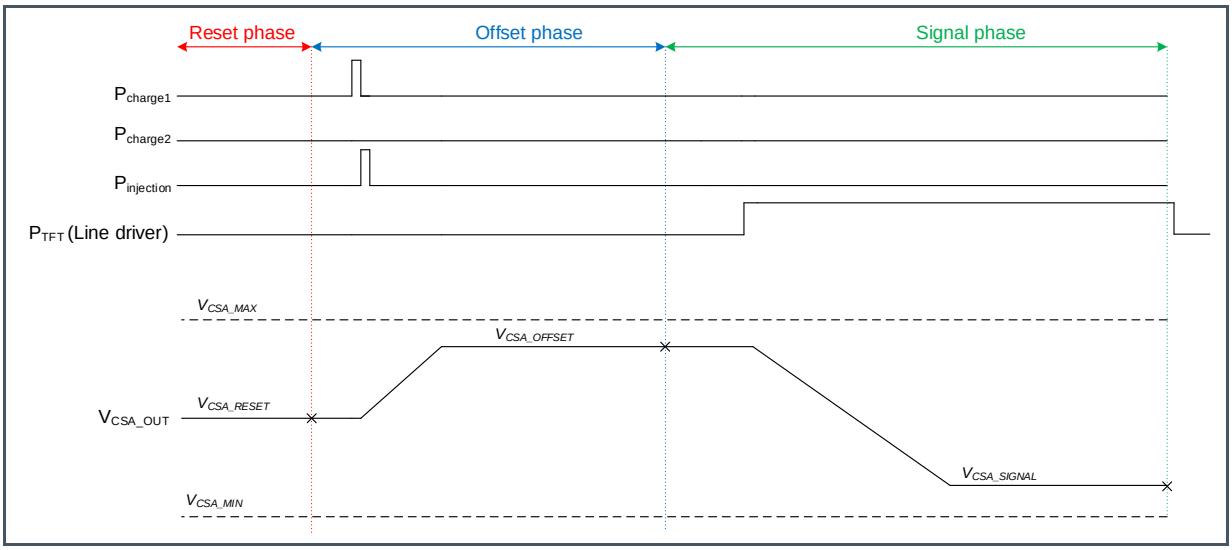
Substituting the values

$$Q_{SIGNAL} = 3pF \cdot (0.2V - 0V) = 0.6pC$$

The CSA output voltage at the end of the signal phase is:

$$V_{CSA\_SIGNAL} = V_{CSA\_OFFSET} - \left(\frac{Q_{SIGNAL}}{C_{FB}}\right) = 2.17V - \left(\frac{0.6pC}{0.84pF}\right) = 1.46V$$

Figure 77:
Charge Injection Timing Diagram During the 3 CSA Phases.

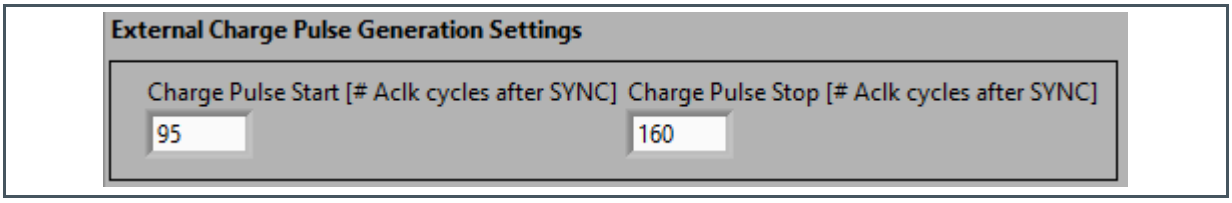


6.4.3 Timing

As described in section 5.3.3 Line Driver Timing, the external charge injection needs to start slightly after the start of the signal phase and it needs to end slightly after the signal phase.

The charge injection timing is defined in the Eval Kit software

Figure 78:
Example of External Charge Pulse Generation Settings for 20 µs Line Time



As shown in the “External-Charge-Generation-Holes_20_us” register map, the signal phase starts at 93 and ends at 158

- TIME Registers (Address 0x27) t_signal_start=93
- TIME Registers (Address 0x28) t_signal_end=158

So the charge injection in this case starts 2 ACLK cycles after the start of signal phase and it ends 2 ACLK cycles after the end of the signal phase.

6.4.4 ADC Digital Output

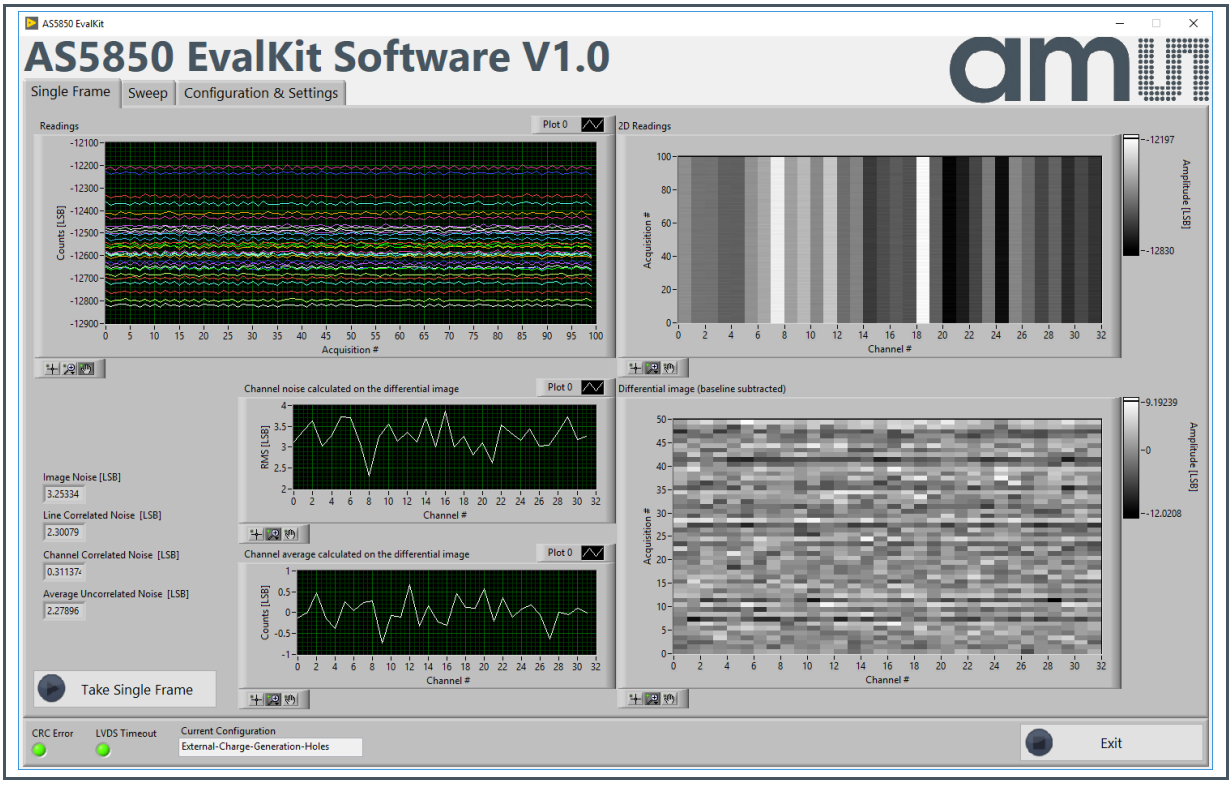
The expected ADC output is calculated as

Equation 22:

$$Output = baseline + \left(\frac{V_{CSA_{OFFSET}} - V_{CSA_{SIGNAL}}}{ADC\ resolution}\right) \cdot CSA\ Polarity =$$

$$= -29300 + \left(\frac{2.17 - 1.46}{40 \cdot 10^{-6}}\right) \cdot +1 = -11550\ LSB$$

Figure 79:
Typical External-Charge-Generation-Holes Single Frame



External charge injection is possible only on the channels connected to the Charge Capacitors, which are 32 on the AS585X sample boards.

6.5 External Charge Generation (electrons)

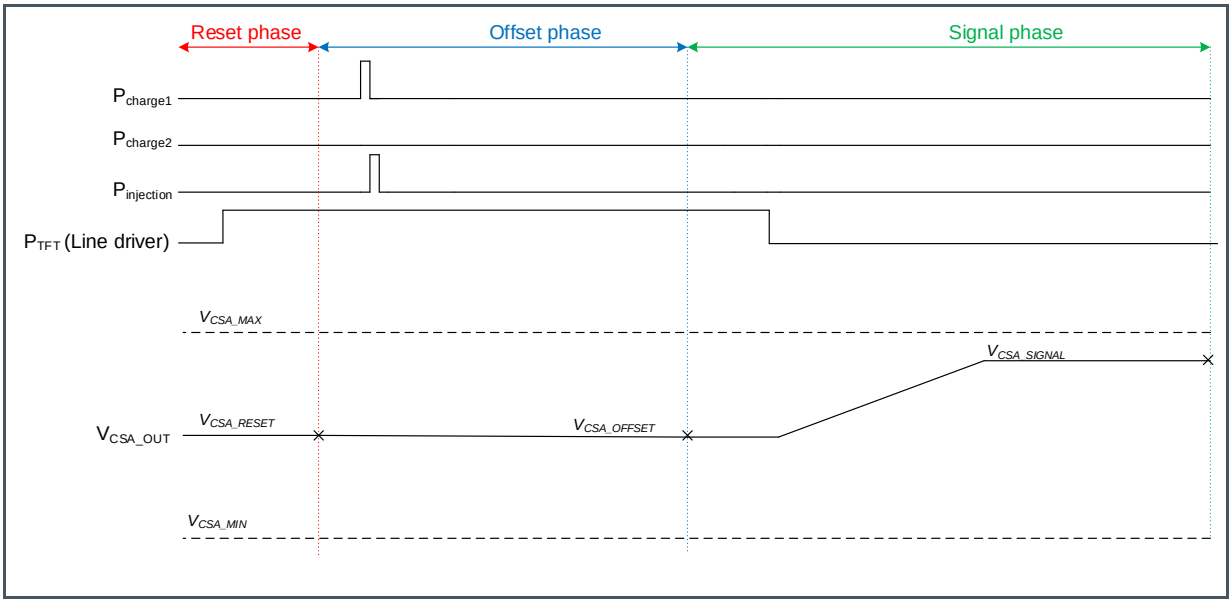
The “External Charge Generation (electrons)” mode can be evaluated only with the COB sample.

The amount of charge externally injected with the Eval Kit charge generation circuitry is expressed in Equation 15

$$Q_{EXT} = C_{CHARGE} \cdot \left(V_{STEP\_HIGH} - V_{STEP\_LOW}\right) = C_{CHARGE} \cdot (V_{DAC} - 0)$$

Its polarity can be inverted by inverting the step function as shown in Figure 80

Figure 80:
Charge Injection Timing Diagram During the 3 CSA Phases.



Thus, the charge will be negative, as only positive voltages are allowed for V_{DAC}

Equation 23:

$$Q_{EXT} = C_{CHARGE} \cdot \left(V_{STEP\_LOW} - V_{STEP\_HIGH}\right) = C_{CHARGE} \cdot (0 - V_{DAC})$$

A negative charge is injected during the signal phase and no charge is injected during the offset phase, as it is not possible to inject holes during the offset phase, because VchargeAux is connected to GND as described in chapter 6.3.1.

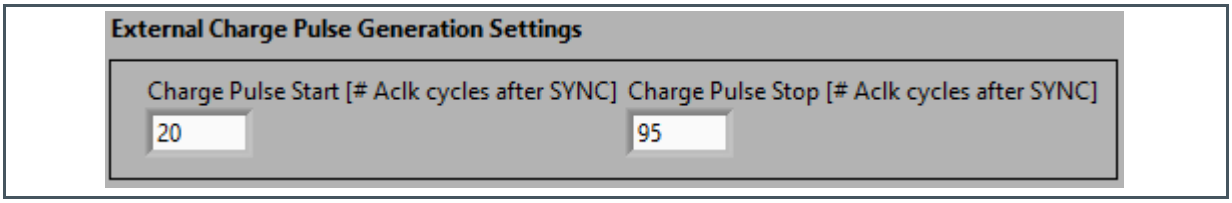
Only half of the CSA dynamic range can be exploited with the Eval Kit in this case.

6.5.1 Timing

The step function can be inverted by adjusting the timing: rise the level of the step during the reset phase and then let it fall back to the low level slightly after the start of the signal phase, leaving it to the low level for the rest of the acquisition, as described in paragraph 5.3.3 Line Driver Timing.

For example, in the case the signal phase starts at 93 and ends at 158, the charge pulse could start at 20 and end at 95, as shown in Figure 81

Figure 81:
External Charge Pulse Generation Settings



7 Other Operation Modes

In order to enable a wide range of applications, the AS585X is highly configurable and it has several other operation modes with respect to those treated in this manual, such as:

- Binning mode
- 240 channels mode
- Readout modes:
  - Readout Mode 1 – All Serial
  - Readout Mode 2 – Charge Acquisition and Signal Conversion Parallel
  - Readout Mode 3 – Signal Conversion and Data Output Parallel
  - Readout Mode 4 – All Parallel

However, a detailed description of all of them is out of the scope of this manual; therefore please get in contact with ams AG to request engineering support to best address a specific solution for your application.

8 Table of Abbreviations

Figure 82:
Table of Abbreviations

Abbreviation	Explanation
ADC	Analog-to-Digital Converter
CDS	Correlated Double Sampling
CSA	Charge Sensing Amplifier
INL	Integral Nonlinearity
LPF	Low-Pass Filter
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
SPI	Serial Peripheral Interface

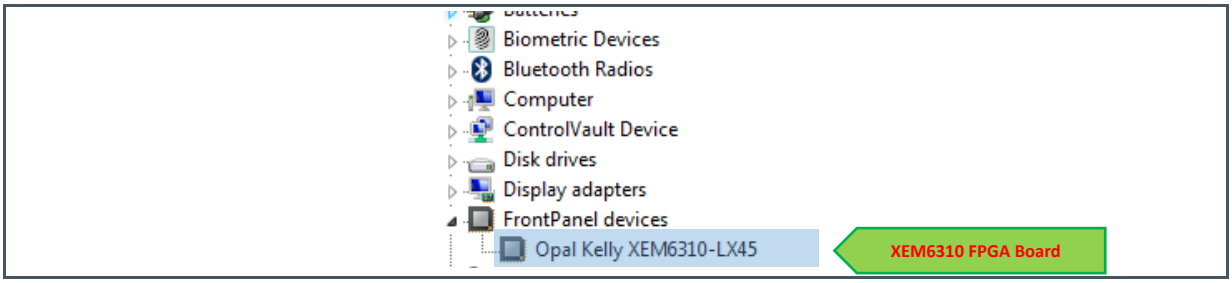
9 Troubleshooting

9.1 Connection Issue

Please check the correct driver installation in the Device Manager.

To start the Device Manager click the Start button and type in the Start Search box **device manager** and then press enter.

Figure 83:
Device Manager Connection



If the XEM6310 does not appear under “FrontPanel devices”, drivers are not correctly installed. Please disconnect the board, uninstall and re-install the software. Then re-connect the board and verify the system is fully functional.

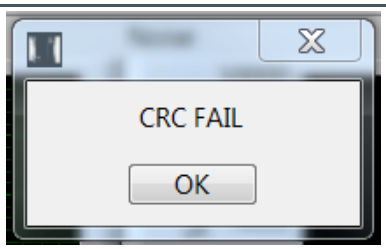
9.2 Screen Limitation Issue

The software front panel’s size cannot be reduced below 1366x768 pixels. This corresponds to the minimum supported screen resolution. In case the screen resolution is below this value and the software interface is not entirely visible, reduce Windows’ font size to Smaller - 100%. The corresponding menu is accessible via Control Panel - Display.

Moreover, always make sure the resolution is set to the native resolution of the screen in the same menu.

9.3 CRC Fail

Figure 84:
CRC Fail



If this dialog message pops up, please check the power supply on the board. If the power supply is connected properly and the problem persists, please use another external power supply instead of the supplied one, as described in section 2.2. If the problem persist, please contact the technical support.

10 Revision Information

Changes from previous version to current revision v1-00	Page
Initial version	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.