



# AS6031-QF\_DK

# **Development Kit User Guide**

# AS6031-QF\_DK User Guide

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#### Introduction 1

The AS6031-DK development kit allows customers a quick and intuitive approach to using the AS6031 UFC in ultrasonic flow meter applications.



# Figure 1: AS6031-QF\_DK Development kit

The kit includes the following elements:

AS6031-QF\_DK\_RB reference board V2.0



PicoProg Lite with USB-C - USB cable



### Figure 2: Functional Blocks

Please download the software for the kit from https://downloads.sciosense.com/as6031 and look for the latest version of UfcEvaluationSoftware....zip.

#### 1.1 **Ordering Codes**

# Table 1: Pin description

Ordering code Part Number		Description					
AS6031-QF_DK V1.0	221020003	AS6031 Demo kit including PICOPROG and cables					
AS6031-QF_DK_RB V2.0	221020002	AS6031 reference board					



# 2 Quick Start Guide

This section describes how to quickly set up the AS6031 development kit, to establish basic operation and to make first measurements.

Please install the software before connecting the evaluation kit to your computer. The software can be downloaded here: <u>https://downloads.sciosense.com/as6031</u>

- Unzip the package to the desired directory,
- Connect the PicoProg Lite to the computer and the AS6031 board to the SPI connector on the PicoProg Lite.
- Connect your spool piece to US\_UP and US\_DOWN. US\_UP fires upstream, means versus flow. US\_DOWN fires downstream, with the flow.
- Open "UFCEvaluationSoftware.exe"

The following screen will appear:

O UFC Evaluation Software v1.2.1		– 🗆 X
ScioSense	Verify Interface and Hardware $^{(j)}$	Projects
Daskbaard     C       Wizard     C       Unance Wearment     C       Results     C       Control     Split Burst       Results & Control     C       Control Control     C       Task Timing     Supplies       Interfaces     Monitoring       Graphs     C       RAM Memory     C	Chip Status C Chip Type ASS031 Communication with Chip OK? OK HS Clock Frequency 7.9863 MHz LP Mode Enubled Measured VCC 3.05 Volt Interface Device Status Interface Device Type PicoProgLite T	Open or Save Project Project files include all configuration settings, firmware data and custom CPU value data. Load Project Save Project Configurations Configs Ready to use with Evaluation System
Registers C Firmware C	Svstem Status	Recently Used Configurations
Start Measurement  Start Measurement  System Reset  Watchdog  Chip Status  TOF SUM  O 00  O 4 00	MCT is Running MCT Count Low MCT Count High Bus Occupied Communication Failed	
Diff. TOF SUM AVG 0 Amplitude Measurement 0 0mV 0 0mV Pube Width Ratio 0 000 0 000 © Reset Rag CLAR 0 Fror Flag CLAR About   Remote Command   Expert Settings	Store Data to File Enable Storing Measurement Data to File	

# Figure 3: Opening page

- Verify that the right device is selected and interface status is ok.
- Select a project or one of the ready configuration files, press "Load Project" or "Load Config" and then on the left side press "Write Config".
- Finally, press "Start Measurement" to begin measuring.





# 3 Hardware Description

# 3.1 Introduction

The AS6031-QF\_DK\_RB board, shown in figure 3, is a front-end for a water or heat meters. The transducers and temperature sensors can be connected to this board directly. It comes with a 32.768 kHz quartz (X2) and a 8 MHz ceramic oscillator (X1).



Figure 4: AS6031-QF\_DK\_RB

# 3.2 Communication Interface

The PicoProg Lite is a USB-to-SPI converter that connects the AS6031 board to a PC. The PICOPROG is registered by the operating system initially as "PicoProg LITE V1.0". The board converts SPI into USB communication. The USB connector is a USB-C one.

The PicoProg Lite comes with two connectors, one for SPI communication and one for I2C communication. For the AS6031 please use the SPI connector.

PicoProg Lite reads interrupt-triggered from the AS6031 board.





# 4 UFC Evaluation Software

The software opens with the dashboard window. It should detect the connected board automatically and indicate operability by green status information (1).

O UFC Evaluation Software v1.2.1		– 🗆 X
ScioSense	Verify Interface and Hardware <sup>①</sup> 1	Projects
Visandoard Wizard Ultrasofic Messurement Results Control Split Burst Temperature Mesurement Results & Control Common Control Task Timing Supplies Interfaces Monitorian	Chip Status       Communication         Chip Type       AS6031         Communication with Chip OK?       OK         HS Clock Frequency       7.9863 MHz         LP Mode       Enabled         Measured VCC       Communication         Interface Device Status       Communication	Open or Save Project Project files include all configuration settings, firmware data and custom CPU value data. Load Project Save Project Configurations Configs Ready to use with Evaluation System
Graphs     C       RAM Memory     C       Registers     C       Firmware     C	Interface Device Type PicoProgLite  PicoProgLite Firmware Version  1.2.1 System Status	Load Config  Recently Used Configurations
Start Measurement Start Measurement Write Config * System Reset Watchdog	MCT is Running     MCT Count Low     MCT Count High     Bus Occupied	Load Config Clear History Import or Export Custom Configuration
Chip Status     MCT is OFF       TOF SUM     ↑     0.0       Diff. TOF SUM AVG     0       Amplitude Measurement     ↑     0 mV       Pulse Width Ratio     ↑     0.00	Communication Failed	Import Config Export Config Export Config as Hex
Reset Flag (CDAR) O Error Flag (CDAR)     About   Remote Commands   Expert Settings     UFC Evaluation Software   © 2020-2022 ScioSense B.V.	Enable Storing Measurement Data to File	

#### Figure 5: Dashboard

The next steps could be to start with one of the default configurations, an existing project or an existing configuration by loading it into the GUI. To write the Data to the Chip you need to click on "Write Config" and then you can start the measurement (3).

Note: when you change parameters in the GUI this is indicated by a star behind "Write Config" (3). Do the write to make sure the chip has the current configuration. The star will then disappear.

Projects include the complete settings of the GUI, including the configuration, the firmware and firmware data, the settings for CPU window and flags.



Figure 6: Dashboard active

On the left green bar the main measurement results are displayed: chip status, time-of-flight (TOF), difference up-down (TOF Difference), amplitude and pulse width ratio (4).

The flags for the measure cycle (5) timer should toggle for an active measurement. The results page will show the detailed ToF results:

UFC Evaluation Software v1.2.1											- 0
ScioSense	TOF Result	s Table 🛈	_				HS Clock	0			10
Dashboard A Vizard C			N for	Avrg 1	\$ 100	÷	Internal HS Clock		_		
Jitrasonic Measurement	# Name		Result [n:	s] Averag	e [ns] Std.De	v. [ps]		7.9865 1	MHz		
Results	1 TOF Sum Aver	age Up	3378	38.55 33	788.55	36.2	HS Clock Di	vider			
Split Burst	2 TOF Sum Aver	age Down	3378	38.55 33	788.55	34.3 6			110.01		
emperature Measurement	3 TOF Difference	e (=Up - Down)		0.00	0.00	39.8	HS clock period (	ideal) 12	HS Cloc	k Divider	Sot
Results & Control	4 TOF Sum (=Up	+ Down)	6757	77.10 67	577.10	58.3		12	5115		Jet
ommon Control Task Timing Supplies	Amplitude	Measure	ment				HS clock period	125.211	2 ns	or HS clock	1.0017
Interfaces	# Name		Result [m	nV] Avrg. [I	nV] Std.De	ev. [mV]	Apply calibr	ated clock	period to display	values	
Monitoring	1 AM UP (mV)		44	12.46	442.46	0.73					
Graphs 🖸	2 AM DOWN (m	V)	44	10.83	440.83	0.65					
RAM Memory C Registers C	Show Deta	led TOF Data		7							
Stop Measurement		TOF		Diffe	rence		Average		Stan	dard Deviatior	1
🖉 Write Config	# Up [ns]	Down [ns]	Δ [ns]	Up [ns]	Down [ns]	Up [ns]	Down [ns]	Δ [ns]	Up [ps]	Down [ps]	Δ [ps] 8
C System Reset	0 32040.05	32040.06	-0.01	-	-	32040.05	32040.06	-0.01	57.3	66.0	73.6
-	1 32541.52	32541.54	-0.02	501.47	501.48	32541.52	32541.54	-0.02	53.8	57.3	74.1
/atchdog	2 33041.23	33041.24	-0.02	499.71	499.71	33041.23	33041.24	-0.02	59.6	47.7	71.0
hip Status MCT is ON	3 33540.43	33540.52	-0.08	499.20	499.27	33540.43	33540.52	-0.08	55.8	53.2	69.4
OF SUM 133788.6 33788.6	4 34038.23	34038.22	0.01	497.80	497.71	34038.23	34038.22	0.01	47.8	53.8	68.1
iff. TOF SUM AVG 0.003	5 34536.05	34535.97	0.08	497.82	497.75	34536.05	34535.97	0.08	58.8	52.6	71.7
unplitude Measurement 1 442 mV 441 mV	6 35035.51	35035.52	-0.01	499.45	499.55	35035.51	35035.52	-0.01	53.9	50.8	67.9
	7 35535.42	35535.34	0.08	499.91	499.82	35535.42	35535.34	0.08	44.4	52.8	59.6
Reset Flag     CLEAR     CLEAR     CLEAR	8 0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.0	0.0	0.0
About   Remote Commands   Expert Settings	9 0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.0	0.0	0.0
JFC Evaluation Software   © 2020-2022 ScioSense B.V.											

# Figure 7: Results page

The ToF results table (6) shows the average of the selected zero crossings per measurement in up and down direction, the difference of up and down (proportional to the flow rate), and the sum of up and down (proportional to speed of sound). By selecting detailed data (7) an additional table pops up that shows each individual zero crossing measurement (8).



The "no. of Avrg." (9) define the numbers of samples for a software average in the GUI. The number on the right, above Std.Dev. define the number of samples used in the mathematics for the calculation of the standard deviation.

The HS Clock block shows the measured period of the high speed clock and the correction factor in comparison to the ideal value. There is a select option for application of this correction factor to the measurement results (10).

The control page shows the main parameters for setting the ultrasonic frontend.

O UFC Evaluation Software v12.1		- a x
ScioSense	Ultrasonic Measurement Control <sup>()</sup>	
Dashboard Wizard	Fire Burst Generator	Amplitude Measurement Show Diagram
Results	Clock Divider for Bunt Generator	AM Peak Detection starts after:
Control		AM peak detection starts after ultrasonic release delay expires 🗢
Split Burst	Fire Burst Frequency	Peak Detection End after ht
Results & Control	No. of Fire Pulses	7
Task Timing	First Hit Level	TOF Measurement
Supplies	Feet Hit Level Up 29 2 2552 mV	Timeout TOF
Interfaces Menitoring		120 yr
Graphs 12	First Mt Level Down	Direction Mode
RAM Memory C	Release Timing	Always starting firing via UP-buffer
Registers 12	Noite Mark Window 1 0.6 us	Selected Start Hit after First Hit Detection
Stop Measurement		
/ West Carlos	Multihit Release Delay Up	No. of IOF Hits for sum
C tystem lanet	Multihit Release Delay Down 3000 \$ 3437.5 ns	
	DxCB (CR_USM_PRC), Bir[19] VSM_RLS_MODE / not used	No. of anored Ht
Wandhaog .	Starfrelease condition der ved try Ultrasonic Release Delay on	
Chip Status MCT is CAL		En Die Pulse Width Detection
DVR. TOF SUM ANG		
Amplitude Measurement 441 mV + 40 mV	Fire Buffer	
Note Wellin Falls	Transducer Fire Buffer Impedance	
Reset Flag (1000)     Error Flag (1000)	Enables 350 Ohm buffer	1
About   Remote Commands   Expert 2 stings		
UFC Evaluation Software   © 2020-2022 Selectense B.V.	PGA	
2V > Stop C1 C2 8 192 samples at 100	MHz   2023-01-25 14:41:44.613	
re The second		v Time 🛞 ▲
LA -	Release delay opens	Position: 23 us v Base: Sublay v
	the measurement	
.2	channel (suppress trigger by noise)	Di Optons -
		Add Channel
N	Noise mask window	V Channel 1 (1±)
	better describes as	Range: 500 mV/dv *
.6	o receive	V Openel 2 (2±)
		Offset: 600 mV -
Cit 1.225V	1	Range: 200 mV/dv 💌
		111111111
	Minimum	
0.2 III''		
<u>م السالييينا</u>		
<u>4  ™</u> -2 us 3 us 8 us	13 us 18 us 23 us 28 us	33 us 38 us 43 us 48 us **
		Manual Trigger   Discovery Z C 5N: 210321A36A48 US8   @/WF3.18.1   Status: OK +

# Figure 8: Control page





In this page you set the fire frequency, derived from the high spedd clock.

With the noise mask window you set the time when to switch from sending to receiving.

The release delay sets the end of a window to suppress wrong triggers by noise.

The first hit level defines the voltage level for the comparator to detect the first hit of the receive burst.

The start hit defines how many waves to wait after first hit level detection before starting collection of ToF data. This time is typically needed by the transducers to follow the fixed fire frequency and to oscillate with a stable period.

The number of Tof hits defines how many zero crossings are summarized for a single measurement in either up or down direction.

Finally, the gain of the PGA is set on this page, too.

Another important page is the Task Timing page:

O UFC Evaluation Software v1.2.1		-	×
ScioSense	Set Timings, Measurement & Calibration Rates $^{()}$		^
Dashboard ^ Wizard C	Settings		
Ultrasonic Measurement Results Control	Base Frequency Select 50 Hz 20 ms		
Split Burst	Cycle Time Task Sequencer 97.7 ms		
Temperature Measurement Results & Control	TOF Rate		
Common Control	Pause between two Ultrasonic Measurements		
Task Timing Supplies	1.0 * T(BF_SEL) ms 20 ms		
Interfaces	Amplitude Measurement Rate		
Monitoring 🗸	Every TOF Trigger		
Stop Measurement	Amplitude Measurement Calibration Rate		
Write Config	Every 10th Amplitude Measurement		
C System Reset	Zero Cross Calibration Rate Window Snip		
	Disabled		
Watchdog	Temperature Measurement every Sequence Cycle Triggers		
Chip Status MCT is ON	0		
TOF SUM 133774.9 133775.4	Temperature Measurement Subtask Handling (Pause Time)		
Diff. TOF SUM AVG -0.504	No Pause, Only One Measurement 🔹 0 ms		
Pulse Width Ratio 10.73 0.73	HS_CLK Calibration Rate		
	Every 100th Measurement		
Reset Flag     CLEAR     O     Error Flag     CLEAR	Voltage Measurement Rate		
About   Remote Commands   Expert Settings UFC Evaluation Software   © 2020-2022 ScioSense B.V.	Every 100th Measurement		~

#### Figure 9: Task timing page

Here you define the sample rate as a combination of the cycle time and the TOF rate (one ToF every N cycles, N typically 1).





Besides the numerical display of the result page the software offers an export of the data into a file as well as a graphical display (which could be fond in the graphs page).



Figure 10: Graphs page

The parameters to be displayed are selectable. By means of the CPU window, any RAM cell can be reported and also graphically displayed.

The export to file is enabled on the main dashboard. The user can select which values should imported.

Note that the file is working with place holders which means that the selection can be changed any time during data acquisition. So you may start with ToF data only, and when you see unexpected behavior then you can add amplitude e.g..



Figure 11: Export selection





The CPU values themselves are defined in the CPU values window and need to correlate with the firmware in the chip. Below is an example of the ScioSense AS6031-F1 Version.

Note: AS6031F1 is a variant of the AS6031 ultrasonic flow converter that comes with a protected flow firmware by ScioSense already programmed into the NVRAM. Based on these algorithms and together with the appropriate calibration and operation parameters, the chip is ready to do the complete flow and volume calculation as well as error handling on chip.

PU Values								-		×
CPU Val	ues at self-defined	RAM Add	resses 🛈							
Results								Current File		
Addr. (Hex)	Description	Raw Data (Hex)	Factor	Result	Unit	Ex				
00	RAM_R_FLOW_VOLUME_INT	00000000	1	0	m³		• ^	Inspect File Related File Except	File	
01	RAM_R_FLOW_VOLUME_FRAC	00000000	2.3283E-10	0	m³			Import File Reload File Export	riie	,
02	RAM_R_FLOW_LPH	00000000	1.52587E-05	0	l/h					
03	RAM_FILTERED_FLOW_LPH	00000000	1.52587E-05	0	l/h					
04	RAM_R_THETA	00000000	1.52587E-05	0	°C		•			
05	RAM_SOUND_VEL	00000000	0.00390625	0	m/s					
06	RAM_FLOW_SPEED	00000000	1.52587E-05	0	m/s					
07	RAM_R_TOF_DIFF	00000000	0.0038147	0	ns					
08	RAM_R_TOF_SUM	00000000	0.0038147	0	ns					
25	RAM_R_FW_STATUS	00000000	1	0						
<						>	~			
Add Item	Remove All			Export No	ne	Export Al				

Figure 12: CPU values example

The monitoring page allows to select flags to be displayed and the flags themselves in action.

<ul> <li>UFC Evaluation Software v1.2.1</li> </ul>				– 🗆 ×
ScioSense	Selected Error Indicators	Interrupt Sources for Remote Interface	Errors	Ô
Cashboard Wizad C Minuer Issesment Results Control Spit Bart Results Control Results Control Cash Issesment Results Control Cash Issesment Sopples Interfaces Monitoring Graphs Cashboard Register C Firmese C C	TOC Timeout ToC Timeout ToC Timeout Amplitude Measurement Timeout Amplitude Measurement Timeout Timeoutate Open Clouit Timeoutate Open Clouit Timeout Unrasonic Sequence Timeout Time	End of Task Sequencer     End of Firmster Transaction     End of Firmster Transaction     End of Biol Chedaum     Synchronous FW BIT Request     Task Sequencer Timeout     Error Flag	TDC Timeout     TDC Timeout     TDC Timeout     TDT Timeout     Anaptitude Measurement Timeout     Temperature Shert Croast     Zero Croas Zalbastion Error     Low Battry Detext     Ultrasonic Sequence Timeout     Temperature Separtnes Timeout     Temperature Sequence Timeout     Lick Advansetegie Error     Change Nump Error     NMM WKU Error	
CPU Volues C Start Measurement Write Config • C System Reset	I2C Acknowledge Error     Charge Plamp Error     NVM FWCU Error     NVM FWCU Error     NVM FWCU Error     NVM FWA Error		NVM FWDU Error NVM FWA Error CFU Error	
Watchdog         MCT is OFF           Chip Stans         MCT is OFF           TO 5 SJM         3 3376.57           Dait TO 5 SJM AGG         4.381           Amplitude Measurement         * 4.371 % 4.484           Puhe Width Ratio         * 0.72         \$ 0.71	CPU Error	ď		
Reset Rag (0000)     Peror Rag (0000)     About   Remote Commands   Expert Settings     UFC Evaluation Software   0 2020-2022 ScioSense B.V.	BNR_AMP_DIFF_TOO_HIGH     BNR_AMP_VAL_TOO_LOW     BNR_PW_DIFF_NOT_OK     BNR_PW_DIFF_NOT_OK			×

#### Figure 13: Monitoring page





For applications with firmware on the chip it is possible to add custom flags according to the firmware. The definition is made in the firmware window.

Barg, Addr. (Hex)         Register Name         Bit Number         B	ownload (	Code and Data	User Cod	e Data	Custom Flags	
Reg. Addr. (Het)         Register Name         Bit Name         Bit Name           27         RAM_R_PW_ERF_LAGS1         1         BNR_AMP_DIFF_TOO_HIGH         0           27         RAM_R_W_URR_FLAGS1         2         BNR_AMP_VAL_TOO_LOW         0           27         RAM_R_W_URR_FLAGS1         3         BNR_W_PVAL_TOO_LOW         0           27         RAM_R_W_URR_FLAGS1         4         BNR_SUMTOF_DEV         0           27         RAM_R_W_URR_FLAGS1         4         BNR_SUMTOF_DEV         0           27         RAM_R_W_URR_FLAGS1         5         BNR_FW_UNCK         0           27         RAM_R_W_URR_FLAGS1         5         BNR_FW_UNCK         0           27         RAM_R_W_URR_FLAGS1         6         BNR_MAS_NOT_CK         0           27         RAM_R_W_URR_FLAGS1         6         BNR_MAS_NOT_CK         0           27         RAM_R_W_URR_FLAGS1         9         BNR_FLOW_UT_NEGUM         0           27         RAM_R_M_URR_FLAGS1         9         BNR_FLOW_UT_NEGUM         0           27         RAM_R_M_URR_FLAGS1         18         BNR_FLOW_UT_NEGUM         0           27         RAM_R_M_URR_FLAGS1         18         BNR_FLOW_UT_NEGUM         0	Custom Flags				Current File	
27         RAM_R_PW_ERR_FLAGS1         1         BNR_AMP_UDF;TOO_HIGH         0         Finder         Expect_	Reg. Addr. (Hex)	Register Name	Bit Number	Bit Name		
27         RAM_R_PM_ERR_FLAGS1         2         INR_AMP_VAL_TOO_LOW         C           27         RAM_R_VM_ERR_FLAGS1         3         INR_PM_DIF_NOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         4         INR_PM_DIF_NOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         5         INR_PM_EMR_DIF_NOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         5         INR_PM_EMR_DIF_NOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         6         INR_MAX_NOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         6         INR_MAXANOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         7         INM_MAREFAULTER         C           27         RAM_R_PM_ERR_FLAGS1         8         INR_PLOW_ERR_FLAGS         C           27         RAM_R_PM_ERR_FLAGS1         9         INR_PLOW_ERR_FLAGS         C           27         RAM_R_PM_ERR_FLAGS1         11         INR_PH_S, FM_VAULD_VMER         C           27         RAM_R_PM_ERR_FLAGS1         12         INR_PH_S, FM_VAULD_VMER         C           27         RAM_R_PM_ERR_FLAGS1         13         INR_PH_S, FM_VAULD_VMER         C           27         RAM_R_M_M_ERR_FLAGS1         14<	27	RAM_R_FW_ERR_FLAGS1	1	BNR_AMP_DIFF_TOO_HIGH	Import from File Reland File Export	
27         RAM_K_PU_RER_FLAGS1         3         INR_PW_DIFF_NOT_OK         0           27         RAM_K_PW_RER_FLAGS1         4         INR_SUMIDE_DIV         0           27         RAM_K_PW_RER_FLAGS1         5         INR_FH_INOT_OK         0           27         RAM_K_PW_RER_FLAGS1         5         INR_FH_INOT_OK         0           27         RAM_K_PW_RER_FLAGS1         6         INR_MAX_NOT_OK         0           27         RAM_K_PW_RER_FLAGS1         7         INR_MEVER_FLAGS1         0           27         RAM_K_PW_RER_FLAGS1         8         INR_FLOW_RE_FLAGS         0           27         RAM_K_PW_RER_FLAGS1         8         INR_FLOW_RE_FLAGS         0           27         RAM_K_PW_RER_FLAGS1         8         INR_VCL_SR         0           27         RAM_K_PW_RER_FLAGS1         10         INR_VCL_SR         0           27         RAM_K_PW_RER_FLAGS1         11         INR_VPL_SR_VCL_SR         0           27         RAM_K_PW_RER_FLAGS1         12         INR_VFL_SR_VM_LDW_REF         0           27         RAM_K_PW_RER_FLAGS1         12         INR_VFL_SR_VR_SR_FLAGS         0           27         RAM_K_PW_RER_FLAGS1         13         INR_VVL_SR_RSR	27	RAM_R_FW_ERR_FLAGS1	2	BNR_AMP_VAL_TOO_LOW	Û	
27         RAM_R_FW_ERR_FLAGS1         4         INR_SUMTOF_DEV         C           27         RAM_R_FW_ERR_FLAGS1         5         INR_FH_NOT_OK         C           27         RAM_R_FW_ERR_FLAGS1         6         INR_MAS_NOT_OK         C           27         RAM_R_FW_ERR_FLAGS1         6         INR_MAS_NOT_OK         C           27         RAM_R_FW_ERR_FLAGS1         7         INR_FLAMMADWARE_FAILURE         C           27         RAM_R_FW_ERR_FLAGS1         8         INR_FLOW_ER_FLAMS         C           27         RAM_R_FW_ERR_FLAGS1         9         INR_FLOW_ER_FLAMS         C           27         RAM_R_FW_ERR_FLAGS1         9         INR_FLOW_ER_FLAMS         C           27         RAM_R_FW_ERR_FLAGS1         11         INR_FLOW_ER_FLAMS         C           27         RAM_R_FW_ERR_FLAGS1         11         INR_FLOW_ERR_FLAMS         C           27         RAM_R_FW_ERR_FLAGS1         12         INR_FW_ERR_FLAMS         C           27         RAM_R_FW_ERR_FLAGS1         13         INR_FW_ERR_FLAMS         C           27         RAM_R_FW_ERR_FLAGS1         13         INR_VE_ERR         C           27         RAM_R_FW_ERR_FLAGS1         13         INR_FW_ERR	27	RAM_R_FW_ERR_FLAGS1	3	BNR_PW_DIFF_NOT_OK		
27         RAM_R_PM_ERR_FLAGS1         5         INR_FHL_NOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         6         INR_MAS_NOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         6         INR_MAS_NOT_OK         C           27         RAM_R_PM_ERR_FLAGS1         7         INR_MADAWAE FAULURE         C           27         RAM_R_PW_ERR_FLAGS1         8         INR_FLOW_ERR_FLAGS1         C           27         RAM_R_PW_ERR_FLAGS1         9         INR_FLOW_ERR_FLAGS1         C           27         RAM_R_PW_ERR_FLAGS1         10         INR_FVS_T_VAULU_WRG         C           27         RAM_R_PW_ERR_FLAGS1         11         INR_FVS_T_VAULU_WRG         C           27         RAM_R_PW_ERR_FLAGS1         12         INR_PVS_T_S_W_UNUU_WRG         C           27         RAM_R_PW_ERR_FLAGS1         12         INR_PVS_T_S_W_UNUU_WRG         C           27         RAM_R_PW_ERR_FLAGS1         13         INR_VVE_ERROR         C           27         RAM_R_FVLORS1         14         INR_VVE_ERROR         C	27	RAM_R_FW_ERR_FLAGS1	4	BNR_SUMTOF_DEV	<b>(</b>	
27         RAM_R_M_USR_FLAGS1         6         NNM_MAS_NOT_OK         C           27         RAM_LUW_ERR_FLAGS1         7         INN_UNARUMARLFALLURE         C           27         RAM_R_W_RR_FLAGS1         8         INN_UNARUMARLFALLURE         C           27         RAM_R_W_RR_FLAGS1         8         INN_UNU_R_M_RAW         C           27         RAM_R_W_RR_FLAGS1         9         INN_UU_RR_M         C           27         RAM_R_W_RR_FLAGS1         10         INN_UU_RR         C           27         RAM_R_W_RR_FLAGS1         11         INN_UU_RR         C           27         RAM_R_W_RR_FLAGS1         12         INN_UU_RR         C           27         RAM_R_W_RR_FLAGS1         13         INN_UU_RR         C           27         RAM_R_W_RR_FLAGS1         13         INN_UU_RR         C           27         RAM_R_W_RR_FLAGS1         14         INN_UU_RR         C	27	RAM_R_FW_ERR_FLAGS1	5	BNR_FHL_NOT_OK	0	
27         RAM_RPW_ERR_FLAGS1         7         INR_HARDWARE_FAILURE         6           27         RAM_RPW_ERR_FLAGS1         8         INR_FLOW_ET_AUXX         6           27         RAM_RPW_ERR_FLAGS1         9         INR_FLOW_ET_AUXX         6           27         RAM_RPW_ERR_FLAGS1         9         INR_FLOW_ET_AUXX         6           27         RAM_RPW_ERR_FLAGS1         9         INR_FLOW_ET_AUXX         6           27         RAM_RPW_ERR_FLAGS1         18         INR_PH_S_FW_AUXD_WING         6           27         RAM_RPW_ERR_FLAGS1         11         INR_PH_S_FW_AUXD_WING         6           27         RAM_RPW_ERR_FLAGS1         12         INR_PH_S_FW_AUXD_WING         6           27         RAM_RPW_ERR_FLAGS1         12         INR_PH_S_FW_AUXD_WING         6           27         RAM_RPW_ERR_FLAGS1         13         INR_PH_S_FW_AUXD_WING         6           27         RAM_RPW_ERR_FLAGS1         13         INR_VELERRING         6           27         RAM_RPW_ERR_FLAGS1         13         INR_VELERRE         6	27	RAM_R_FW_ERR_FLAGS1	6	BNR_MEAS_NOT_OK	<b>a</b>	
27         RAM_R_PW_ERR_FLAGS1         a         INR_FLOW_BT_ZMAX         C           27         RAM_R_PW_ERR_FLAGS1         9         INR_FLOW_IT_NECIM         C           27         RAM_R_PW_ERR_FLAGS1         10         INR_FLOW_IT_NECIM         C           27         RAM_R_PW_ERR_FLAGS1         10         INR_FV_S_RR_F         C           27         RAM_R_PW_ERR_FLAGS1         11         INR_FP_S_FW_VALID_WING         C           27         RAM_R_PW_ERR_FLAGS1         12         INR_FP_S_FW_VALID_WING         C           27         RAM_R_PW_ERR_FLAGS1         13         INR_FP_S_FW_VALID_WING         C           27         RAM_R_PW_ERR_FLAGS1         13         INR_VELERROR         C           27         RAM_R_PW_ERR_FLAGS1         13         INR_VELERROR         C	27	RAM_R_FW_ERR_FLAGS1	7	BNR_HARDWARE_FAILURE	0	
27         RAM_E_PU_ERR_FLAGS1         9         ININ_FLOW_LT_NEGUM         1           27         RAM_LT_WERR_FLAGS1         10         ININ_FV_ERW_NOLD         1         1           27         RAM_E_PU_ERR_FLAGS1         10         ININ_FV_E_W_NOLD         1 <td< td=""><td>27</td><td>RAM_R_FW_ERR_FLAGS1</td><td>8</td><td>BNR_FLOW_BT_2MAX</td><td>0</td><td></td></td<>	27	RAM_R_FW_ERR_FLAGS1	8	BNR_FLOW_BT_2MAX	0	
27         RAM_R_PW_ERR_FLAGS1         10         RNR_VOL_ERR         10           27         RAM_R_PW_ERR_FLAGS1         11         RNR_PM_S_PW_UNID_WRG         10           27         RAM_R_VU_ERR_FLAGS1         12         RNR_PM_S_PW_UNID_WRG         10           27         RAM_R_VW_ERR_FLAGS1         12         RNR_VM_ERR_ERR         10           27         RAM_R_VW_ERR_FLAGS1         13         RNR_VM_ERR         10           27         RAM_R_VW_ERR_FLAGS1         13         RNR_VM_ERRER         10	27	RAM_R_FW_ERR_FLAGS1	9	BNR_FLOW_LT_NEGUM	Ū.	
27         RAM_R.PW_ERR_FLAGS1         11         INR_PH_S_FW_VAID_WRG         Image: Second Seco	27	RAM_R_FW_ERR_FLAGS1	10	BNR_VOL_ERR	0	
27         RAM_R_PW_ERR_FLAGS1         12         INR_PH_S_FW_UMP_DET_ERR         Image: Comparison of the comparis	27	RAM_R_FW_ERR_FLAGS1	11	BNR_PH_S_FW_VALID_WRG	0	
27 RAM.R.FW.ERR.FLAGS1 13 BNR.VEL.ERROR 27 RAM.R.FW.ERR.FLAGS1 14 BNR.BUBBLE	27	RAM_R_FW_ERR_FLAGS1	12	BNR_PH_S_FW_JUMP_DET_ER	R 🗊	
27 RAM_R_FW_ERR_FLAGS1 14 BNR_BUBBLE	27	RAM_R_FW_ERR_FLAGS1	13	BNR_VEL_ERROR		
	27	RAM_R_FW_ERR_FLAGS1	14	BNR_BUBBLE	<b>a</b> .	

## Figure 14: Monitoring Example custom flags

If you want to work with firmware on the AS6031 the you need the Firmware window.

Download Code and Data	User Code Data Cus	tom Flags
Q Verify Firmware	Import Firmware User Code from File	12 > Compile Firmware
<u>Î</u> Erase Firmware	🦆 Import Firmware Data from File	🛃 Download FW Code & Data
Open CPU Assembler Instruction Help  හ		Sys. Reset & Start Measurement after Download
<u>Open CPU Assembler Instruction Help ೆ</u> Checksums Software	Checksums Hardware	Sys. Reset & Start Measurement after Download
Open CPU Assembler Instruction Help 2 Checksums Software Firmware Code User	Checksums Hardware	Sys. Reset & Start Measurement after Download       Lock FW after Download       Checksums FWD       O     Firmware Code User     0
Open CPU Assembler Instruction Help ක් Checksums Software Firmware Code User	Checksums Hardware Firmware Code User Firmware Code ScioSense	O       Firmware Code User       0         3F91       Firmware Code ScioSense       3F91
Open CPU Assembler Instruction Help C Checksums Software Firmware Code User	Checksums Hardware D Firmware Code User Firmware Code ScioSense Firmware Data User	Sys. Reset & Start Measurement after Download       Lock FW after Download       Checksums FWD       Firmware Code User     0       Firmware Code ScioSense     3F91       Firmware Data User     0

Figure 15: Firmware window

On the main page you can load the files with the firmware hex code and the firmware data (12). You download them (13) and monitor the checksums to see the success of the process.

The User Code page sets a focus to the firmware hex file.

The Data page allows to review the firmware data in detail, to add a description and also a scaling factor to convert the integer value into a reasonable physical value.

The assembler converts a text file into a hex file. There is no editor integrated. We recommend standard text editors like Notepad++.





Firmwar	e			_		_		×
Do	wnload Code and Da	ata	User (	Code	Data	Custom	n Flags	
FW	Data					Read 🕻	Current File	
#	Name	Signed	Value (dec)	Value (hex)	Factor	Calculated		
0	FWD_FWU_CS user code check		115021	0001C14D	1	115021	Import from File Reload File	
1	FWD_FWDU_CS user data chec		27283	00006A93	1	27283	Export Export Hex Values to File	
2	FWD_JUMP_FLAG		1	00000001	1	1		
3	FWD_ERROR_COUNT_CONF1		4294967295	FFFFFFFF	1	4294967295	Iransfer Configuration Settings	
4	FWD_ERROR_COUNT_CONF2		4294967295	FFFFFFF	1	4294967295	From GUI to FW Data From FW Data to GUI	
5	FWD_ERROR_COUNT_21		0	00000000	1	0	Transfer Firmware Parameters	
6	FWD_ERROR_COUNT_43		0	00000000	1	0	Set Bootloader Release Code	
7	FWD_ERROR_COUNT_INV21		4294967295	FFFFFFFF	1	4294967295		
8	FWD_ERROR_COUNT_INV43		4294967295	FFFFFFF	1	4294967295	FW Data	
9			0	00000000	1	0	Download Recall Read	
10			0	00000000	1	0	Chastering	~
11			0	00000000	1	0	Checksums	5
12			0	00000000	1	0	By Software By Hardware FWD	_
13			0	00000000	1	0	User 6B3B 0 0	)
14			0	00000000	1	0	ScioSense 46F 46F	=
						~		

#### Figure 16: Firmware Data page

The settings for the firmware data are stored in the project files, but can also be imported/exported.

You can read the firmware data that are in the chip by means of a recall and read and then transfer them into the GUI parameter settings (firmware data include the configuration).

Vice versa, you can transfer the configuration from the GUI into the firmware data and with a download into the non-volatile RAM of the chip.

For more details about how to write your own firmware please take a look into the application note: "AS6031/40 How to write custom firmware". <u>https://www.sciosense.com/wp-</u> <u>content/uploads/documents/SC-001548-AN-1-AS60xx-How-to-Write-Custom-Firmware.pdf</u>



5 Schematics, Layers & BOM



Figure 17: AS6031-QF\_DK\_RB schematics









Figure 18: AS6031-QF\_DK\_RB layout 2:1t



Figure 19: AS6031-QF\_DK\_RB assembly 2:1

Table 2: Bill of materials for AS6031-QF\_DK\_RB V2.0

Quantity	Designator	Value	Comment	Footprint
3	C1, C10, C11	10p	C603	0603
1	C2	nc	C603	0603
5	C3, C4, C5, C7, C28	100n	C603	0603
1	C6	680n	C603	0603
1	C8	0R	C603	0603
1	C9	330n	C603	0603
2	C12, C32	100u	C805	0805
1	C13	10n	C603	0603



CONTENTS PAGE

1	C14	2u2	C603	0603
1	C18	22p	C603	0603
1	C29	100n C0G	C1206	1206R
2	J1, J5		ST/254_7_1R	ST/254_7_1R
3	J2, J3, J4		ST/254_2	ST/254_2
5	J6, J12, J13, J14, J15		PAD1.8mm	PAD1.8mm
3	R1, R2, R3	4R7	R603	0603
2	R4, R11	1k	R805	0805
1	R5	5.6k	R603	0603
1	R6	2.2k	R603	0603
1	R8	10M	R603	0603
1	R9	nc	R603	0603
1	R10	560k	R603	0603
1	R12	22k	R805	0805
1	R16	1k	R603	0603
1	R19	1M	R603	0603
12	TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP17, TP22, TP23		PAD1mm	PAD1mm
1	U1		AS6031-BQF	48QFN_7x7
1	U2	3,0V	XC6206	SOT23_TOREX
1	U3		LMP7711	SOT23_6
1	X1	8MHz	Q/CSTCR_G+	Q/CSTCR_G - CSTNE8MHz
1	X2	32,768kHz	Q/KX-327XS	Q/KX-327XS





# 6 RoHS Compliance & ScioSense Green Statement

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ScioSense Green (RoHS compliant and no Sb/Br): ScioSense Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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# 8 Revision information

#### Table 3: Revision history

Revision	Date	Comment	Page
2.0	2020 May 19	Change of ownership from ams to ScioSense, status to release	All
3.0	2020 Jun 30	Document number changed	All
4.0	2021 Apr 28	Software description now refers to new Software, iESLab plastic spool piece removed	All
5.0	2021 Oct 22	Reference to update schematics and layout of reference board. PICOPROG picture. Transfer into new ScioSense layout	All
6.0	2023 Feb 10	Old PICOPROG replaced by new PicoProg Lite. Section for software description added	All

#### Note(s) and/or Footnote(s):

- 1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- 2. Correction of typographical errors is not explicitly mentioned.