Document Title

1M x 8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Date	Remark
1.0	-. Initial Draft	Aug. 7 2013	Preliminary
2.0	-. Amend Functional Block Diagram and Pin Configurations	Mar. 7 2017	

FEATURES

- Process Technology : 0.15 µm Full CMOS
- Organization : 1M x 8 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V(Min.)
- Three state output and TTL Compatible
- Package Type : 48-FPBGA, 44-TSOP2

GENERAL DESCRIPTION

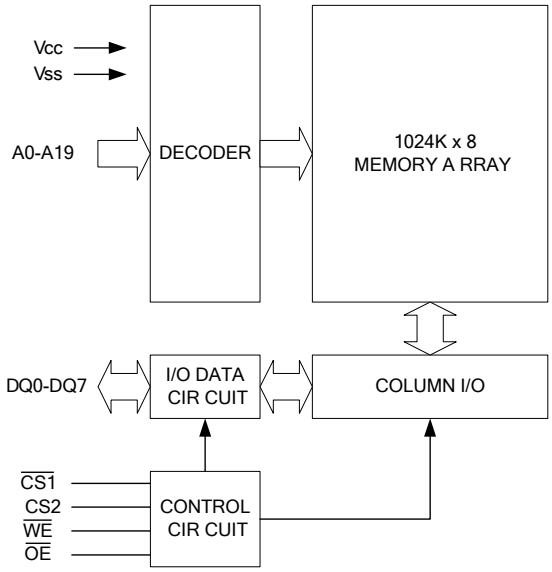
The AS6C8008A families are fabricated by Alliance Memory's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back- up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		Package Type
				Standby (I_{SB1},TYP.)	Operating (Icc1,Max.)	
AS6C8008A-45BIN	Industrial -40 ~ 85℃	2.7 ~ 3.6 V	45ns	2 mA[1)]	4 mA	48-FPBGA
AS6C8008A-45ZIN						44-TSOPII

[1)]Typical values are measured at Vcc=3.3V, T_A=25°C and not 100% tested.

FUNCTIONAL BLOCK DIAGRAM

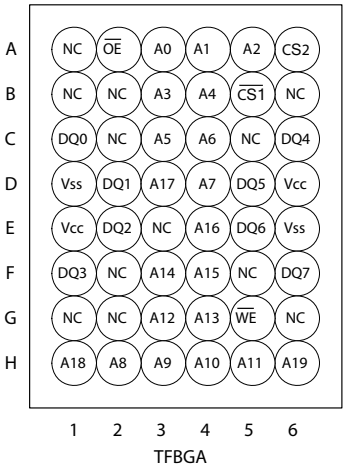


PIN DESCRIPTION

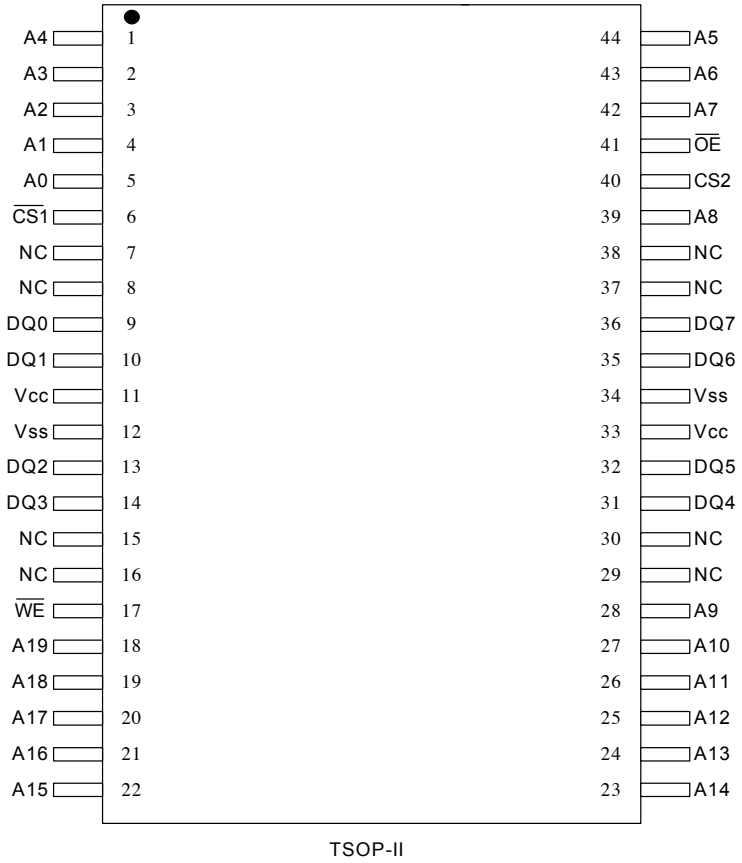
SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATIONS

TFBGA - 48:Top view(ball down)



44 - TSOPII:Top view



ABSOLUTE MAXIMUM RATINGS[1)]

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.2 to 4.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	℃

1. Stresses greater than those listed under "nav" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	DQ0~7	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

Note: X = Don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	V_{CC} + 0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. TA= -40 to 85°C, otherwise specified
2. Overshoot: VCC +2.0 V in case of pulse width ≤ 20ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not100% tested

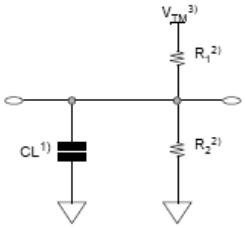
DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	$V_{IN}=V_{SS}$ to V_{CC}		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{IO}=V_{SS}$ to V_{CC}		-1	-	1	µA
Operating power supply	I_{CC}	I_{IO}=0mA $\overline{CS1}=V_{IL}$, CS2=$\overline{WE}=V_{IH}$, $V_{IN}=V_{IH}$ or , V_{IL}		-	-	2	mA
Average operating current	I_{CC1}	Cycle time=1 s, 100% duty, I_{IO}=0mA, $\overline{CS1}\leq$0.2V, CS2$\geq V_{CC}$-0.2V, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$-0.2V		-	-	4	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS1}=V_{IL}$, CS2=V_{IH}, $V_{IN}=V_{IL}$ or V_{IH}	45ns	-	-	45	mA
			55ns	-	-	35	
			70ns	-	-	25	
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Standby Current (TTL)	I_{SB}	$\overline{CS1}=V_{IH}$, CS2=V_{IL}, Other inputs=V_{IH} or V_{IL}		-	-	0.5	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS1}\geq V_{CC}$- 0.2V, CS2$\geq V_{CC}$- 0.2V (CS1 controlled) or 0V<CS2<0.2V (CS2 controlled), Other inputs = 0~V_{CC} (Typ. condition : V_{CC}=3.3V @ 25oC) (Max. condition : V_{CC}=3.6V @ 85°C)	LF	-	2 1)	15	µA

1. Typical values are measured at Vcc=3.3V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)
Input Pulse Level : 0.4 to 2.4V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 1.5V
Output Load (See right) : $CL^{1)}$ = 100pF+ 1 TTL(70nsec)
$CL^{1)}$ = 30pF + 1 TTL(45ns/55ns)
1. Including scope and Jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM}=2.8V
4. CL = 5pF + 1 TTL (measurement with t_{LZ}, t_{HZ}, t_{OLZ}, t_{OHZ}, t_{WHZ})



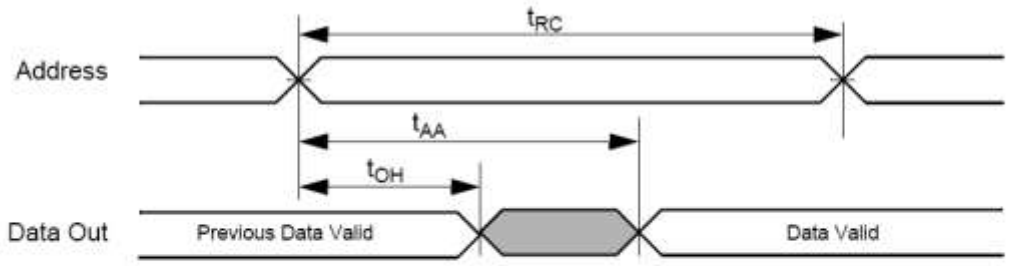
READ CYCLE (V_{CC} =2.7 to 3.6V, Gnd = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	45ns		Unit
		Min	Max	
Read cycle time	^tRC	45	-	ns
Address access time	^tAA	-	45	ns
Chip select to output	$^tCO1$, $^tCO2$	-	45	ns
Output enable to valid output	^tOE	-	30	ns
Chip select to low-Z output	$^tLZ1$, $^tLZ2$	5	-	ns
Output enable to low-Z output	^tOLZ	5	-	ns
Chip disable to high-Z output	$^tHZ1$, $^tHZ2$	0	20	ns
Output disable to high-Z output	^tOHZ	0	20	ns
Output hold from address change	^tOH	10	-	ns

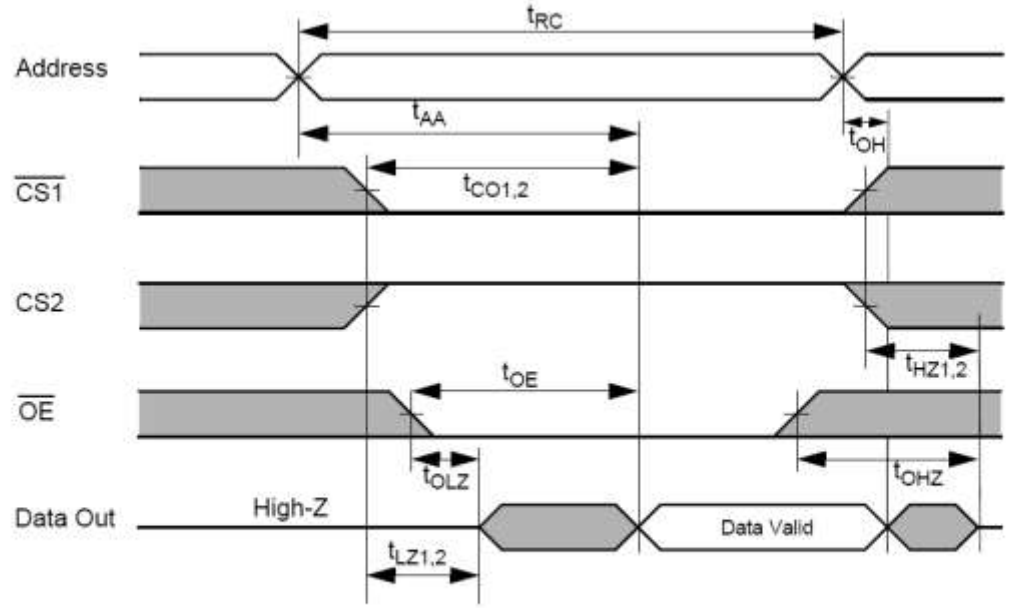
Parameter	Symbol	45ns		Unit
		Min	Max	
Write cycle time	^tWC	45	-	ns
Chip select to end of write	$^tCW1$,$^tCW2$	45	-	ns
Address setup time	^tAS	0	-	ns
Address valid to end of write	^tAW	45	-	ns
Write pulse width	^tWP	45	-	ns
Write recovery time	^tWR	0	-	ns
Write to ouput high-Z	^tWHZ	0	20	ns
Data to write time overlap	^tDW	25	-	ns
Data hold from write time	^tDH	0	-	ns
End write to output low-Z	^tOW	5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH})



TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})

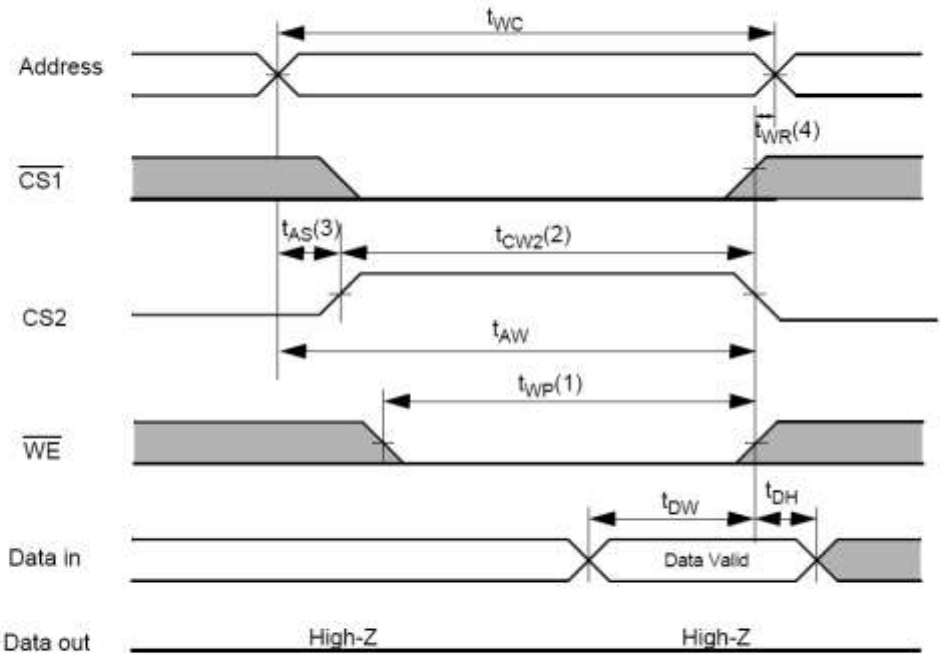


NOTES (READ CYCLE)

1.$t_{HZ1,2}$ and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2.At any given temperature and voltage condition, $t_{HZ1,2}$(Max.) is less than $t_{LZ1,2}$(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ goes low, CS2 goes high and $\overline{WE}$ goes low. A write ends at the earliest transition among $\overline{CS1}$ goes high, CS2 goes low and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low.

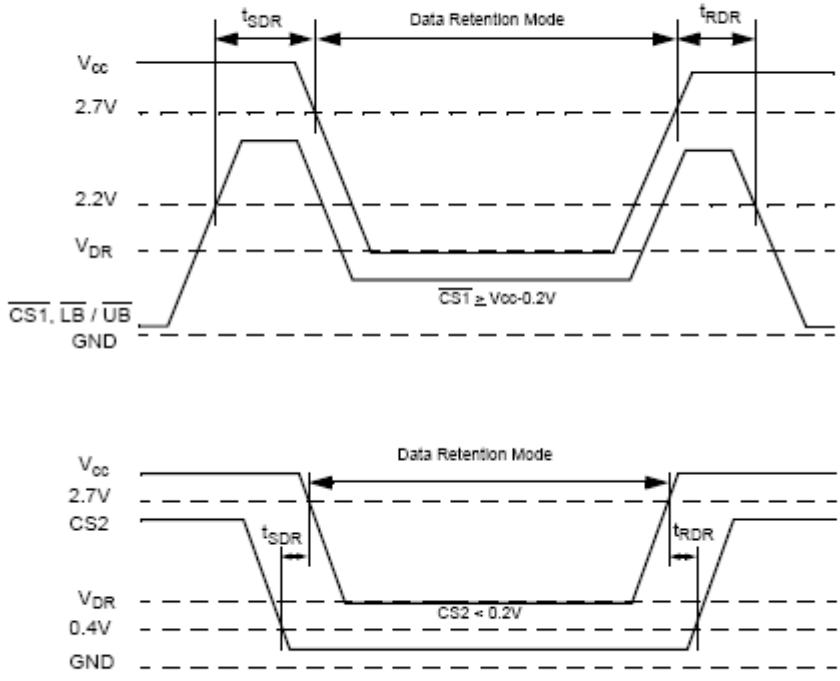
DATA RETENTION CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	^{v}DR	I_{SB1} Test Condition (Chip Disabled)[1)]	1.5	-	3.6	V
Data Retention Current	^{I}DR	V_{CC}=1.5V, I_{SB1} Test Condition (Chip Disabled)[1)]	-	-	4	µA
Chip Deselect to Data Retention Time	^{t}SDR	See data retention wave form	0	-	-	ns
Operation Recovery Time	^{t}RDR		^{t}RC	-	-	

NOTES

1. See the I_{SB1} measurement condition of datasheet page 5.

DATA RETENTION WAVE FORM



PACKAGE DIMENSION

44 - TSOP2 (0.8mm pin pitch)

Unit : millimeters / inches