



## Datasheet

DS001046

# AS7343

## 14-Channel Multi-Spectral Sensor

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# 1 General Description

The **ams** AS7343 is a 14-channel highly versatile, multi-purpose spectral sensor enabling new consumer, commercial, industrial and laboratory applications. It is optimized for reflective, transmissive and emissive measurements including color matching, fluid or reagent analysis, lateral flow test applications and spectral identification in the visible range.

The spectral response is defined by individual channels covering approximately 380 nm to 1000 nm with 11 channels centered in the visible spectrum (VIS), plus one near-infrared (NIR) and a clear channel.

AS7343 integrates high-precision optical filters onto standard CMOS silicon via deposited interference filter technology. A built-in aperture controls the light entering the sensor array to increase accuracy. A programmable digital GPIO and LED driver enable light source and trigger/sync control. Device control and spectral data access is implemented through a serial I<sup>2</sup>C interface. The device is available in an ultra-low profile package with dimensions of 3.1 mm x 2 mm x 1 mm.

## 1.1 Key Benefits & Features

The benefits and features of AS7343, 14-Channel Multi-Spectral Sensor, are listed below:

**Figure 1:**  
**Added Value of Using AS7343**

Benefits	Features
Highly versatile multi-purpose spectral sensor	<ul style="list-style-type: none"> <li>• 14 channels between 380 nm and 1000 nm</li> <li>• Reflective, transmissive and emissive applications</li> </ul>
Highest sensitivity	<ul style="list-style-type: none"> <li>• Enables ultra-low light operation</li> <li>• Enables operation behind dark glass or additional external filters</li> </ul>
Low power consumption and minimum I <sup>2</sup> C traffic	<ul style="list-style-type: none"> <li>• 1.8 V VDD operation</li> <li>• Configurable sleep mode</li> <li>• Interrupt-driven device</li> </ul>
Ultra-high integration	<ul style="list-style-type: none"> <li>• On chip interference filter technology</li> <li>• Integrated LED driver and 6 integrated ADCs</li> <li>• 3.1 mm x 2 mm x 1 mm package outline</li> </ul>

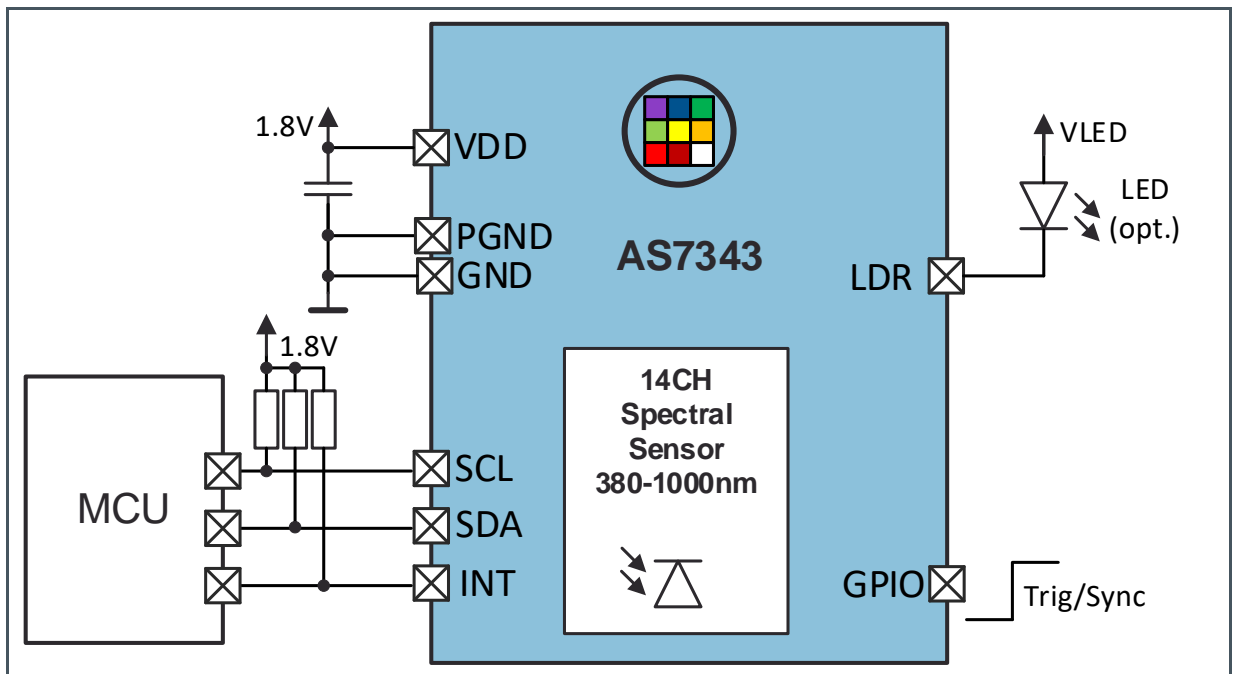
## 1.2 Applications

- Emissive light measurement
- Transmissive and reflective measurements such as fluid or color measurements
- Photoelectric smoke detectors

## 1.3 Block Diagram

The functional blocks of this device are shown below:

**Figure 2 :**  
**Functional Blocks of AS7343**



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## 2 Ordering Information

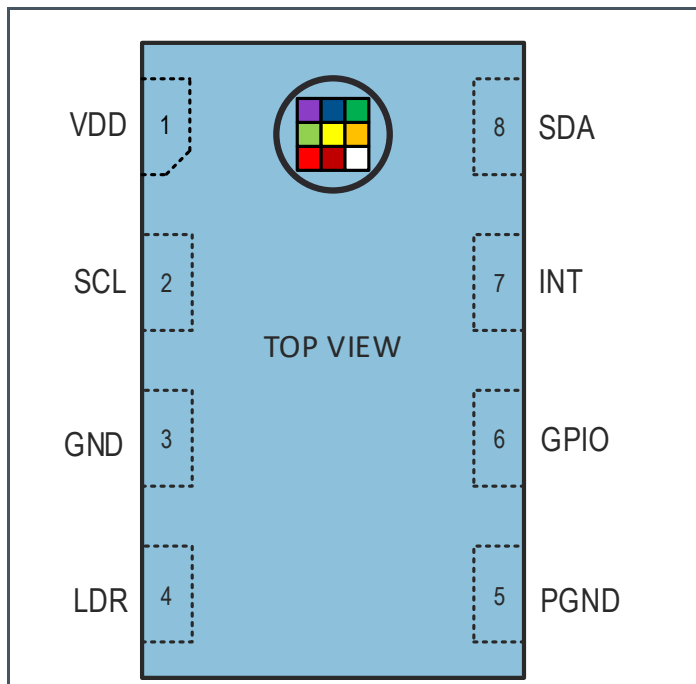
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Ordering Code	Package	Delivery Form	Delivery Quantity	I2C Slave Address
AS7343-DLGT	OLGA-8	Tape & Reel 13-inch	10000 pcs/reel	0x39
AS7343-DLGM	OLGA-8	Tape & Reel 7-inch	500 pcs/reel	0x39
AS7343B-DLGT	OLGA-8	Tape & Reel 13-inch	10000 pcs/reel	0x29

# 3 Pin Assignment

## 3.1 Pin Diagram

Figure 3:  
Pin Assignment of AS7343 (TOP VIEW)



## 3.2 Pin Description

Figure 4:  
Pin Description of AS7343

Pin Number	Pin Name	Pin Type <sup>(1)</sup>	Description
1	VDD	P	Positive supply voltage terminal
2	SCL	DI	Serial interface clock signal line for I <sup>2</sup> C interface. Connect pull up resistor to 1.8 V.
3	GND	P	Ground. All voltages referenced to GND
4	LDR	A_I/O	LED current sink input. If not used leave pin unconnected.
5	PGND	P	Ground. All voltages referenced to GND
6	GPIO	D_I/O	General purpose input/output. Default output open drain. If not used leave pin unconnected.

Pin Number	Pin Name	Pin Type <sup>(1)</sup>	Description
7	INT	DO_OD	Interrupt. Open drain output active low. Connect pull up resistor to 1.8 V. If not used leave pin unconnected.
8	SDA	D_I/O	Serial interface data signal line for I <sup>2</sup> C interface. Connect pull up resistor to 1.8 V.

- (1) Explanation of abbreviations:
- DI Digital Input
  - D\_I/O Digital Input/Output
  - DO\_OD Digital Output, open drain
  - P Power pin
  - A\_I/O Analog pin

## 4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltages with respect to GND/PGND. Device parameters are guaranteed at  $V_{DD}=1.8\text{ V}$  and  $T_A=25\text{ °C}$  unless otherwise noted.

**Figure 5:**  
**Absolute Maximum Ratings of AS7343**

Symbol	Parameter	Min	Max	Unit	Comments
<b>Electrical Parameters</b>					
$V_{DD} / V_{GND}$	Supply Voltage to Ground	-0.3	1.98	V	Applicable for pin VDD
$V_{ANA\_MAX}$	Analog Pins	-0.3	3.6	V	Applicable for pin LDR
$V_{DIG\_MAX}$	Digital Pins	-0.3	3.6	V	Applicable for pins SCL, SDA, GPIO and INT
$I_{SCR}$	Input Current (latch-up immunity)		$\pm 100$	mA	AEC-Q100-004E
$I_O$	Output Terminal Current	-1	20	mA	
<b>Electrostatic Discharge</b>					
$ESD_{HBM}$	Electrostatic Discharge HBM		$\pm 2000$	V	JS-001-2017
$ESD_{CDM}$	Electrostatic Discharge CDM		$\pm 500$	V	JS-002-2018
<b>Temperature Ranges and Storage Conditions</b>					
$T_A$	Operating Ambient Temperature	-30	85	°C	
$T_{STRG}$	Storage Temperature Range	-40	85	°C	
$T_{BODY}$	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 <sup>(1)</sup>
$RH_{NC}$	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level		3		Maximum floor life time of 168h

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn)



## 5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at VDD=1.8 V and T<sub>A</sub>=25 °C unless otherwise noted.

**Figure 6:**  
Electrical Characteristics of AS7343

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply Voltage		1.7	1.8	1.98	V
T <sub>A</sub>	Operating free-air temperature <sup>(1)</sup>		-30	25	85	°C
<b>Power Consumption</b>						
IDD	Supply Current <sup>(2)</sup>	VDD=1.8 V; T <sub>A</sub> =25 °C Active mode <sup>(3)</sup>		210	280	μA
		VDD=1.8 V; T <sub>A</sub> =25 °C Idle mode <sup>(4)</sup>		40	60	μA
		VDD=1.8 V; T <sub>A</sub> =25 °C Sleep mode <sup>(5)</sup>		0.7	5	μA
<b>Digital Pins</b>						
V <sub>IH</sub>	SCL,SDA input high voltage		1.26			V
V <sub>IL</sub>	SCL,SDA input low voltage				0.54	V
V <sub>OL</sub>	INT, SDA output low voltage	6 mA sink current			0.4	V
C <sub>I</sub>	Input pin capacitance				10	pF
I <sub>leak</sub>	Leakage current into SCL,SDA,INT pins		-5		5	μA
<b>GPIO</b>						
C <sub>LOAD</sub>	Maximum capacitive load GPIO				20	pF
<b>LED Driver</b>						
V <sub>LDR</sub>	LDR compliance voltage	I <sub>LDR</sub> = 4 mA ; LED_HALF = "0"			240	mV
		I <sub>LDR</sub> = 4 mA ; LED_HALF = "1"			130	
		I <sub>LDR</sub> 134 mA ; LED_HALF = "0"			280	mV
		I <sub>LDR</sub> 134 mA ; LED_HALF = "1"			180	

- (1) While the device is operational across the temperature range, functionality will vary with temperature.
- (2) Supply current values are shown at the VDD pin and do not include current through pin LDR.
- (3) Active state occurs during active integration. (PON = "1" ; SP\_EN = "1") If wait is enabled (WEN = "1"), supply current is lower during the wait period
- (4) Idle state occurs when PON = "1" and all functions are disabled
- (5) Sleep state occurs when PON = "0" and I<sup>2</sup>C bus is idle. If I<sup>2</sup>C traffic is active device automatically enters idle mode.

## 6 Optical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at VDD=1.8 V and T<sub>A</sub>=25 °C unless otherwise noted.

**Figure 7:**  
**AS7343 Optical Channel Summary**

Channel	Peak Wavelength [nm] <sup>(1)(2)</sup>			Full Width Half Maximum [nm]
	(min)	λ <sub>p</sub> (typ)	(max)	(typ)
F1	395	405	415	30
F2	415	425	435	22
FZ	440	450	460	55
F3	465	475	485	30
F4	505	515	525	40
FY	545	555	565	100
F5	540	550	560	35
FXL	590	600	610	80
F6	630	640	650	50
F7	680	690	700	55
F8	735	745	755	60
NIR	845	855	865	54

- (1) Parameter measured on a production ongoing sample bases on glass using diffused light. The table above is valid for full sensor response including diffuser, package and photodiode response.
- (2) Peak Wavelength is validated by smoothed/averaged monochromator measurement data.

**Figure 8:**  
**Optical Characteristics of Spectral Channels, AGAIN: 1024x, Integration Time: 27.8 ms**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>e_F1</sub>	Irradiance responsivity channel F1	LED_396nm ; Ee= 155 mW/m <sup>2</sup> LED_408 nm ; Ee= 155 mW/m <sup>2</sup>	4311	5749	7186	counts
R <sub>e_F2</sub>	Irradiance responsivity channel F2	LED_408nm ; Ee= 155 mW/m <sup>2</sup> LED_448nm ; Ee= 155 mW/m <sup>2</sup>	1317	1756	2196	counts
R <sub>e_FZ</sub>	Irradiance responsivity channel FZ	LED_428nm ; Ee= 155 mW/m <sup>2</sup> LED_480nm ; Ee= 155 mW/m <sup>2</sup>	1627	2169	2711	counts
R <sub>e_F3</sub>	Irradiance responsivity channel F3	LED_448nm ; Ee= 155 mW/m <sup>2</sup> LED_500nm ; Ee= 155 mW/m <sup>2</sup>	577	770	962	counts
R <sub>e_F4</sub>	Irradiance responsivity channel F4	LED_500nm ; Ee= 155 mW/m <sup>2</sup> LED_534nm ; Ee= 155 mW/m <sup>2</sup>	2356	3141	3926	counts
R <sub>e_FY</sub>	Irradiance responsivity channel FY	LED_534nm ; Ee= 155 mW/m <sup>2</sup> LED_593nm ; Ee= 155 mW/m <sup>2</sup>	2810	3747	4684	counts
R <sub>e_F5</sub>	Irradiance responsivity channel F5	LED_531nm ; Ee= 155 mW/m <sup>2</sup> LED_594nm ; Ee= 155 mW/m <sup>2</sup>	1180	1574	1967	counts
R <sub>e_FXL</sub>	Irradiance responsivity channel FXL	LED_593nm ; Ee= 155 mW/m <sup>2</sup> LED_628nm ; Ee= 155 mW/m <sup>2</sup>	3582	4776	5970	counts
R <sub>e_F6</sub>	Irradiance responsivity channel F6	LED_618nm ; Ee= 155 mW/m <sup>2</sup> LED_665nm ; Ee= 155 mW/m <sup>2</sup>	2502	3336	4170	counts
R <sub>e_F7</sub>	Irradiance responsivity channel F7	LED_685nm ; Ee= 155 mW/m <sup>2</sup> LED_715nm ; Ee= 155 mW/m <sup>2</sup>	4095	5435	6774	counts
R <sub>e_F8</sub>	Irradiance responsivity channel F8	LED_715nm ; Ee= 155 mW/m <sup>2</sup> LED_766nm ; Ee= 155 mW/m <sup>2</sup>	648	864	1080	counts
R <sub>e_NIR</sub>	Irradiance responsivity channel NIR	LED_849nm ; Ee= 155 mW/m <sup>2</sup> LED_903nm ; Ee= 155 mW/m <sup>2</sup>	7936	10581	13226	counts

**Figure 9:**  
**Optical Characteristics of Broadband Channels, AGAIN: 1024x, FD\_GAIN: 64x, Integration Time: 27.8 ms**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>e_FD</sub>	Irradiance responsivity channel Flicker	LED_593nm ; Ee= 155 mW/m <sup>2</sup>	3233	4311	5389	counts
		LED_766nm ; Ee= 155 mW/m <sup>2</sup>				
		FD_GAIN=64x				
R <sub>e_VIS</sub>	Irradiance responsivity channel VIS	LED_396nm ; Ee= 155 mW/m <sup>2</sup>	749	999	1248	counts
		LED_766nm ; Ee= 155 mW/m <sup>2</sup>				
		2 VIS PDs read-out				

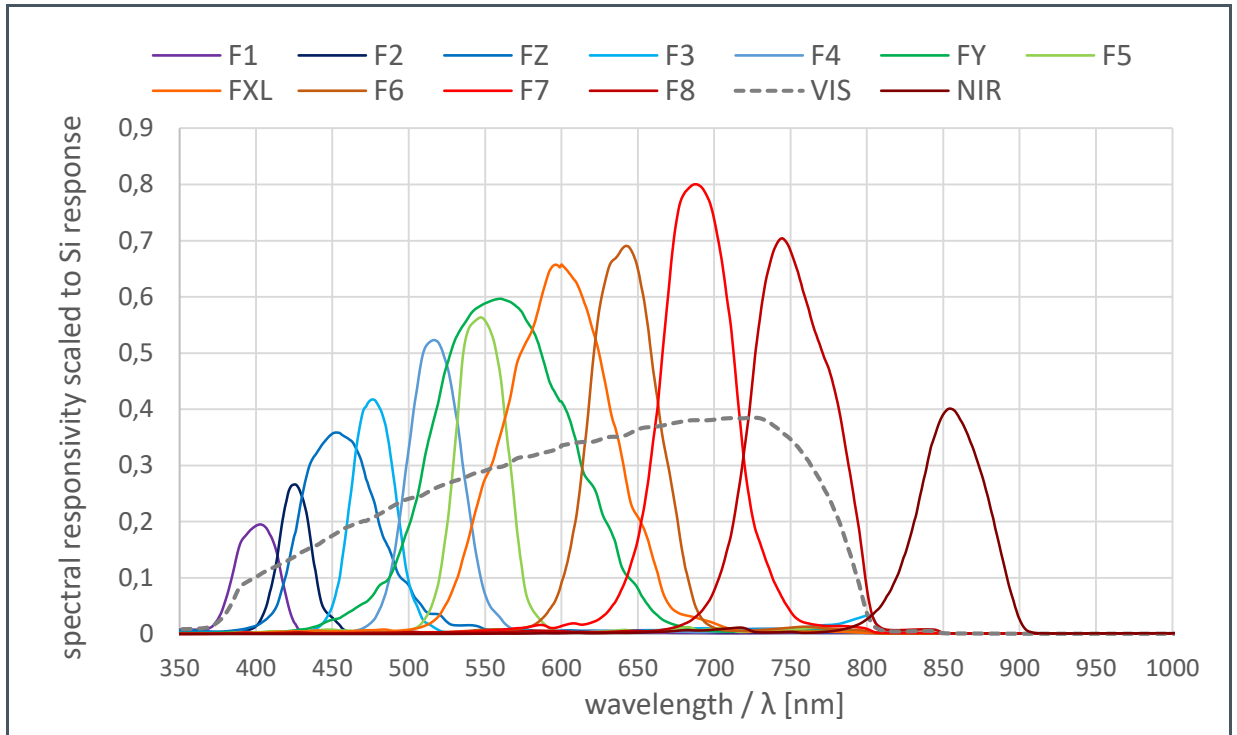
**Figure 10:**  
**Optical Characteristics of AS7343, AGAIN: 128x, Integration Time: 11 ms (unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dark <sub>1</sub> <sup>(1)</sup>	Dark ADC count value	E <sub>e</sub> = 0 μW/cm <sup>2</sup> AGAIN: 512x Integration time: 98 ms		0	5	counts
Gain <sup>(2)</sup> ratio	Optical gain ratios, relative to 64x gain setting	AGAIN: 0.5x	7.49	7.9	8.28	See note <sup>(3)</sup>
		AGAIN: 1x	15	15.8	16.5	
		AGAIN: 2x	30	31.6	33.2	
		AGAIN: 4x	61	64	67	
		AGAIN: 8x	117	124	130	
		AGAIN: 16x	235	247	259	
		AGAIN: 32x	0.475	0.5	0.525	
		AGAIN: 64x		1		
		AGAIN: 128x	1.9	2	2.1	
		AGAIN: 256x	3.9	4.1	4.3	
		AGAIN: 512x	8.1	8.6	9.1	
		AGAIN: 1024x	15.2	16.9	18.6	
		AGAIN: 2048x	28.2	34.75	41.3	
ADC noise <sup>(4)</sup>		White LED, 2700 K Integration time: 100 ms		0.05		% full scale
t <sub>int</sub>	Typical integration time <sup>(5)</sup>	ASTEP = 599 ATIME = 29		50		ms
t <sub>ASTEP</sub>	Integration time step size	ASTEP = 999		2.78		ms
h <sub>ca</sub>	Half cone angle	On the sensor		40		deg

- (1) The typical 3-sigma distribution is between 0 and 1 counts for AGAIN setting of 16x.
- (2) The gain ratios are relative to 64x gain setting and are calculated relative to the response with integration time: 11 ms and AGAIN: 128x.
- (3) ADC noise is calculated as the standard deviation of relative to full scale.
- (4) Integration time, in milliseconds, is equal to: (ATIME + 1) x (ASTEP + 1) x 2.78 μs
- (5) AGAIN ratio 0.5x to 16x is multiplied by 1000 for easier readability

# 7 Typical Operating Characteristics

Figure 11:  
Spectral Responsivity

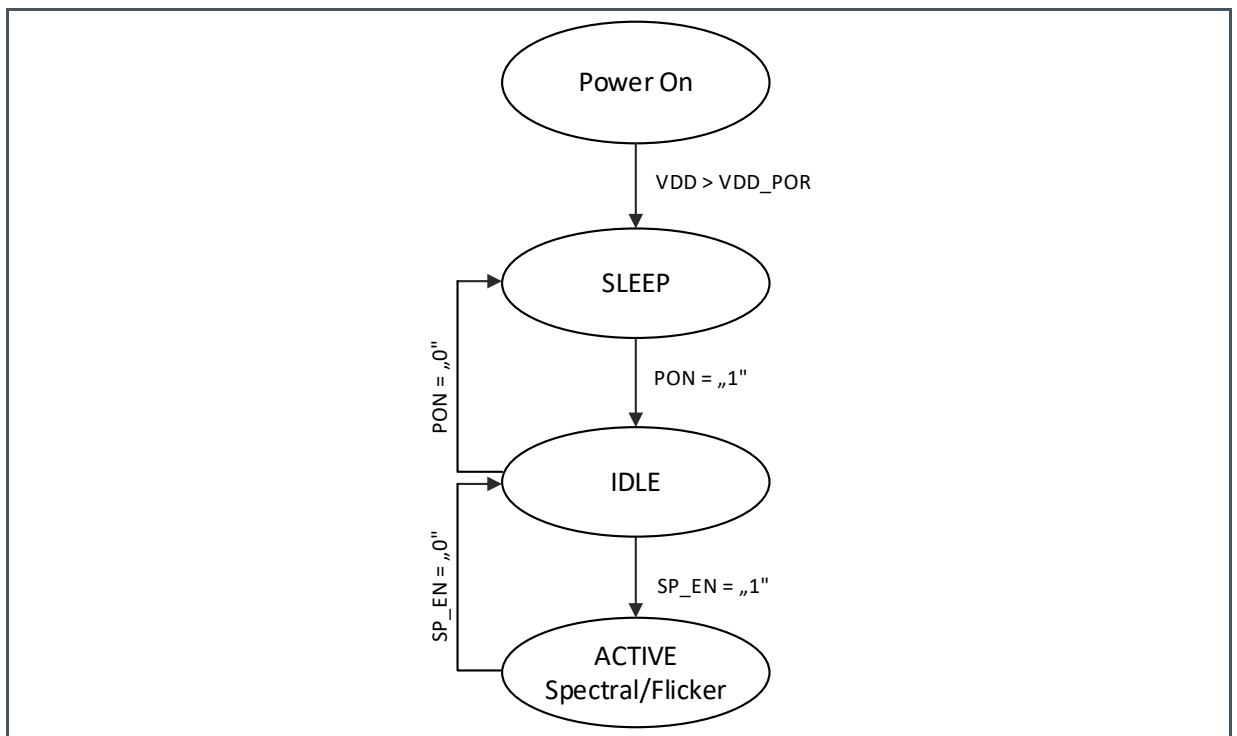


## 8 Functional Description

Upon power-up (POR), the device initializes. During initialization (typically 200  $\mu$ s), the device will deterministically send NAK on I<sup>2</sup>C and cannot accept I<sup>2</sup>C transactions. All communication with the device must be delayed and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state, the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I<sup>2</sup>C transaction occurs during this state, the I<sup>2</sup>C core wakes up temporarily to service the communication. Once the Power ON bit, "PON", is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever the spectral measurement is enabled (SP\_EN = "1") the device enters the ACTIVE state. If the spectral measurement is disabled (SP\_EN = "0") the device returns to the IDLE state. The figure below describes a simplified state diagram and the typical supply currents in each state.

If Sleep after Interrupt is enabled (SAI = "1" in register 0xAC), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI\_ACTIVE bit is cleared (the status bit is in register 0xA7 and the clear status bit is in register 0xFA).

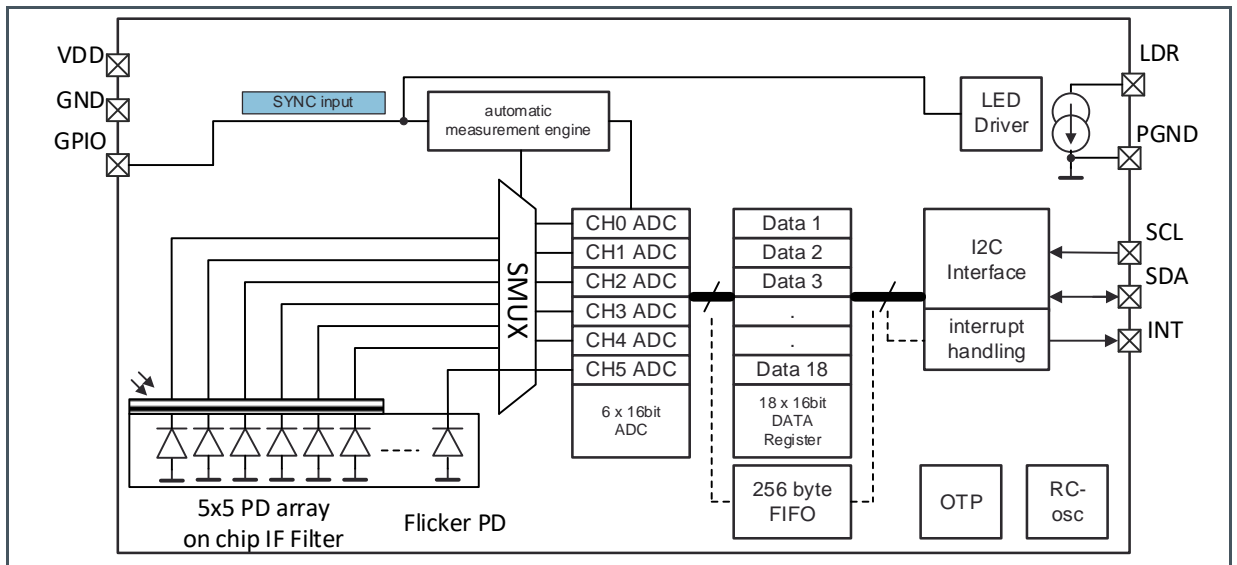
**Figure 12:**  
Simplified State Diagram



## 8.1 Device Architecture

The device features six independent 16-bit ADCs. Gain and integration time of the six ADCs can be adjusted with the I<sup>2</sup>C interface. A wait time can be programmed to automatically set a delay between two consecutive spectral measurements and to reduce overall power consumption. Once a measurement is started, the device is automatically processing the channels and storing the measurement data on chip

**Figure 13:**  
**Simplified Block Diagram**

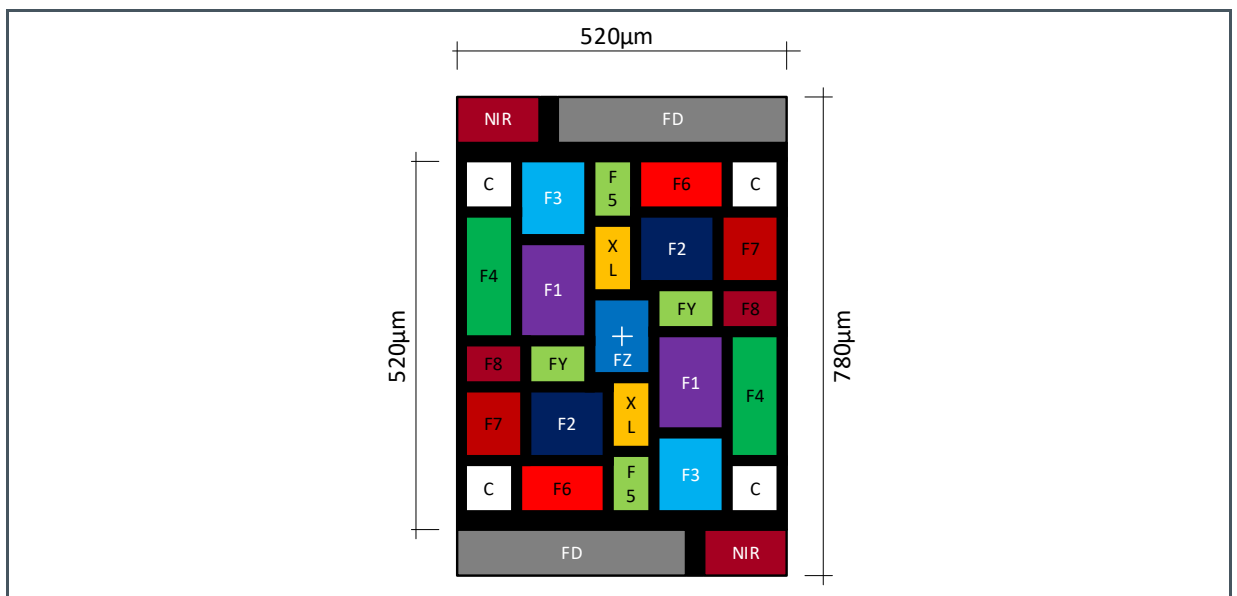




## 8.2 Sensor Array

The device features a 5x5-photodiode array. On top and below the photodiode array there are two photodiodes with dedicated functions such as flicker detection (“FD”) and near- infrared response (“NIR”). The photodiode “C” represents a photodiode without filter and is responsive in the visible spectral range. (“VIS”).

**Figure 14:**  
**Sensor Array**



## 8.3 GPIO

The GPIO can be used synchronization input to start/stop the spectral measurement. It also allows synchronizing the LED driver (LDR) with an external start/stop signal. Default state of the GPIO is “output”.

## 8.4 Interrupt (INT)

The interrupt (INT) can be used to define thresholds and read-out the device only when the channel threshold has been reached. The pin is active low.

## 8.5 LED Driver (LDR)

The LED driver is programmable and can be used to drive external LEDs. It is also possible to synchronize the LED driver with an external start/stop signal via pin GPIO.

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## 9 I<sup>2</sup>C Interface

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The device uses I<sup>2</sup>C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I<sup>2</sup>C bus is released). During consecutive Read transactions, the future/repeated I<sup>2</sup>C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1. All 16-bit fields have a latching scheme for reading and writing. In general, it is recommended to use I<sup>2</sup>C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

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### 9.1 I<sup>2</sup>C Address

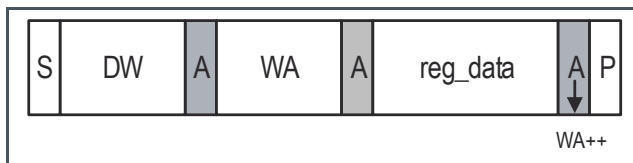
**Figure 15:**  
AS7343 I<sup>2</sup>C Slave Address

Device	I <sup>2</sup> C Address
AS7343	0x39
AS7343B	0x29

## 9.2 I<sup>2</sup>C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP (P). Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (A/N) on the bus. If the slave transmits N, the master may issue a STOP.

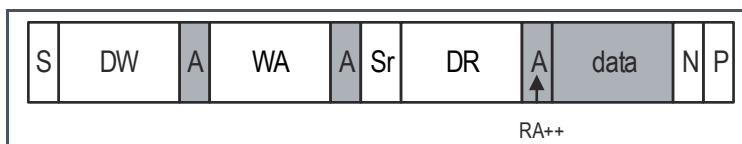
**Figure 16:**  
I<sup>2</sup>C Byte Write



## 9.3 I<sup>2</sup>C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

**Figure 17:**  
I<sup>2</sup>C Read



## 9.4 Timing Characteristics

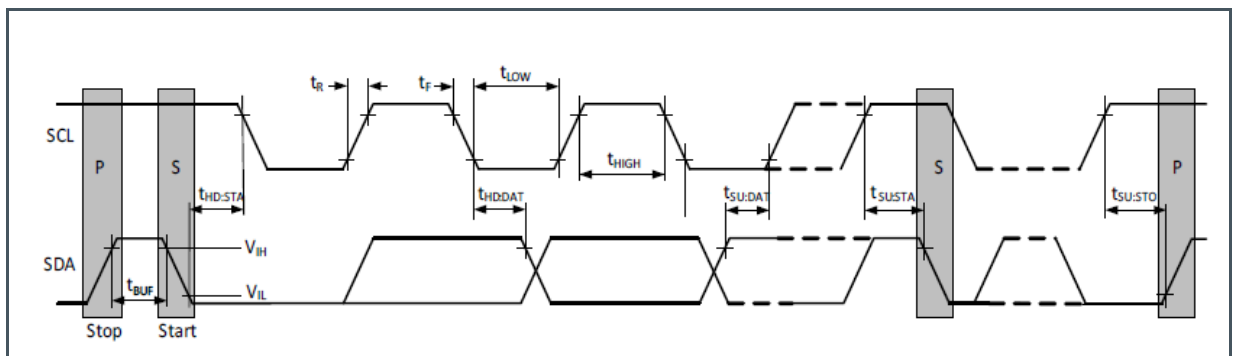
**Figure 18:**  
I<sup>2</sup>C Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency			1	MHz
t <sub>BUF</sub>	Bus free time between start and stop condition	1.3			μs
t <sub>HS,STA</sub>	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SU;STA}$	Repeated start condition setup time	0.6			ns
$t_{SU;STO}$	Stop condition setup time	0.6			
$t_{LOW}$	SCL clock low period	1.3			
$t_{HIGH}$	SCL clock high period	0.6			
$t_{HD;DAT}$	Data hold time	0			
$t_{SU;DAT}$	Data setup time	100			
$t_F$	Clock/data fall time			300	
$t_R$	Clock/data rise time			300	

## 9.5 Timing Diagrams

Figure 19:  
I<sup>2</sup>C Slave Timing Diagram



# 10 Register Description

The device is controlled and monitored by registers accessed through the I<sup>2</sup>C serial interface. These registers provide device control functions and can be read to determine device status and acquire device data.

The register set is summarized below. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. Two-byte fields are always latched with the low byte followed by the high byte. The “Name” column illustrates the purpose of each register by highlighting the function associated to each bit. The bits are shown from MSB (D7) to LSB (D0). GRAY fields are reserved and their values must not be changed at any time.

In order to access registers from 0x58 to 0x66 bit REG\_BANK in register CFG0 (0xBF) needs to be set to “1”. For register access of registers 0x80 and above bit REG\_BANK needs to be set to “0”.

## 10.1 Register Overview

**Figure 20:**  
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	
0x58	AUXID	[Reserved]					AUXID [3:0]			
0x59	REVID	[Reserved]						REVID [2:0]		
0x5A	ID	ID [7:0]								
0x66	CFG12	[Reserved]						SP_TH_CH [2:0]		
0x80	ENABLE	[Reserved]	FDEN	[Reserved]	SMUXE N	WEN	[Reserved]	SP_EN	PON	
0x81	ATIME	ATIME [7:0]								
0x83	WTIME	WTIME [7:0]								
0x84	SP_TH_L	SP_TH_L_LSB [7:0]								
0x85		SP_TH_L_MSB [7:0]								
0x86	SP_TH_H	SP_TH_H_LSB [7:0]								
0x87		SP_TH_H_MSB [7:0]								
0x93	STATUS	ASAT	[Reserved]			AINT	FINT	[Reserved]	SINT	
0x94	ASTATUS	ASAT_ STATUS	[Reserved]			AGAIN_STATUS [3:0]				
0x95	DATA_0	DATA_0_L [7:0]								
0x96		DATA_0_H [7:0]								
0x97	DATA_1	DATA_1_L [7:0]								
0x98		DATA_1_H [7:0]								
0x99	DATA_2	DATA_2_L [7:0]								

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x9A					DATA_2_H [7:0]				
0x9B	DATA_3				DATA_3_L [7:0]				
0x9C					DATA_3_H [7:0]				
0x9D	DATA_4				DATA_4_L [7:0]				
0x9E					DATA_4_H [7:0]				
0x9F	DATA_5				DATA_5_L [7:0]				
0xA0					DATA_5_H [7:0]				
0xA1	DATA_6				DATA_6_L [7:0]				
0xA2					DATA_6_H [7:0]				
0xA3	DATA_7				DATA_7_L [7:0]				
0xA4					DATA_7_H [7:0]				
0xA5	DATA_8				DATA_8_L [7:0]				
0xA6					DATA_8_H [7:0]				
0xA7	DATA_9				DATA_9_L [7:0]				
0xA8					DATA_9_H [7:0]				
0xA9	DATA_10				DATA_10_L [7:0]				
0xAA					DATA_10_H [7:0]				
0xAB	DATA_11				DATA_11_L [7:0]				
0xAC					DATA_11_H [7:0]				
0xAD	DATA_12				DATA_12_L [7:0]				
0xAE					DATA_12_H [7:0]				
0xAF	DATA_13				DATA_13_L [7:0]				
0xB0					DATA_13_H [7:0]				
0xB1	DATA_14				DATA_14_L [7:0]				
0xB2					DATA_14_H [7:0]				
0xB3	DATA_15				DATA_15_L [7:0]				
0xB4					DATA_15_H [7:0]				
0xB5	DATA_16				DATA_16_L [7:0]				
0xB6					DATA_16_H [7:0]				
0xB7	DATA_17				DATA_17_L [7:0]				
0xB8					DATA_17_H [7:0]				
0x90	STATUS 2		AVALID		ASAT_ DIG	ASAT_ ANA		FDSAT_ ANA	FDSAT_ DIG
0x91	STATUS 3			INT_SP_H	INT_SP_L				
0xBB	STATUS 5					SINT_ FD	SINT_ SMUX		
0xBC	STATUS 4	FIFO_ OV		OVTEMP	FD_ TRIG		SP_ TRIG	SAL_ ACT	INT_ BUS Y
0xBF	CFG 0			LOW_ POWER	REG_ BANK		WLONG		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	
0xC6	CFG1				AGAIN[4:0]					
0xC7	CFG3				SAI					
0xF5	CFG6				SMUX_		CMD[4:3]			
0xC9	CFG8	FIFO_TH [7:6]								
0xCA	CFG9	SIEN		SIEN						
		_FD		_SMUX						
0x65	CFG10							FD_PERS [2:0]		
0xCF	PERS							APERS [3:0]		
0x6B	GPIO					GPIO_	GPIO_	GPIO_	GPIO_	
						INV	IN_EN	OUT	IN	
0xD4	ASTEP	ASTEP [7:0]								
0xD5		ASTEP [15:8]								
0xD6	CFG20	FD_FIF	auto_SMUX							
		O_8b								
0xCD	LED	LED_AC		LED_DRIVE [6:0]						
		T								
0xD7	AGC_GAIN_	AGC_FD_GAIN_MAX [7:4]								
	MAX									
0xDE	AZ_CONFIG	AT_NTH_ITERATION [7:0]								
0xE0	FD_TIME_1	FD_TIME [7:0]								
0xE2	FD_TIME_2	FD_GAIN [7:3]			FD_TIME [10:8]					
0xDF	FD_CFG0	FIFO_W								
		RITE_F								
		D								
0xE3	FD_STATUS			FD_	FD_	FD_	FD_	FD_	FD_	
				VALID	SAT	120HZ_	100Hz_	120Hz	100Hz	
						VALID	VALID			
0xF9	INTENAB	ASIEN				SP_IEN	FIEN		SIEN	
0xFA	CONTROL					SW_	SP_MAN	FIFO_	CLEAR_	
						RESET	_AZ	CLR	SAL_ACT	
0xFC	FIFO_MAP	FIFO_WRITE_CH5_DATA – FIFO_WRITE_CH0_DATA [6:1]						ASTATUS		
0xFD	FIFO_LVL	FIFO_LVL [7:0]								
0xFE	FDATA	FDATA_L [7:0]								
0xFF		FDATA_H [15:8]								

## 10.2 Detailed Register Description

For easier readability, the detailed register description is done in groups of registers related to dedicated device functions. This is not necessarily related to its register address.

Explanation of register access abbreviations:

RW = read or write

R = read only

W = write only

SC = self-clearing after access

### 10.2.1 Enable and Configuration Registers

The following registers are needed to power up and configure the device. To operate the device set bit PON = "1" first (register 0x80) after that configure the device and enable interrupts before setting SP\_EN = "1". Changing configuration while SP\_EN = "1" may result in invalid results.

#### ENABLE Register (Address 0x80)

Figure 21:  
ENABLE Register

Addr: 0x80		ENABLE		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0	RW	Reserved
6	FDEN	0	RW	<b>Flicker Detection Enable.</b> 0: Flicker Detection disabled 1: Flicker Detection enabled
5	Reserved	0	RW	Reserved
4	SMUXEN	0	RW	<b>SMUX Enable.</b> 1: Starts SMUX command Note: This bit gets cleared automatically as soon as SMUX operation is finished
3	WEN	0	RW	<b>Wait Enable.</b> 0: Wait time between two consecutive spectral measurements disabled 1: Wait time between two consecutive spectral measurements enabled
2	Reserved	0	RW	Reserved
1	SP_EN	0	RW	<b>Spectral Measurement Enable.</b> 0: Spectral Measurement Disabled 1: Spectral Measurement Enabled



Addr: 0x80		ENABLE		
Bit	Bit Name	Default	Access	Bit Description
0	PON	0	RW	<p><b>Power ON.</b> 0: AS7343 disabled 1: AS7343 enabled Note: When bit is set, internal oscillator is activated, allowing timers and ADC channels to operate.</p>

### GPIO Register (Address 0x6B)

Figure 22:  
GPIO Register

Addr: 0x6B		GPIO		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0		Reserved
3	GPIO_INV	0	RW	<p><b>GPIO Invert.</b> If set, the GPIO output is inverted.</p>
2	GPIO_IN_EN	0	RW	<p><b>GPIO Input Enable.</b> If set, the GPIO pin accepts a non-floating input.</p>
1	GPIO_OUT	1	RW	<p><b>GPIO Output.</b> If set, the output state of the GPIO is active directly.</p>
0	GPIO_IN	0	R	<p><b>GPIO Input.</b> Indicates the status of the GPIO input if GPIO_IN_EN is set.</p>

### LED Register (Address 0xCD)

Figure 23:  
LED Register

Addr: 0xCD		LED		
Bit	Bit Name	Default	Access	Bit Description
7	LED_ACT	0	RW	<p><b>LED Control.</b> 0: External LED connected to pin LDR off 1: External LED connected to pin LDR on</p>
6:0	LED_DRIVE	000 0100	RW	<p><b>LED Driving Strength.</b> 000 0000: 4 mA 000 0001: 6 mA 000 0010: 8 mA 000 0011: 10 mA <b>000 0100: 12 mA</b></p>

Addr: 0xCD		LED		
Bit	Bit Name	Default	Access	Bit Description
				.....
				111 1110: 256 mA
				111 1111: 258 mA

**INTENAB Register (Address 0xF9)**

Figure 24:  
INTENAB Register

Addr: 0xF9		INTENAB		
Bit	Bit Name	Default	Access	Bit Description
7	ASIEN	0	RW	<b>Spectral and Flicker Detect Saturation Interrupt Enable.</b> When asserted permits saturation interrupts to be generated.
6:4	Reserved			Reserved
3	SP_IEN	0	RW	<b>Spectral Interrupt Enable.</b> When asserted permits interrupts to be generated, subject to the spectral thresholds and persistence filter. Bit is mirrored in the ENABLE register.
2	F_IEN	0	RW	<b>FIFO Buffer Interrupt Enable.</b> When asserted permits interrupt to be generated when FIFO_LVL exceeds the FIFO threshold condition.
1	Reserved	0		Reserved
0	SIEN		RW	<b>System Interrupt Enable.</b> When asserted permits system interrupts to be generated. Indicates that flicker detection status has changed or SMUX operation has finished.

**CONTROL Register (Address 0xFA)**

Figure 25:  
CONTROL Register

Addr: 0xFA		CONTROL		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0		Reserved
3	SW_RESET	0	RW	<b>Software Reset</b> When set the device will force a power on reset.
2	SP_MAN_AZ	0	RW	<b>Spectral Engine Manual Autozero.</b>

Addr: 0xFA		CONTROL		
Bit	Bit Name	Default	Access	Bit Description
				Starts a manual autozero of the spectral engines. Set SP_EN = 0 before starting a manual autozero for it to work.
1	FIFO_CLR	0	RW	<b>FIFO Buffer Clear.</b> Clears all FIFO data, FINT, FIFO_OV, and FIFO_LVL.
0	CLEAR_SAI_ACT	0	RW	<b>Clear Sleep-After-Interrupt Active.</b> Clears SAI_ACTIVE, ends sleep, and restarts device operation.

### 10.2.2 ADC Timing Configuration / Integration Time

The integration time is set using the ATIME (0x81) and ASTEP (0xD4, 0xD5) registers. The integration time, in milliseconds, is equal to:

#### Equation 1: Setting the integration time

$$t_{int} = (ATIME + 1) \times (ASTEP + 1) \times 2.78\mu s$$

It is not allowed that both settings –ATIME and ASTEP – are set to “0”.

The integration time also defines the full-scale ADC value, which is equal to:

#### Equation 2: ADC full scale value<sup>1</sup>

$$ADC_{fullscale} = (ATIME + 1) \times (ASTEP + 1)$$

#### ATIME Register (Address 0x81)

Figure 26:  
ATIME Register

Addr: 0x81		ATIME								
Bit	Bit Name	Default	Access	Bit Description						
7:0	ATIME	0x00	RW	<b>Integration time.</b> Sets the number of integration steps from 1 to 255. <table border="1" style="margin-top: 5px;"> <thead> <tr> <th>Value</th> <th>Integration Time</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>ASTEP</td> </tr> <tr> <td>n</td> <td>ASTEP x (n+1)</td> </tr> </tbody> </table>	Value	Integration Time	0	ASTEP	n	ASTEP x (n+1)
Value	Integration Time									
0	ASTEP									
n	ASTEP x (n+1)									

<sup>1</sup> The maximum ADC count is 65535. Any ATIME/ASTEP field setting resulting in higher ADC full-scale values would result in a full-scale of 65535.

Addr: 0x81		ATIME			
Bit	Bit Name	Default	Access	Bit Description	
				255	ASTEP x 256

### ASTEP Register (Address 0xD4, 0xD5)

Figure 27:  
ASTEP Register

Addr: 0xD4, 0xD5		ASTEP												
Bit	Bit Name	Default	Access	Bit Description										
7:0	ASTEP 0xCA	999	RW	<b>Integration Time Step Size.</b> Sets the integration time per step in increments of 2.78 $\mu$ s. The default value is 999.										
				<table border="1"> <thead> <tr> <th>VALUE</th> <th>STEP SIZE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>2.78 <math>\mu</math>s</td> </tr> <tr> <td>n</td> <td>2.78 <math>\mu</math>s x (n+1)</td> </tr> <tr> <td>599</td> <td>1.67 ms</td> </tr> <tr> <td>999</td> <td>2.78 ms</td> </tr> </tbody> </table>	VALUE	STEP SIZE	0	2.78 $\mu$ s	n	2.78 $\mu$ s x (n+1)	599	1.67 ms	999	2.78 ms
VALUE	STEP SIZE													
0	2.78 $\mu$ s													
n	2.78 $\mu$ s x (n+1)													
599	1.67 ms													
999	2.78 ms													
15:8	ASTEP 0xCB			<table border="1"> <tbody> <tr> <td>17999</td> <td>50 ms</td> </tr> <tr> <td>65534</td> <td>182 ms</td> </tr> <tr> <td>65535</td> <td>Reserved, do not use</td> </tr> </tbody> </table>	17999	50 ms	65534	182 ms	65535	Reserved, do not use				
17999	50 ms													
65534	182 ms													
65535	Reserved, do not use													

### WTIME Register (Address 0x83)

If wait is enabled (WEN = “1” register 0x80), each new measurement is started based on WTIME. It is necessary for WTIME to be sufficiently long for spectral integration and any other functions to be completed within the period. The device will warn the user if the timing is configured incorrectly. If WTIME is too short, then SP\_TRIG in register STATUS6 (ADDR: 0xA7) will be set to “1”.

Figure 28:  
WTIME Register

Addr: 0x83		WTIME								
Bit	Bit Name	Default	Access	Bit Description						
7:0	WTIME	0x00	RW	<b>Spectral Measurement Wait Time.</b> 8-bit value to specify the delay between two consecutive spectral measurements.						
				<table border="1"> <thead> <tr> <th>Value</th> <th>Wait Cycles</th> <th>Wait Time</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>1</td> <td>2.78 ms</td> </tr> </tbody> </table>	Value	Wait Cycles	Wait Time	0x00	1	2.78 ms
Value	Wait Cycles	Wait Time								
0x00	1	2.78 ms								

Addr: 0x83		WTIME		
Bit	Bit Name	Default	Access	Bit Description
				0x01      2      5.56 ms
				n          n      2.78 ms x (n+1)
				0xff      256      711 ms

**FD\_TIME Register (Address 0xE0, 0xE2)**

The register FD Time 1 and FD Time 2 can be used to configure the integration time and gain (ADC 5) of the flicker detection independently from the other ADCs. The FD\_TIME register is an 11-bit register with the MSB in register 0xDA (bit 10:8) and the LSB in register 0xD8 (bit 7:0). The bit FDEN (register 0x80) must be set to “1” in order to use the FD\_TIME registers. If the bit FDEN is not set, ADC5 runs automatically with the same gain and integration time as ADC0 to ADC4.

**Equation 3: Calculating the flicker detection integration time**

$$t_{int\_FD} = FD\_TIME \times 2.78\mu s$$

**Figure 29:**  
FD Time\_1 Register

Addr: 0xE0		FD_TIME_1		
Bit	Bit Name	Default	Access	Bit Description
7:0	FD_TIME [7:0]	0110 0111	RW	LSB of flicker detection integration time. Note: must not be changed during FDEN = 1 and PON = 1.

Figure 30:  
FD Time\_2 Register

Addr: 0xE2		FD_TIME_2		
Bit	Bit Name	Default	Access	Bit Description
<b>Flicker Detection Gain Setting (ADC5)</b>				
<b>VALUE</b>				
<b>GAIN</b>				
				0
				1
				2
				3
				4
				5
				6
				7
				8
				9
				10
				11
				12
7:3	FD_GAIN	9	RW	0.5x 1x 2x 4x 8x 16x 32x 64x 128x 256x 512x 1024x 2048x
2:0	FD_TIME [10:8]	1	RW	MSB of flicker detection integration time. Note: must not be changed during FDEN = 1 and PON = 1.

### 10.2.3 ADC Configuration

The following registers provide configuration for the 6 integrated ADCs (CH0 to CH5). It is possible to adjust the gain and setup the auto zero compensation for the ADCs.

#### CFG1 Register (Address 0xC6)

Figure 31:  
CFG1 Register

Addr: 0xC6		CFG1		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	0		Reserved
				<b>Spectral Engines Gain Setting.</b> Sets the spectral sensitivity.
				<b>VALUE</b> <b>GAIN</b>
				0                                  0.5x
				1                                  1x
				2                                  2x
				3                                  4x
4:0	AGAIN	9	RW	4                                  8x
				5                                  16x
				6                                  32x
				7                                  64x
				8                                  128x
				9                                  256x
				10                                 512x
				11                                 1024x
				12                                 2048x

#### CFG10 Register (Address 0x65)

Figure 32:  
CFG10 Register

Addr: 0x65		CFG10		
Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved	Reserved	Reserved	Reserved

Addr: 0x65		CFG10		
Bit	Bit Name	Default	Access	Bit Description
2:0	FD_PERS	2	RW	<p><b>Flicker Detect Persistence.</b> Sets the number of consecutive flicker detect results that must be different before the flicker detect status will be changed. Flicker detection interrupts on SINT are affected by this setting. Flicker detect persistence is equal to <math>2^{(FD\_PERS-1)}</math> Setting "0" equals to every time.</p>

**AZ\_CONFIG Register (Address 0xDE)**

The following register configures how often the spectral engine offsets are reset (auto zero) to compensate for changes of the device temperature. The typical time auto zero needs to be completed is 15 ms.

**Figure 33:**  
AZ\_CONFIG Register

Addr: 0xDE		AZ_CONFIG																
Bit	Bit Name	Default	Access	Bit Description														
7:0	AZ_NTH_ITERATION	255	RW	<p><b>AUTOZERO FREQUENCY.</b> Sets the frequency at which the device performs auto zero of the spectral engines. Note: If FDEN = "1" auto zero is also done for ADC 5. The flicker detection measurement will be interrupted and restarted in this case.</p> <table border="1"> <thead> <tr> <th>VALUE</th> <th>AUTOZERO FREQUENCY</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Never (not recommended)</td> </tr> <tr> <td>1</td> <td>Every integration cycle</td> </tr> <tr> <td>2</td> <td>Every 2 cycles</td> </tr> <tr> <td>...</td> <td>Every "AZ_NTH_ITERATION" cycle</td> </tr> <tr> <td>254</td> <td>Every 254 cycles</td> </tr> <tr> <td>255</td> <td>Only before first measurement cycle</td> </tr> </tbody> </table>	VALUE	AUTOZERO FREQUENCY	0	Never (not recommended)	1	Every integration cycle	2	Every 2 cycles	...	Every "AZ_NTH_ITERATION" cycle	254	Every 254 cycles	255	Only before first measurement cycle
VALUE	AUTOZERO FREQUENCY																	
0	Never (not recommended)																	
1	Every integration cycle																	
2	Every 2 cycles																	
...	Every "AZ_NTH_ITERATION" cycle																	
254	Every 254 cycles																	
255	Only before first measurement cycle																	



**AGC\_GAIN\_MAX Register (Address 0xD7)**

**Figure 34:**  
AGC\_GAIN\_MAX Register

Addr: 0xD7		AGC_GAIN_MAX		
Bit	Bit Name	Default	Access	Bit Description
7:4	AGC_FD_GAIN_MAX	9	RW	<p><b>Flicker Detection AGC Gain Max.</b> Sets the maximum gain for flicker detection to <math>2^{AGC\_FD\_GAIN\_MAX}</math>. Default value is 9 (256x). The range can be set from 0 (0.5x) to 10 (2048x).</p>
3:0	Reserved	9	Reserved	<b>Reserved</b>

**CFG8 Register (Address 0xC9)**

**Figure 35:**  
CFG8 Register

Addr: 0xC9		CFG8												
Bit	Bit Name	Default	Access	Bit Description										
7:6	FIFO_TH	2	RW	<p><b>FIFO Threshold.</b> Sets a threshold on the FIFO level that triggers the first FIFO buffer interrupt (FINT).</p> <table border="1"> <thead> <tr> <th>VALUE</th> <th>FIFO_LVL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>4</td> </tr> <tr> <td>2</td> <td>8</td> </tr> <tr> <td>3</td> <td>16</td> </tr> </tbody> </table>	VALUE	FIFO_LVL	0	1	1	4	2	8	3	16
VALUE	FIFO_LVL													
0	1													
1	4													
2	8													
3	16													
5:0	Reserved	0		Reserved										

## 10.2.4 Device Identification

The following registers provided device identification. Device ID, revision ID and auxiliary ID are read only.

### AUXID Register (Address 0x58)

Figure 36:  
AUXID Register

Addr: 0x58		AUXID		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved			Reserved
3:0	AUXID	0000	R	<b>Auxiliary Identification</b>

### REVID Register (Address 0x59)

Figure 37:  
REVID Register

Addr: 0x59		REVID		
Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved			Reserved
2:0	REV_ID	000	R	<b>Revision Number Identification</b>

### ID Register (Address 0x5A)

Figure 38:  
ID Register

Addr: 0x5A		ID		
Bit	Bit Name	Default	Access	Bit Description
7:0	ID	10000001	R	<b>Part Number Identification</b> Value 10000001

## 10.2.5 Spectral Interrupt Configuration

The spectral interrupt threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit CH0\_DATA values (ADC CH0). If SP\_IEN (register 0xF9) is enabled and CH0\_DATA is not between the two thresholds for the number of consecutive measurements specified in APERS (register 0xBD) an interrupt is set.

### SP\_TH\_L\_LSB Register (Address 0x84)

Figure 39:  
SP\_TH\_L\_LSB Register

Addr: 0x84		SP_TH_L_LSB		
Bit	Bit Name	Default	Access	Bit Description
7:0	SP_TH_L_LSB	0x00	RW	<b>Spectral Low Threshold LSB</b> This register provides the low byte of the low interrupt threshold (CH0).

### SP\_TH\_L\_MSB Register (Address 0x85)

Figure 40:  
SP\_TH\_L\_MSB Register

Addr: 0x85		SP_TH_L_MSB		
Bit	Bit Name	Default	Access	Bit Description
7:0	SP_TH_L_MSB	0x00	RW	<b>Spectral Low Threshold MSB</b> This register provides the high byte of the low interrupt threshold (CH0). Both SP_TH_L registers are combined to a 16-bit threshold. If the value captured by channel 0 is below the low threshold and the APERS value is reached the bit SP_IEN is set and an interrupt is generated. There is an 8-bit data latch implemented that stores the written low byte until the high byte is written. Both bytes will be applied at the same time to avoid an invalid threshold. Note: The LSB register cannot be changed without writing to the MSB register. It is recommended to write to SP_TH_L_LSB and SP_TH_L_MSB within one I <sup>2</sup> C command.

**SP\_TH\_H\_LSB Register (Address 0x86)**

Figure 41:  
SP\_TH\_H\_LSB Register

Addr: 0x86		SP_TH_H_LSB		
Bit	Bit Name	Default	Access	Bit Description
7:0	SP_TH_H_LSB	0x00	RW	<b>Spectral High Threshold LSB</b> This register provides the low byte of the high interrupt threshold (CH0).

**SP\_TH\_H\_MSB Register (Address 0x87)**

Figure 42:  
SP\_TH\_H\_MSB Register

Addr: 0x87		SP_TH_H_MSB		
Bit	Bit Name	Default	Access	Bit Description
7:0	SP_TH_H_MSB	0x00	RW	<b>Spectral High Threshold MSB</b> This register provides the high byte of the high interrupt threshold (CH0).  Both SP_TH_H registers are combined to a 16-bit threshold. If the value captured by channel 0 is above the high threshold and the APERS value is reached the bit SP_IEN is set and an interrupt is generated.

**CFG12 Register (Address 0x66)**

Figure 43:  
CFG12 Register

Addr: 0x66		CFG12										
Bit	Bit Name	Default	Access	Bit Description								
7:3	Reserved	0		Reserved								
2:0	SP_TH_CH	0	RW	<b>Spectral Threshold Channel.</b> Sets the channel used for interrupts and persistence, if enabled, to determine device status and gain settings.								
				<table border="1"> <thead> <tr> <th>VALUE</th> <th>CHANNEL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CH0</td> </tr> <tr> <td>1</td> <td>CH1</td> </tr> <tr> <td>2</td> <td>CH2</td> </tr> </tbody> </table>	VALUE	CHANNEL	0	CH0	1	CH1	2	CH2
VALUE	CHANNEL											
0	CH0											
1	CH1											
2	CH2											

Addr: 0x66		CFG12		
Bit	Bit Name	Default	Access	Bit Description
				3 CH3
				4 CH4
				5 CH5

## 10.2.6 Device Status Registers

The following registers provide status of the device and indicate details about saturation, interrupts, over temperature, device execution and ambient light flicker detection.

### STATUS Register (Address 0x93)

The primary status register for AS7343 indicates if there are saturation or interrupt events that need to be handled by the user. This register is self-clearing, meaning that writing a “1” to any bit in the register clears that status bit. In this way, the user should read the STATUS register, handle all indicated event(s) and then write the register value back to STATUS to clear the handled events. Writing “0” will not clear those bits if they have a value of “1”, which means that new events that occurred since the last read of the STATUS register will not be accidentally cleared. In case channel saturation has happened (ASAT or FDSAT) it is recommended to discard the measurement results and re-configure device configuration such as AGAIN and Integration Time to avoid saturation.

Figure 44:  
STATUS Register

Addr: 0x93		STATUS		
Bit	Bit Name	Default	Access	Bit Description
7	ASAT	0	R, SC	<b>Spectral and Flicker Detect Saturation.</b> If ASIEN is set, indicates Spectral saturation. Check STATUS2 register to distinguish between analog or digital saturation.
6:4	Reserved	0	R	Reserved
3	AINT	0	R, SC	<b>Spectral Channel Interrupt.</b> If SP_IEN is set, indicates that a spectral event that met the programmed thresholds and persistence (APERS) occurred.
2	FINT	0	R, SC	<b>FIFO Buffer Interrupt.</b> If FIEN is set, indicates that the FIFO_LVL fulfills the threshold condition. If cleared by writing 1, the interrupt will be asserted again as more data is collected. To fully clear this interrupt, all data must be read from the FIFO buffer.
1	Reserved	0	R	Reserved
0	SINT	0	R, SC	<b>System Interrupt.</b>

Addr: 0x93		STATUS		
Bit	Bit Name	Default	Access	Bit Description
				If SIEN is set, indicates that system interrupt is set. Refer to Status5 register.

### STATUS 2 Register (Address 0x90)

Figure 45:  
STATUS 2 Register

Addr: 0x90		STATUS 2		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0		Reserved
6	AVALID	0	R	<b>Spectral Valid.</b> Indicates that the spectral measurement has been completed
5	Reserved	0		Reserved
4	ASAT_DIGITAL	0	R	<b>Digital Saturation.</b> Indicates that the maximum counter value has been reached. Maximum counter value depends on integration time set in the ATIME register.
3	ASAT_ANALOG	0	R	<b>Analog Saturation.</b> Indicates that the intensity of ambient light has exceeded the maximum integration level for the spectral analog circuit.
2	Reserved	0	R	Reserved
1	FDSAT_ANALOG	0	R	<b>Flicker Detect Analog Saturation.</b> Indicates that the intensity of ambient light has exceeded the maximum integration level for the analog circuit for flicker detection.
0	FDSAT_DIGITAL	0	R	<b>Flicker Detect Digital Saturation.</b> Indicates that the maximum counter value has been reached during flicker detection.

### STATUS 3 Register (Address 0x91)

Figure 46:  
STATUS 3 Register

Addr: 0x91		STATUS 3		
Bit	Bit Name	Default	Access	Bit Description
7:6	Reserved	0		Reserved
5	INT_SP_H	0	R	<b>Spectral Interrupt High.</b>

Addr: 0x91		STATUS 3		
Bit	Bit Name	Default	Access	Bit Description
				Indicates that a spectral interrupt occurred because the data exceeded the high threshold.
4	INT_SP_L	0	R	<b>Spectral Interrupt Low.</b> Indicates that a spectral interrupt occurred because the data is below the low threshold.
3:0	Reserved	0		Reserved

### STATUS 5 Register (Address 0xBB)

Figure 47:  
STATUS 5 Register

Addr: 0xBB		STATUS 5		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0		Reserved
3	SINT_FD	0	R	<b>Flicker Detect Interrupt.</b> If SIEN_FD is set, indicates that the FD_STATUS register status has changed
2	SINT_SMUX	0	R	<b>SMUX Operation Interrupt.</b> Indicates that SMUX command execution has finished.
1:0	Reserved	0		Reserved

### STATUS 4 Register (Address 0xBC)

Figure 48:  
STATUS 4 Register

Addr: 0xBC		STATUS 4		
Bit	Bit Name	Default	Access	Bit Description
7	FIFO_OV	0	R	<b>FIFO Buffer Overflow.</b> Indicates that the FIFO buffer overflowed and information has been lost. Bit is automatically cleared when the FIFO buffer is read
6	Reserved	0	R	Reserved
5	OVTEMP	0	R	<b>Over Temperature Detected.</b> Indicates the device temperature is too high. Write 1 to clear this bit.
4	FD_TRIG	0	R	<b>Flicker Detect Trigger Error.</b> Indicates that there is a timing error that prevents flicker detect from working correctly.

Addr: 0xBC		STATUS 4		
Bit	Bit Name	Default	Access	Bit Description
3	Reserved	0		Reserved
2	SP_TRIG	0	R	<b>Spectral Trigger Error.</b> Indicates that there is a timing error. The WTIME is too short for the selected ATIME.
1	SAI_ACTIVE	0	R	<b>Sleep after Interrupt Active.</b> Indicates that the device is in SLEEP due to an interrupt. To exit SLEEP mode, clear this bit.
0	INT_BUSY	0	R	<b>Initialization Busy.</b> Indicates that the device is initializing. This bit will remain 1 for about 300 μs after power on. Do not interact with the device until initialization is complete.

### FD\_STATUS Register (Address 0xE3)

Figure 49:  
FD STATUS Register

Addr: 0xE3		FD_STATUS		
Bit	Bit Name	Default	Access	Bit Description
7:6	Reserved			Reserved
5	FD_MEASUREMENT_VALID	0	R	<b>Flicker Detection Measurement Valid.</b> Indicates that flicker detection measurement is complete. Write 1 to this bit to clear this field.
4	FD_SATURATION_DETECTED	0	R	<b>Flicker Saturation Detected.</b> Indicates that saturation occurred during the last flicker detection measurement, and the result may not be valid. Write 1 to this bit to clear this field.
3	FD_120HZ_FLICKER_VALID	0	R	<b>Flicker Detection 120 Hz Flicker Valid.</b> Indicates that the 120 Hz flicker detection calculation is valid. Write 1 to this bit to clear this field.
2	FD_100HZ_FLICKER_VALID	0	R	<b>Flicker Detection 100 Hz Flicker Valid.</b> Indicates that the 100 Hz flicker detection calculation is valid. Write 1 to this bit to clear this field.
1	FD_120HZ_FLICKER	0	R	<b>Flicker Detected at 120 Hz.</b> Indicates if an ambient light source is flickering at 120 Hz.
0	FD_100HZ_FLICKER	0	R	<b>Flicker Detected at 100 Hz.</b> Indicates if an ambient light source is flickering at 100 Hz.



## 10.2.7 Spectral Data and Status

The ASTATUS register provides saturation and gain status associated to each set of spectral data. Reading the ASTATUS register (0x94) latches all 36 spectral data bytes to that status read. Reading these bytes consecutively (0x94 to 0xB8) ensures that the data is concurrent. All spectral data are stored as 16-bit values. If flicker detection is enabled, spectral channel five (CH5 ADC) is used for the flicker detection function. The ASTATUS and spectral data registers are read only.

### ASTATUS Register (Address 0x94)

Figure 50:  
ASTATUS Register

Addr: 0x94		ASTATUS		
Bit	Bit Name	Default	Access	Bit Description
7	ASAT_STATUS	0	R, SC	<b>Saturation Status.</b> Indicates if the latched data is affected by analog or digital saturation.
6:4	Reserved	0	R	Reserved
3:0	AGAIN_STATUS	0	R, SC	<b>Gain Status.</b> Indicates the gain applied for the spectral data latched to this ASTATUS read.

### DATA Register (Address 0x95/0xB8)

Figure 51:  
DATA\_L Register

Addr: 0x95/97/99..B7		DATA_N_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	DATA_L	0	R	Spectral Data – low byte

Figure 52:  
DATA\_H Register

Addr: 0x96/98/9A..B8		DATA_N_H		
Bit	Bit Name	Default	Access	Bit Description
7:0	DATA_H	0	R	Spectral Data – high byte

## 10.2.8 Miscellaneous Configuration

### CFG0 Register (Address 0xBF)

Figure 53:  
CFG0 Register

Addr: 0xBF		CFG0		
Bit	Bit Name	Default	Access	Bit Description
7:6	Reserved	0		Reserved
5	LOW_POWER	0	RW	<b>Low Power Idle.</b> When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled.
4	REG_BANK	0	RW	<b>Register Bank Access</b> 0: Register access to register 0x80 and above 1: Register access to register 0x20 to 0x7F Note: Bit needs to be set to access registers 0x20 to 0x7F. If registers 0x80 and above needs to be accessed bit needs to be set to "0".
3	Reserved	0		Reserved
2	WLONG	0	RW	<b>Trigger Long.</b> Increases the WTIME setting by a factor of 16.
1:0	Reserved	0		Reserved

### CFG3 Register (Address 0xC7)

Figure 54:  
CFG3 Register

Addr: 0xC7		CFG3		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	0		Reserved
4	SAI	0	RW	<b>Sleep After Interrupt.</b> If set, the oscillator is turned off whenever an interrupt is active. SAI_ACTIVE is set in this event. To activate the oscillator again, clear all interrupts and clear the SAI_ACTIVE bit.
3:0	Reserved	0xC		Reserved

**CFG6 Register (Address 0xF5)**

Figure 55:  
CFG6 Register

Addr: 0xF5		CFG6												
Bit	Bit Name	Default	Access	Bit Description										
				<b>SMUX Command.</b> Selects the SMUX command to execute when setting SMUXEN gets set. Do not change during ongoing SMUX operation.										
				<table border="1"> <thead> <tr> <th>VALUE</th> <th>SMUX_CMD</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>ROM code initialization of SMUX</td> </tr> <tr> <td>1</td> <td>Read SMUX configuration to RAM from SMUX chain</td> </tr> <tr> <td>2</td> <td>Write SMUX configuration from RAM to SMUX chain</td> </tr> <tr> <td>3</td> <td>Reserved, do not use</td> </tr> </tbody> </table>	VALUE	SMUX_CMD	0	ROM code initialization of SMUX	1	Read SMUX configuration to RAM from SMUX chain	2	Write SMUX configuration from RAM to SMUX chain	3	Reserved, do not use
VALUE	SMUX_CMD													
0	ROM code initialization of SMUX													
1	Read SMUX configuration to RAM from SMUX chain													
2	Write SMUX configuration from RAM to SMUX chain													
3	Reserved, do not use													
4:3	SMUX_CMD	2	RW											

**CFG9 Register (Address 0xCA)**

Figure 56:  
CFG9 Register

Addr: 0xCA		CFG9		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0		Reserved
6	SIEN_FD	0	RW	<b>System Interrupt Flicker Detection.</b> Enables system interrupt when flicker detection status change has occurred.
5	Reserved			Reserved
4	SIEN_SMUX	0	RW	<b>System Interrupt SMUX Operation.</b> Enables system interrupt when SMUX command has finished
3:0	Reserved			Reserved

**CFG20 Register (Address 0xD6)**

**Figure 57:**  
CFG20 Register

Addr: 0xD6		CFG20		
Bit	Bit Name	Default	Access	Bit Description
7	FD_FIFO_8b	0	RW	<p><b>Enable 8bit FIFO mode for Flicker Detection.</b>                      0: disabled                      1: enabled                      Note: FD_TIME must be smaller than 256, else flicker data might be larger than 8 bit. In that case flicker data gets saturated to 0xFF.</p>
6:5	auto_smux	0	RW	<p><b>Automatic channel read-out</b>  <b>0:</b> 6 Channel                      FZ, FY, FXL, NIR, 2xVIS, FD  <b>1:</b> reserved  <b>2:</b> automatic 12 channel                      Cycle 1: FZ, FY, FXL, NIR, 2xVIS, FD                      Cycle 2: F2, F3, F4, F6, 2xVIS, FD  <b>3:</b> automatic 18 channel                      Cycle 1: FZ, FY, FXL, NIR, 2xVIS, FD                      Cycle 2: F2, F3, F4, F6, 2xVIS, FD                      Cycle 3: F1, F5, F7, F8, 2xVIS, FD                      Note: the bit "auto_smux" should only be changed before a measurement is started.                      Once a measurement is started the device is automatically processing the channels as per definition above and storing the measurement results in the eighteen data registers.                      2xVIS: per default the "Top Left" and "Bot Right" VIS/CLEAR PD is read-out</p>
4:0	Reserved			Reserved

**PERS Register (Address 0xCF)**

**Figure 58:**  
PERS Register

Addr: 0xCF		PERS		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0		Reserved
3:0	APERS	0	RW	<b>Spectral Interrupt Persistence.</b>

Addr: 0xCF		PERS																						
Bit	Bit Name	Default	Access	Bit Description																				
				<p>Defines a filter for the number of consecutive occurrences that spectral data must remain outside the threshold range between SP_TH_L and SP_TH_H before an interrupt is generated. The spectral data channel used for the persistence filter is set by SP_TH_CHANNEL. Any sample that is inside the threshold range resets the counter to 0.</p> <table border="1"> <thead> <tr> <th>VALUE</th> <th>CHANNEL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Every spectral cycle generates an interrupt</td> </tr> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>2</td> <td>2</td> </tr> <tr> <td>3</td> <td>3</td> </tr> <tr> <td>4</td> <td>5</td> </tr> <tr> <td>5</td> <td>10</td> </tr> <tr> <td>...</td> <td>5 x (APERS – 3)</td> </tr> <tr> <td>14</td> <td>55</td> </tr> <tr> <td>15</td> <td>60</td> </tr> </tbody> </table>	VALUE	CHANNEL	0	Every spectral cycle generates an interrupt	1	1	2	2	3	3	4	5	5	10	...	5 x (APERS – 3)	14	55	15	60
VALUE	CHANNEL																							
0	Every spectral cycle generates an interrupt																							
1	1																							
2	2																							
3	3																							
4	5																							
5	10																							
...	5 x (APERS – 3)																							
14	55																							
15	60																							

## 10.2.9 FIFO Buffer Data and Status

The FIFO buffer is used to poll spectral data with fewer I<sup>2</sup>C read and write transactions. The FIFO buffer is 256 bytes of RAM containing 128 two-byte datasets. If the FIFO overflows (i.e. 129 datasets before host reads data from the FIFO buffer), an overflow flag will be set and new data will be lost. The Host acquires data by reading addresses: 0xFE – 0xFF. The register address pointer automatically wraps from 0xFF to 0xFE as data are read. Data can be read one byte at a time or in blocks, (there is no block-read length limit). When reading single bytes, the internal FIFO read pointer and the FIFO Buffer Level, FIFO\_LVL, are updated each time register 0xFF is read. For block-reads, the internal FIFO read pointer and the FIFO Buffer Level, FIFO\_LVL update for each two-byte entry. If the FIFO continues to be accessed after FIFO\_LVL = 0, the device will return 0 for all data. The FINT interrupt indicates when there is valid data in the FIFO buffer. The amount of unread data is indicated by the FIFO\_LVL.

### FIFO\_MAP Register (Address 0xFC)

Figure 59:  
FIFO\_MAP Register

Addr: 0xFC		FIFO_MAP		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0		Reserved
6	FIFO_WRITE_CH5_DATA	0	RW	<b>FIFO Write CH5 Data.</b> If set, CH5 data is written to the FIFO Buffer. (two bytes per sample) Note: If flicker detection is enabled, this bit is ignored. Refer to register 0xD7 for FDEN="1".
5	FIFO_WRITE_CH4_DATA	0	RW	<b>FIFO Write CH4 Data.</b> If set, CH4 data is written to the FIFO Buffer. (two bytes per sample)
4	FIFO_WRITE_CH3_DATA	0	RW	<b>FIFO Write CH3 Data.</b> If set, CH3 data is written to the FIFO Buffer. (two bytes per sample)
3	FIFO_WRITE_CH2_DATA	0	RW	<b>FIFO Write CH2 Data.</b> If set, CH2 data is written to the FIFO Buffer. (two bytes per sample)
2	FIFO_WRITE_CH1_DATA	0	RW	<b>FIFO Write CH1 Data.</b> If set, CH1 data is written to the FIFO Buffer. (two bytes per sample)
1	FIFO_WRITE_CH0_DATA	0	RW	<b>FIFO Write CH0 Data.</b> If set, CH0 data is written to the FIFO Buffer. (two bytes per sample)
0	FIFO_WRITE_ASTATUS	0	RW	<b>FIFO Write Status.</b> If set, ASTATUS (one byte per sample) is written to the FIFO Buffer.

**FIFO\_CFG0 Register (Address 0xDF)**

**Figure 60:**  
FIFO\_CFG0 Register

Addr: 0xDF		FIFO_CFG0		
Bit	Bit Name	Default	Access	Bit Description
7	FIFO_WRITE_FD	0	RW	<b>FIFO Write Flicker Detection</b> If set flicker raw data is written into FIFO (one byte per sample) Note: This bit is ignored if flicker detection is disabled. Refer to register 0xFC for FDEN="0".
6:0	Reserved	0100001		Reserved, do not change

**FIFO\_LVL Register (Address 0xFD)**

**Figure 61:**  
FIFO\_LVL Register

Addr: 0xFD		FIFO_LVL		
Bit	Bit Name	Default	Access	Bit Description
7:0	FIFO_LVL	0	R	<b>FIFO Buffer Level.</b> Indicates the number of entries (each are 2 bytes) available in the FIFO buffer waiting for readout. The FIFO RAM is 256byte, the FIFO_LVL range is from 0 entries to 128 entries.

**FDATA Register (Address 0xFE and 0xFF)**

**Figure 62:**  
FDATA\_L Register

Addr: 0xFE		FDATA_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	FDATA	0	R	FIFO Buffer Data

Figure 63:  
FDATA\_H Register

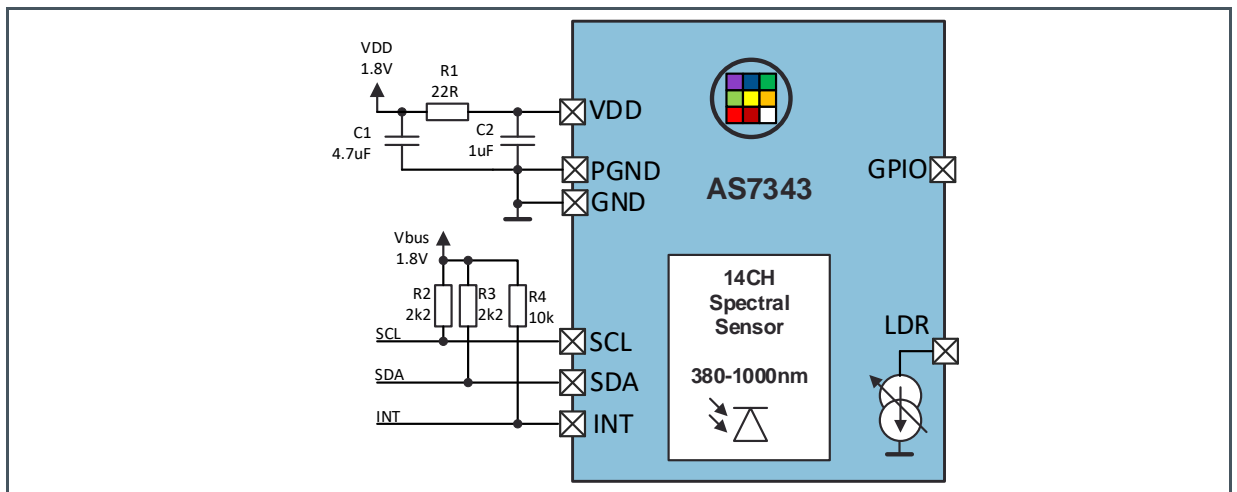
Addr: 0xFF		FDATA_H		
Bit	Bit Name	Default	Access	Bit Description
15:8	FDATA	0	R	FIFO Buffer Data



# 11 Application Information

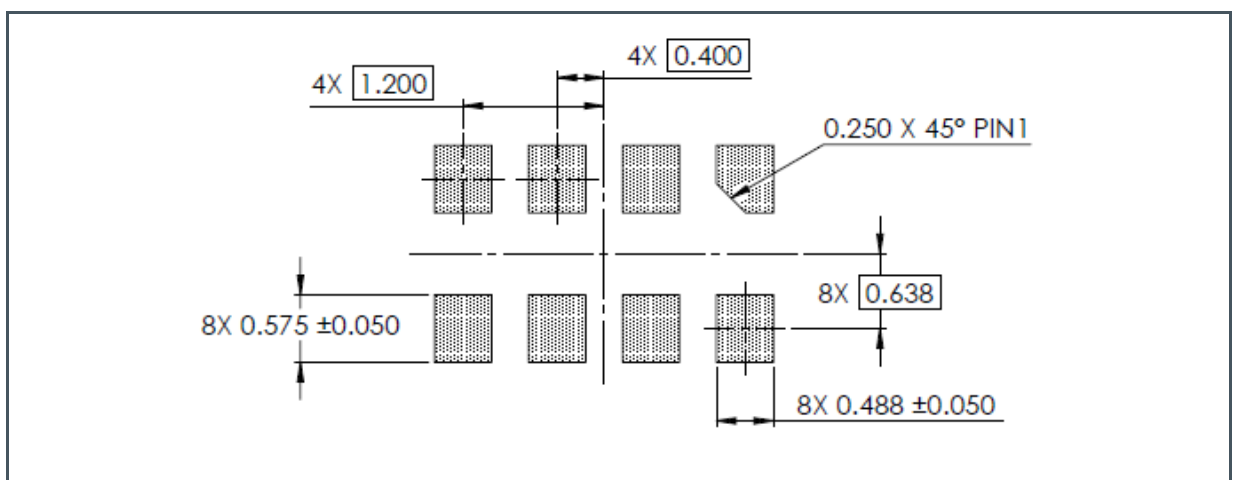
## 11.1 Schematic

Figure 64:  
Application Example



## 11.2 PCB Pad Layout

Figure 65:  
Recommended PCB Pad Layout

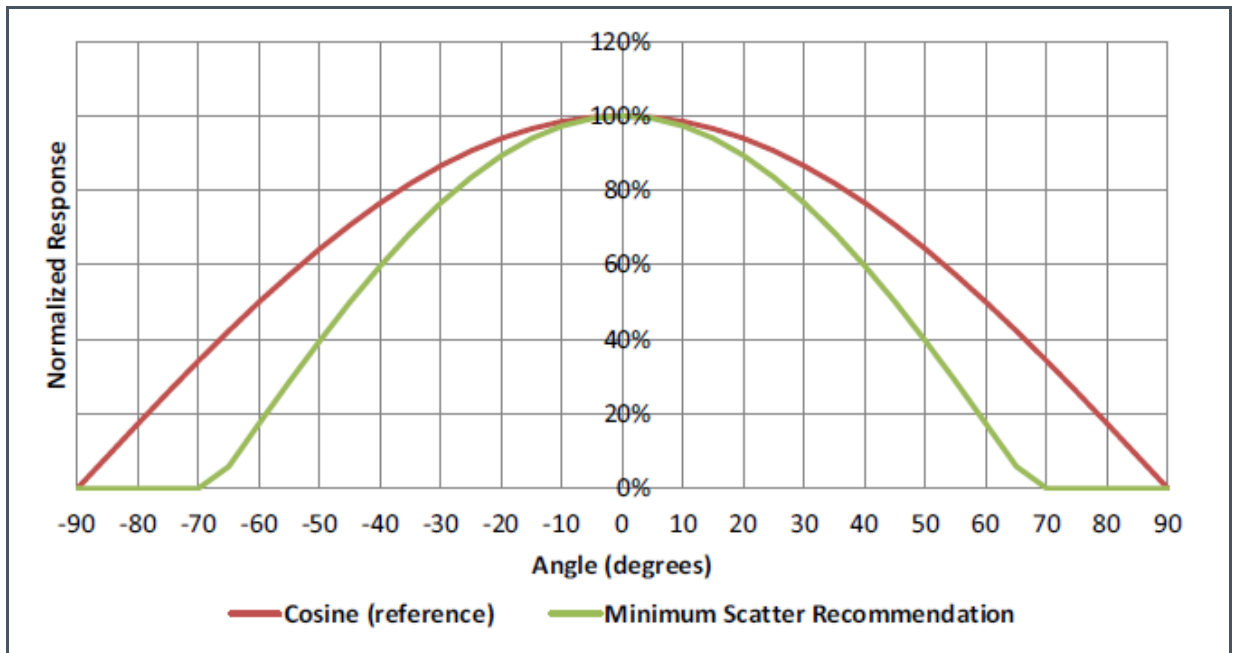


- (1) All dimensions are in millimeters.
- (2) Dimension tolerances are 0.05 mm unless otherwise noted.
- (3) This drawing is subject to change without notice.

### 11.3 Application Optical Requirements

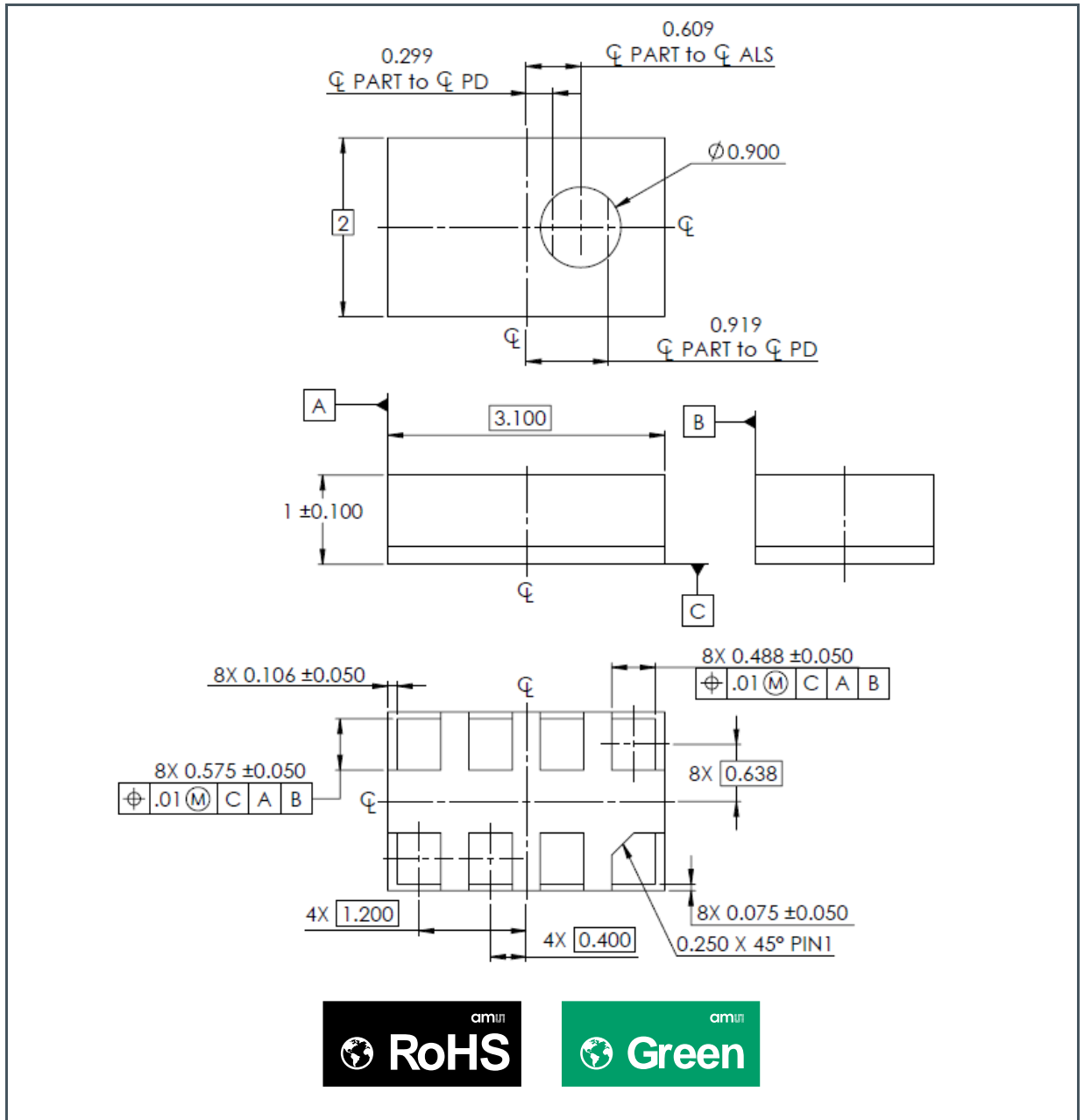
For optimal performance, an achromatic diffuser shall be placed above the device aperture. The recommended solution is a bulk diffuser that meets the minimum recommended scattering characteristic shown below. For more details refer to the optical design guide or contact **ams**.

Figure 66:  
Diffuser Characteristics



# 12 Package Drawings & Markings

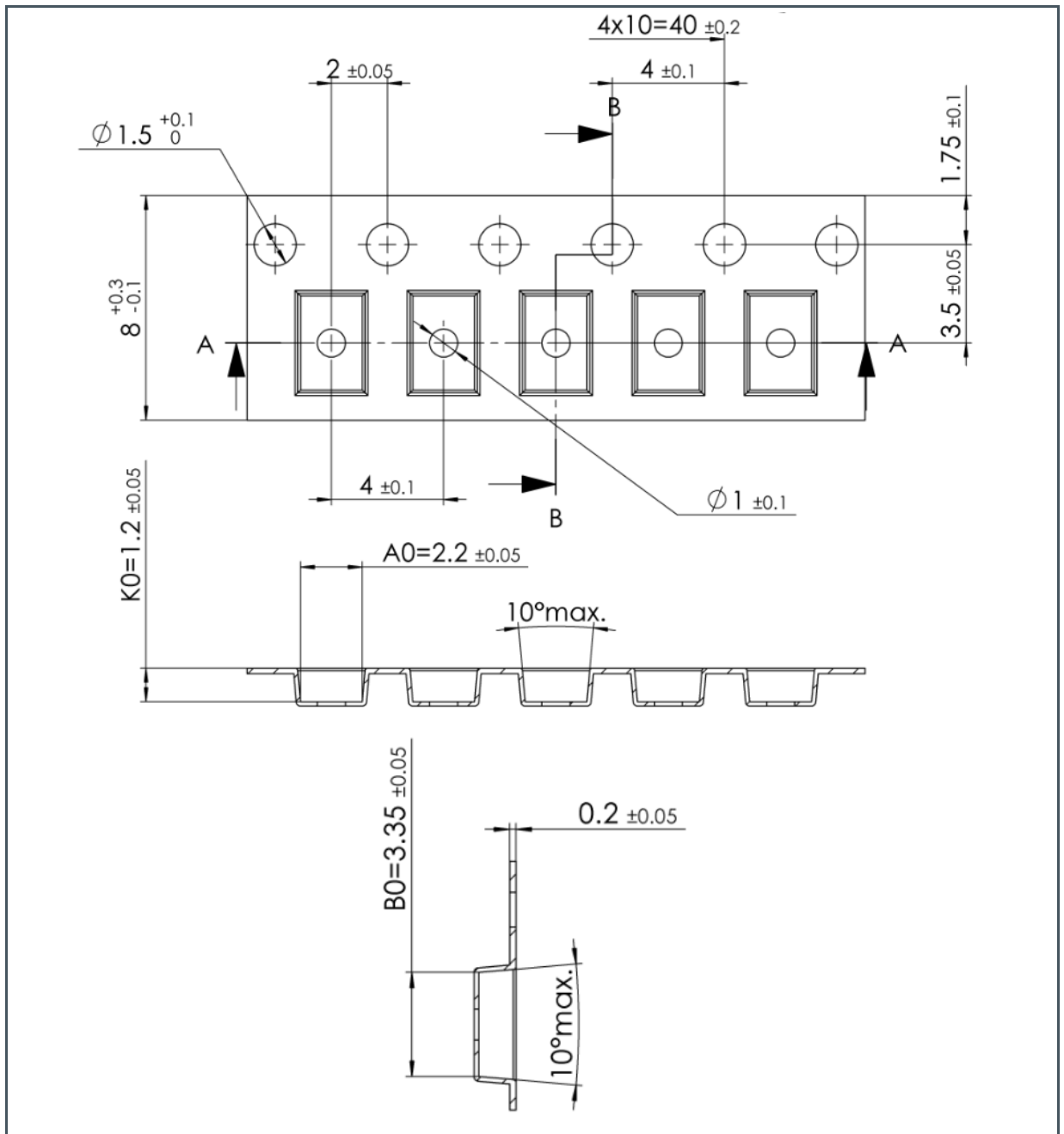
Figure 67:  
OLGA8 Package Outline Drawing



- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Dimensioning and tolerance conform to ASME Y14.5M-1994.
- (3) This package contains no lead (Pb).
- (4) This drawing is subject to change without notice.

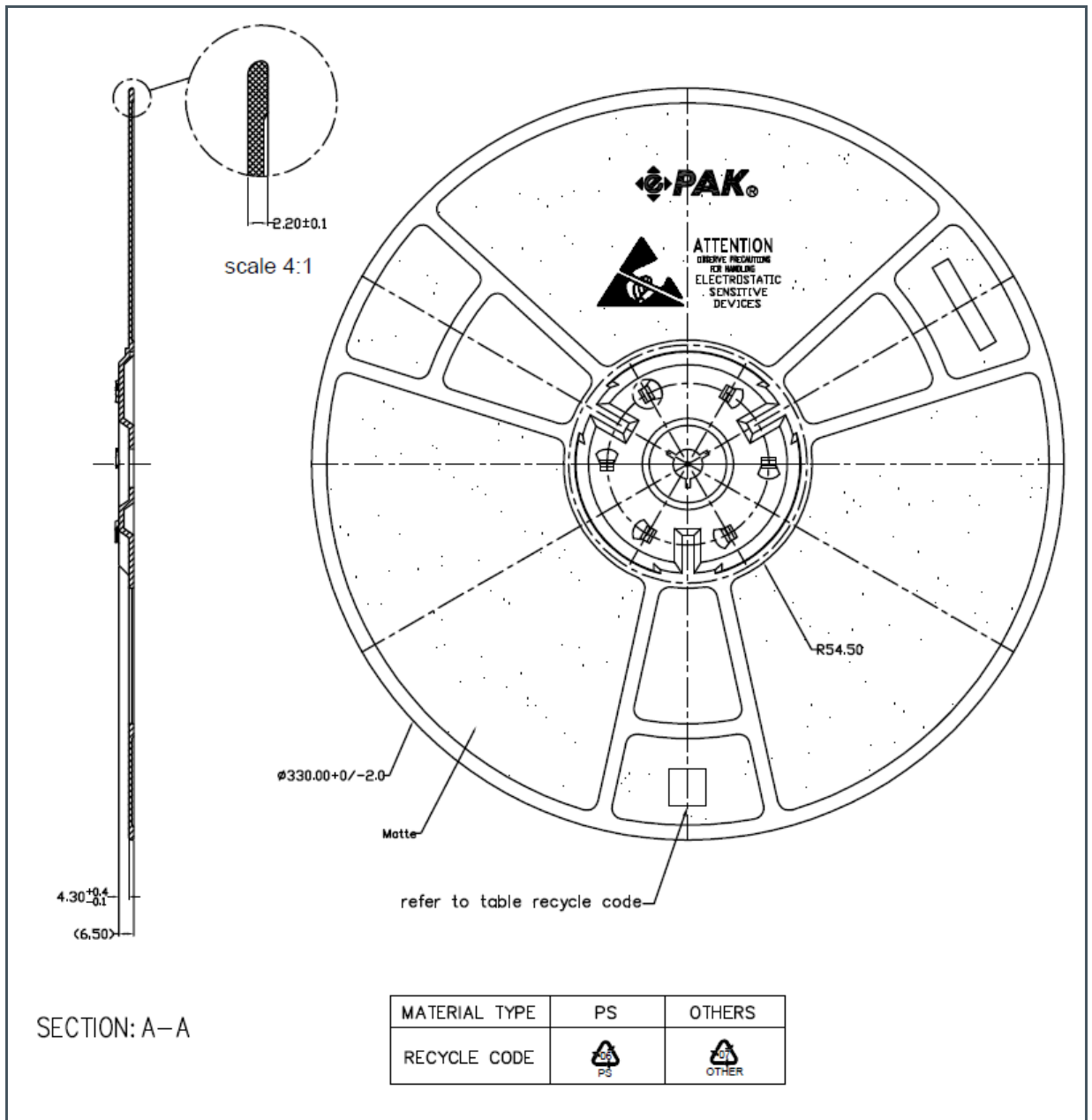
# 13 Tape & Reel Information

Figure 68:  
AS7343 OLGA8 Tape Dimensions



- (1) All dimensions are in millimeters. Angles in degrees.
- (2) This drawing is subject to change without notice.

Figure 69:  
AS7343 OLGA8 Reel Dimensions

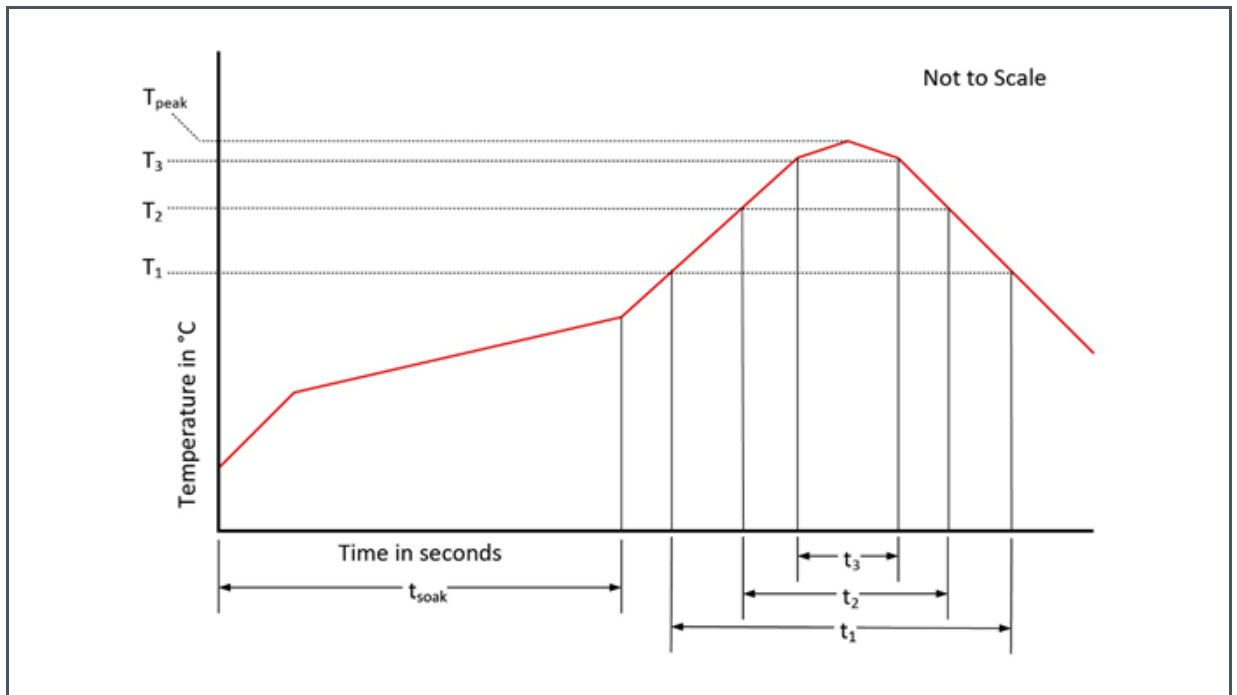


- (1) All dimensions are in millimeters. Angles in degrees.
- (2) This drawing is subject to change without notice.

# 14 Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

**Figure 70:**  
Solder Reflow Profile Graph



**Figure 71:**  
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	$t_{soak}$	2 to 3 minutes
Time above 217 °C (T1)	$t_1$	Max 60 s
Time above 230 °C (T2)	$t_2$	Max 50 s
Time above $T_{peak} - 10$ °C (T3)	$t_3$	Max 10 s
Peak temperature in reflow	$T_{peak}$	260 °C
Temperature gradient in cooling		Max -5 °C/s

---

## 14.1 Storage Information

### 14.1.1 Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

### 14.1.2 Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40 °C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

### 14.1.3 Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

### 14.1.4 Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50 °C for 12 hours.

# 15 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v2-00	Page
Initial version	
Updated REG_BANK description in chapter 10	21

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.