

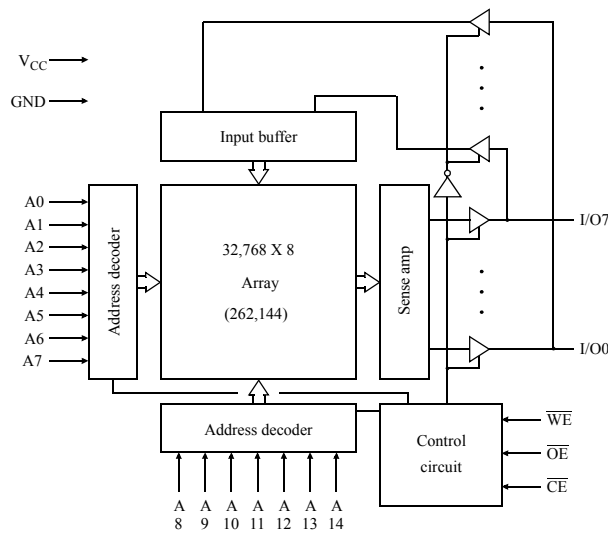


5V 32K X 8 CMOS SRAM (Common I/O)

Features

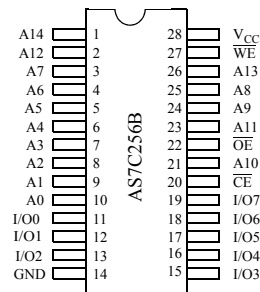
- Industrial (-40° to 85°C) temperature
- Organization: 32,768 words × 8 bits
- High speed
  - 15 ns address access time
  - 6 ns output enable access time
- Low power consumption via chip deselect
- One chip select plus one Output Enable pin
- Bidirectional data inputs and outputs
- TTL-compatible
- 28-pin JEDEC standard packages
  - 300 mil SOJ
  - 8 × 13.4 mm TSOP
  - 300 mil PDIP
- ESD protection ≥ 2000 volts

Logic block diagram

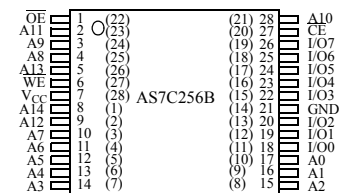


Pin arrangement

28-pin DIP, SOJ (300 mil)



28-pin TSOP 1 (8×13.4mm)



Note: This part is compatible with both pin numbering conventions used by various manufacturers.



## Functional description

The AS7C256B is a 5V high-performance CMOS 262,144-bit Static Random-Access Memory (SRAM) device organized as 32,768 words  $\times$  8 bits. It is designed for memory applications requiring fast data access at low voltage, including Pentium™, PowerPC™, and portable computing. Alliance's advanced circuit design and process techniques permit 5.0V operation without sacrificing performance or operating margins.

The device enters *standby mode* when  $\overline{CE}$  is high. Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 12 ns with output enable access times ( $t_{OE}$ ) of 6 ns are ideal for high-performance applications. The chip enable ( $\overline{CE}$ ) input permits easy memory expansion with multiple-bank memory organizations.

A write cycle is accomplished by asserting chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or  $\overline{CE}$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) LOW, with write enable ( $\overline{WE}$ ) high. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is high, or write enable is low, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible. Operation is from a single 5.0 $\pm$ 0.5V supply. The AS7C256B is packaged in high volume industry standard packages.

## Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on $V_{CC}$ relative to GND	$V_{I1}$	-0.5	+7.0	V
Voltage on any pin relative to GND	$V_{I2}$	-0.5	$V_{CC} + 0.5$	V
Power dissipation	$P_D$	-	1.25	W
Storage temperature (plastic)	$T_{stg}$	-55	+125	°C
Ambient temperature with $V_{CC}$ applied	$T_{bias}$	-55	+125	°C
DC current into outputs (low)	$I_{OUT}$	-	50	mA

### Note:

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
L	H	H	High Z	Output disable ( $I_{CC}$ )
L	H	L	$D_{OUT}$	Read ( $I_{CC}$ )
L	L	X	$D_{IN}$	Write ( $I_{CC}$ )

### Notes:

H =  $V_{IH}$ , L =  $V_{IL}$ , x = Don't care.

$V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$ .

Other inputs  $\geq V_{HC}$  or  $V_{LC}$ .



### Recommended operating conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage	$V_{IH}$	2.2	–	$V_{CC}+0.5$	V
	$V_{IL}^{(1)}$	$-0.5^{(1)}$	–	0.8	V
Ambient operating temperature (Industrial)	$T_A$	–40	–	85	°C

#### Note:

<sup>1</sup>  $V_{IL}$  min = –1.5V for pulse width less than 10ns, once per cycle.

### DC operating characteristics (over the operating range)<sup>1</sup>

Parameter	Symbol	Test conditions	AS7C256B-17		Unit
			Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{in} = \text{GND to } V_{CC}$	–	5	$\mu\text{A}$
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}, \overline{CS} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	–	5	$\mu\text{A}$
Operating power supply current	$I_{CC}$	$V_{CC} = \text{Max}, \overline{CE} \leq V_{IL}$ $f = f_{\text{Max}}, I_{OUT} = 0\text{mA}$	–	150	mA
Standby power supply current	$I_{SB}$	$V_{CC} = \text{Max}, \overline{CE} \geq V_{IH}$ $f = f_{\text{Max}}, I_{OUT} = 0\text{mA}$	–	40	mA
	$I_{SB1}$	$V_{CC} = \text{Max}, \overline{CE} \geq V_{CC}-0.2\text{V}$ $V_{IN} \leq \text{GND} + 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}, f = 0^{(2)}$	–	15	mA
Output voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	–	0.4	V
	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4	–	V

#### Notes:

All values are maximum guaranteed values.

$f_{\text{Max}} = 1/t_{RC}$ , only address inputs cycling at  $f_{\text{Max}}$ ,  $f = 0$  means that no inputs are cycling.

### Capacitance ( $f = 1\text{MHz}, T_a = \text{room temperature}, V_{CC} = \text{NOMINAL}$ )<sup>2</sup>

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	A, $\overline{CE}$ , $\overline{WE}$ , $\overline{OE}$	$V_{in} = 3\text{dV}$	7	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{out} = 3\text{dV}$	7	pF

#### Note:

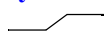


This parameter is guaranteed by device characterization, but is not production tested.



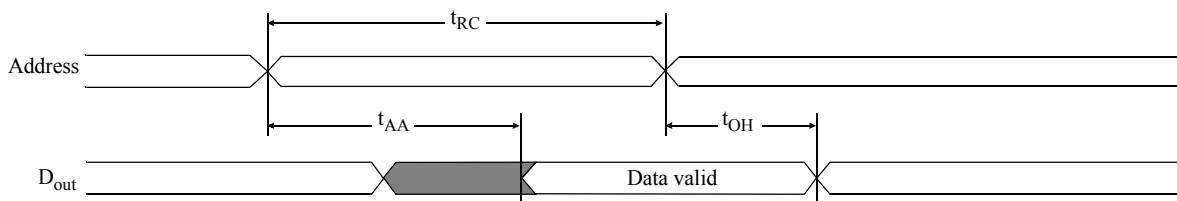
### Read cycle (over the operating range)<sup>3,9</sup>

Parameter	Symbol	AS7C256B-17		Unit	Notes
		Min	Max		
Read cycle time	$t_{RC}$	15	-	ns	
Address access time	$t_{AA}$		15	ns	3
Chip enable ( $\overline{CE}$ ) access time	$t_{ACE}$		15	ns	3
Output enable ( $\overline{OE}$ ) access time	$t_{OE}$	-	7	ns	
Output hold from address change	$t_{OH}$	3	-	ns	5
$\overline{CE}$ LOW to output in low Z	$t_{CLZ}$	4	-	ns	4, 5
$\overline{CE}$ HIGH to output in high Z	$t_{CHZ}$	0	7	ns	4, 5
$\overline{OE}$ LOW to output in low Z	$t_{OLZ}$	0	-	ns	4, 5
$\overline{OE}$ HIGH to output in high Z	$t_{OHZ}$	0	6	ns	4, 5
Power up time	$t_{PU}$	0	-	ns	4, 5
Power down time	$t_{PD}$	-	15	ns	4, 5

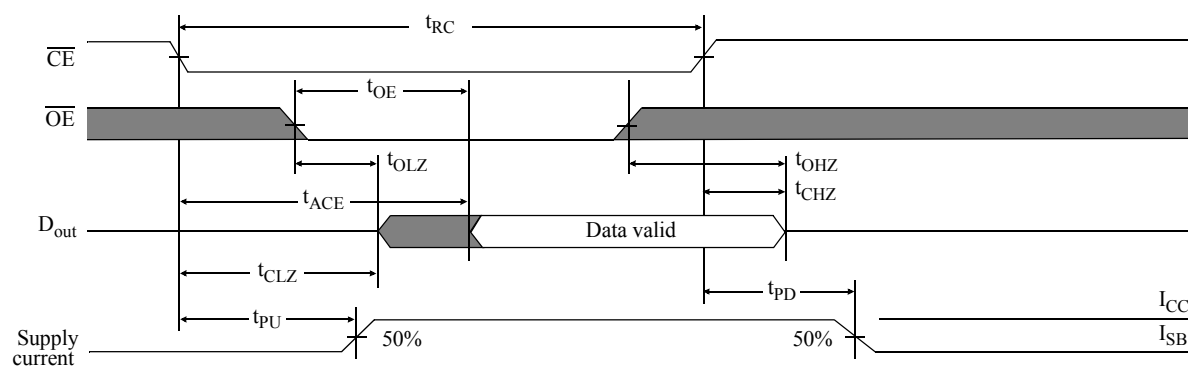
### Key to switching waveforms

 Rising input    
  Falling input    
  Undefined output/don't care

### Read waveform 1 (address controlled)<sup>3,6,7,9</sup>



### Read waveform 2 ( $\overline{CE}$ controlled)<sup>3,6,8,9</sup>



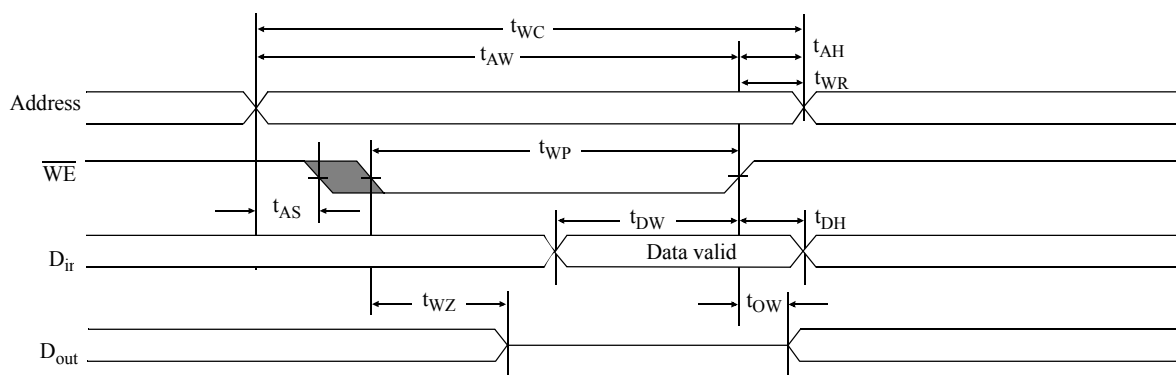


### Write cycle (over the operating range)<sup>11</sup>

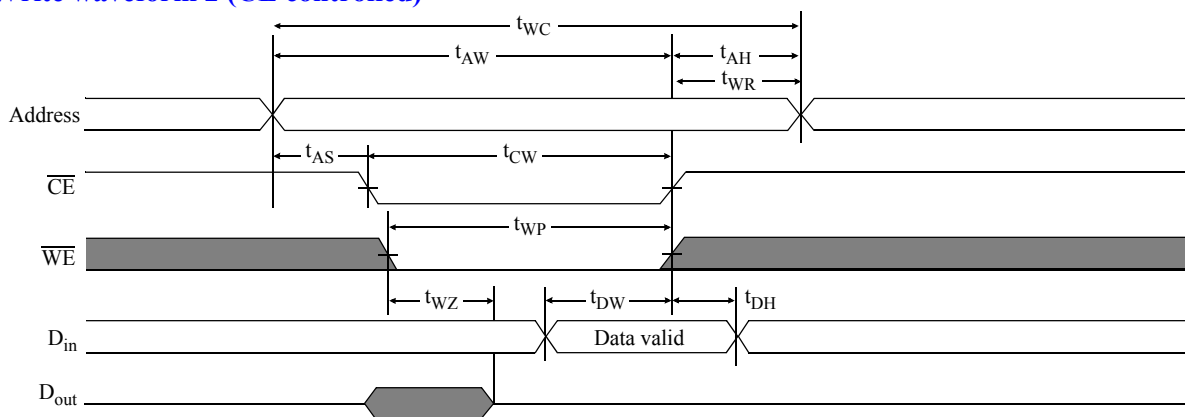
Parameter	Symbol	AS7C256B-15		Unit	Notes
		Min	Max		
Write cycle time	$t_{WC}$	15	–	ns	
Chip enable to write end	$t_{CW}$	10	–	ns	
Address setup to write end	$t_{AW}$	10	–	ns	
Address setup time	$t_{AS}$	0	–	ns	
Write pulse width	$t_{WP}$	10	–	ns	
Write recovery time	$t_{WR}$	0	–	ns	
Address hold from end of write	$t_{AH}$	0	–	ns	
Data valid to write end	$t_{DW}$	7	–	ns	
Data hold time	$t_{DH}$	0	–	ns	4, 5
Write enable to output in high Z	$t_{WZ}$	0	6	ns	4, 5
Output active from write end	$t_{OW}$	4	–	ns	4, 5

Shaded areas contain advance information.

### Write waveform 1 ( $\overline{WE}$ controlled)<sup>10,11</sup>



### Write waveform 2 ( $\overline{CE}$ controlled)<sup>10,11</sup>





### AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to  $V_{CC}$ . See Figure A.
- Input rise and fall times: 3 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

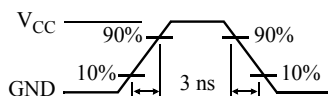


Figure A: Input pulse

Thevenin equivalent

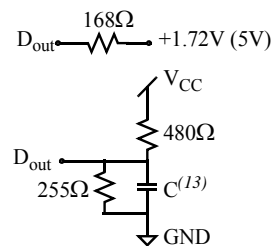


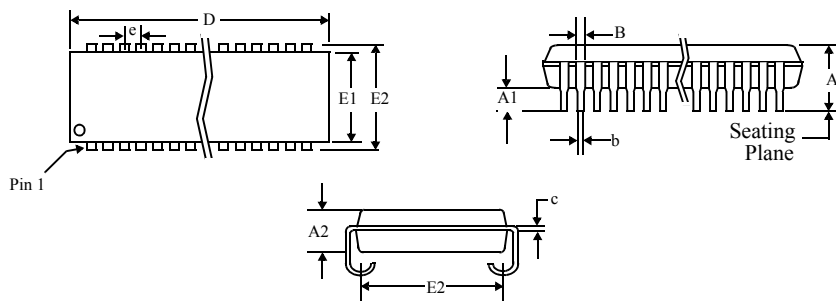
Figure B: Output load

### Notes

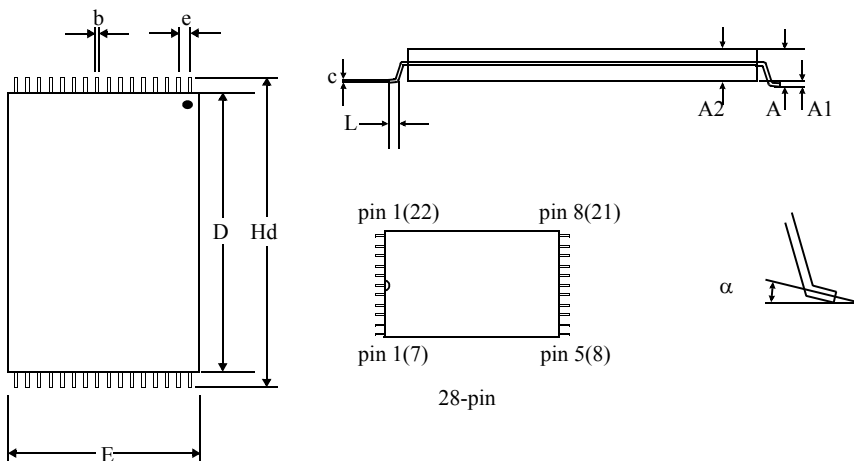
- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{CE}$  is required to meet  $I_{SB}$  specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see *AC Test Conditions*, Figures A and B.
- 4 These parameters are specified with  $C_L = 5\text{pF}$ , as in Figures B. Transition is measured  $\pm 200\text{mV}$  from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- 6  $\overline{WE}$  is High for read cycle.
- 7  $\overline{CE}$  and  $\overline{OE}$  are Low for read cycle.
- 8 Address valid prior to or coincident with  $\overline{CE}$  transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10  $\overline{CE}$  or  $\overline{WE}$  must be High during address transitions. Either  $\overline{CE}$  or  $\overline{WE}$  asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12  $\overline{CE1}$  and  $\overline{CE2}$  have identical timing.
- 13  $C = 30\text{pF}$ , except on High Z and Low Z parameters, where  $C = 5\text{pF}$ .



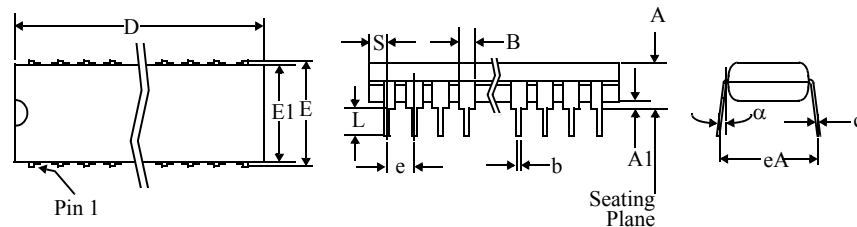
Package diagrams



28-pin SOJ		
	Min	Max
in mils		
A	-	0.140
A1	0.025	-
A2	0.095	0.105
B	0.028 TYP	
b	0.018 TYP	
c	0.010 TYP	
D	-	0.730
E	0.245	0.285
E1	0.295	0.305
E2	0.327	0.347
e	0.050 BSC	



28-pin TSOP 8×13.4 mm		
	Min	Max
A	-	1.20
A1	0.10	0.20
A2	0.95	1.05
b	0.15	0.25
c	0.10	0.20
D	11.60	11.80
e	0.55 nominal	
E	8.0 nominal	
Hd	13.30	13.50
L	0.50	0.70
α	0°	5°



28-pin PDIP		
	Min	Max
in mils		
A	-	0.180
A1	0.010	-
B	0.040	0.065
b	0.014	0.022
c	0.008	0.014
D	-	1.400
E	0.295	0.320
E1	0.278	0.298
e	0.100 BSC	
eA	0.330	0.380
L	0.120	0.140
a	0°	15°
S	-	0.055

Note: This part is compatible with both pin numbering conventions used by various manufacturers.