1M X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 10ns
- **Very low power consumption:**
  Operating current:
    80mA(TYP. 10ns)
  Standby current (Normal version):
    3mA(TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
Package: 44-pin 400 mil TSOP-II
            48-ball 6mmx8mm TFBGA

GENERAL DESCRIPTION

The AS7C38096A is a 8M-bit high speed CMOS static random access memory organized as 1,024K words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C38096A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible
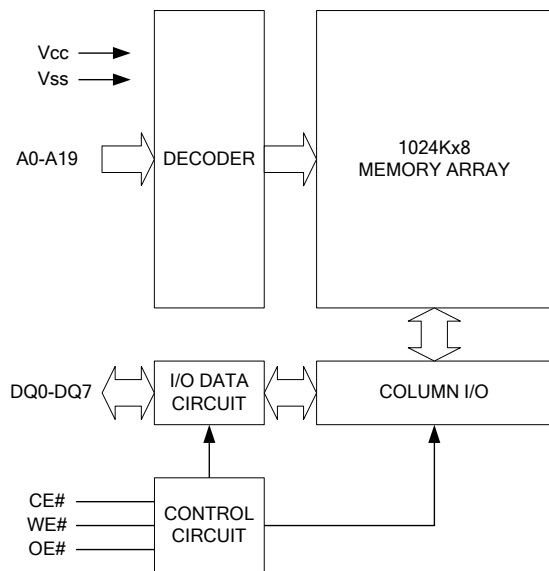
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{cc1},TYP.)
AS7C38096A	-40 ~ 85℃	2.7 ~ 3.6V	10ns	3mA	80/70mA

1M X 8 BIT HIGH SPEED CMOS SRAM

FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

1M X 8 BIT HIGH SPEED CMOS SRAM

PIN CONFIGURATION

44-pin TSOP(Type II)

Pin	Signal		Pin	Signal
1	NC		44	NC
2	NC		43	NC
3	A4		42	NC
4	A3		41	A5
5	A2		40	A6
6	A1		39	A7
7	A0		38	A8
8	CE#		37	OE#
9	DQ0		36	DQ7
10	DQ1		35	DQ6
11	Vcc		34	Vss
12	Vss		33	Vcc
13	DQ2		32	DQ5
14	DQ3		31	DQ4
15	WE#		30	A9
16	A19		29	A10
17	A18		28	A11
18	A17		27	A12
19	A16		26	A13
20	A15		25	A14
21	NC		24	NC
22	NC		23	NC

AS7C38096A

TSOP-II

48-ball 6mmx8mm TFBGA

	1	2	3	4	5	6
A	NC	OE#	A0	A1	A2	NC
B	NC	NC	A3	A4	CE#	NC
C	DQ0	NC	A5	A6	NC	DQ4
D	Vss	DQ1	A17	A7	DQ5	Vcc
E	Vcc	DQ2	NC	A16	DQ6	Vss
F	DQ3	NC	A14	A15	NC	DQ7
G	NC	NC	A12	A13	WE#	NC
H	A18	A8	A9	A10	A11	A19

TFBGA

3

1M X 8 BIT HIGH SPEED CMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	-40 to 85	℃
Storage Temperature	T_{STG}	-65 to 150	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC}
Read	L	L	H	D_{OUT}	I_{CC}
Write	L	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. [4]	MAX.	UNIT
Supply Voltage	V_{CC}		-10	2.7	3.3	3.6	V
Input High Voltage	V_{IH} [1]			2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} [2]			- 0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -8mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} =4mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	CE# = V_{IL} , $I_{I/O}$ = 0mA ;f=max	-10	-	100	130	mA
	I_{CC1}	CE# $\geqq V_{CC}$ - 0.2V, Other pin is at 0.2V or Vcc-0. $I_{I/O}$ = 0mA;f=max	-10		80	110	mA
Standby Power Supply Current	I_{sb}	CE# $\geqq$ Vih Other pin is at Vil or Vih				40	mA
Standby Power Supply Current	I_{SB1}	CE# $\geqq V_{CC}$ - 0.2V; Other pin is at 0.2V or Vcc-0.2V			3	25	mA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.

1M X 8 BIT HIGH SPEED CMOS SRAM

4. Typical values are included for reference only and are not guaranteed or tested.

   Typical valued are measured at $V_{CC} = V_{CC}$(TYP.) and $T_A = 25°C$

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

speed	10ns
Input Pulse Levels	0.2V to Vcc-0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL,$ $I_{OH}/I_{OL} = -4mA/8mA$

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C38096A-10		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	ns
Address Access Time	t_{AA}	-	10	ns
Chip Enable Access Time	t_{ACE}	-	10	ns
Output Enable Access Time	t_{OE}	-	4.5	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	2	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	4	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	4	ns
Output Hold from Address Change	t_{OH}	2	-	ns

(2) WRITE CYCLE

| PARAMETER	SYM.	AS7C38096A-10		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	ns
Address Valid to End of Write	t_{AW}	8	-	ns
Chip Enable to End of Write	t_{CW}	8	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	8	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	2	-	ns
Write to Output in High-Z	t_{WHZ}*	-	4	ns

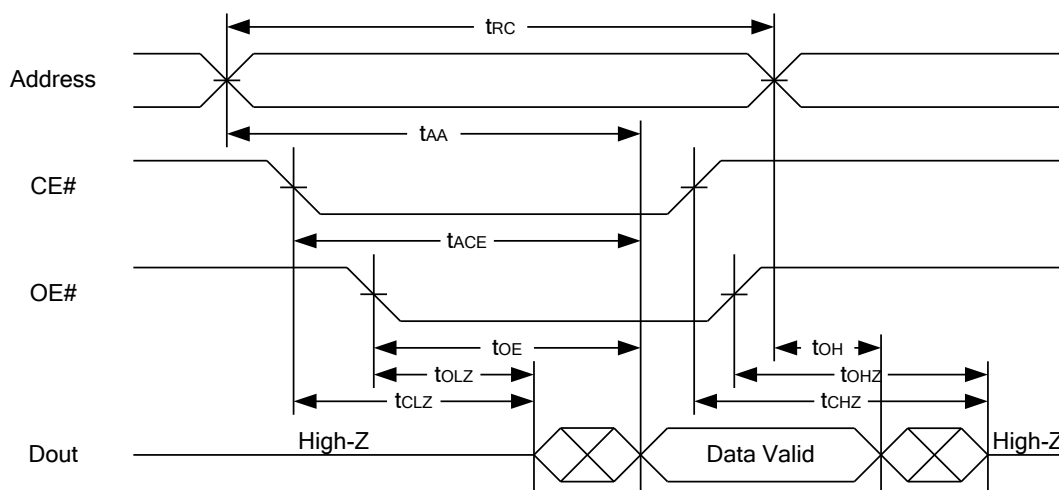*These parameters are guaranteed by device characterization, but not production tested.

1M X 8 BIT HIGH SPEED CMOS SRAM

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)
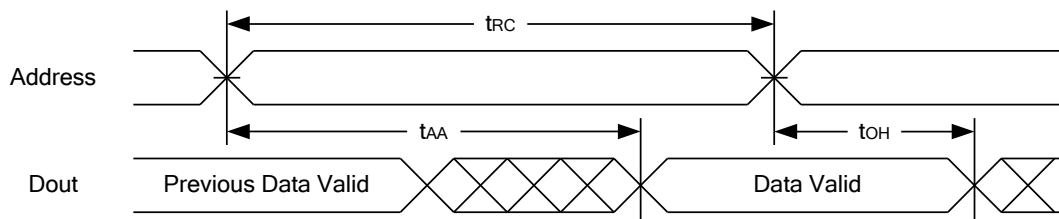
**READ CYCLE 2** (CE# and OE# Controlled) (1,3,4,5)

Notes :
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low.; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

1M X 8 BIT HIGH SPEED CMOS SRAM

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)
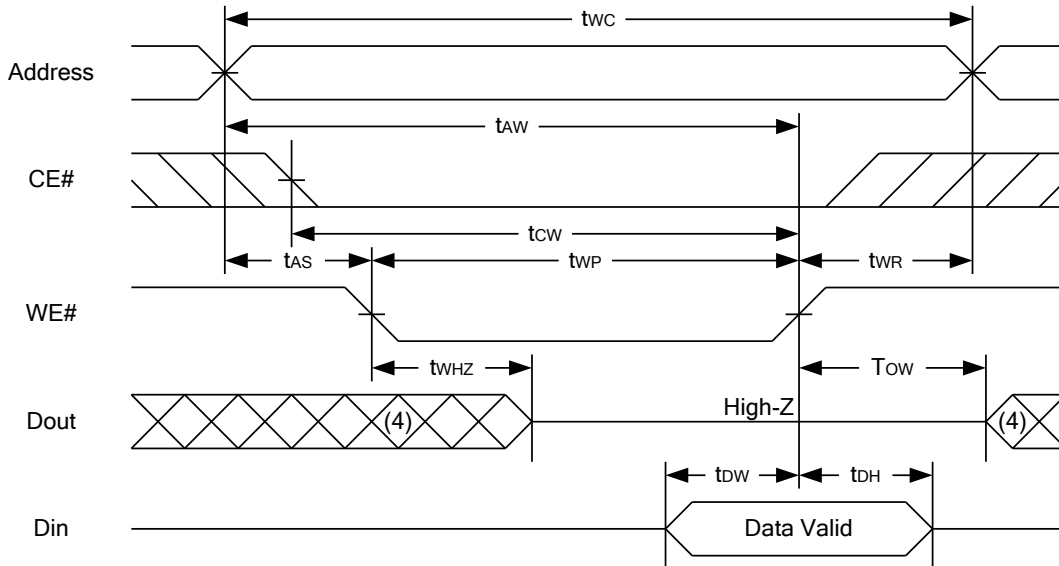
WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)
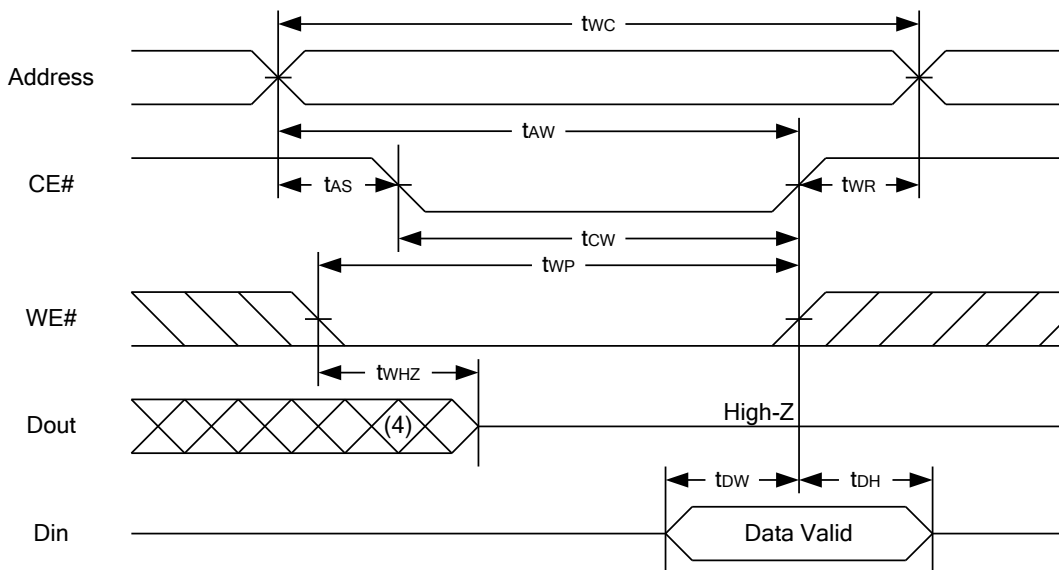
Notes :

1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
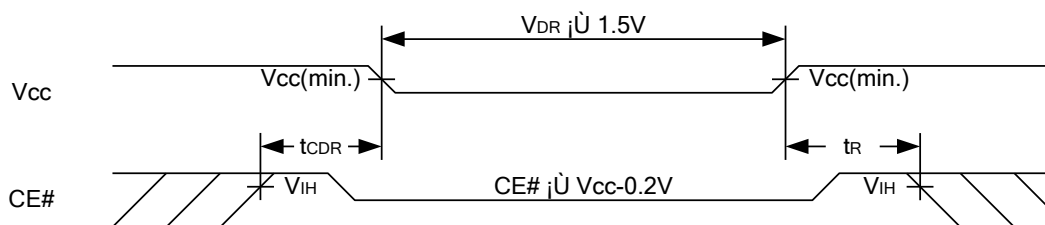
1M X 8 BIT HIGH SPEED CMOS SRAM

DATA RETENTION CHARACTERISTICS

| PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# $\geq$ V_{CC} - 0.2V	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} =1.5V CE# $\geq V_{CC}$ - 0.2V; Other pin is at 0.2V or Vcc-0.2V	- -	3	25	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC*}	-	-	ns

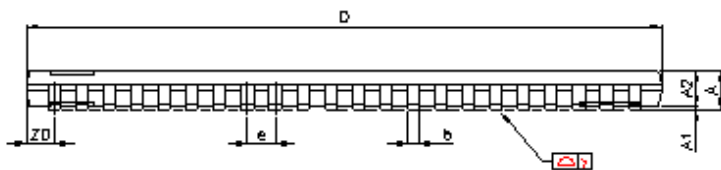t_{RC*} = Read Cycle Time
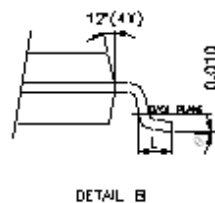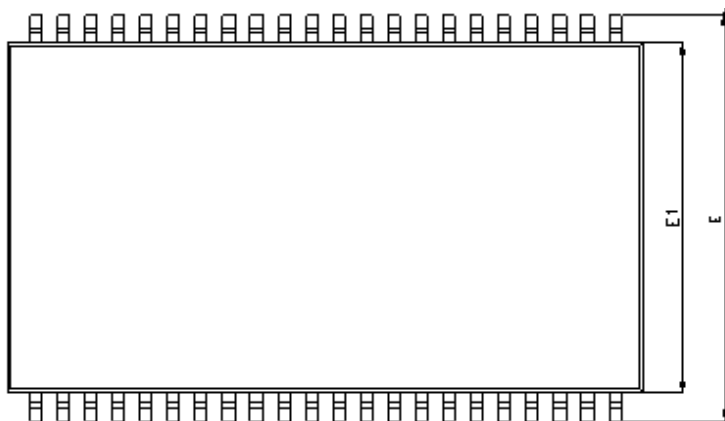
DATA RETENTION WAVEFORM

1M X 8 BIT HIGH SPEED CMOS SRAM

PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-Ⅱ Package Outline Dimension
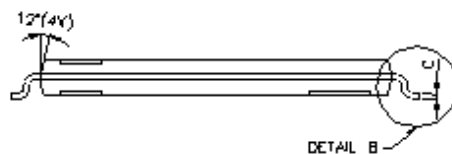
SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
Θ	0°	3°	6°	0°	3°	6°

1M X 8 BIT HIGH SPEED CMOS SRAM

48-ball 6mm × 8mm TFBGA Package Outline Dimension

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

SOLDER BALL

Øb(48x PLACES)

DETAIL B
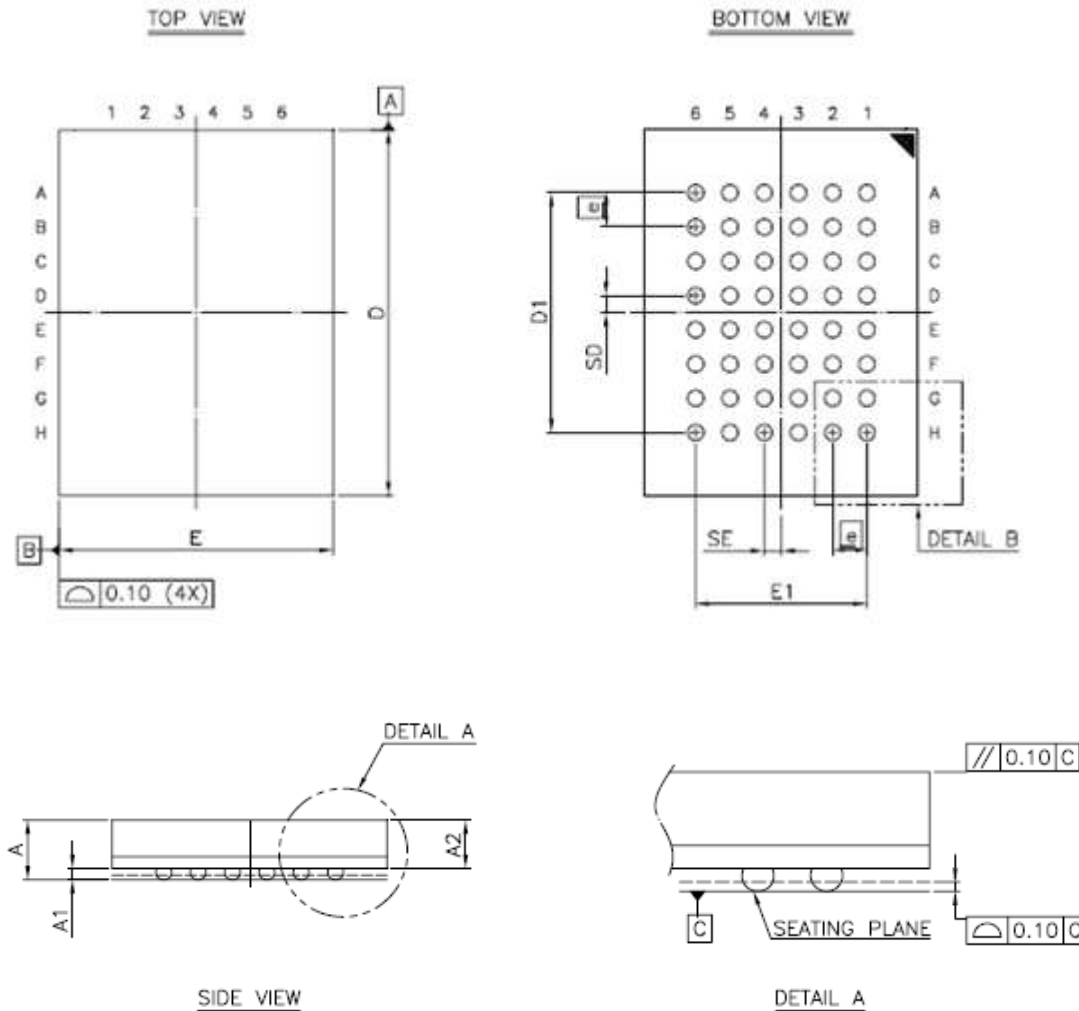
SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		
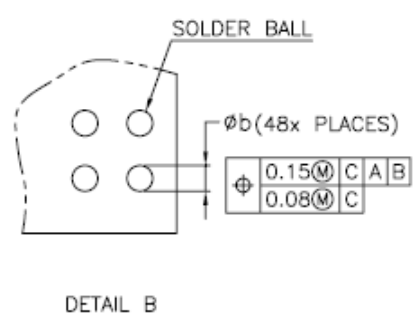
NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.