# AT-107-PIN

## Digital Attenuator
## 31.5 dB, 6-Bit, TTL Driver, DC-2.0 GHz

Rev. V9

### Features

- Attenuation: 0.5 dB steps to 31.5 dB
- Temperature Stability: ± 0.18 dB from –55°C to +85°C Typical
- Low DC Power Consumption
- Hermetic Surface Mount Package
- Integral TTL Driver
- 50 Ohm Nominal Impedance
- Lead-Free CR-13 Package
- 260°C Reflow Compatible
- RoHS* Compliant

### Description

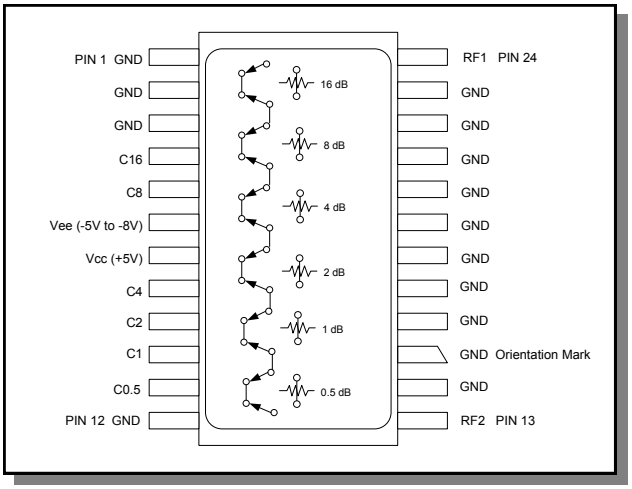
M/A-COM's AT-107-PIN is a GaAs FET 6-bit digital attenuator with a 0.5 dB minimum step size and 31.5 dB total attenuation. This attenuator and integral TTL driver is in a hermetically sealed ceramic 24-lead surface mount package. The AT-107-PIN is ideally suited for use where accuracy, fast switching, very low power consumption and low intermodulation products are required. Typical applications include dynamic range setting in precision receiver circuits and other gain/leveling control circuits. Environmental screening is available. Contact the factory for information.

### Ordering Information

| Part Number | Package |
|---|---|
| AT-107-PIN | Bulk Packaging |
| AT-107-TB | Sample Test Board |

Note: Reference Application Note M513 for reel size information.

### Functional Schematic




### Pin Configuration

| Pin No. | Function | Pin No. | Function |
|---|---|---|---|
| 1 | GND | 13 | RF2 |
| 2 | GND | 14 | GND |
| 3 | GND | 15 | GND |
| 4 | C16 | 16 | GND |
| 5 | C8 | 17 | GND |
| 6 | Vee (-5V to -8V) | 18 | GND |
| 7 | Vcc (+5V) | 19 | GND |
| 8 | C4 | 20 | GND |
| 9 | C2 | 21 | GND |
| 10 | C1 | 22 | GND |
| 11 | C0.5 | 23 | GND |
| 12 | GND | 24 | RF1 |

The metal bottom of the case must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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### Electrical Specifications: $T_A$ = -55°C to +85°C [1]

| Parameter | Test Conditions | Frequency | Units | Min | Typ | Max |
|---|---|---|---|---|---|---|
| Reference Insertion Loss | — | DC - 0.5 GHz<br>DC - 1.0 GHz<br>DC - 2.0 GHz | dB<br>dB<br>dB | —<br>—<br>— | —<br>—<br>— | 3.2<br>3.6<br>4.0 |
| Attenuation Accuracy [2] | Any Single Bit<br><br>Any Combination of Bits | DC - 1.0 GHz<br>DC - 2.0 GHz<br>DC - 1.0 GHz<br><br>DC - 2.0 GHz | ± (0.15 +3% of atten. setting in dB) dB<br>± (0.2 +3% of atten. setting in dB) dB<br>± (0.2 +3% of atten. setting in dB) dB<br>or ± 0.4 dB, whichever is greater<br>± (0.2 +3% of atten. setting in dB) dB<br>or ± 0.4 dB, whichever is greater | | | |
| VSWR | — | DC - 2.0 GHz | Ratio | — | — | 1.8:1 |
| Trise, Tfall | 10% to 90% | — | ns | — | 9 | — |
| Ton, Toff | 50% Control to 90/10% RF | — | ns | — | 45 | — |
| Transients | In-Band (peak-peak) | — | mV | — | 40 | — |
| 1 dB Compression | Input Power<br>Input Power | 0.05 GHz<br>0.5 - 2.0 GHz | dBm<br>dBm | —<br>— | +21<br>+29 | —<br>— |
| Input IP3 | For two-tone Input Power<br>Up to +5 dBm | 0.05 GHz<br>0.5 - 2.0 GHz | dBm<br>dBm | —<br>— | +35<br>+48 | —<br>— |
| Input IP2 | For two-tone Input Power<br>Up to +5 dBm | 0.05 GHz<br>0.5 - 2.0 GHz | dBm<br>dBm | —<br>— | +45<br>+79 | —<br>— |
| Vcc | — | — | V | 4.5 | 5.0 | 5.5 |
| Vee | — | — | V | -8.0 | — | -5.0 |
| Icc | Vcc = 4.5 to 5.5V<br>Vctl = 0 to 0.8V, or Vcc – 2.1V to Vcc | — | mA | — | — | 6.0 |
| Iee | Vee = -5.0 to -8.0V | — | mA | — | — | 1.0 |
| Vctl<br>Vctl | Logic 0 (TTL)<br>Logic 1 (TTL) | —<br>— | V<br>V | 0.0<br>2.0 | —<br>— | 0.8<br>5.0 |
| Input Leakage Current (Low) | 0 to 0.8V | — | µA | — | — | 1.0 |
| Input Leakage Current (High) | 2.0 to 5.0V | — | µA | — | — | 1.0 |

1. All specifications apply when operated with bias voltages of +5V for Vcc and –5.0V for Vee.
2. This attenuator is guaranteed monotonic.

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### Absolute Maximum Ratings [3,4]

| Parameter | Absolute Maximum |
|---|---|
| Max Input Power<br>0.05 GHz<br>0.5 - 2.0 GHz | <br>+27 dBm<br>+34 dBm |
| $V_{CC}$ | -0.5V ≤ $V_{CC}$ ≤ +7.0V |
| $V_{EE}$ | -8.5V ≤ $V_{EE}$ ≤ +0.5V |
| $V_{CC}$ - $V_{EE}$ | -0.5V ≤ $V_{CC}$ - $V_{EE}$ ≤ 14.5V |
| Vin[5] | -0.5V ≤ Vin ≤ $V_{CC}$ + 0.5V |
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. M/A-COM does not recommend sustained operation near these survivability limits.
5. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

### Handling Procedures

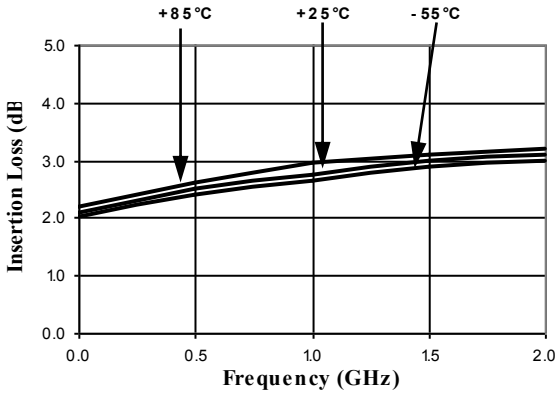
Please observe the following precautions to avoid damage:

### Static Sensitivity

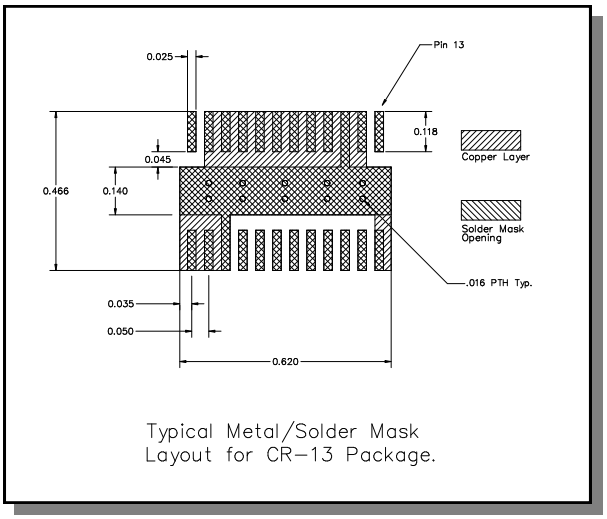
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

### Typical Performance Curves

***Insertion Loss vs. Frequency***




### Recommended PCB Configuration



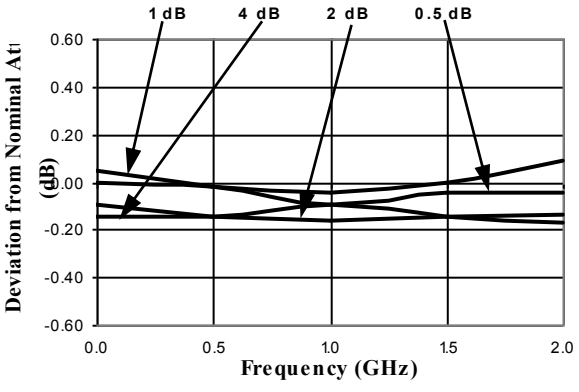

Typical Metal/Solder Mask Layout for CR-13 Package.

### Truth Table (Digital Attenuator)

| Control Inputs | | | | | | |
|---|---|---|---|---|---|---|
| C6 | C5 | C4 | C3 | C2 | C1 | Attenuation |
| 0 | 0 | 0 | 0 | 0 | 0 | Reference |
| 0 | 0 | 0 | 0 | 0 | 1 | 0.5 dB |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 dB |
| 0 | 0 | 0 | 1 | 0 | 0 | 2 dB |
| 0 | 0 | 1 | 0 | 0 | 0 | 4 dB |
| 0 | 1 | 0 | 0 | 0 | 0 | 8 dB |
| 1 | 0 | 0 | 0 | 0 | 0 | 16 dB |
| 1 | 1 | 1 | 1 | 1 | 1 | 31.5 dB |

0 = TTL Low; 1 = TTL High

***Attenuation Accuracy vs. Frequency***



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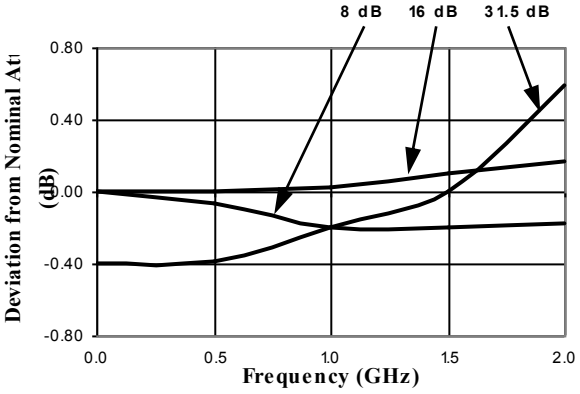
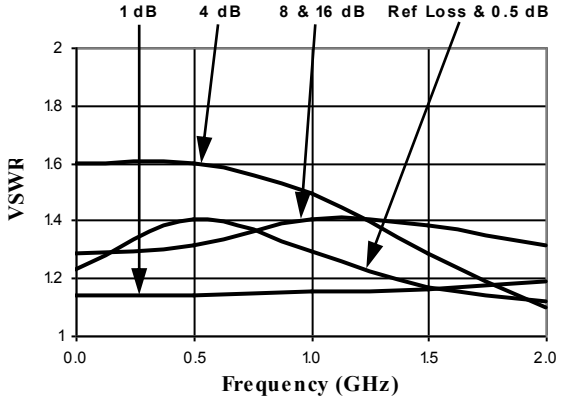
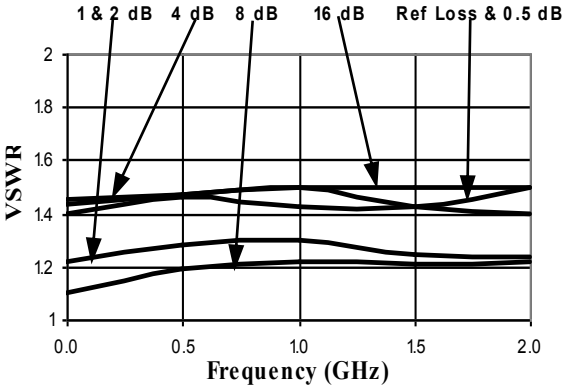


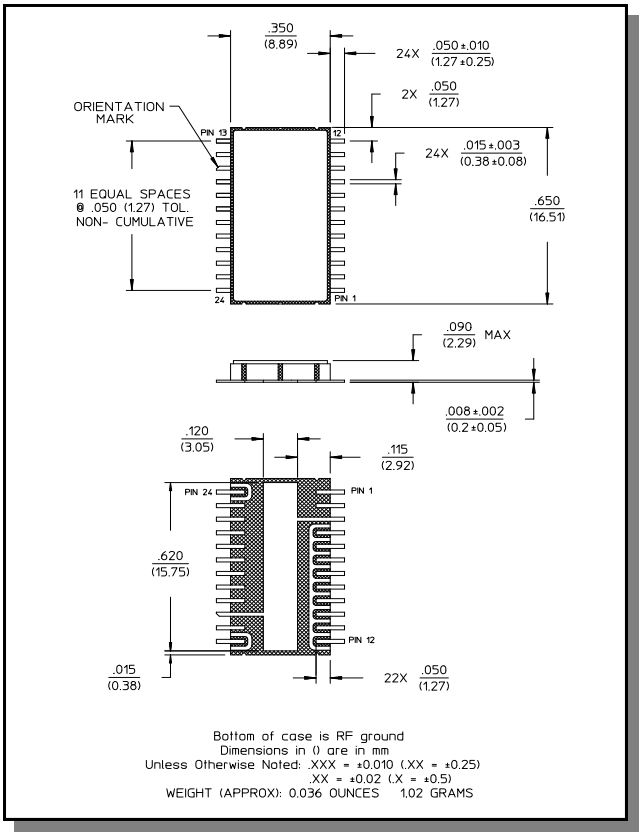

***RF1 VSWR vs. Frequency***




***RF2 VSWR vs. Frequency***




## *Lead-Free,* CR-13 Ceramic Package†




† Reference Application Note M538 for lead-free solder reflow recommendations.