









































## AC Characteristics <sup>(1)</sup>

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t <sub>PD2</sub>	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		20	ns
t <sub>SU</sub>	Global Clock Setup Time	6		7		11		16		20		ns
t <sub>H</sub>	Global Clock Hold Time	0		0		0		0		0		ns
t <sub>FSU</sub>	Global Clock Setup Time of Fast Input	3		3		3		3		3		ns
t <sub>FH</sub>	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		MHz
t <sub>COP</sub>	Global Clock to Output Delay		4.5		5		8		10		13	ns
t <sub>CH</sub>	Global Clock High Time	3		4		5		6		7		ns
t <sub>CL</sub>	Global Clock Low Time	3		4		5		6		7		ns
t <sub>ASU</sub>	Array Clock Setup Time	3		3		4		4		5		ns
t <sub>AH</sub>	Array Clock Hold Time	2		3		4		5		6		ns
t <sub>ACOP</sub>	Array Clock Output Delay		7.5		10		15		20		25	ns
t <sub>ACH</sub>	Array Clock High Time	3		4		6		8		10		ns
t <sub>ACL</sub>	Array Clock Low Time	3		4		6		8		10		ns
t <sub>CNT</sub>	Minimum Clock Global Period		8		10		13		17		22	ns
f <sub>CNT</sub>	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t <sub>ACNT</sub>	Minimum Array Clock Period		8		10		13		17		22	ns
f <sub>ACNT</sub>	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz
f <sub>MAX</sub>	Maximum Clock Frequency	166.7		125		100		41.7		33.3		MHz
t <sub>IN</sub>	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t <sub>IO</sub>	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t <sub>FIN</sub>	Fast Input Delay		1		1		2		2		2	ns
t <sub>SEXP</sub>	Foldback Term Delay		4		5		8		10		12	ns
t <sub>PEXP</sub>	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t <sub>LAD</sub>	Logic Array Delay		3		5		6		7		8	ns
t <sub>LAC</sub>	Logic Control Delay		3		5		6		7		8	ns
t <sub>IOE</sub>	Internal Output Enable Delay		2		2		3		3		4	ns
t <sub>OD1</sub>	Output Buffer and Pad Delay (Slow slew rate = OFF; V <sub>CCIO</sub> = 5V; C <sub>L</sub> = 35 pF)		2		1.5		4		5		6	ns

## AC Characteristics (Continued)<sup>(1)</sup>

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>OD2</sub>	Output Buffer and Pad Delay (Slow slew rate = OFF; V <sub>CCIO</sub> = 3.3V; C <sub>L</sub> = 35 pF)		2.5		2.0		5		6		7	ns
t <sub>OD3</sub>	Output Buffer and Pad Delay (Slow slew rate = ON; V <sub>CCIO</sub> = 5V or 3.3V; C <sub>L</sub> = 35 pF)		5		5.5		8		10		12	ns
t <sub>ZX1</sub>	Output Buffer Enable Delay (Slow slew rate = OFF; V <sub>CCIO</sub> = 5.0V; C <sub>L</sub> = 35 pF)		4.0		5.0		7		9		10	ns
t <sub>ZX2</sub>	Output Buffer Enable Delay (Slow slew rate = OFF; V <sub>CCIO</sub> = 3.3V; C <sub>L</sub> = 35 pF)		4.5		5.5		7		9		10	ns
t <sub>ZX3</sub>	Output Buffer Enable Delay (Slow slew rate = ON; V <sub>CCIO</sub> = 5.0V/3.3V; C <sub>L</sub> = 35 pF)		9		9		10		11		12	ns
t <sub>xZ</sub>	Output Buffer Disable Delay (C <sub>L</sub> = 5 pF)		4		5		6		7		8	ns
t <sub>SU</sub>	Register Setup Time	3		2		4		5		6		ns
t <sub>H</sub>	Register Hold Time	2		3		4		5		6		ns
t <sub>FSU</sub>	Register Setup Time of Fast Input	3		3		2		2		3		ns
t <sub>FH</sub>	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
t <sub>RD</sub>	Register Delay		1		2		1		2		2	ns
t <sub>COMB</sub>	Combinatorial Delay		1		2		1		2		2	ns
t <sub>IC</sub>	Array Clock Delay		3		5		6		7		8	ns
t <sub>EN</sub>	Register Enable Time		3		5		6		7		8	ns
t <sub>GLOB</sub>	Global Control Delay		1		1		1		1		1	ns
t <sub>PRE</sub>	Register Preset Time		2		3		4		5		6	ns
t <sub>CLR</sub>	Register Clear Time		2		3		4		5		6	ns
t <sub>UIM</sub>	Switch Matrix Delay		1		1		2		2		2	ns
t <sub>RPA</sub>	Reduced-power Adder <sup>(2)</sup>		10		11		13		14		15	ns

- Notes: 1. See ordering information for valid part numbers.  
 2. The t<sub>RPA</sub> parameter must be added to the t<sub>LAD</sub>, t<sub>LAC</sub>, t<sub>TIC</sub>, t<sub>ACL</sub>, and t<sub>SEXP</sub> parameters for macrocells running in the reduced-power mode.























