

AC Characteristics ⁽¹⁾

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t _{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		20	ns
t _{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t _H	Global Clock Hold Time	0		0		0		0		0		ns
t _{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		3		ns
t _{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		MHz
t _{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t _{CH}	Global Clock High Time	3		4		5		6		7		ns
t _{CL}	Global Clock Low Time	3		4		5		6		7		ns
t _{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t _{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t _{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t _{ACH}	Array Clock High Time	3		4		6		8		10		ns
t _{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t _{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f _{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t _{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f _{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz
f _{MAX}	Maximum Clock Frequency	166.7		125		100		41.7		33.3		MHz
t _{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t _{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t _{FIN}	Fast Input Delay		1		1		2		2		2	ns
t _{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t _{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t _{LAD}	Logic Array Delay		3		5		6		7		8	ns
t _{LAC}	Logic Control Delay		3		5		6		7		8	ns
t _{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t _{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V _{CCIO} = 5V; C _L = 35 pF)		2		1.5		4		5		6	ns

AC Characteristics (Continued)⁽¹⁾

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; V _{CCIO} = 3.3V; C _L = 35 pF)		2.5		2.0		5		6		7	ns
t _{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V _{CCIO} = 5V or 3.3V; C _L = 35 pF)		5		5.5		8		10		12	ns
t _{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V _{CCIO} = 5.0V; C _L = 35 pF)		4.0		5.0		7		9		10	ns
t _{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V _{CCIO} = 3.3V; C _L = 35 pF)		4.5		5.5		7		9		10	ns
t _{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V _{CCIO} = 5.0V/3.3V; C _L = 35 pF)		9		9		10		11		12	ns
t _{xZ}	Output Buffer Disable Delay (C _L = 5 pF)		4		5		6		7		8	ns
t _{SU}	Register Setup Time	3		2		4		5		6		ns
t _H	Register Hold Time	2		3		4		5		6		ns
t _{FSU}	Register Setup Time of Fast Input	3		3		2		2		3		ns
t _{FH}	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
t _{RD}	Register Delay		1		2		1		2		2	ns
t _{COMB}	Combinatorial Delay		1		2		1		2		2	ns
t _{IC}	Array Clock Delay		3		5		6		7		8	ns
t _{EN}	Register Enable Time		3		5		6		7		8	ns
t _{GLOB}	Global Control Delay		1		1		1		1		1	ns
t _{PRE}	Register Preset Time		2		3		4		5		6	ns
t _{CLR}	Register Clear Time		2		3		4		5		6	ns
t _{UIM}	Switch Matrix Delay		1		1		2		2		2	ns
t _{RPA}	Reduced-power Adder ⁽²⁾		10		11		13		14		15	ns

- Notes:
1. See ordering information for valid part numbers.
 2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.

