Features

- Industry-standard architecture
  - Emulates Many 20-pin PALs®
  - Low-cost, easy to use software tools
- High speed electrically-erasable programmable logic devices (EE PLD)
  - 5ns maximum pin-to-pin delay
- Low power, 100µA pin controlled power-down mode option
- CMOS and TTL compatible inputs and outputs
  - I/O pin keeper circuits
- Advanced flash technology
  - Reprogrammable
  - 100% tested
- High reliability CMOS process
  - 20 year data retention
  - 100 erase/write cycles
  - 2,000V ESD protection
  - 200mA latchup immunity
- Commercial and industrial temperature ranges
- Dual-in-line and surface mount packages in standard pinouts
- PCI compliant
- Green (ROHS compliant) package options available

Description

The Atmel® ATF16V8C is a high performance EECMOS programmable logic device (PLD) that utilizes the Atmel proven electrically-erasable (EE) Flash memory technology. Offered options include speeds down to 5ns and a 100µA pin-controlled power-down mode. All speed ranges are specified over the full 5V ± 10% range for industrial temperature ranges, and 5V ± 5% for commercial range 5V devices.

The ATF16V8C incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation are configured automatically with software, and allow highly complex logic functions to be realized.

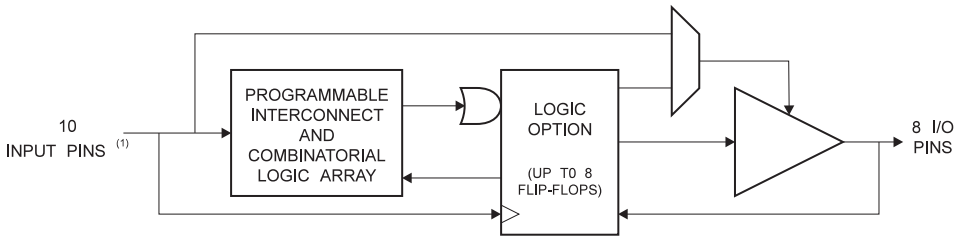
The ATF16V8C can significantly reduce total system power, thereby enhancing system reliability and reducing power supply costs. When pin 4 is configured as the power-down control pin, supply current drops to less than 100µA whenever the pin is high. If the power-down feature isn't required for a particular application, pin 4 may be used as a logic input. Also, the pin-keeper circuits eliminate the need for internal pull-up resistors along with their attendant power consumption.

High Performance Electrically-erasable Programmable Logic Devices

Atmel ATF16V8C

0425H–PLD–3/11

Figure 0-1. Block diagram

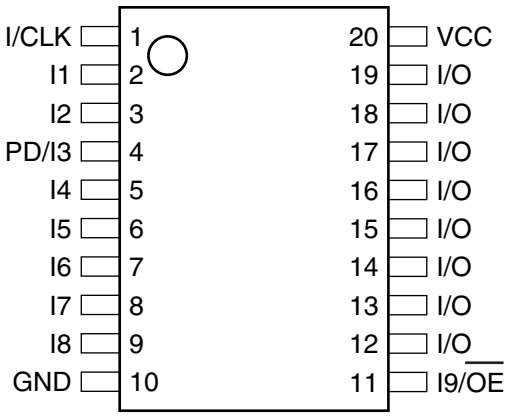


Note: 1. Includes optional PD control pin

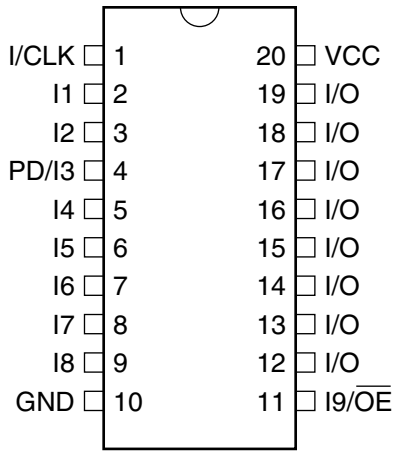
Figure 0-2. Pin configurations

Pin name	Function
CLK	Clock
I	Logic inputs
I/O	Bidirectinoal buffers
$\overline{OE}$	Output enable
V_{CC}	+5V supply
PD	Power-down

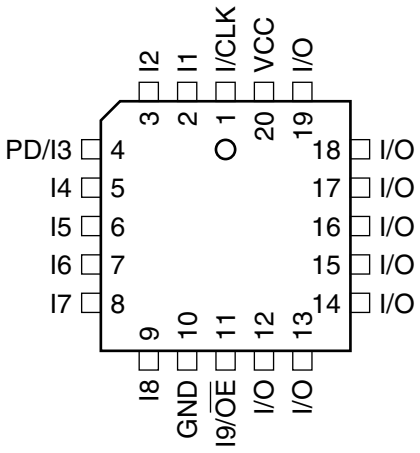
TSSOP
Top view



DIP/SOIC
Top view



PLCC
Top view



1. Absolute maximum ratings*

Temperature under bias	-40°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-2.0V to +7.0V(1)
Voltage on input pins with respect to ground during programming	-2.0V to +14.0V(1)
Programming voltage with respect to ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20ns.

2. DC and AC characteristics

Table 2-1. DC and AC operating conditions

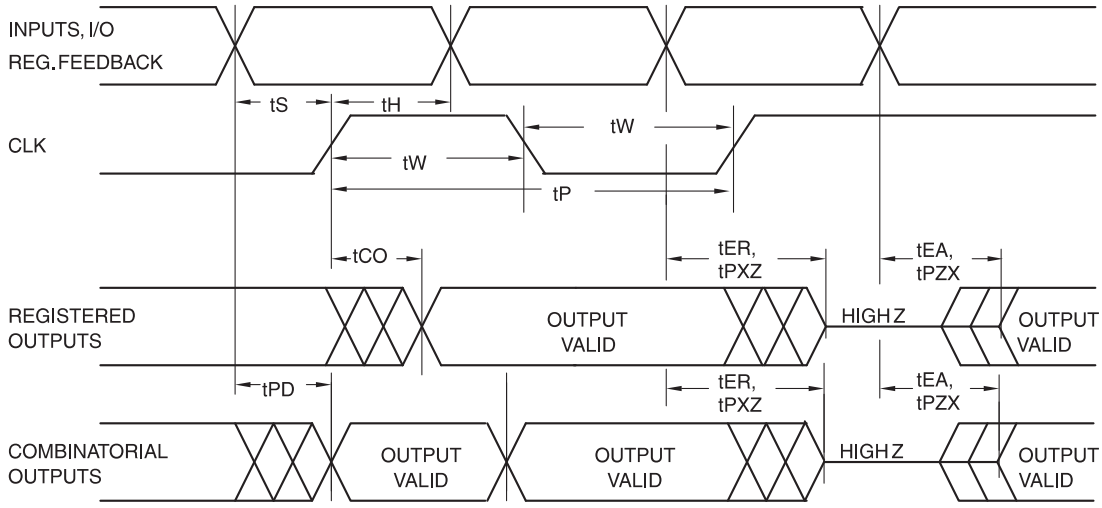
	Commercial	Industrial
Operating temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} power supply	5V ± 5%	5V ± 10%

Table 2-2. DC characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}	Input or I/O low leakage current	$0 \le V_{IN} \le V_{IL}$ (Max)				-10.0	µA
I_{IH}	Input or I/O high leakage current	$3.5 \le V_{IN} \le V_{CC}$				10.0	µA
I_{CC1}(1)	Power supply current, standby	15MHz, V_{CC} = Max, V_{IN} = 0, V_{CC}, outputs open	Com.			115	mA
			Ind.			130	mA
I_{PD}	Power supply current, Power-down mode	V_{CC} = Max, V_{IN} = 0, V_{CC}	Com.		10	100	µA
			Ind.		10	105	µA
I_{OS}	Output short circuit current	V_{OUT} = 0.5V; V_{CC} = 5V; T_A = 25°C				-150	mA
V_{IL}	Input low voltage	Min < V_{CC} < Max		-0.5		0.8	V
V_{IH}	Input high voltage			2.0		V_{CC} + 1	V
V_{OL}	Output low voltage	V_{CC} = Min; All outputs I_{OL} = 24mA	Com., Ind.			0.5	V
V_{OH}	Output high voltage	V_{CC} = Min I_{OL} = -4.0mA		2.4			V
I_{OL}	Output low current	V_{CC} = Min	Com.	24.0			mA
			Ind.	12.0			mA
I_{OH}	Output high current	V_{CC} = Min	Com., Ind.	-4.0			mA

Note: 1. All I_{CC} parameters measured with outputs open

Figure 3. AC waveforms



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

Table 3-1. AC characteristics

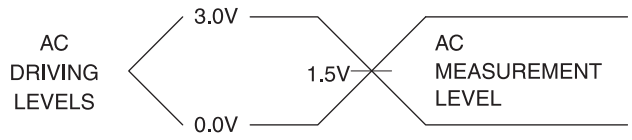
Symbol	Parameter	-5		-7		-10		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or feedback to non-registered output	1	5	3	7.5	3	10	ns
t_{CF}	Clock to feedback		3		3		6	ns
t_{CO}	Clock to output	1	4	2	5	2	7	ns
t_S	Input or feedback setup time	3		5		7.5		ns
t_H	Input hold time	0		0		0		ns
t_P	Clock period	6		8		12		ns
t_W	Clock width	3		4		6		ns
f_{MAX}	External feedback $1/(t_S + t_{CO})$		142		100		68	MHz
	Internal feedback $1/(t_S + t_{CF})$		166		125		74	MHz
	No feedback $1/(t_P)$		166		125		83	MHz
t_{EA}	Input to output enable – product term	2	6	3	9	3	10	ns
t_{ER}	Input to output disable – product term	2	5	2	9	2	10	ns
t_{PZX}	$\overline{OE}$ pin to output enable	2	5	2	6	2	10	ns
t_{PXZ}	$\overline{OE}$ pin to output disable	1.5	5	1.5	6	1.5	10	ns

Table 3-2. Power-down AC characteristics[1][2][3]

Symbol	Parameter	-5		-7		-10		Units
		Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid Input before PD High	5.0		7.5		10		ns
t_{GVDH}	Valid $\overline{OE}$ before PD High	0		0		0		ns
t_{CVDH}	Valid Clock before PD High	0		0		0		ns
t_{DHIX}	Input Don't Care after PD High		5.0		7.5		10	ns
t_{DHGX}	$\overline{OE}$ Don't Care after PD High		5.0		7.5		10	ns
t_{DHCX}	Clock Don't Care after PD High		5.0		7.5		10	ns
t_{DLIV}	PD Low to Valid Input		5.0		7.5		10	ns
t_{DLGV}	PD Low to Valid $\overline{OE}$		15.0		20.0		25	ns
t_{DLCV}	PD Low to Valid Clock		15.0		20.0		25	ns
t_{DLOV}	PD Low to Valid Output		20.0		25.0		30	ns

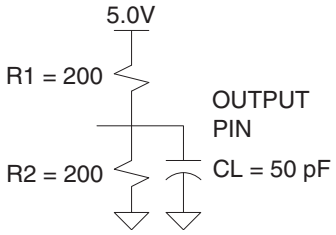
Note: 1. Output data is latched and held
2. HI-Z outputs remain HI-Z
3. Clock and input transitions are ignored

4. Input test waveforms and measurement levels:



t_R, t_F < 1.5ns (10% to 90%)

5. Output test loads



6. Pin capacitance

Table 6-1. Pin capacitance

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

7. Power-up reset

Registers of the ATF16V8C are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic, from below 0.7V
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3. The signals from which the clock is derived must remain stable during t_{PR}

Figure 8. Power-up reset

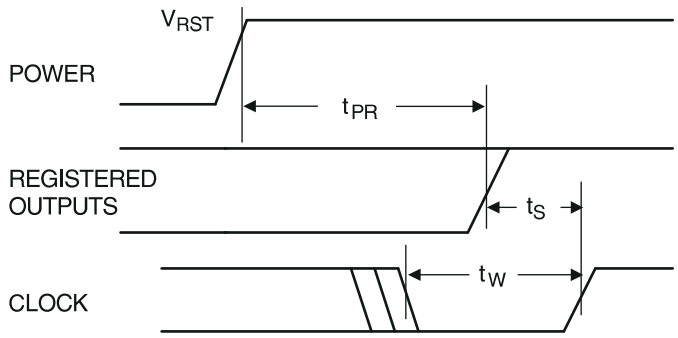


Table 8-1. Power-up reset parameters

Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

9. Power-down mode

The ATF16V8C includes an optional pin controlled powerdown feature. Device pin 4 may be configured as the power-down pin. When this feature is enabled and the power-down pin is high, total current consumption drops to less than 100µA. In the power-down mode, all output data and internal logic states are latched and held. All registered and combinatorial output data remains valid. Any outputs that were in a high-Z state at the onset of power-down will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. The input and I/O pin-keeper circuits remain active to insure that pins do not float to indeterminate levels. This helps to further reduce system power.

Selection of the power-down option is specified in the ATF16V8C logic design file. The logic compiler will include this option selection in the otherwise standard 16V8 JEDEC fuse file. When the power-down feature is not specified in the design file, pin 4 is available as a logic input, and there is no power-down pin. This allows the ATF16V8C to be programmed using any existing standard 16V8 fuse file.

Note: Some programmers list the JEDEC-compatible 16V8C (No PD used) separately from the non-JEDEC compatible 16V8CEXT. (EXT for extended features.)

10. Registered output preload

Registers of the ATF16V8C are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by approved programmers.

11. Security fuse usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8C fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit user signature remains accessible.

The security fuse will be programmed last, as its effect is immediate.

12. Input and I/O pin-keeper circuits

The ATF16V8C contains internal input and I/O pin-keeper circuits. These circuits allow each ATF16V8C pin to hold its previous value even when it is not being driven by an external source or by the device's output buffer. This helps insure that all logic array inputs are at known, valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin-keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin-keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40µA.

Figure 13. Input diagram

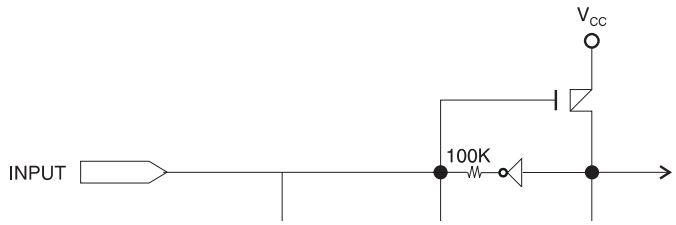
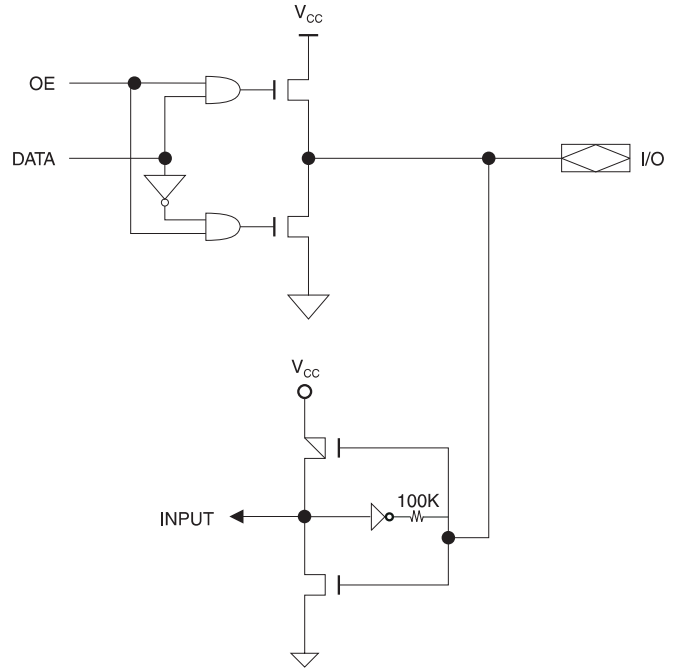


Figure 14. I/O diagram



15. Functional logic diagram description

The logic option and functional diagrams describe the ATF16V8C architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8C can be configured in one of three different modes. Each mode makes the ATF16V8C look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8C universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8C can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the content of the ATF16V8C. Eight bytes (64 fuses) of user signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The user signature is accessible regardless of the state of the security fuse.

Table 15-1. Compiler mode selection

	Registered	Complex	Simple	Auto select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
With PD ENABLE	P16V8PDR[1]	P16V8PDC[1]	P16V8PD[1]	P16V8PDS[1]
CUPL, Atmel-CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8A
With PD ENABLE	G16V8CPMS	G16V8CPMA	G16V8CPAS	G16V8CP
LOG/iC	GAL16V8_R[2]	GAL16V8_C7[2]	GAL16V8_C8[2]	GAL16V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Synario/Atmel-Synario	NA	NA	NA	ATF16V8C ALL
With PD ENABLE	NA	NA	NA	ATF16V8C (PD) ALL[1]
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

Note: 1. Please call Atmel PLD Hotline at (408) 436-4333 for more information
2. Only applicable for version 3.4 or lower

16. Macrocell configuration

Software compilers support the three different OMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable ($\overline{OE}$) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with $\overline{OE}$ controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without $\overline{OE}$ control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode,** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode,** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode,** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

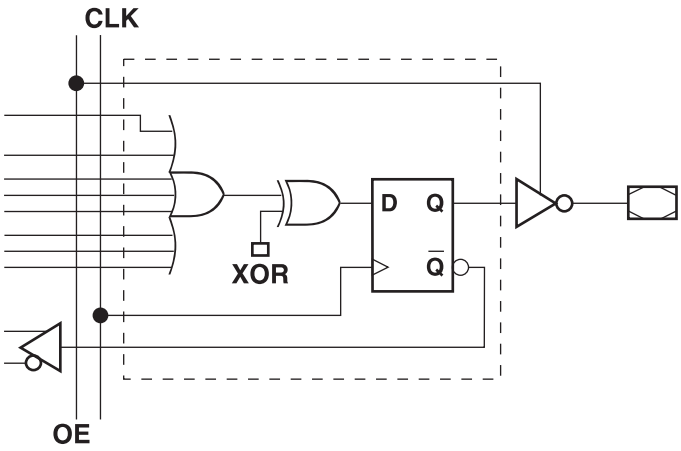
16.1 Atmel ATF16V8C registered mode

PAL device emulation/PAL replacement. The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the $\overline{OE}$ pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

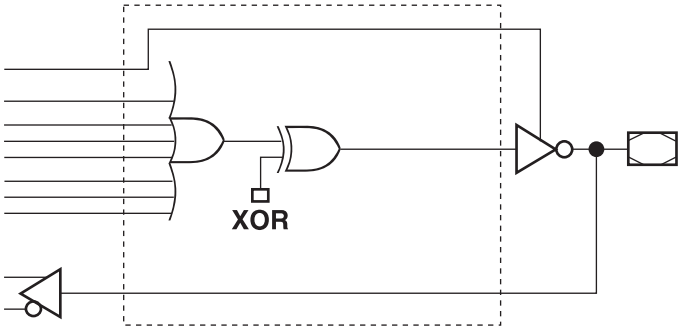
16R8	16RP8
16R6	16RP6
16R4	16RP4

Figure 17. Registered configuration for registered mode[1][2]



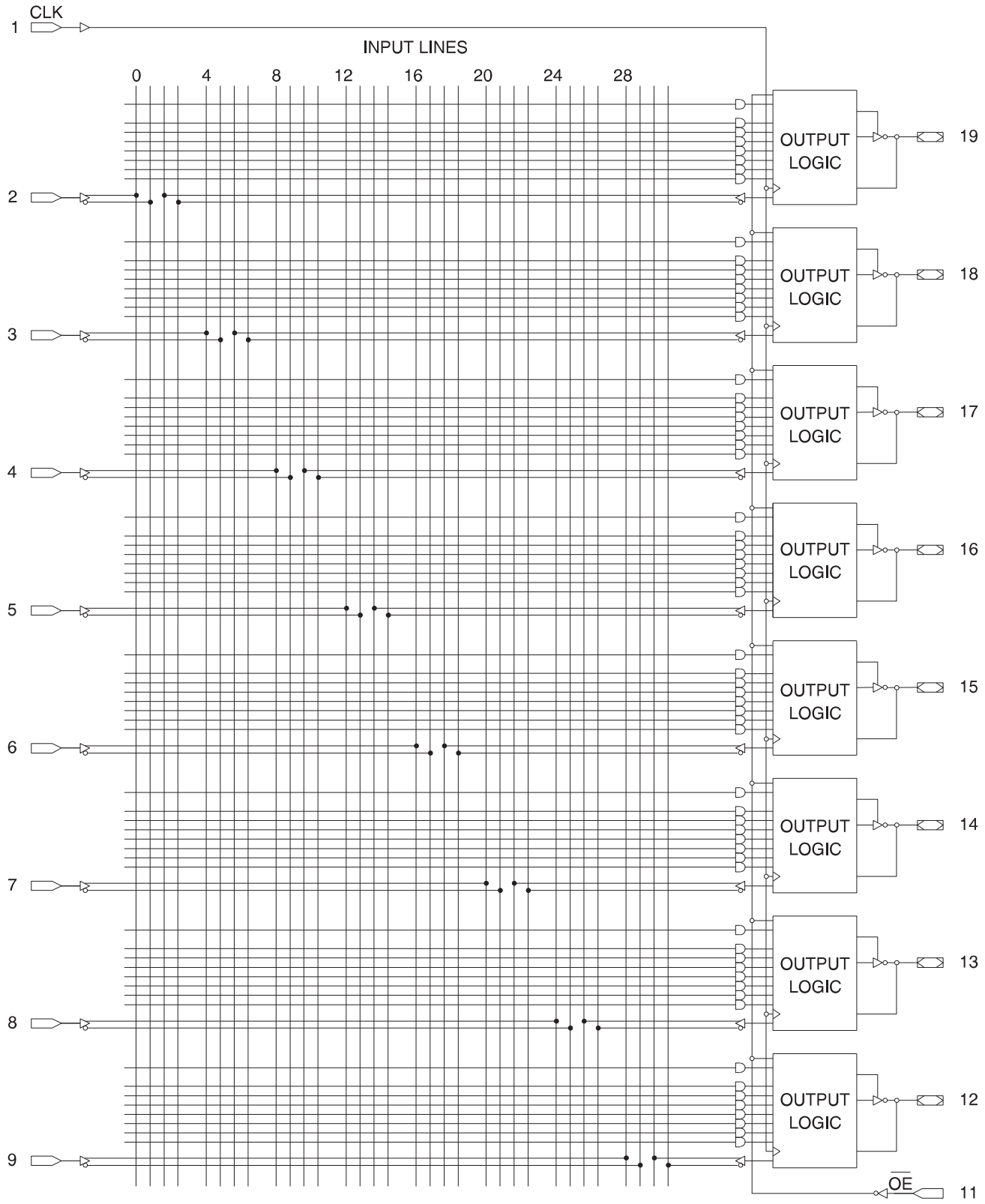
Notes:
1. Pin 1 controls common CLK for the registered outputs.
   Pin 11 controls common $\overline{OE}$ for the registered outputs.
   Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 18. Combinatorial configuration for registered mode[1][2]



Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 19. Registered mode logic diagram



Note: * Input not available if power-down mode is enabled

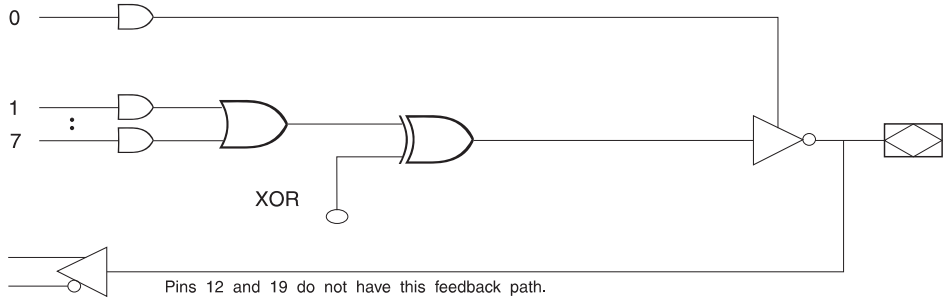
20. Atmel ATF16V8C complex mode

PAL device emulation/PAL replacement. In the complex mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

Combinatorial applications with an $\overline{OE}$ requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8
16H8
16P8

Figure 21. Complex Mode Option



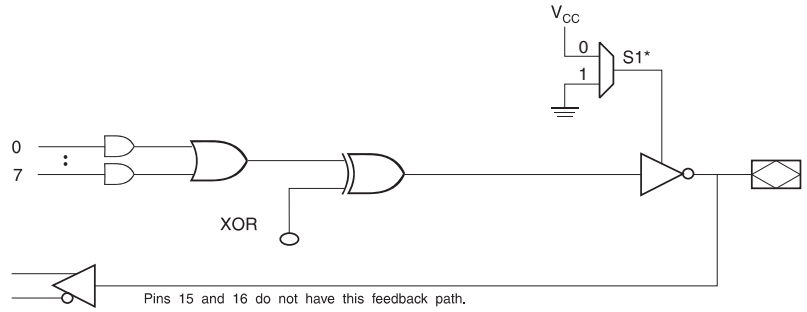
22. Atmel ATF16V8C simple mode

PAL device emulation/PAL replacement. In the simple mode, eight product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without $\overline{OE}$ control. The following simple PALs can be emulated using this mode:

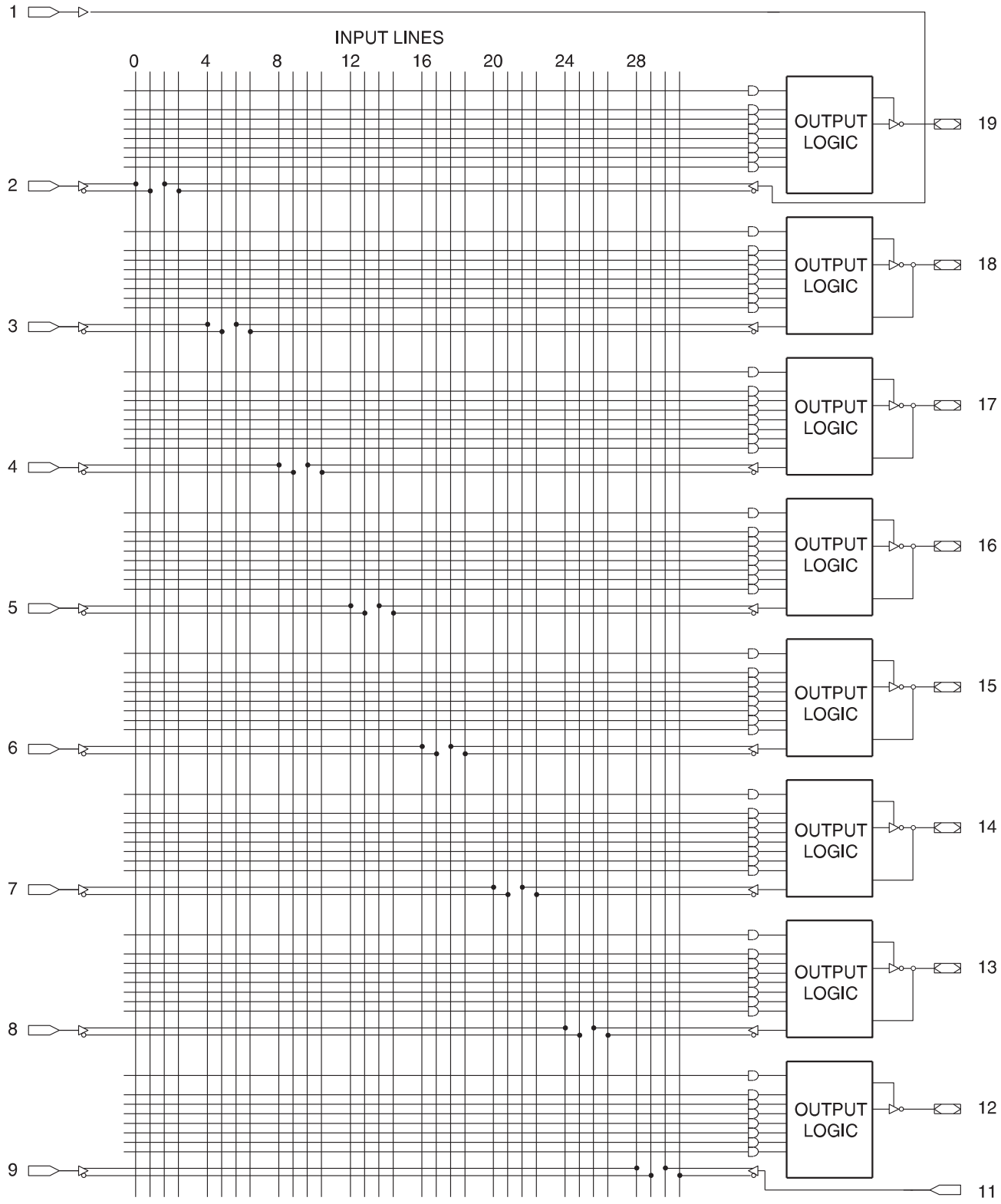
10L8 10H8 10P8
12L6 12H6 12P6
14L4 14H4 14P4
16L2 16H2 16P2

Figure 23. Simple mode option



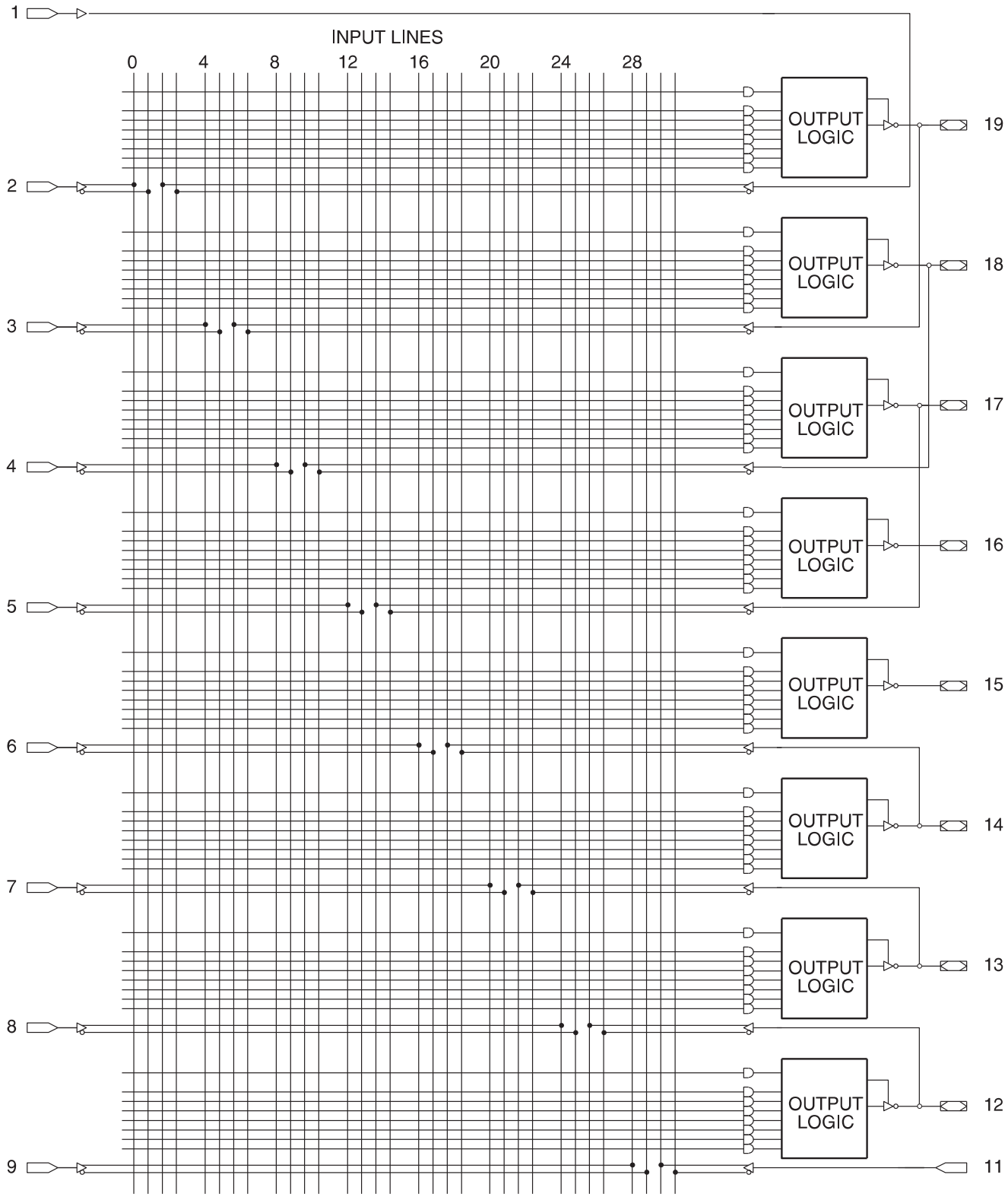
* - Pins 15 and 16 are always enabled.

Figure 24. Complex mode logic diagram



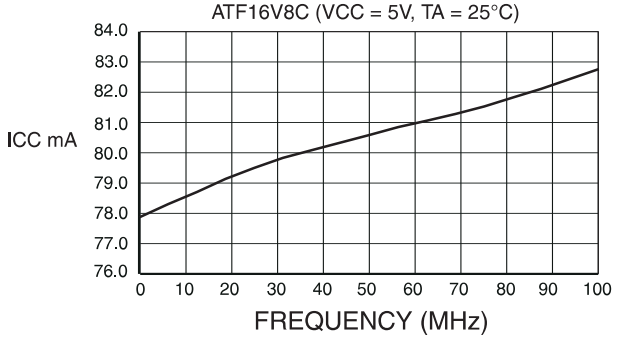
Note: * Input not available if power-down mode is enabled

Note: Simple mode logic diagram

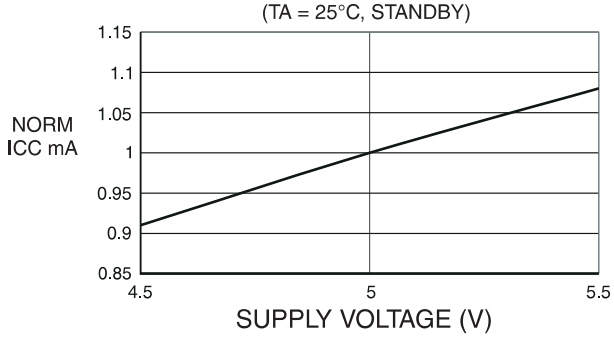


Note: * Input not available if power-down mode is enabled

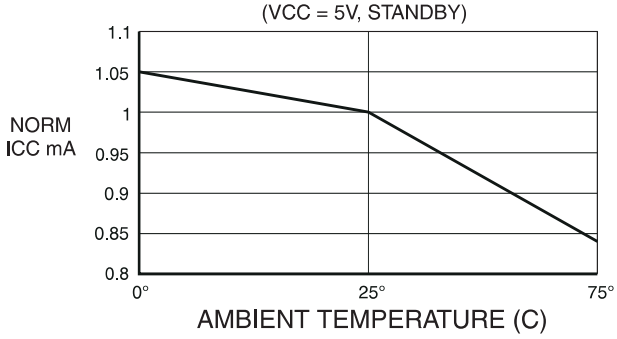
SUPPLY CURRENT
VS. INPUT FREQUENCY
ATF16V8C (VCC = 5V, TA = 25°C)



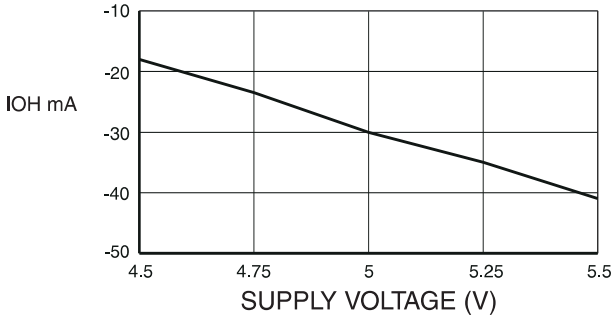
NORMALIZED SUPPLY CURRENT
VS. SUPPLY VOLTAGE
(TA = 25°C, STANDBY)



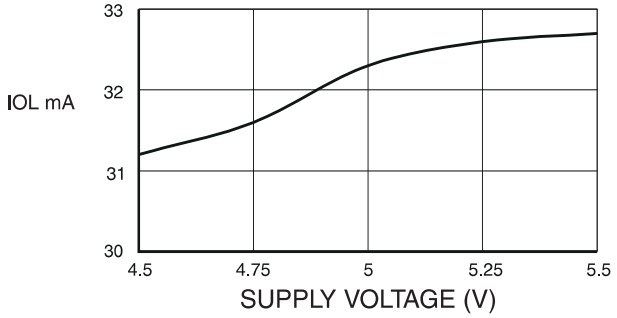
NORMALIZED SUPPLY CURRENT
VS. AMBIENT TEMPERATURE
(VCC = 5V, STANDBY)



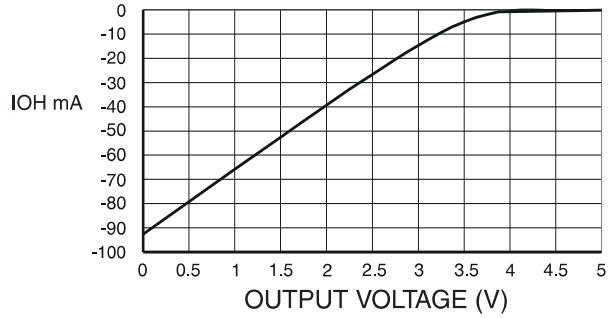
OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE (VOH = 2.4V, TA = 25°C)



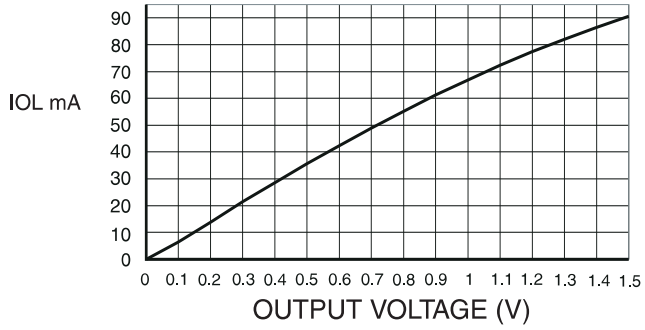
OUTPUT SINK CURRENT
VS. SUPPLY VOLTAGE (TA = 25°C, VOL = 0.45V)



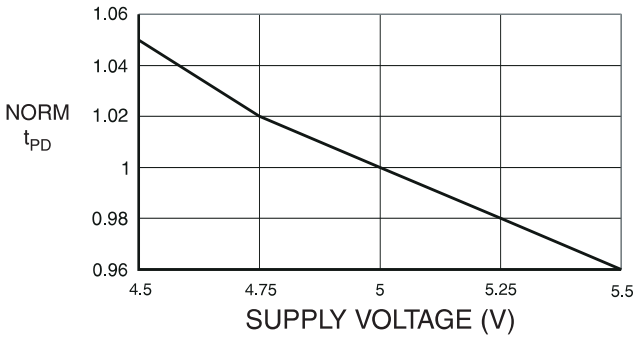
OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)



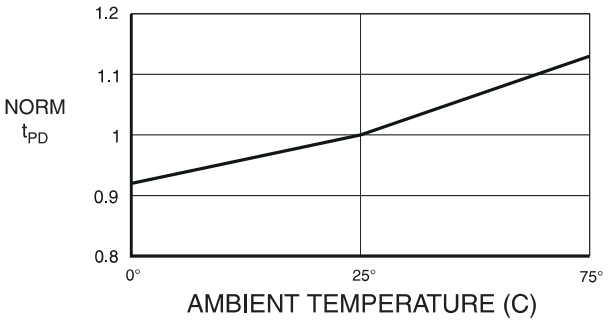
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)



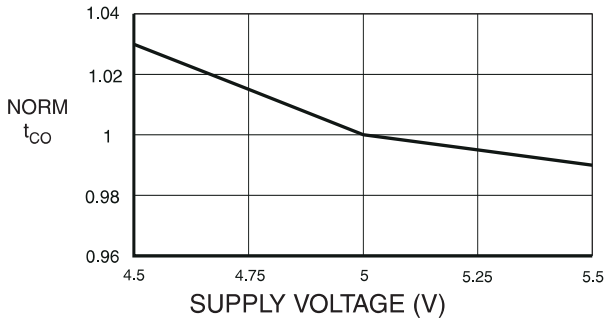
NORMALIZED t_{PD}
VS. SUPPLY VOLTAGE (TA = 25°C)



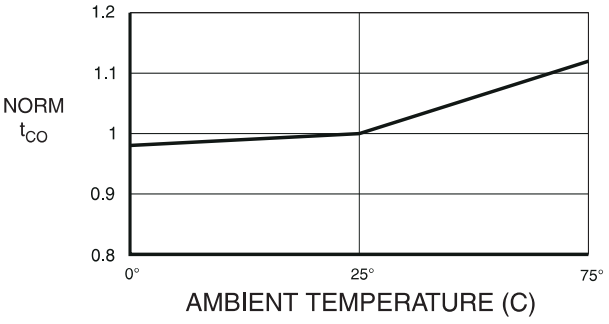
NORMALIZED t_{PD}
VS. AMBIENT TEMPERATURE (VCC = 5V)



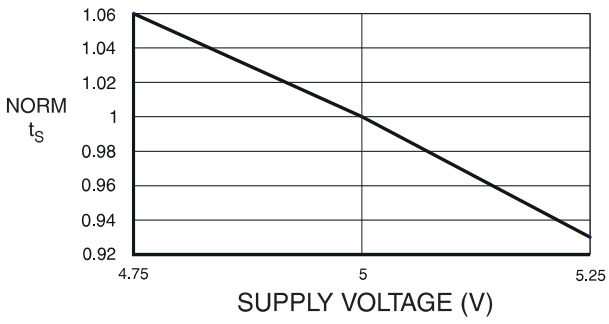
NORMALIZED t_{CO}
VS. SUPPLY VOLTAGE (TA = 25°C)



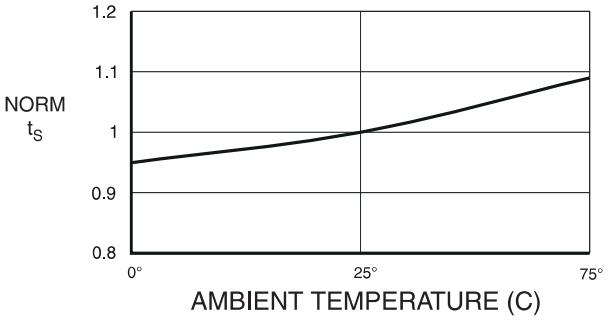
NORMALIZED t_{CO}
VS. AMBIENT TEMPERATURE (VCC = 5V)



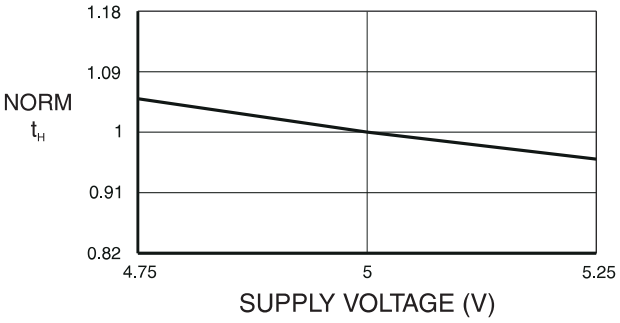
NORMALIZED t_S
VS. SUPPLY VOLTAGE (TA = 25°C)



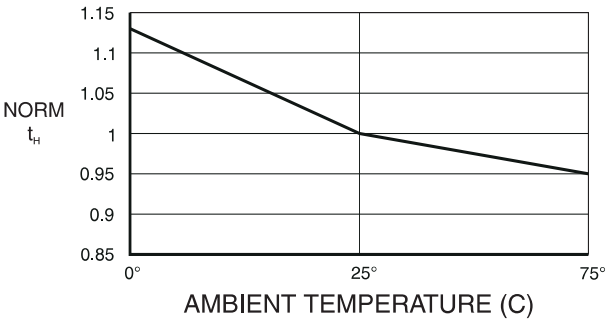
NORMALIZED t_S
VS. AMBIENT TEMPERATURE (VCC = 5V)



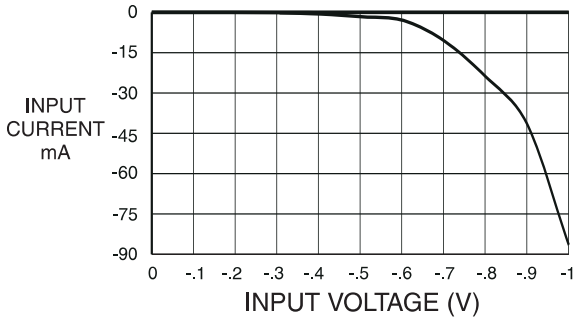
NORMALIZED t_H
VS. SUPPLY VOLTAGE (TA = 25°C)

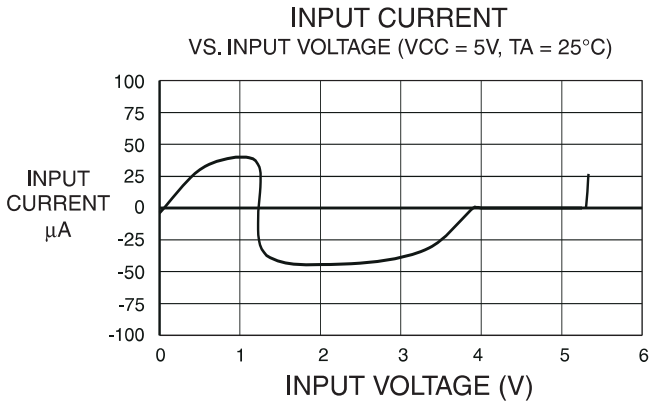


NORMALIZED t_H
VS. AMBIENT TEMPERATURE (VCC = 5V)



INPUT CLAMP CURRENT
VS. INPUT VOLTAGE (TA = 25°C, VCC = 5V)




INPUT CURRENT
VS. INPUT VOLTAGE (VCC = 5V, TA = 25°C)
INPUT CURRENT µA
100
75
50
25
0
-25
-50
-75
-100
0
1
2
3
4
5
6
INPUT VOLTAGE (V)

25. Ordering information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Atmel ordering code*	Package	Operation range
5	3	*4*	ATF16V8C-5JX	20J	Commercial (0°C to 70°C)
7.5	5	*5*	ATF16V8C-7JU ATF16V8C-7PU ATF16V8C-7SU	20J 20P3 20S	Industrial (-40°C to 85°C)
5	3	4	ATF16V8C-5JC	20J	Commercial (0°C to 70°C)
7.5	5	5	ATF16V8C-7JC ATF16V8C-7PC ATF16V8C-7SC ATF16V8C-7XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
			ATF16V8C-7JI ATF16V8C-7PI ATF16V8C-7SI ATF16V8C-7XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)
10	7.5	7	ATF16V8C-10JI	20J	Industrial (-40°C to 85°C)

Using "C" Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the "I" to the "C" device (7ns "C" = 10ns "I") and de-rate power by 30%.

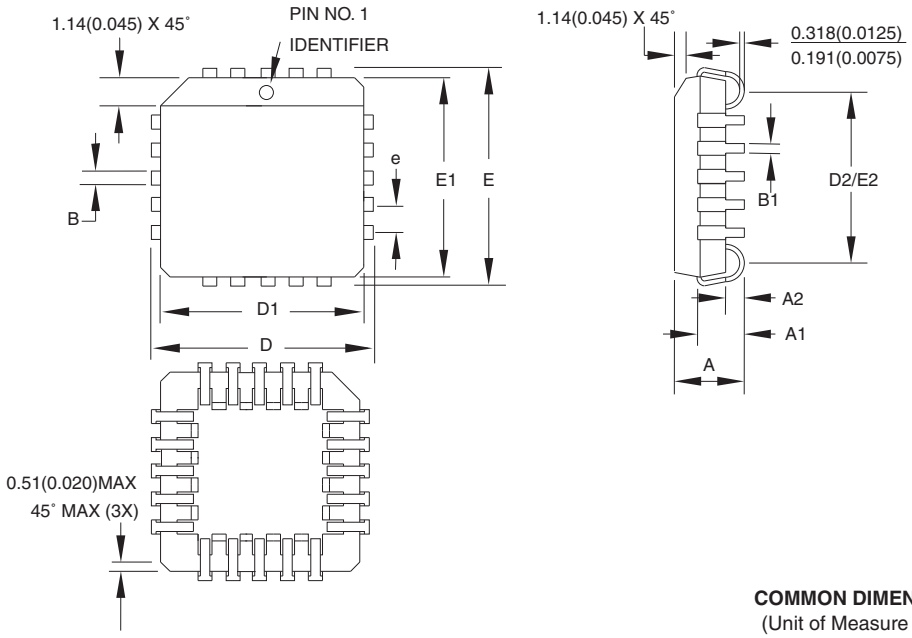
Notes: 1. *Shaded parts are being obsoleted in 2011

2. The suffix, "U" and "X" as part of the ordering code, implies the package is ROHS compliant and lead free

Package type	
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20-lead, 0.300" Wide, Plastic Gull-Wing Small Outline (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

26. Package Drawings

20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

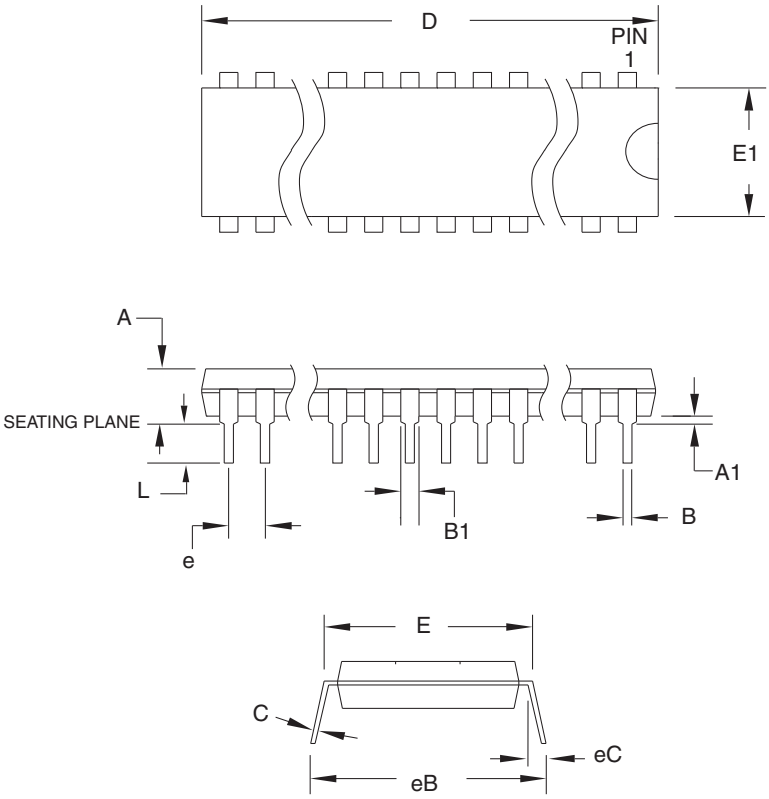
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

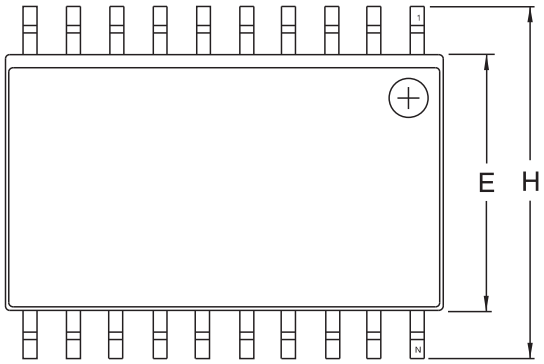
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

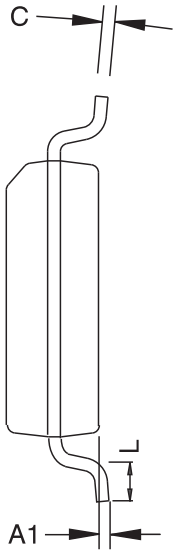
1/23/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	D

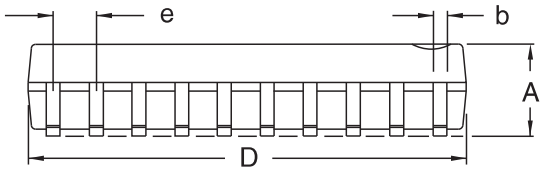
20S – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

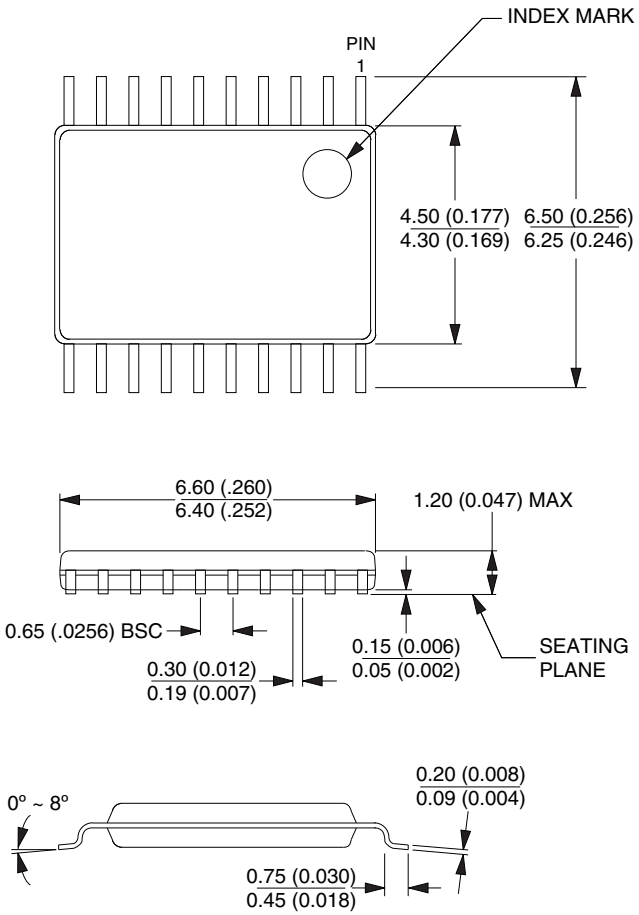
Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

11/6/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	B

20X – TSSOP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC



10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	20X	C

27. Revision history

Doc. rev.	Date	Comments
0425H	03/2011	Added green (ROHS compliant) package options Removed lead based packaged from ordering section