

5. Preload and Observability of Registered Outputs

The ATF2500Cs registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 10.25V to 10.75V signal on SMP lead 42. When the preload clock SMP lead 23 is pulsed high, the data on the I/O pins is placed into the 12 registers chosen by the Q select and even/odd select pins.

Register 2 observability mode is entered by placing an 10.25V to 10.75V signal on pin/lead 2. In this mode, the contents of the buried register bank will appear on the associated outputs when the OE control signals are active.

Figure 5-1. Preload Waveforms

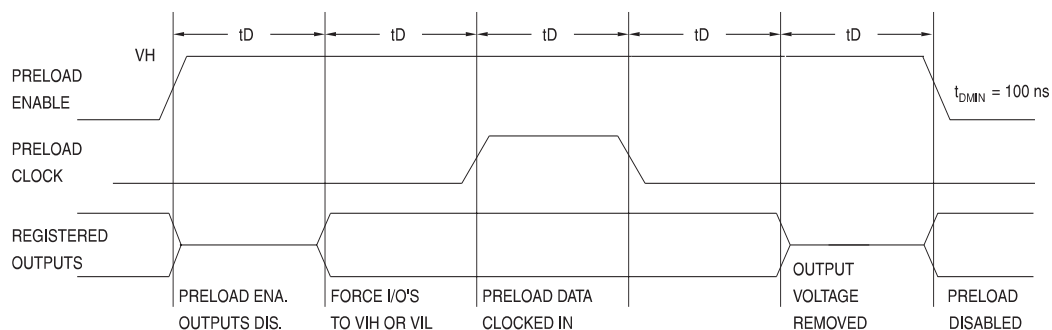


Table 5-1. Preload Levels

Level Forced on Odd I/O Pin during PRELOAD Cycle	Q Select Pin State	Even/Odd Select	Even Q1 State after Cycle	Even Q2 State after Cycle	Odd Q1 State after Cycle	Odd Q2 State after Cycle
V_{IH}/V_{IL}	Low	Low	High/Low	X	X	X
V_{IH}/V_{IL}	High	Low	X	High/Low	X	X
V_{IH}/V_{IL}	Low	High	X	X	High/Low	X
V_{IH}/V_{IL}	High	High	X	X	X	High/Low

