

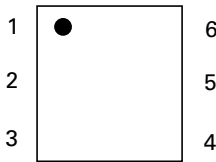
Battrax® Series - Dual Port Negative - MS-013



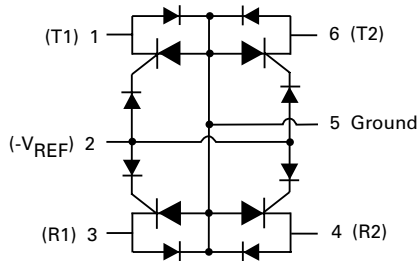
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Electrical Characteristics

Part Number	Marking	V_{DRM} @ $I_{DRM} = 5\mu A$	V_S @ 100V/ μs	I_H	I_S	I_T	V_T @ $I_T = 2.2$ Amps	V_F	Capacitance*	
		V min	V max	mA min	mA max	A max	V max	V max	pF min	pF max
B1101UC4Lxx	B1101UC4	$-I-V_{REF} + I - 1.2V$	$-I-V_{REF} + I - 10V$	100	100	2.2	4	5	30	200
B1161UC4Lxx	B1161UC4	$-I-V_{REF} + I - 1.2V$	$-I-V_{REF} + I - 10V$	160	100	2.2	4	5	30	200
B1201UC4Lxx	B1201UC4	$-I-V_{REF} + I - 1.2V$	$-I-V_{REF} + I - 10V$	200	100	2.2	4	5	30	200

Notes:
 - Absolute maximum ratings measured at $T_A = 25^\circ C$ (unless otherwise noted).
 - Components are uni-directional
 - All electrical characteristics shown are defined from Tip (pin 1 & 6) to Ground (pin 5) and Ring (pin 3 & 4) to Ground (pin 5)
 - Components are polarity sensitive and are not appropriate for positive ringing systems.

Description

The Dual Port Negative Battrax® Protection Thyristor Series are programmable SIDACtor® components designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

Dual port protection is provided by a programmable device that is referenced to a negative voltage source while internal diodes provide protection from positive surge events.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- RoHS Compliant and Lead-Free
- Dual-port protection
- Gate trigger tracking device
- Fails short circuit when surged in excess of ratings
- Integrated diode for positive voltage surges
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Additional Information



- V_{REF} Max Value for the negative Battrax is -200 V.
 - XX = Part Number Suffix: 'TP' (Tube Pack) or 'RP' (Reel Pack).
 * Off-state capacitance (C_o) is measured across pins 1 & 5, 3 & 5, 4 & 5, and 6 & 5 at 1 MHz with a 2V bias.

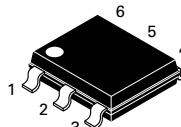
Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt A/ μ s max
	0.2/310 ¹	2/10 ¹	8/20 ¹	10/160 ¹	10/560 ¹	5/320 ¹	10/360 ¹	10/1000 ¹	5/310 ¹		
	0.5/700 ²	2/10 ²	1.2/50 ²	10/160 ²	10/560 ²	9/720 ²	10/360 ²	10/1000 ²	10/700 ²		
C	50	500	400	200	150	200	175	100	200	50	500

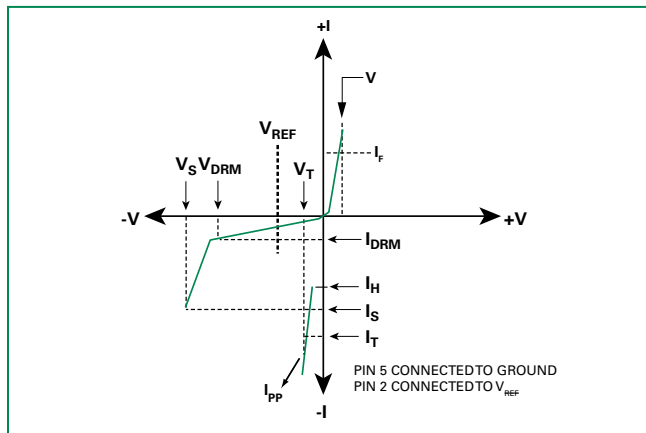
Notes:

- 1 Current waveform in μ s
- 2 Voltage waveform in μ s
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C (I_{PP} rating assumes V_{REF} equals -48 V)
- The component must initially be in thermal equilibrium with -40°C $\leq T_J \leq$ +150°C

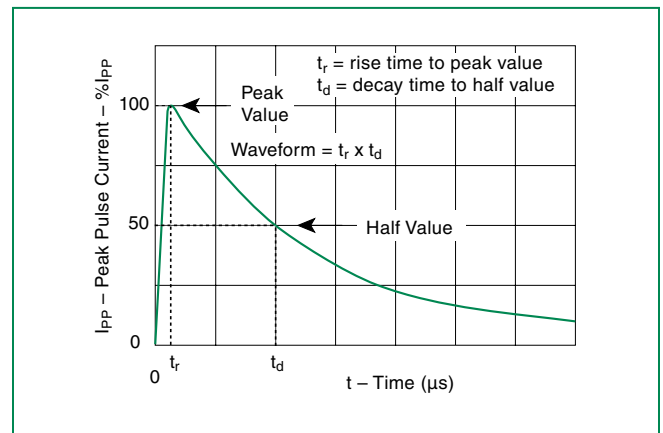
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +125	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

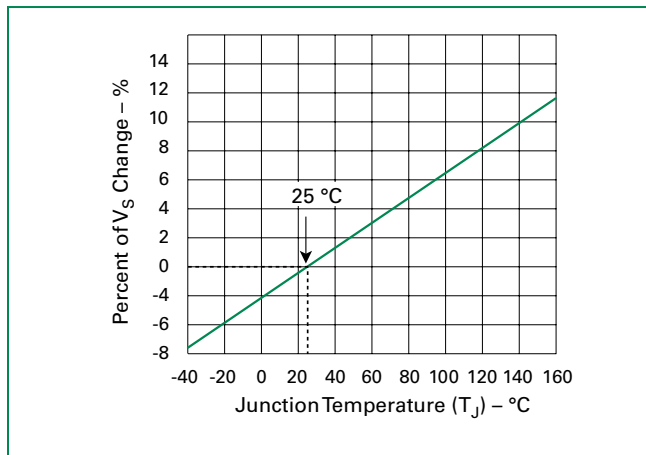
V-I Characteristics



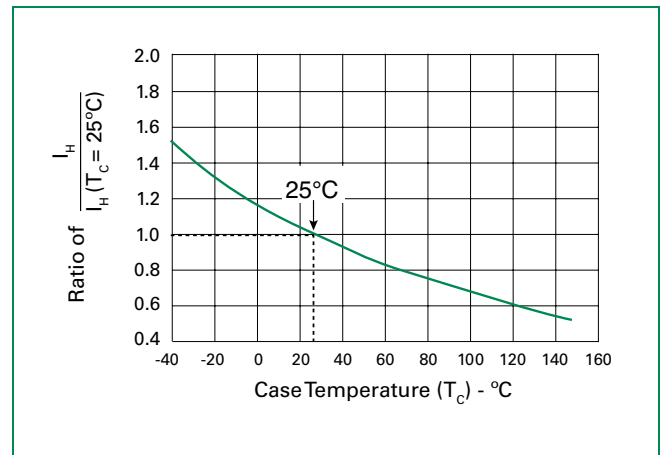
$t_r \times t_d$ Pulse Waveform



Normalized V_S Change vs. Junction Temperature

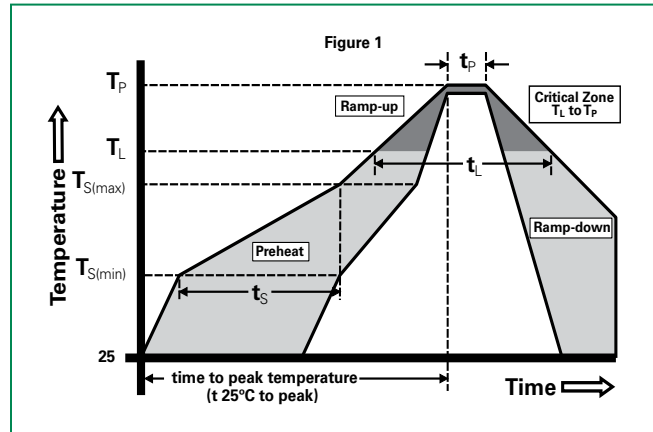


Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{s(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_p)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_p)		8 min. Max.
Do not exceed		+260°C



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{DC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



Part Marking

