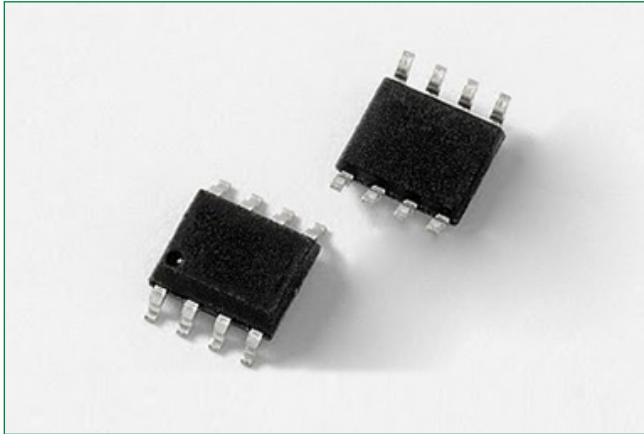


# B61089BDR, Single port negative voltage tracking SLIC protector SOP-8

## Programmable Battery tracking protection



### Description

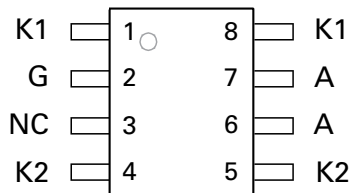
The B61089BDR is a single channel SLIC (Subscriber Line Interface circuit) battery tracking protector. It consists of a pair of identical protection thyristors integrated with two anti-series diodes to protect the SLIC against lightning induced surges and power fault events.

The gated thyristor protectors which have crowbarbing function, provide tracking battery protection down to -170V. The anti-series diode provides protection of positive surge events by diverting the surge energy to the ground.

The B61089BDR has a robust surge current capability which help the telecom and datacom products to comply with different surge standards such as Telcordia GR-1089, ITU-T K.20, K.21 and YD/T950. For compliance with Enhanced Levels test conditions of ITU-T, TIA968-B, or GR-1089, additional series resistance in the Tip / Ring pairs may be required.

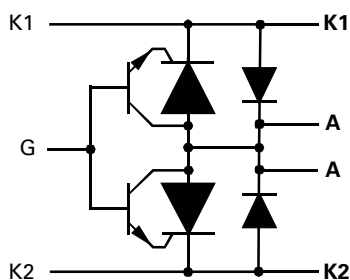
The SLIC chipset voltage reference may change as the on-hook/off-hook line condition changes. Therefore, this component is referenced to the  $-V_{BAT}$  so that its negative protection threshold follows this changing reference voltage level. This B61089BDR utilizes a transistor gain network so that a low 5 mA current level will activate the thyristor based portion of this protector component during negative events. This also allows an easier turn on during slow rising power fault events. For all positive disturbances, the fast switching diode connected to earth reference will provide the needed protection.

### Pinout Designation



Pin #	Pin Name	Description
1, 4, 5, 8	K1, K2	Connect to subscriber lines (Tip/Ring)
2	G	Connect to battery (Reference Voltage)
6, 7	A	Connect to ground (earth)

### Schematic Symbol



### Features

- Single port negative voltage tracking programmable component
- Supports battery voltages down to -170V
- Low gate triggering current 5 mA max
- Fails in a short circuit condition when it is surged in excess of its ratings to protect all downstream equipment
- Surge capability does not degrade after multiple surge events within its ratings
- High holding current -150mA min
- Specified 2/10 limiting voltage
- Integrated diodes for positive surge protection
- MSL: Level 1 - unlimited
- RoHS compliant and lead-free

### Applicable Global Standards

- Wireless In the Local Loop (WLL)
- Voice applications which require regenerated POTS
- VoIP applications
- PBX
- FXS applications
- Digital Pair Gain systems (DPG) and Digital Loop Carrier systems (DLC)
- Small Office Home Office (SOHO)

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### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Test Conditions	Value	Unit
$I_{PPSM}^*$	Non-repetitive peak on-state pulse current	10/1000 $\mu\text{s}$	35	A
		5/310 $\mu\text{s}$	65	
		2/10 $\mu\text{s}$	180	
		8/20 $\mu\text{s}$	170	
$I_{TSM}/I_{FSM}^*$	Non repetitive peak on-state current, 50Hz/60Hz	0.5s	12	A
		1s	9	
		5s	7	
		30s	4	
		900s	3	
$I_{GSM}^*$	Non repetitive peak gate current, 2/10 $\mu\text{s}$ pulse, cathodes commoned		40	A
$V_{DRM}$	Repetitive peak off-state voltage, $V_{GK}=0$		-170	V
$V_{GKRM}$	Repetitive peak gate-cathode voltage, $V_{KA}=0$		-167	V
$T_A$	Operating free-air temperature range		-40 - 85	$^\circ\text{C}$
$T_{STG}$	Storage temperature range		-40 - 150	$^\circ\text{C}$
$T_J$	Junction temperature		-40 - 150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering during 10s		260	$^\circ\text{C}$
$R_{\theta JA}$	Junction to ambient thermal resistance	$P_{tot} = 0.8 \text{ W}, T_A = 25^\circ\text{C}, 5 \text{ cm}^2, \text{FR4 PCB}$	160	$^\circ\text{C/W}$

\* Notes :

- Initially the protector must be in thermal equilibrium with  $T_J=25^\circ\text{C}$ . The surge may be repeated after the component returns to its initial conditions.

- These non-repetitive rated currents are peak values for either polarity. The rated current values may be applied to any cathode-anode terminal pair. Additionally, all cathode-anode terminal pairs may have their rated current values applied simultaneously (in this case the anode terminal current will be four times the rated current value of an individual terminal pair).

### Electrical Characteristics

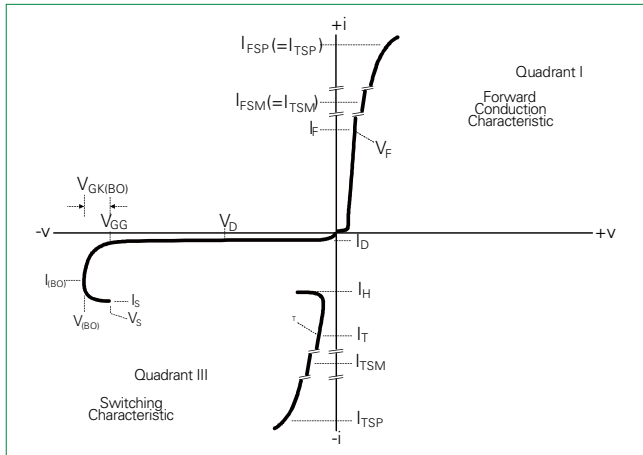
Symbol	Parameter	Test Conditions	Max	Unit
$V_F$	Forward voltage	$I_F=5\text{A}, t_w=200\mu\text{s}$	3	V
$V_{FRM}$	Impulse peak forward recovery voltage	2/10 $\mu\text{s}$ , $I_{TM}=-27\text{A}, R_s=50\Omega, di/dt=-27\text{A}/\mu\text{s}$	12	V
$I_D$	Off-state current	$V_D = V_{DRM}, V_{GK}=0, T_J=25^\circ\text{C}$	-5	$\mu\text{A}$
$V_{(BO)}$	Impulse breakover voltage	2/10 $\mu\text{s}$ , $I_{TM}=-27\text{A}, R_s=50\Omega, di/dt=-27\text{A}/\mu\text{s}, V_{GG}=-100\text{V}$	-115	V
$V_{GK(BO)}$	Gate-cathode impulse breakover voltage	2/10 $\mu\text{s}$ , $I_{TM}=-27\text{A}, R_s=50\Omega, di/dt=-27\text{A}/\mu\text{s}, V_{GG}=-100\text{V}$	20	V
$I_H$	Holding current	$I_T=-1\text{A}, di/dt=1\text{A}/\text{ms}, V_{GG}=-100\text{V}$	-150 (min)	mA
$I_{GKS}$	Gate reverse current	$V_{GG}=V_{GK}=V_{GKRM}, V_{KA}=0, T_J=25^\circ\text{C}$	-5	$\mu\text{A}$
$I_{GT}$	Gate trigger current	$I_T=-3\text{A}, t_{plg}^* \geq 20\mu\text{s}, V_{GG}=-100\text{V}, T_J=25^\circ\text{C}$	5	mA
$V_{GT}$	Gate trigger voltage	$I_T=-3\text{A}, t_{plg}^* \geq 20\mu\text{s}, V_{GG}=-100\text{V}$	2.5	V
$C_{KA}$	Cathode-anode off-state capacitance	$f=1\text{MHz}, V_d=1\text{V}, I_G=0, V_D=-3\text{V}$	100	pF
		$f=1\text{MHz}, V_d=1\text{V}, I_G=0, V_D=-48\text{V}$	50	

\* $T_{plg}$ : gate pulse time

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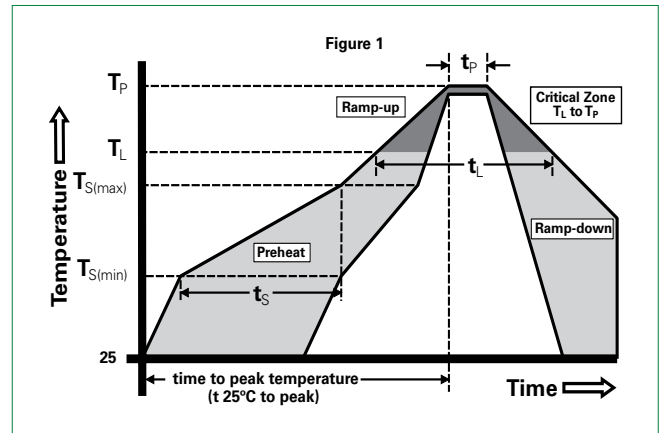
### V-I Characteristics



Parameter	Symbol
Off-state current	I <sub>D</sub>
Repetitive peak off-state voltage	V <sub>DRM</sub>
On-state Current(RMS)	I <sub>T</sub>
Non-repetitive Peak On-state Current	I <sub>TSM</sub>
Holding current	I <sub>H</sub>
Breakover voltage	V <sub>(BO)</sub>
Forward voltage	V <sub>F</sub>
Gate-cathode impulse breakover voltage	V <sub>GK(BO)</sub>
Gate trigger current	I <sub>GT</sub>
SLIC supply voltage	V <sub>GG</sub>

### Soldering Parameters

Reflow Condition	Pb-Free assembly	
Pre Heat	-Temperature Min (T <sub>s(min)</sub> )	+150°C
	-Temperature Max (T <sub>s(max)</sub> )	+200°C
	-Time (Min to Max) (t <sub>2</sub> )	60-120 secs.
Average ramp up rate (Liquidus Temp (T <sub>L</sub> ) to peak)	3°C/sec. Max.	
T <sub>S(max)</sub> to T <sub>L</sub> - Ramp-up Rate	3°C/sec. Max.	
Reflow	-Temperature (T <sub>L</sub> ) (Liquidus)	+217°C
	-Temperature (t <sub>1</sub> )	60-150 secs.
Peak Temp (T <sub>p</sub> )	+260(+0/-5)°C	
Time within 5°C of actual Peak Temp (t <sub>p</sub> )	30 secs. Max.	
Ramp-down Rate	6°C/sec. Max.	
Time 25°C to Peak Temp (T <sub>p</sub> )	8 min. Max.	
Do not exceed	+260°C	



### Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized compound meeting flammability rating V-0

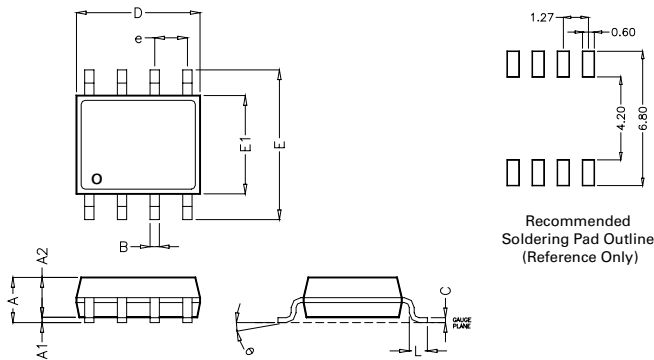
### Environmental Specifications

High Temp Voltage Blocking	*Rated 75V (A=75V, K=0V, G=0V) +150°C, 1008hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-55°C to +150°C, 15 min. dwell, 1000cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	Rated 50V (A=50V, K=0V, G=0V) (+85°C) 85% RH, 1008 hrs. EIA/JEDEC, JESD22-A-101
Resistance to Solder Heat	+260°C, 10 secs. JESD22-A111
Moisture Sensitivity Level	*85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1"

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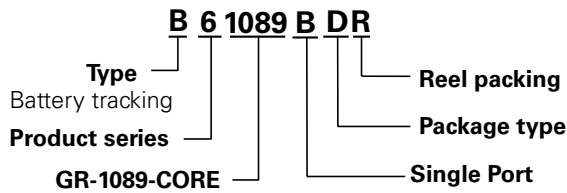
### Dimensions – MS-012 (SOP-8)



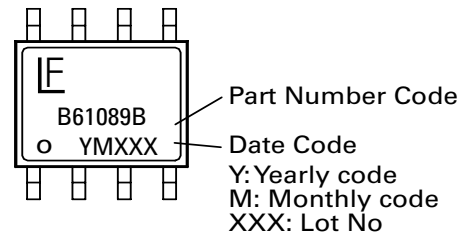
Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.043	0.065	1.25	1.65
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.17	0.25
D	0.189	0.197	4.80	5.00
E	0.228	0.244	5.80	6.20
E1	0.150	0.157	3.80	4.00
e	0.050 BSC*		1.27 BSC*	
L	0.016	0.050	0.40	1.27

\* BSC = Basic Spacing between Centers

### Part Numbering



### Part Marking



### Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
D	MS-012 SMT 8-pin SOP-8 Tape and Reel Pack	2500	N/A	EIA-481-D

### Tape and Reel Specifications – MS-012 (SOP-8)

