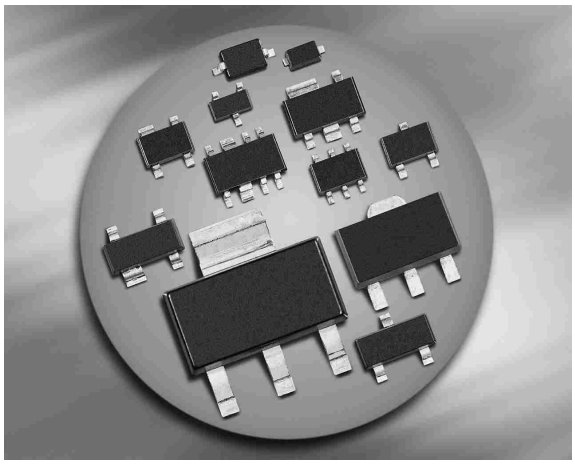
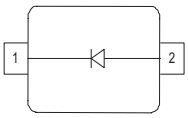
Silicon PIN Diode

- Series diode for mobile communication in low loss transmit-receiver switches
- Band switch for TV-tuners
- Very low forward resistance (typ. 0.65 Ω @ 5 mA)
- Low capacitance (typ. 0.5 pF @ 0V)
- Fast switching applications
- Pb-free (RoHS compliant) package



RoHS

BAR65-02L
BAR65-02V
BAR65-03W



Type	Package	Configuration	L_S(nH)	Marking
BAR65-02L*	TSLP-2-1	single, leadless	0.4	NN
BAR65-02V	SC79	single	0.6	N
BAR65-03W	SOD323	single	1.8	blue M

* Preliminary Data

Maximum Ratings at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	30	V
Forward current	I_F	100	mA
Total power dissipation	P_{tot}		mW
BAR65-02L, $T_S \leq$ 128°C		250	
BAR65-02V, $T_S \leq$ 118°C		250	
BAR65-03W, $T_S \leq$ 113°C		250	
Junction temperature	T_j	150	°C
Operating temperature range	T_{op}	-55 ... 125	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point[1)]	R_{thJS}		K/W
BAR65-02L		≤ 90	
BAR65-02V		≤ 130	
BAR65-03W		≤ 145	

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Reverse current V_R = 20 V	I_R	-	-	20	nA
Forward voltage I_F = 100 mA	V_F	-	0.93	1	V

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

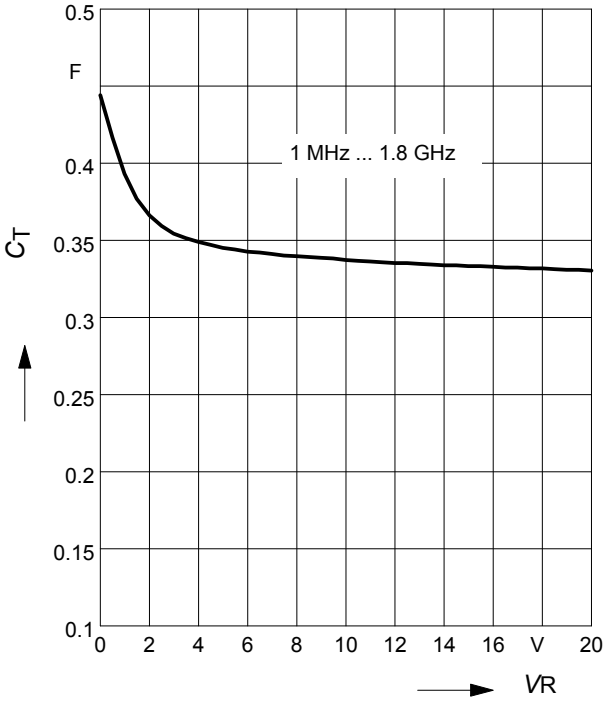
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics					
Diode capacitance	C_T				pF
V_R = 1 V, f = 1 MHz		-	0.45	0.9	
V_R = 3 V, f = 1 MHz		-	0.4	0.8	
V_R = 0 V, f = 100 MHz ... 1.8 GHz		-	0.5	-	
Reverse parallel resistance	R_P				kΩ
V_R = 0 V, f = 100 MHz		-	700	-	
V_R = 0 V, f = 1 GHz		-	10	-	
V_R = 0 V, f = 1.8 GHz		-	5	-	
Forward resistance	r_f				Ω
I_F = 1 mA, f = 100 MHz		-	1	-	
I_F = 5 mA, f = 100 MHz		-	0.65	0.95	
I_F = 10 mA, f = 100 MHz		-	0.56	0.9	
Charge carrier life time I_F = 10 mA, I_R = 6 mA, measured at I_R = 3 mA, R_L = 100 Ω	τ_{rr}	-	80	-	ns
I-region width	W_I	-	3.5	-	µm
Insertion loss[1)]	I_L				dB
I_F = 1 mA, f = 1.8 GHz		-	0.08	-	
I_F = 5 mA, f = 1.8 GHz		-	0.06	-	
I_F = 10 mA, f = 1.8 GHz		-	0.05	-	
Isolation[1)]	I_{SO}				
V_R = 0 V, f = 0.9 GHz		-	12	-	
V_R = 0 V, f = 1.8 GHz		-	7	-	
V_R = 0 V, f = 2.45 GHz		-	5	-	

[1]BAR65-02L in series configuration, Z = 50Ω

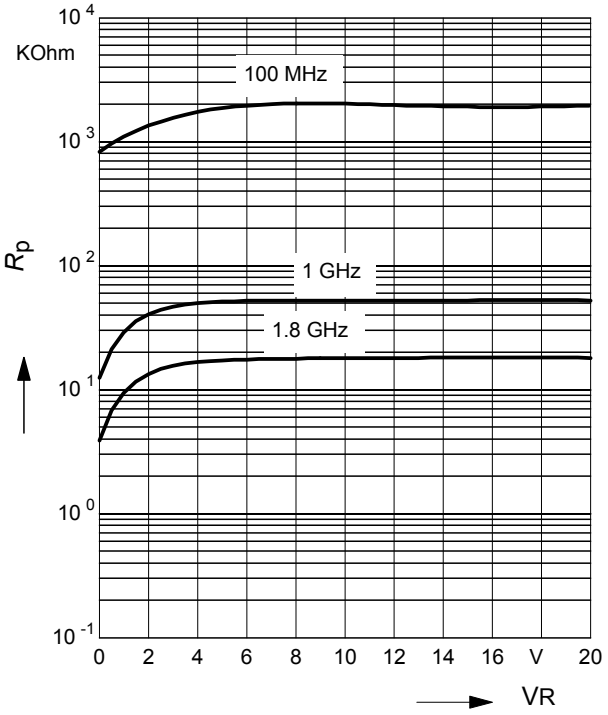
Diode capacitance $C_T = f(V_R)$

f = Parameter



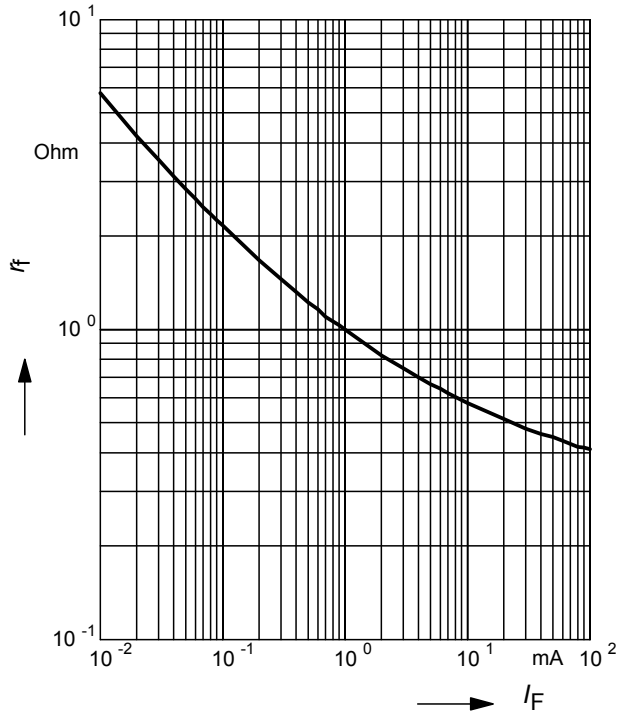
Reverse parallel resistance $R_P = f(V_R)$

f = Parameter



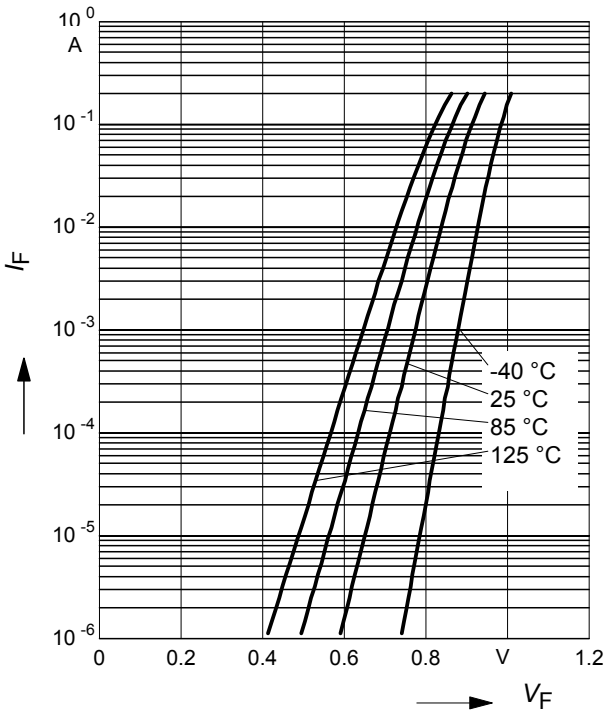
Forward resistance $r_f = f(I_F)$

f = 100MHz



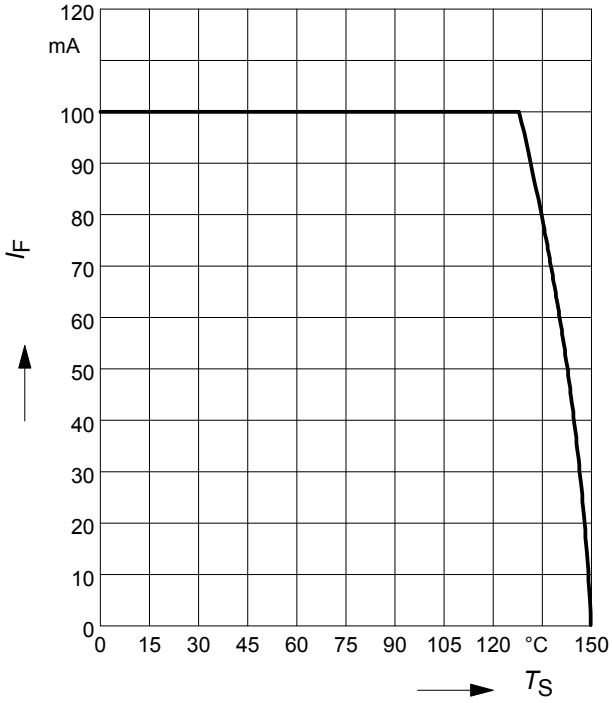
Forward current $I_F = f(V_F)$

T_A = Parameter



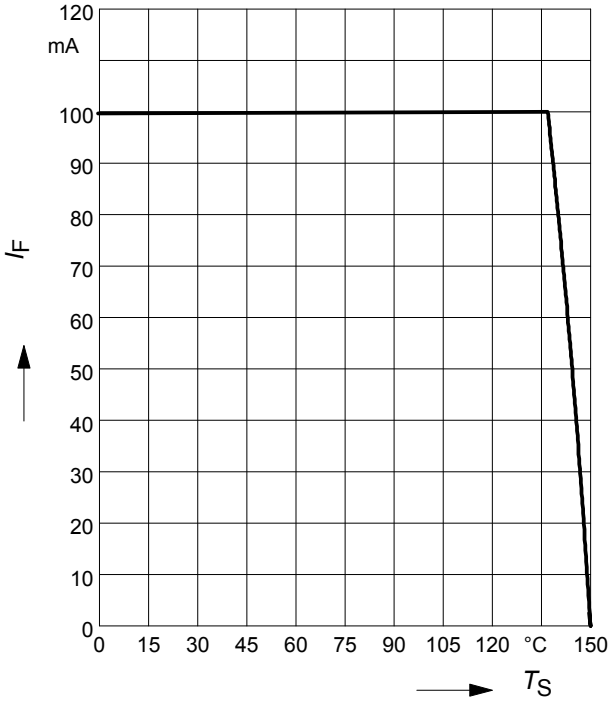
Forward current $I_F = f(T_S)$

BAR65-02L



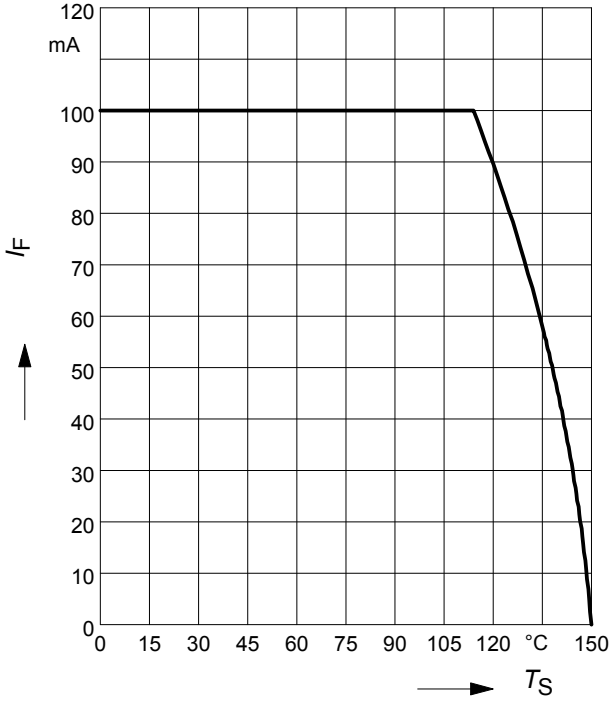
Forward current $I_F = f(T_S)$

BAR65-02V



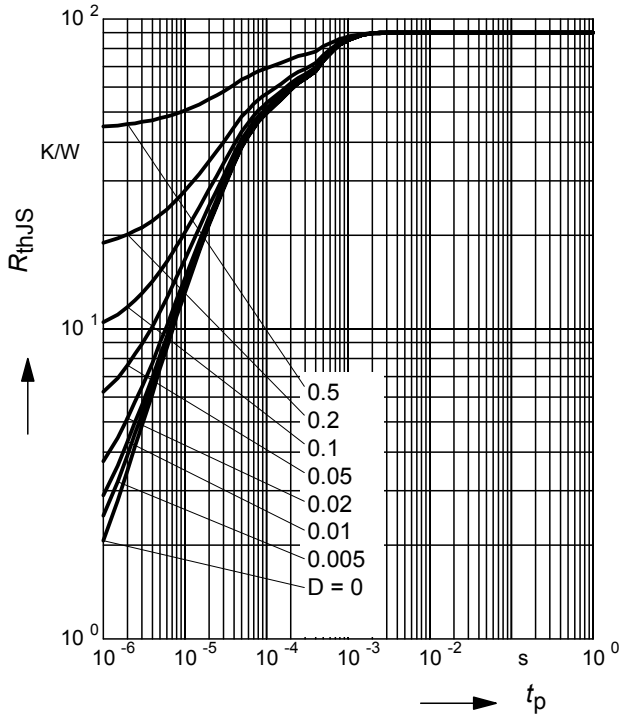
Forward current $I_F = f(T_S)$

BAR65-03W



Permissible Puls Load $R_{thJS} = f(t_p)$

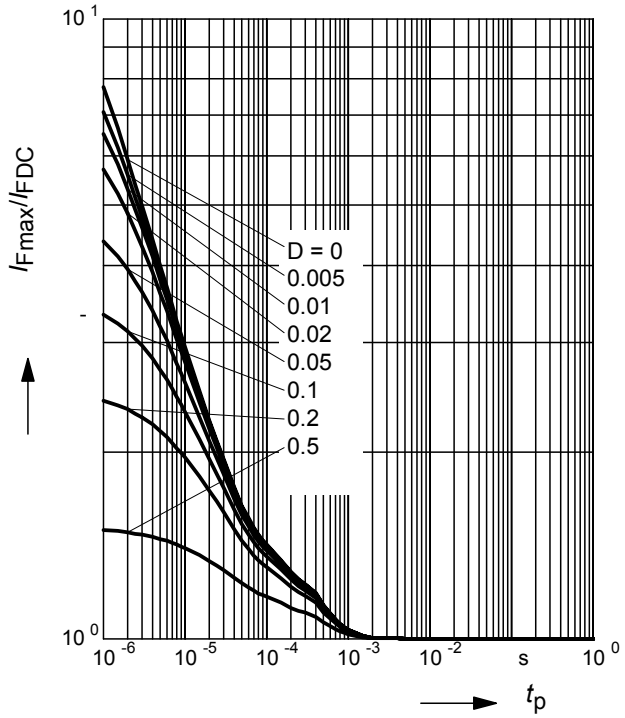
BAR65-02L



Permissible Pulse Load

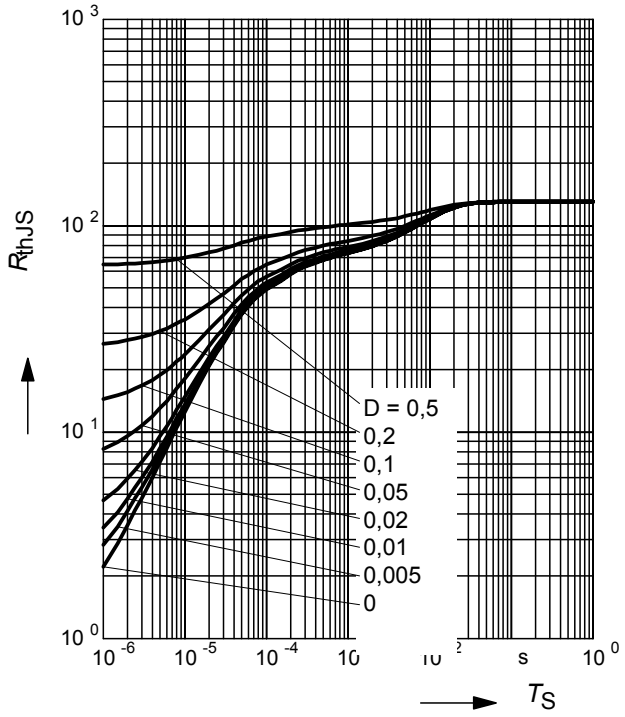
$I_{Fmax}/I_{FDC} = f(t_p)$

BAR65-02L



Permissible Puls Load $R_{thJS} = f(t_p)$

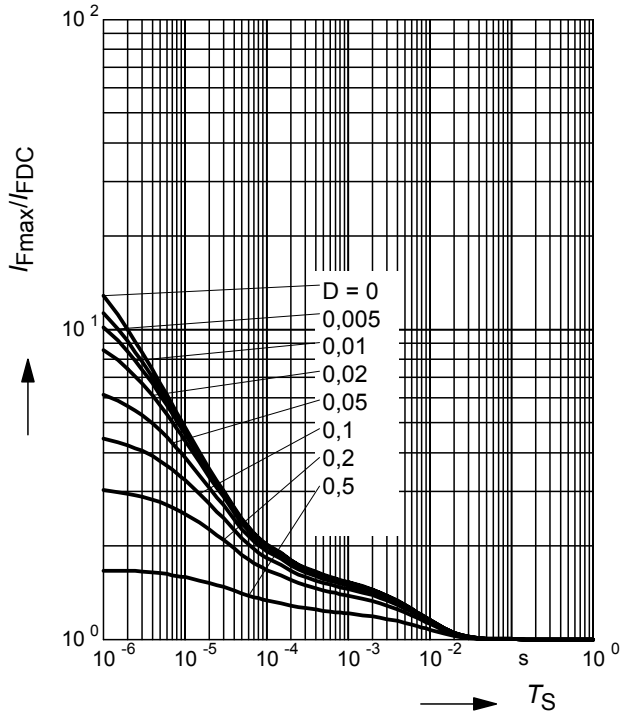
BAR65-02V



Permissible Pulse Load

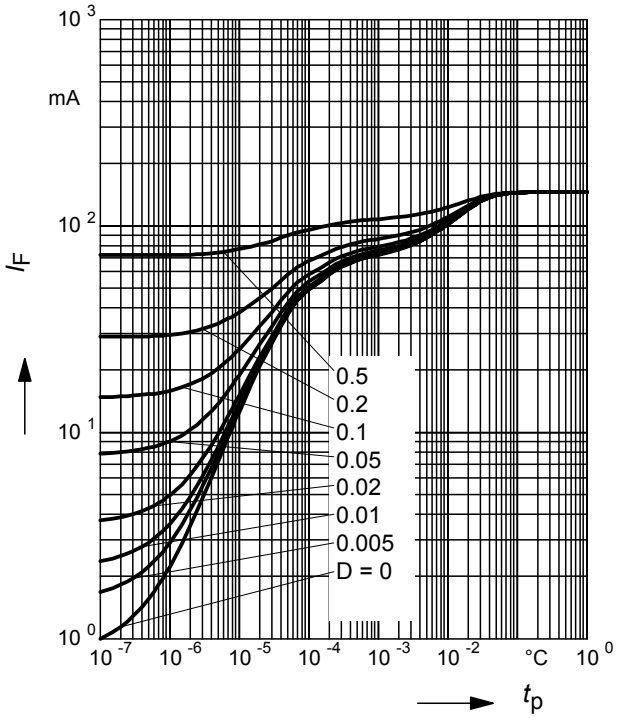
$I_{Fmax}/I_{FDC} = f(t_p)$

BAR65-02V



Permissible Puls Load $R_{thJS} = f(t_p)$

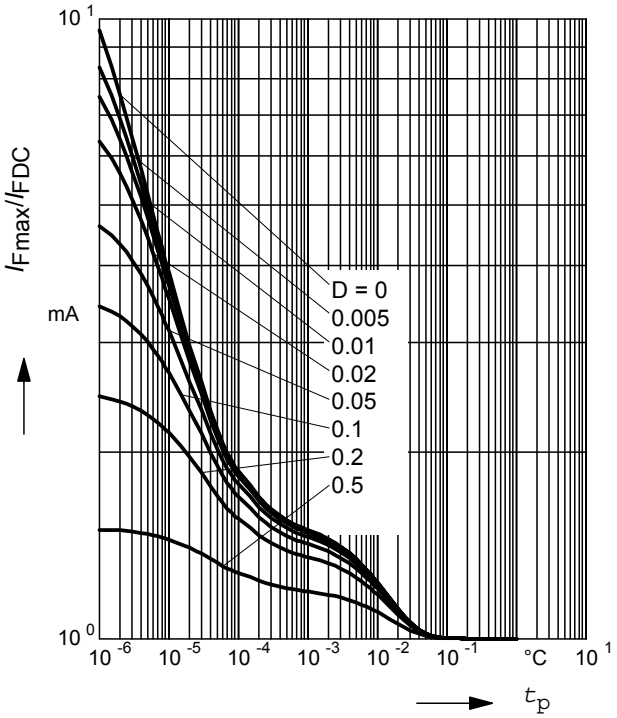
BAR65-03W



Permissible Pulse Load

$I_{Fmax}/ I_{FDC} = f(t_p)$

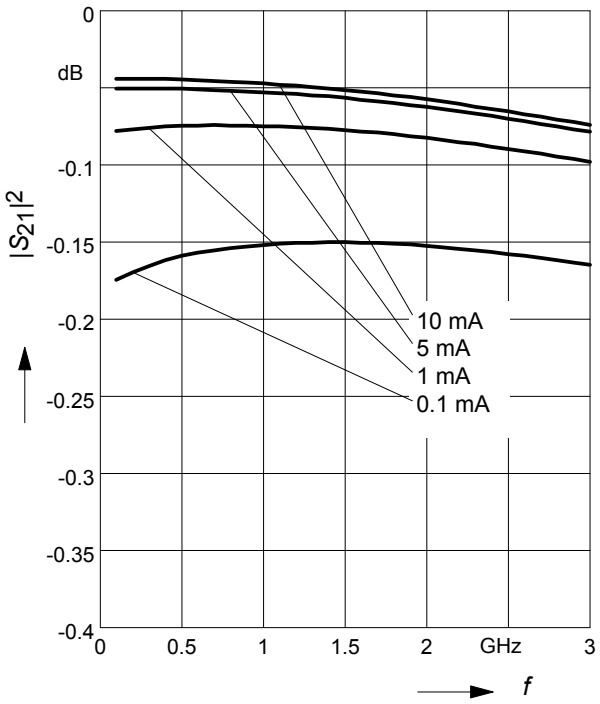
BAR65-03W



Insertion loss $I_L = -|S_{21}|^2 = f(f)$

I_F = Parameter

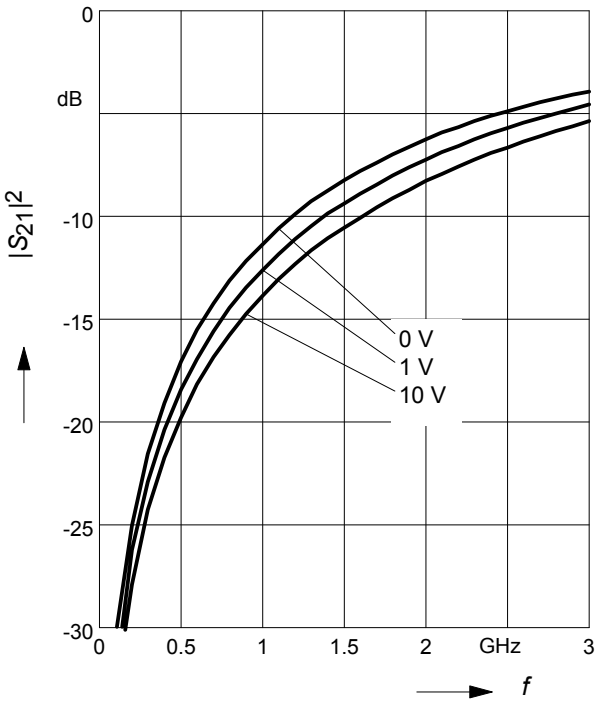
BAR65-02L in series configuration, $Z = 50\Omega$



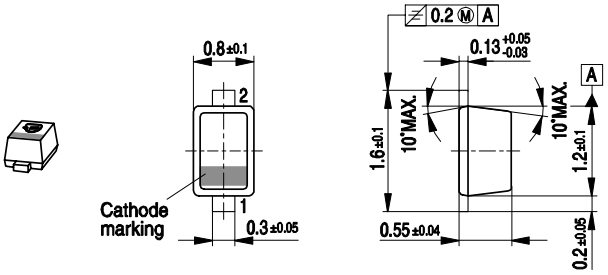
Isolation $I_{SO} = -|S_{21}|^2 = f(f)$

V_R = Parameter

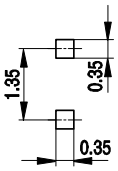
BAR65-02L in series configuration $Z = 50\Omega$



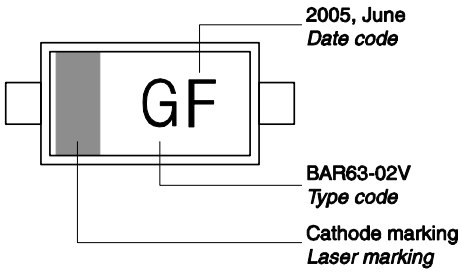
Package Outline



Foot Print

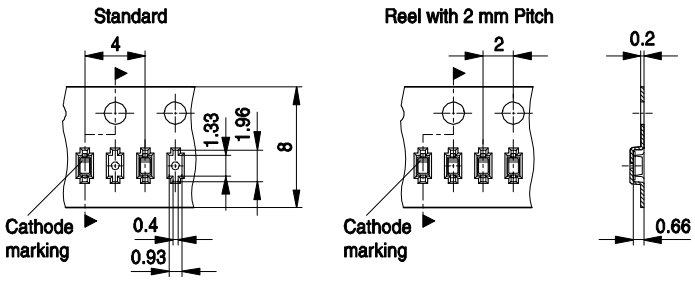


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø180 mm = 8.000 Pieces/Reel (2 mm Pitch)
Reel ø330 mm = 10.000 Pieces/Reel

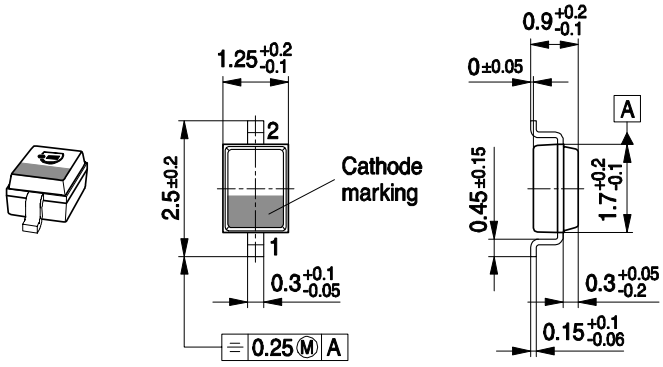


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75[1)]) CES-Code

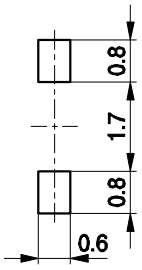
Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

1) New Marking Layout for SC75, implemented at October 2005.

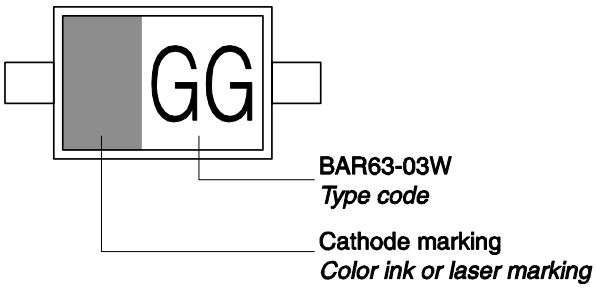
Package Outline



Foot Print

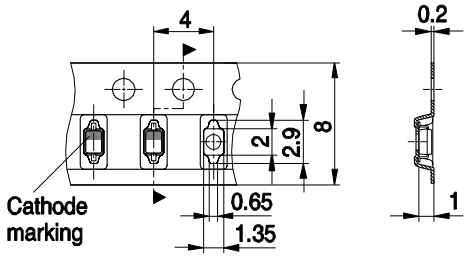


Marking Layout (Example)

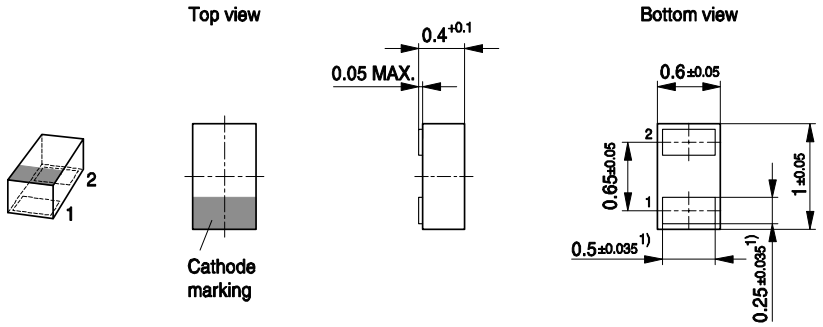


Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



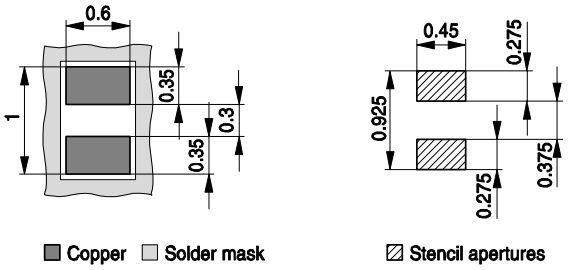
Package Outline



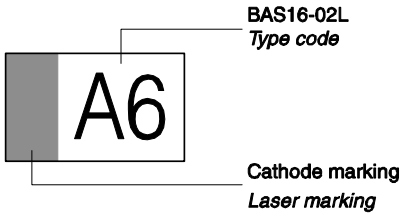
1) Dimension applies to plated terminal

Foot Print

For board assembly information please refer to Infineon website "Packages"



Marking Layout (Example)



Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel
Reel ø330 mm = 50.000 Pieces/Reel (optional)