Isolated DC/DC Converters ICs

Built-in Automotive Switching MOSFET Isolated Flyback Converter ICs BD7F205EFJ-C Evaluation Board

BD7F205EFJ-EVK-001

Overview

This evaluation board outputs an isolated 6.2 V, 16.5 V and 6.2 V voltage from an input of 8 V to 32 V, and can output a maximum output power 6 W.

BD7F205EFJ-C is an isolated flyback converter that does not require a photocoupler.

Feedback circuit by the transformer's tertiary winding or photocouplers becomes unnecessary, contributing to reduction of set parts.

It also has a number of built-in protection functions that enable the design of isolated power supply applications for high reliability.

Figure 1. BD7F205EFJ-EVK-001

Performance Specifications

This is a typical value and does not guarantee the characteristics.

Unless otherwise specified, V_{IN} = 12 V, I_{OUT} = 0.1 A, Ta = 25 °C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input voltage range	V_{IN}	8	12	32	V	
Output voltage 1	V_{OUT1}	5.5	6.2	6.9	V	I_{OUT1} = 0.1 A
Output voltage 2	V_{OUT2}	14.8	16.5	18.2	V	I_{OUT2} = 0.1 A
Output voltage 3	V_{OUT3}	5.5	6.2	6.9	V	I_{OUT3} = 0.1 A
Output current 1	I_{OUT1}	0		0.3	A	
Output current 2	I_{OUT2}	0		0.1	A	
Output current 3	I_{OUT3}	0		0.3	A	
Maximum output power	P_{OUT}	-	-	6	W	
Standby power	P_{INSTBY}	-	40	100	mW	I_{OUT} = 0 A V_{IN} = 12 V
Power Supply Efficiency	η	60	75	-	%	P_{OUT} = 2 W

Operating Procedure

1. Necessary equipment

(1) DC power supply of V to 32 V, 10 W / 5 A or more
(2) Load device up to 5 W
(3) DC voltmeter

2. Connecting the Equipment

(1) Preset the DC power supply to 8 V to 32 V and turn off the power output.
(2) Set the load to less than or equal to the rated current of each output and disable the load.
(3) Connect the positive terminal of the power supply to the VIN terminal and the negative terminal to the GND terminal with a pair of wires.
(4) Connect the positive terminal of the load to VOUT terminal and the negative terminal to GND terminal with a pair of wires.
(5) When connecting a wattmeter, connect as shown below. (Refer to your power meter User's Manual for more information)
(6) Connect the positive terminal of the DC voltmeter to VOUT terminal and the negative terminal to GND terminal for measuring the output voltage.
(7) Turn on the output of the DC power supply.
(8) Check that the DC voltmeter display is at the set voltage.
(9) Activates the load.

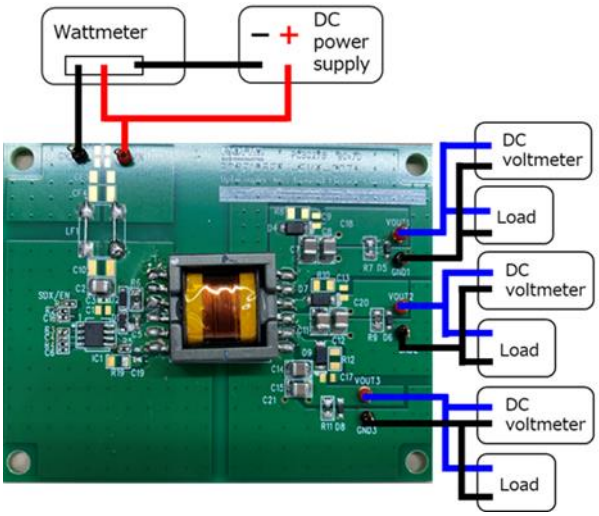


Figure 2. Connection Diagram

Application circuit

The evaluation board operates with an average frequency of approximately 363 kHz.

Monitoring the flyback voltage due to the voltage at the output provides primary-side feedback control that eliminates the need for photocouplers and auxiliary windings.

Operation starts when the VIN pin voltage exceeds UVLO detect voltage of 3.4 V (Typ) and SDXEN pin Enable pin voltage of 2.0 V (Typ).

The circuit diagram of the demonstration board is shown in the figure below, and the parts list is shown on page 12.

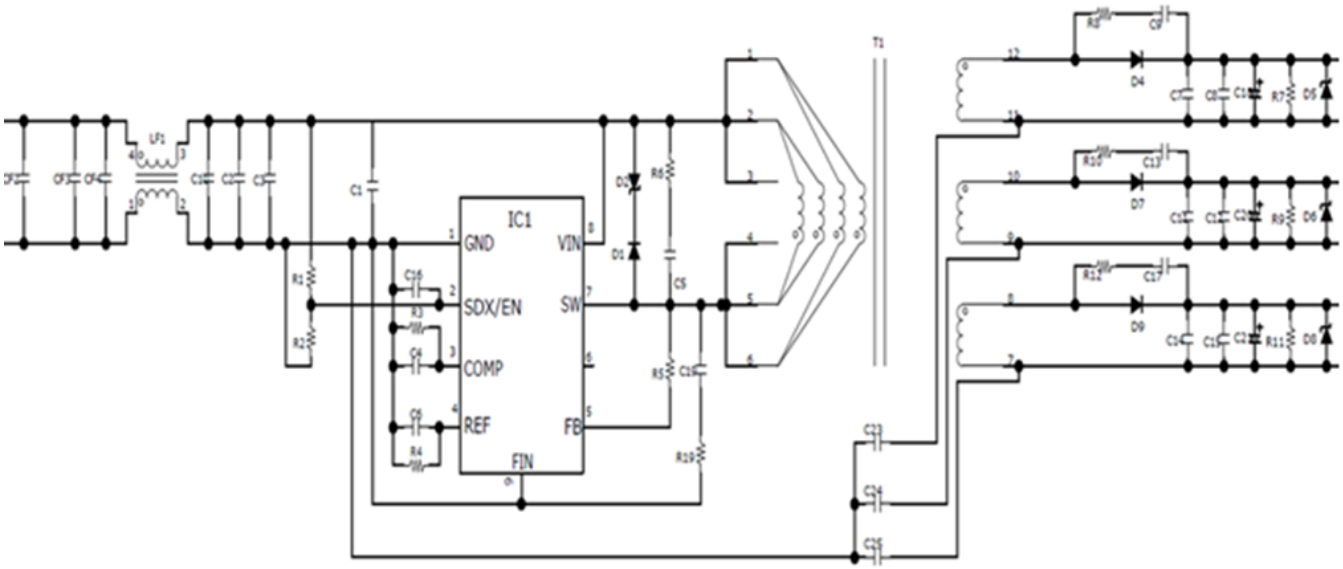


Figure 3. Circuit diagram

Outline of BD7F205EFJ-C

Features

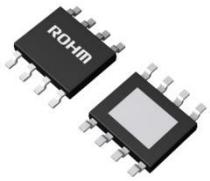
- AEC-Q100 (Grade-1)
- No Need for Optocoupler and Third Winding of Transformer
- Output voltage is set by two external resistors and transformer winding ratio.
- Uses proprietary adaptive ON-time control technology
- Highly efficient light load mode (PFM operation)
- Shutdown and Enable control
- Burst voltage design possible
- 60 V Built-in-switching MOSFET
- Spread frequency spectrum
- Soft start function
- Load current compensation function
- Various protection functions
  - Undervoltage protection (UVLO)
  - Overcurrent protection (OCP)
  - Overheat protection (TSD)
  - REF pin open protection (REFOPEN)
  - Short-circuit protection (SCP)
  - Battery short-circuit protection (BSP)

Critical Characteristics

- Input voltage range :
  - VIN terminal 3.4 V to 42.0 V
  - SW pin to 60 V
- Switching frequency : 363 kHz (Typ)
- Reference voltage accuracy: ±2.8 % (Typ)
- Shutdown current 0 μA (Typ)
- Operating temperature range -40 °C to +125 °C

Package W (Typ) x D (Typ) x H (Max)

HTSOP-J8 4.9 mm x 6.0 mm x 1.0 mm



Applications

Insulated power supply for automotive use (E-Comp, Inverter etc)

Insulated power supply for industrial equipment

Pin Layout

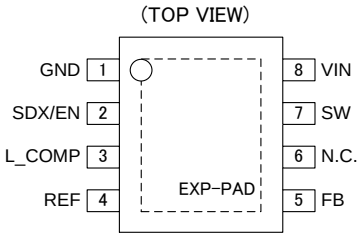


Figure 4. Pin layout drawing

PIN ASSIGNMENT

No.	Pin name	Function
1	GND	GND terminal
2	SDX/EN	Shutdown/Enable control pin
3	L_COMP	Load current compensation value setting pin
4	REF	Output voltage setting pin
5	FB	Output voltage setting pin
6	N.C.	No Connect
7	SW	Switching output pin
8	VIN	Power input terminal
-	EXP-PAD	Rear heat dissipation pin

Measurement data

1. Load regulation

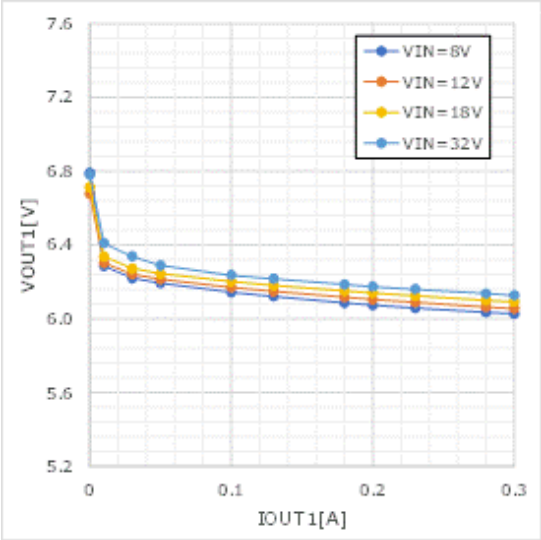


Figure 5. Output Voltage1 vs Output Current1
IOUT2=30mA, IOUT3=50mA

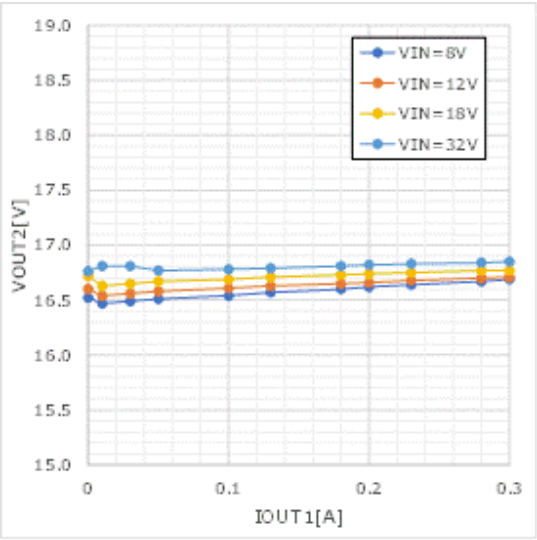


Figure 6. Output Voltage2 vs Output Current1
IOUT2=30mA, IOUT3=50mA

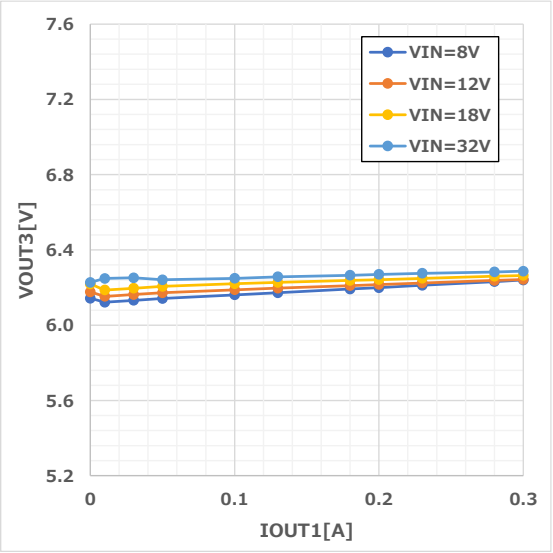


Figure 7. Output Voltage3 vs Output Current1
IOUT2=30mA, IOUT3=50mA

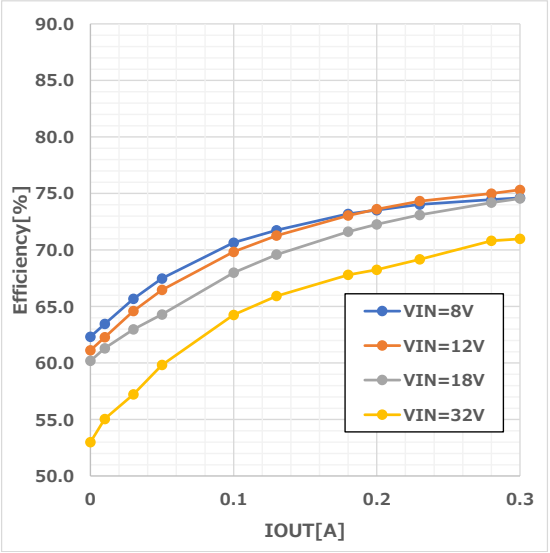


Figure 8. Efficiency vs Output Current1
IOUT2=30mA, IOUT3=50mA

Measured data-continued

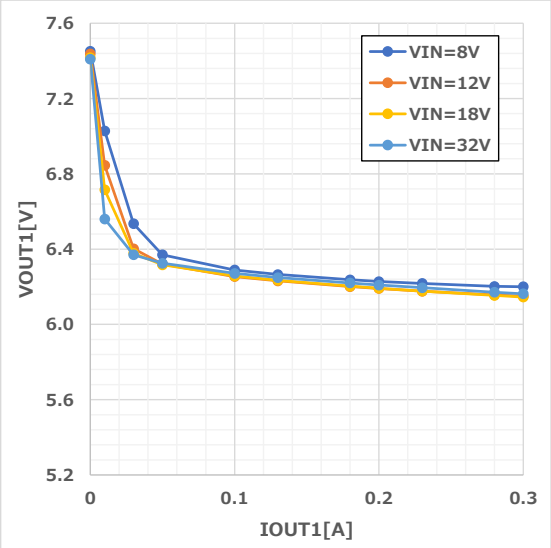


Figure 9. Output Voltage1 vs Output Current1
IOUT2=100mA, IOUT3=300mA

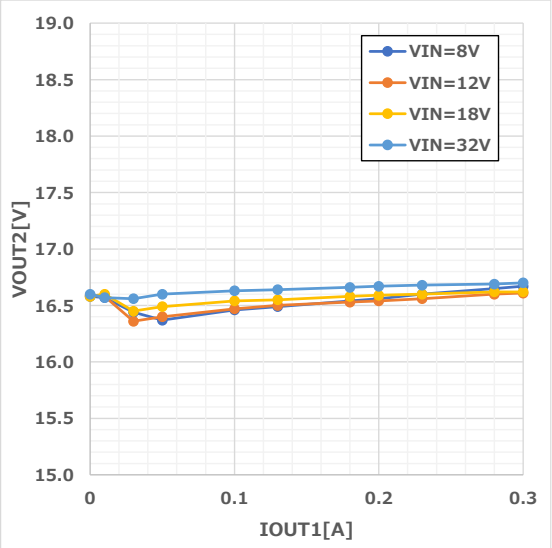


Figure 10. Output Voltage2 vs Output Current1
IOUT2=100mA, IOUT3=300mA

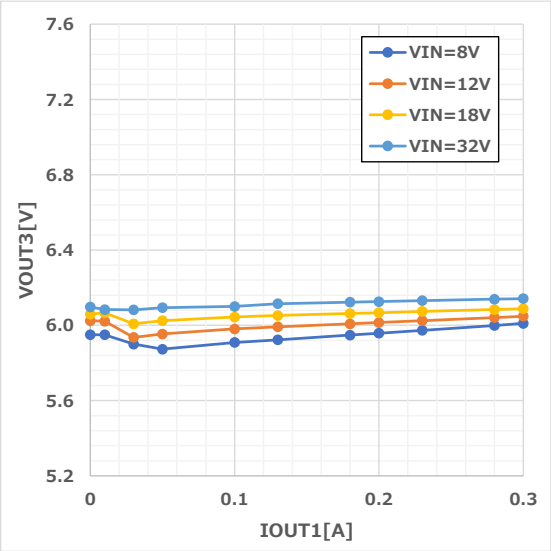


Figure 11. Output Voltage3 vs Output Current1
IOUT2=100mA, IOUT3=300mA

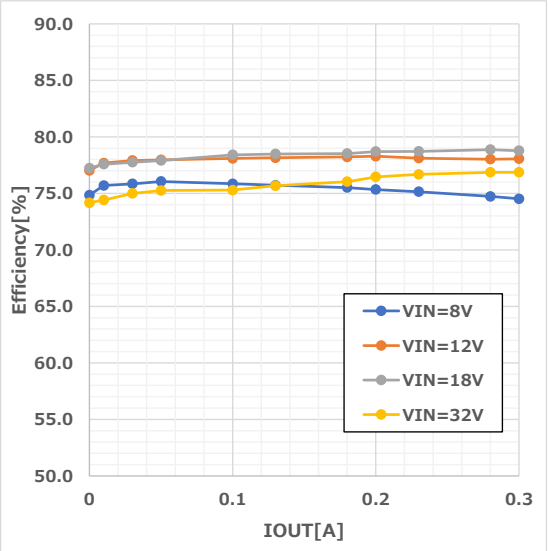


Figure 12. Efficiency vs Output Current1
IOUT2=100mA, IOUT3=300mA

Measured data-continued

2. Line regulation

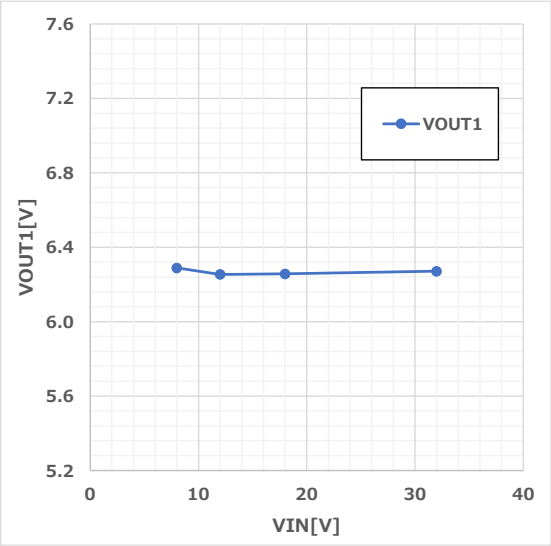


Figure 13. Output Voltage1 vs Input Voltage
IOUT1=100mA, IOUT2=100mA, IOUT3=300mA

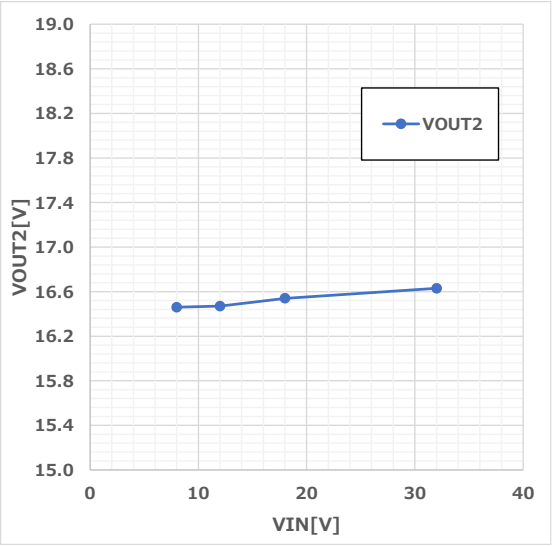


Figure 14. Output Voltage2 vs Input Voltage
IOUT1=100mA, IOUT2=100mA, IOUT3=300mA

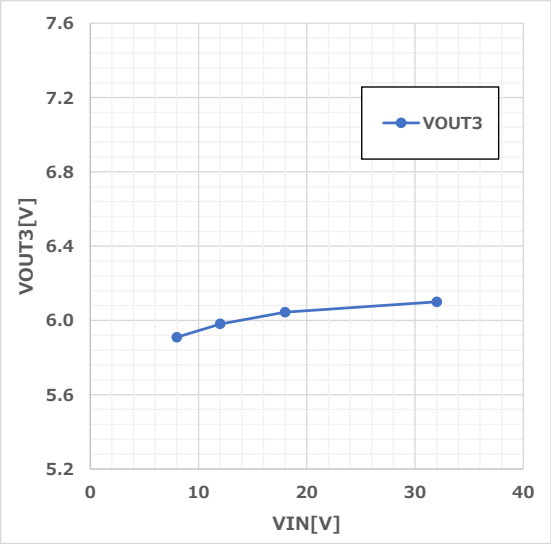


Figure 15. Output Voltage3 vs Input Voltage
IOUT1=100mA, IOUT2=100mA, IOUT3=300mA

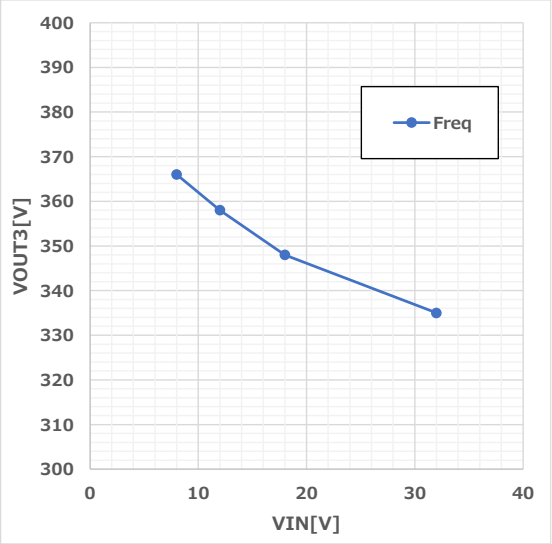


Figure 16. Frequency vs Input Voltage
IOUT1=100mA, IOUT2=100mA, IOUT3=300mA

Measured data-continued

3. Switching waveform

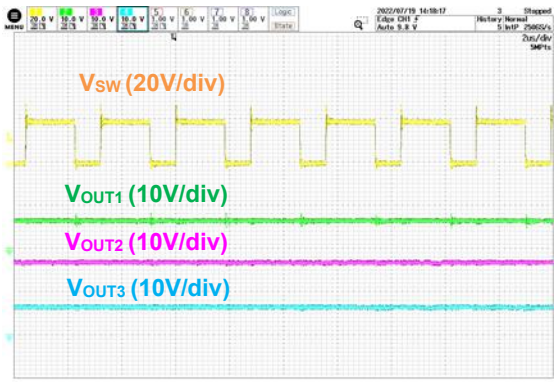


Figure 17. MOSFET Waveform
Vin = 12 V, IOUT1,3 = 0.1 A, IOUT2 = 0.05 A

Figure 18. MOSFET Waveform
Vin = 12 V, IOUT1,3 = 0.3 A, IOUT2 = 0.1 A

4. Load response waveform

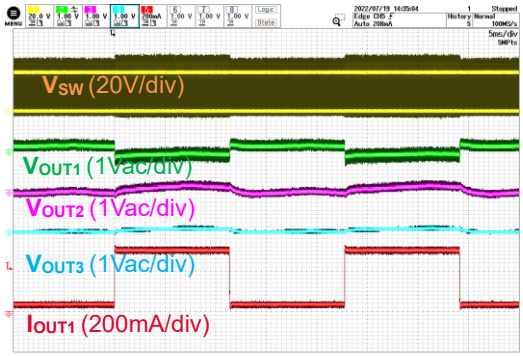


Figure 19. Load response
Vin = 12 V, IOUT2 = 0.05 A, IOUT3 = 0.1 A
IOUT1 = 30 mA to 300 mA

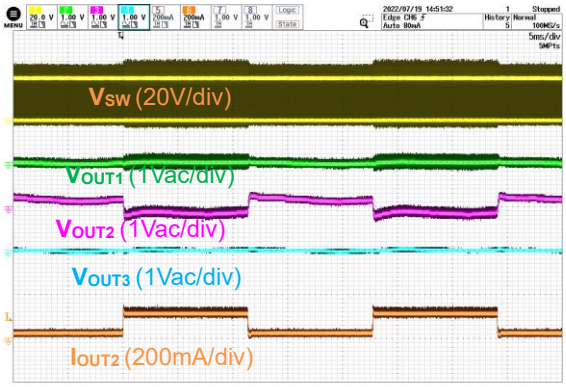


Figure 20. Load response
Vin = 12 V, IOUT1 = 0.1 A, IOUT3 = 0.1 A
IOUT2 = 10 mA to 100 mA

5. Output ripple voltage waveform

*This ripple is due to spread spectrum.

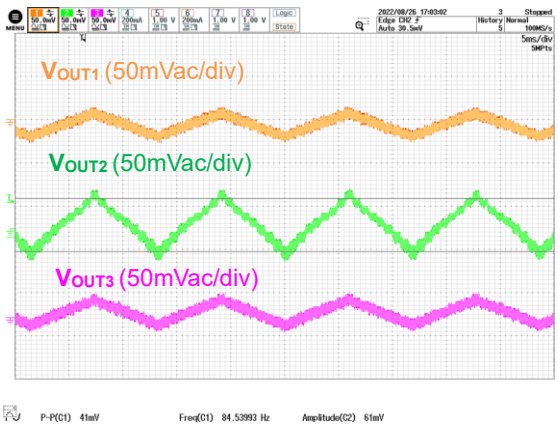


Figure 21. Output voltage ripple Waveform
VIN = 12 V / IO1,2,3=0.1, 0.05, 0.1 A

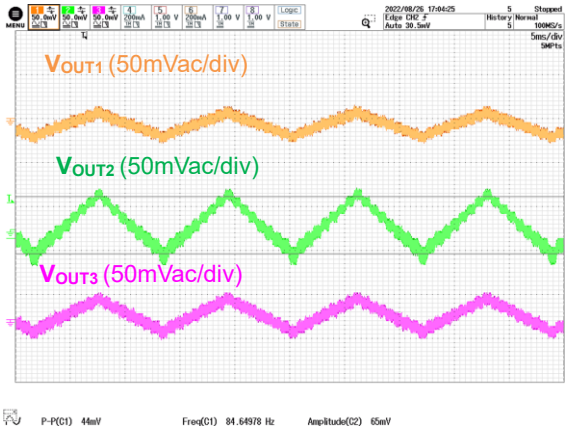


Figure 22. Output voltage ripple Waveform
VIN = 12 V / IO1,2,3=0.3, 0.1, 0.3 A

Measured data-continued

6. Startup/stop waveform

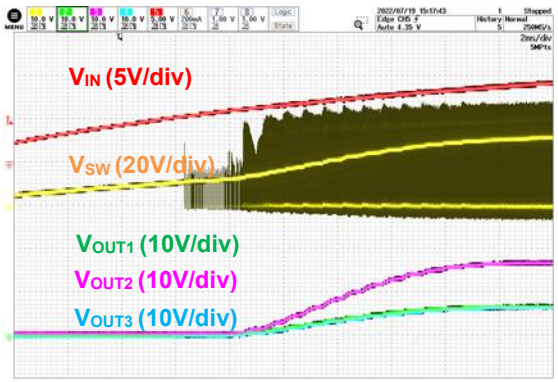


Figure 23. Start Up Waveform

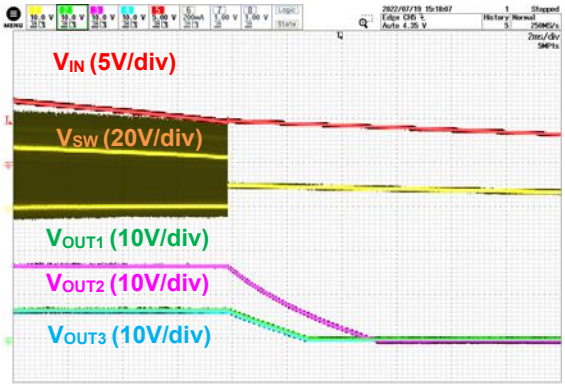


Figure 24. Shut Down Waveform

7. Output short waveform

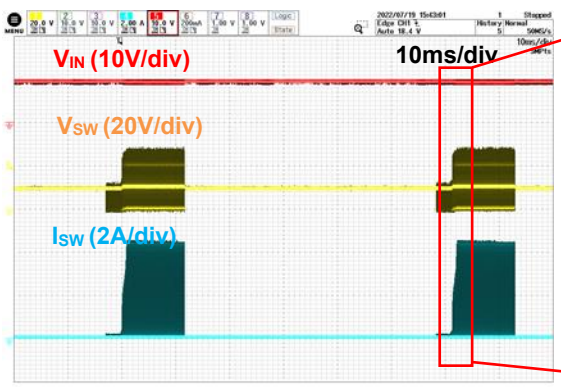


Figure 25. VOUT Short Waveform
Vin = 8 V

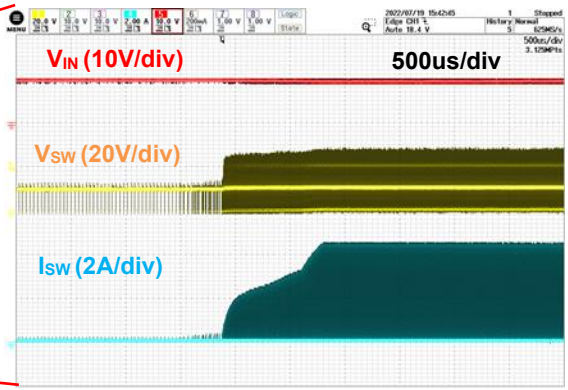


Figure 26. VOUT Short Waveform (ZOOM)
Vin = 8 V

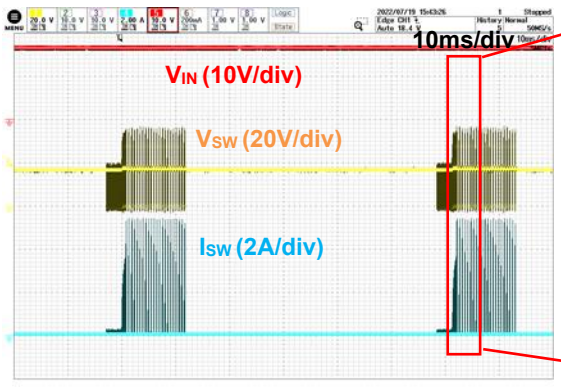


Figure 27. VOUT Short Waveform
Vin = 15 V

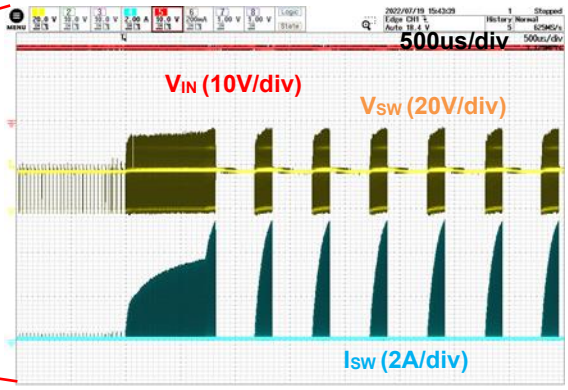


Figure 28. VOUT Short Waveform (ZOOM)
Vin = 15 V

Measured data-continued

Component surface temperature

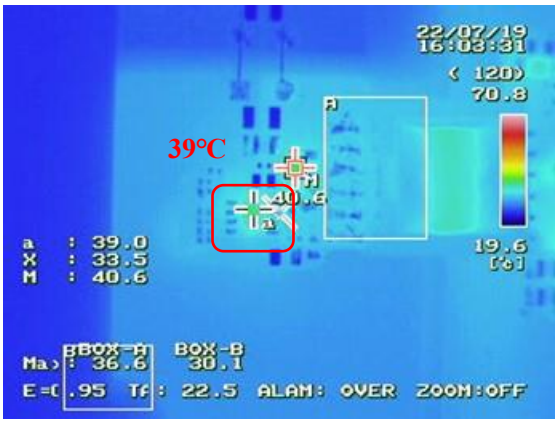


Figure 29. Surface Temperature
Vin = 8 V, IOUT1 = 0.3 A, IOUT2 = 0.1 A
IOUT3 = 0.3 A (Ta = 25℃)

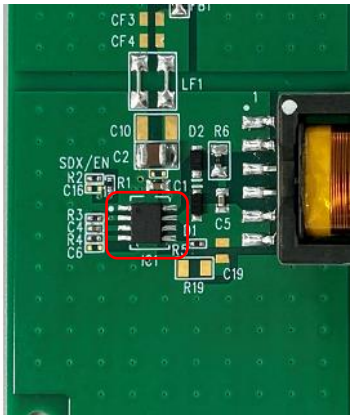


Figure 30. Surface Temperature Reference

Table 1. Tj Calculation

Item	Design BD7F205EFJ	unit	comment
VIN(TYP)	8	V	
VOUT	6.25	V	
VF	0.6	V	
Pomax	5.4375	W	
Io_max	0.870	A	POUT/VOUT
Np	11	-	
Ns	12	-	
Efficiency	85	%	
Iin_ave	0.800	A	POUT/EFFI/VIN
Lp	18.00	uH	
Ipeak(turnOFF)	2.09	A	Iin_ave/DUTY+VIN/LP*Ton/2
Ids(turnON)	1.55	A	Iin_ave/DUTY-VIN/LP*Ton/2
Vds	14.28	V	VIN+(Np/Ns)*(VOUT+VF)
Ron(Ta=25℃)	0.180	Ω	
Ron(Ta=120℃)	0.300	Ω	
Fsw	363	kHz	
tr	40	ns	rising time
tf	30	ns	falling time
Ton	1.211	us	1/FREQ*DUTY
DUTY	44.0	%	(Np/Ns)*(VOUT+VF)/((Np/Ns)*(VOUT+VF)+VIN)
ICC	1.0	mA	
Thermal Resistance ΨJT	13.0	℃/W	2s2p(℃/W)
①Loss calculation	0.072W	W	①P=1/6*Ipeak*Vds*tf*Fsw
②Loss calculation	0.436W	W	②P=(Ipeak-(Ipeak-IO)/2)*(Ipeak-(Ipeak-IO)/2)*Ron_total * Duty
③Loss calculation	0.054W	W	③P=1/6*Ion*Vds*tr*Fsw
④Loss calculation	0.008W	W	④P=VIN*ICC
Total loss	0.570W	W	
ΔTj	7.41	℃	
Topr_max	125	℃	
Tc	39	℃	
Tj	146.4	℃	Tj=Topr_max+ΔTj
Judge	○	—	Tj < 150℃

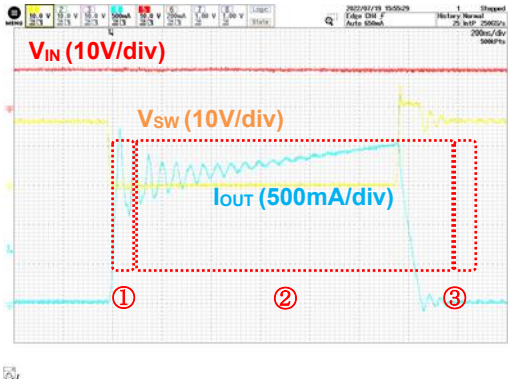


Figure 31. Peak Current Waveform
Vin = 8 V, IOUT1 = 0.3 A, IOUT2 = 0.1 A
IOUT3 = 0.3 A

Tj calculation of IC is calculated using the above table.
Loss of IC is divided into 1: Turn on loss, 2: conduction loss, 3: Turn off loss, and 4: ICC.
Calculate the loss according to Table1 from the actual current waveform and power supply spec.
In this case, Tj is estimated to be 39 °C because Tc = 30.3 °C and ΔTj = 7.41 °C.
Tj should be designed to be 150 °C or less.
In this case, when Ta = 125 °C, Tj = 146 °C, and Tj = 150 °C is not reached, so it can be judged that there is no problem in the whole temperature range.

Circuit diagrams

(Condition) V_{IN} = 8 V to 32 V, V_{OUT} = 16.5 V, 0.2 A

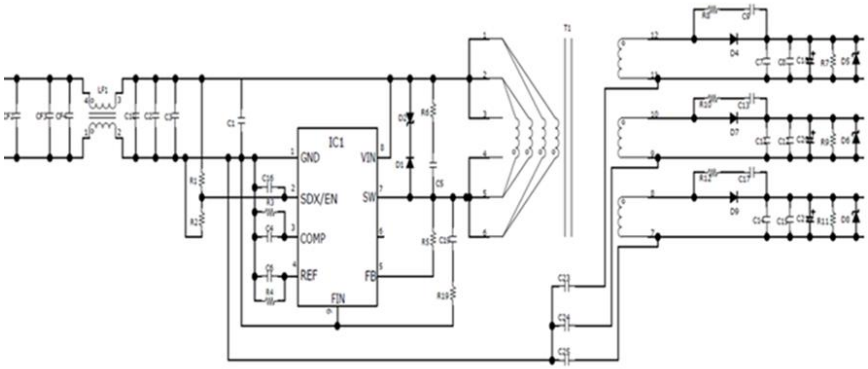


Figure 32. BD7F205EFJ-EVK-001 Schematic

Bill of Materials

C1	C_VIN1	0.1uF/50V	GCM188L81H104KA57D
C2	C_VIN2	10uF/50V	GCM32EC71H106KA01
C4	C_L_COMP	0.1uF/50V	GCM155R71H104KE37
C5	C_snubber	1000pF/100V	GCM1887U2A102JA16
C7	C_OUT1	22uF/25V	GCM32EC71E226KE35
C8	C_OUT1	22uF/25V	GCM32EC71E226KE35
C11	C_OUT2	22uF/25V	GCM32EC71E226KE35
C12	C_OUT2	22uF/25V	GCM32EC71E226KE35
C14	C_OUT3	22uF/25V	GCM32EC71E226KE35
C15	C_OUT3	22uF/25V	GCM32EC71E226KE35
R1	R_EN	180kΩ	MCR01PZPF1803
R2	R_EN	120kΩ	MCR01PZPF1203
R3	R_L_COMP	10kΩ	MCR01PZPF1002
R4	R_REF	2.7kΩ	MCR01PZPF2701
R5	R_FB	31.6kΩ	MCR01PZPF3162
R6	R_snubber1	1kΩ	MCR03PZPZFX1001
R7	R_OUT1	4.7kΩ	MCR03PZPZFX4701
R9	R_OUT2	2.2kΩ	ESRC03PZPZF2201
R11	R_OUT3	4.7kΩ	MCR03PZPZFX4701
LF1	Filter	short	
T1	Trans	18uH	
D1	D_snubber1	100V/1A	RB168MM100TFTR
D2	D_snubber2	9.1V	KDZV9.1B
D4	D_second1	100V/1A	RB168LAM100TF
D5	D_OUT1	7.5V	UDZV7.5B
D6	D_OUT2	20V	UDZV20B
D7	D_second2	200V/1A	RF101LAM2STF
D8	D_OUT3	7.5V	UDZV7.5B
D9	D_second3	100V/1A	RB168LAM100TF
IC			BD7F205EFJ-C

*Parts are subject to change without notice.

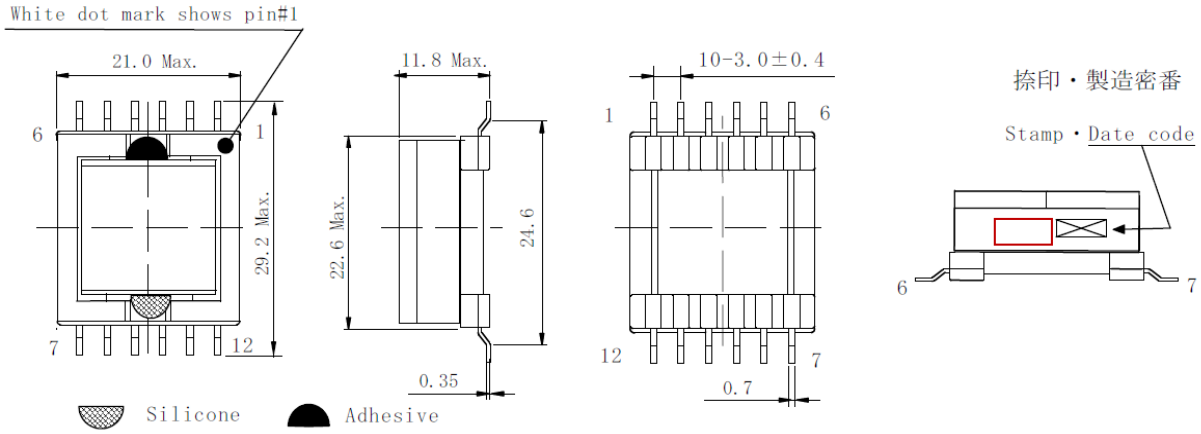
Transformer specifications

Manufacturer : Sumida Electric Co., Ltd.

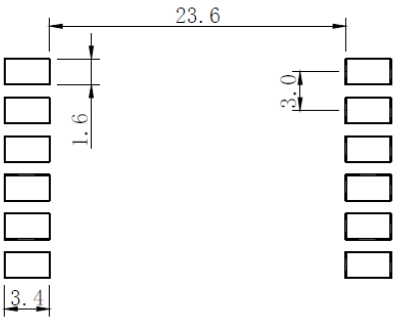
https://job.mynavi.jp/conts/n/sp/23/54430_23sumida/

Product name: CEFD2010-00399-T381R

■ External Dimensions



■ Recommended Land



RoHS
compliance
Cd:Max.0.01wt%
others:Max.0.1wt%

■ Terminal connection diagram

“S”印は巻始めを示す。
“S” indicates the winding start.
□印はチューブにて絶縁処理すること。
□ shall be insulated by tube.
端子1-2間及び5-6間はパターンにより接続してご使用下さい。
Pin 1-2 、Pin 5-6 should be connected together when using on PCB.

“•”は極性を示す。
“•” Indicates the same polarity.

Transformer Specifications-continued

■ Winding wire and linear/linear type

端子番号 Terminal No.	5-2	12-11	10-9	8-7	6-1
巻数 Turns	11T	12T	31T	12T	11T
本数 Strands	2	2	1	1	2
線径・線種 Wire (diameter & type)	0.23 UEW		0.14 UEW	0.23 UEW	

■ ELECTRICAL CHARACTERISTICS

項目 Item	規 格 Specification	測定条件 Measuring conditions
インダクタンス (5,6-1,2) Inductance	18μH±10% Within	100kHz, 1V
飽和電流 (5,6-1,2) Saturation Current	3.3A	at 125℃
耐電圧 (1,2,5,6)-(7,8,9, 10,11, 12) Withstanding voltage	AC 2500Vrms 1minute	50Hz/60Hz

※ 耐電圧の規格に対して、1.2倍の電圧値で２秒間にて全数検査実施致します。
As to withstand voltage, every part should be tested with 1.2 times of standard voltage for 2 seconds.

※ 飽和電流：インダクタンスが公称値の90 %に減少するときの直流電流の値。
Saturation current: The value of DC current when the inductance decreases to 90% of the nominal value.

Application Design Example

1. Transformer design

1.1 Determining the volume ratio N_P/N_S

The winding ratio is a parameter that sets the output voltage, maximum output power, duty, and SW terminal voltage.

The duty of the flyback converter is calculated by the following equation:

$$Duty = \frac{\frac{N_P}{N_S} \times (V_{OUT} + V_F)}{V_{IN} + \frac{N_P}{N_S} \times (V_{OUT} + V_F)} \quad [\%]$$

N_P : Primary transformer turns

N_S : Secondary transformer turns

V_{OUT} : Output voltage (Since there are 3 outputs, the design is based on output voltage 1)

V_F : Forward voltage of the output diode on the secondary side

V_{IN} : VIN pin voltage

From the above formula, the winding ratio is calculated as follows.

$$\frac{N_P}{N_{S1}} = \frac{D_{TYP}}{1 - D_{TYP}} \times \frac{V_{IN}}{V_{OUT} + V_F}$$

D_{typ} : Duty at VIN Voltage (Typ)

It is recommended to set D_{TYP} from 30% to 50% at the VIN voltage in the middle of the operating range.

Initially, set D_{TYP} = 40 %. (This time, set the Duty to 35%)

In this case, the following formula is used.

$$\frac{N_P}{N_{S1}} = \frac{0.35}{1 - 0.35} \times \frac{12V}{6.2V + 0.6V} = 0.92$$

Therefore, we will proceed with designing with a Np/Ns1 of 0.92.

The turn ratio is also limited by the maximum duty D_{MAX} determined from the minimum incoming voltage.

Make sure that D_{MAX} given by the equation below does not exceed 70%. If this is the case, set D_{TYP} so that it becomes smaller. If it exceeds 70 %, the OFF time will be shortened. Therefore, the output voltage may deviate due to deviations in the flyback voltage detection.

$$\frac{N_P}{N_{S1}} = \frac{D_{MAX}}{1 - D_{MAX}} \times \frac{V_{IN(Min)}}{V_{OUT(Max)} + V_{F(Max)}}$$

D_{MAX} : Maximum duty of VIN voltage (Min) condition

$V_{OUT(Max)}$: Maximum output voltage (Since there are 3 outputs, the design is based on output voltage 1)

$V_{F(Max)}$: Forward voltage of secondary diode (Max)

$$D_{MAX} = \frac{0.92}{\frac{8V}{6.2V + 0.6V} + 0.5} = 0.44 < 0.70$$

For this reason, there is no problem in this design.

D_{MAX} of this designer is 0.44 and 0.70 or less, so it is judged without any problem.

Determining the Volume Ratio N_P/N_S-continued

The flyback voltage V_{OR} is calculated by the following equation.

$$V_{OR} = (V_{OUT} + V_F) \times \frac{N_P}{N_{S1}} \quad [\mathrm{V}]$$

$$V_{OR} = (6.2V + 0.6V) \times 0.92 = 6.3\ V$$

Set so that the SW terminal voltage calculated below does not exceed the withstand voltage.

$$V_{SW} = V_{IN(Max)} + V_{OR} + V_{SURGE}$$

For example, if the derating against the SW pin withstand voltage is 90 %, the SW terminal voltage,

$60\ V \times (100\ \% - 10\ \%) = 54\ V$ It should be designed to be within 54 V.

This is designed with $V_{IN(Max)}$ = 32 V, V_{OR} = 6.3 V.

V_{SURGE} at this time is as follows.

$$54\ V - (32\ V + 6.3\ V) = 15.7\ V$$

Therefore, the surge voltage must be less than 15.7 V.

V_{SURGE} is caused by the leaking magnetic fluxes of the transformers.

If V_{SURGE} is large, the transformer structure needs to be reviewed and the snubber circuitry needs to be adjusted.

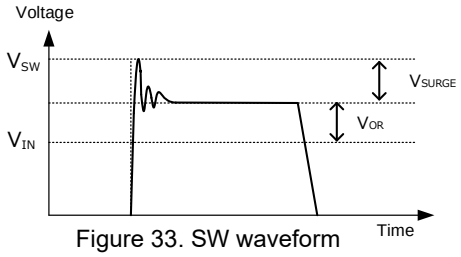


Figure 33. SW waveform

1.2 Calculating L_P, L_S

Set L_P, L_S to enable continuous current mode operation.

Determine by using the current continuous-mode depth k to obtain L_P, L_S.

k is expressed from I_{SPK}, I_{SB} of Figure 32 by the following equation.

$$k = (I_{SPK} - I_{SB})/I_{SPK}$$

I_{spk}: Secondary transformer peak current

I_{sb} : Secondary transformer bottom current

K : Constant representing the depth of the current continuous mode (When designing, use k = 0.25 as a guide.)

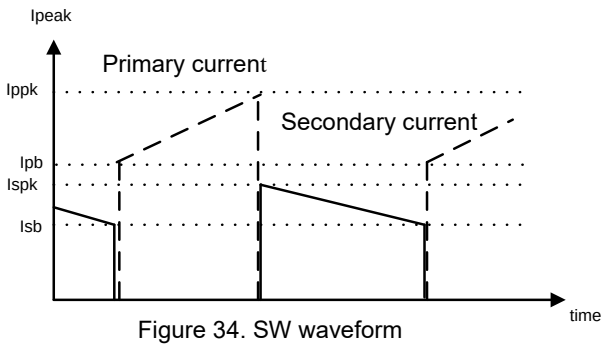


Figure 34. SW waveform

I_{ppk}: Primary transformer peak current

I_{pb} : Primary transformer bottom current

Transformer design-continued

The maximum peak current on the primary side of the IC is determined by I_{LIMIT} of electrical characteristics.
I_{LIMIT} minimum-value determines the secondary min-peak current $I_{SPK1(Min)}$.

$$I_{SPK1(Min)} = I_{LIMIT(Min)} \times \frac{N_P}{N_S} \quad [A]$$

The secondary peak current $I_{SPK2(Max)}$ is calculated from the maximum output current $I_{OUT(Max)}$ by the following equation.

$$I_{SPK2(Max)} = \frac{2 \times I_{OUT(Max)}}{(1 - D_{MAX}) \times (2 - k)} \times \frac{1}{\eta} \quad [A]$$

η : Use a power supply efficiency of 70 % as a guideline.
$I_{OUT(Max)}$: Max. secondary output current (Determined by maximum power of 3 outputs ÷ output voltage 1)

$I_{SPK2(Max)} < I_{SPK1(Min)}$ must be met in order for $I_{OUT(Max)}$ to be printed.
If the conditions cannot be satisfied, change k to redesign. With higher k values in discontinuous mode
The operating load area becomes wider. When k = 1, discontinuous mode operation is performed in all areas.
This IC is continuous
A low k-value is recommended to achieve high-speed response and low EMI characteristics by mode operation.
Even if the k value is high, there is no problem with power supply operation.

The secondary-side index $L_{S(Max)}$ is calculated by the following equation.

$$L_{S(Max)} = \frac{(2 - k) \times (V_{OUT} + V_F) \times (1 - D_{MAX})^2}{2 \times I_{OUT(Max)} \times f_{sw(Max)} \times k} \quad [\mu H]$$

$$L_{S(Max)} = \frac{(2 - 0.25) \times (6.2V + 0.6V) \times (1 - 0.44)^2}{2 \times 0.85 \times 430kHz \times 0.25} = 21\mu H$$

$f_{SW(Max)}$: Switching frequency This switching frequency should be calculated at 430 kHz.
$I_{OUT(Max)}$: Max. secondary output current (Determined by maximum power of 3 outputs ÷ output voltage 1)

At this time, the primary inductance Lp is obtained by the following equation.

$$L_P = L_S \times (\frac{N_P}{N_S})^2 \quad [\mu H]$$

$$L_P = 21\mu H \times (0.92)^2 = 18\mu H$$

From the above, we will proceed with the design as Lp:18μH, Ls:21μH in this design.

Application Design Examples-continued

2. Output voltage

When the built-in switching MOSFET is turned OFF, the SW pin voltage V_{SW} becomes higher than the VIN pin voltage. Since the difference between the SW pin voltage and the VIN pin voltage is equal to the primary flyback voltage, the secondary output voltage is calculated from this voltage. The SW pin voltage V_{SW} at turn-off is calculated by the following equation.

$$V_{SW} = V_{IN} + \frac{N_P}{N_S} \times (V_{OUT} + V_F) \quad [\mathrm{V}]$$

V_{SW} : SW pin voltage
V_{IN} : VIN pin voltage
N_P : No. of primary transformer turns
N_S : Secondary transformer turns
V_{OUT} : Output voltage
V_F : Forward voltage of the output diode on the secondary side

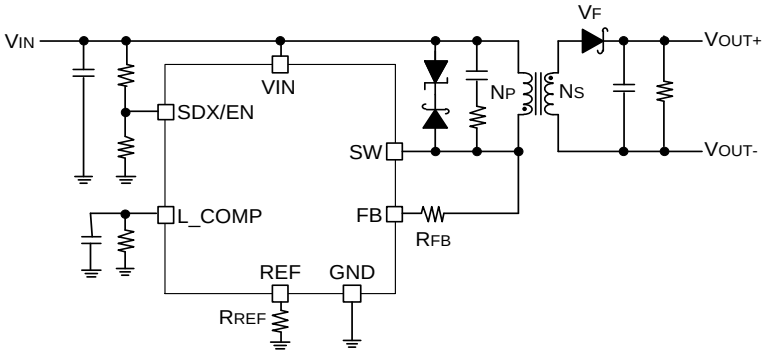


Figure 35. Application Block Diagram

The primary flyback voltage is converted to the FB-pin inrush current I_{FB} by the external resistor R_{FB} between FB-SW terminals. Since the FB pin voltage becomes almost equal to the VIN pin voltage by the IC's internal circuit, the FB pin inrush current I_{RFB} is calculated by the following equation.

$$I_{FB} = \frac{V_{SW} - V_{FB}}{R_{FB}} = \frac{V_{IN} + \frac{N_P}{N_S} \times (V_{OUT} + V_F) - V_{FB}}{R_{FB}} = \frac{\frac{N_P}{N_S} \times (V_{OUT} + V_F)}{R_{FB}} \quad [\mathrm{A}]$$

I_{FB} : FB pin inrush current
V_{FB} : FB terminal voltage
R_{FB} : External resistor between FB and SW pins

2. Output Voltage- continued

In addition, since the FB pin inrush current I_{RFB} flows to the external resistor R_{REF} between the REF terminal and GND terminal, the REF terminal voltage is calculated by the following equation.

$$V_{REF} = \frac{R_{REF}}{R_{FB}} \times \frac{N_P}{N_S} \times (V_{OUT} + V_F) \quad [V]$$

V_{REF} : REF pin voltage
R_{REF} : External resistor between REF pin and GND pin

Because the current that flows to the REF pin becomes I_{REF} when the REF pin voltage is V_{INTREF} for R_{REF},

$R_{REF} = \frac{0.54V}{200\mu A} = 2.7\ k\Omega$ The resistor must be set.

The REF pin voltage is input to the comparator with the reference voltage inside the IC. The REF pin voltage is equal to the reference voltage by the internal circuit of the IC. Therefore, the output voltage and the REF pin voltage are calculated by the following equations.

$$V_{OUT} = \frac{R_{FB}}{R_{REF}} \times \frac{N_S}{N_P} \times V_{INTREF} - V_F \quad [V]$$

As can be seen from this equation, the output voltage V_{OUT} can be set by the transformer turn ratio (N_P/N_S) on the primary and secondary sides and the resistance ratio between R_{FB} and R_{REF}.

From the above equation, the external resistor R_{FB} between the FB pin and SW terminal can be calculated by the following equation.

$$R_{FB} = \frac{R_{REF}}{V_{INTREF}} \times \frac{N_P}{N_S} \times (V_{OUT} + V_F) \quad [\Omega]$$

In this designer, R_{FB} is determined as follows.

$$R_{FB} = \frac{2.7k\Omega}{0.54V} \times 0.94 \times (6.2V + 0.6V) = 31.96\ k\Omega$$

R_{FB} is set to 31.6kohm.
However, the ESR on the secondary side of the transformer is a factor that lowers the output voltage as in V_F of the above equation.
Also, when the transformer is not coupled, the number of turns of N_P/N_S is shifted, which causes the output voltage to decrease.
Therefore, finally adjust the output voltage by checking the actual device.

Application Design Examples-continued

R_{FB} has been decided, let's decide the winding ratios of the other output transformers.

Since Np/Ns1 is 0.92, we designed Np=11T and Ns1=12T.

At this time, the formula for output voltage 2 is as follows.

$$V_{OUT} = \frac{R_{FB}}{R_{REF}} \times \frac{N_{S2}}{N_P} \times V_{INTREF} - V_F$$

Therefore, Ns2=31T. Determine Ns3 as 12T by the same formula.

3. Output Capacitor

Place the output capacitor as close to the secondary diode as possible.

The output capacitance value C_{OUT} is set from the output ripple voltage ΔV_O and the start-up time.

The output ripple voltage generated by one switching is calculated as follows.

$$\Delta V_O = \frac{I_{OUT(Max)} \times D_{MAX}}{f_{SW(Max)} \times C_{OUT}} \quad [V]$$

On the other hand, when output capacitor is large, start-up time is long.

When SCP detection mask time ($t_{MASKSCP}$) in start-up is passed, if REF voltage is lower than V_{SCP}, power supply cannot output. Therefore, C_{OUT} must be satisfied below condition.

$$C_{OUT} \leq \frac{1}{2} \times \frac{t_{MASKSCP(Min)} \times \{\left(I_{LIMIT(Min)} \times \frac{N_P}{N_S}\right) \times (1 - Duty) - I_{OUT(Max)}\}}{V_{OUT} \times (\frac{V_{SCP(Max)}}{V_{INTREF(Min)}})} \quad [\mu F]$$

Where $\frac{V_{SCP(Max)}}{V_{INTREF(Min)}}$ = 0.762

A large capacitor capacitance value is required to hold the output voltage during load response or power supply voltage response.

A capacitance value of 20 µF or more is recommended as a guideline for the output voltage capacitance.

Ceramic capacitors are affected by temperature characteristics, capacitance variation, DC bias characteristics, etc. The capacitance value may decrease. Pay attention to these points when selecting parts.

4. Input Capacitor

Use a ceramic capacitor for the input capacitor and place it as close to the IC as possible.

Capacitance of the capacitor should be 10 µF or more.

Application Design Examples-continued

5. Secondary output diode

A Schottky barrier diode or a fast recovery diode with low V_F is recommended because the forward voltage V_F of the secondary output diode causes an error in the output voltage. When selecting a secondary output diode, the peak of the secondary reverse voltage must not exceed the rating of the diode. The secondary RMS current I_{SRMS} must also be set so that it does not exceed the rating.

Generally, 30 % or more of the reverse-direction breakdown voltage V_R is recommended.

$$V_R = (V_{IN(Max)} \times \frac{N_S}{N_P} + V_{OUT}) \times 1.3 + V_{SURGE} \quad [V]$$

V_R : Reverse voltage of the secondary output diode
$V_{IN(Max)}$: VIN pin maximum voltage
N_P : No. of primary transformer turns
N_S : Secondary transformer turns
V_{OUT} : Output voltage
V_{SURGE}: Transformer surge voltage generated in the diode

It is recommended that the rated current of the secondary output diode be at least twice that of I_{SRMS}.

6. Output Resistance and Zener Diode (Minimum Load Current)

The output voltage rises when no load is applied or when light load is applied. The reason for this is that the MAXIMUM is in the OFF-time t_{OFF_MAX} when the IC is under light load.

This is because switching is always performed at the minimum frequency determined by the minimum ON-time t_{ON_MIN}. For the power P_{O_MIN} determined by the switching frequency of this lowest frequency, when the secondary load is lighter than this, the output voltage is

It moves up. P_{O_MIN} is calculated by the following equation:

$$P_{O\_MIN} = \frac{{V_{IN(Max)}}^2}{2 \times L_P} \times {t_{ON\_MIN(Max)}}^2 \times \frac{1}{t_{ON\_MIN(Max)} + t_{OFF\_MAX(Min)}} \quad [W]$$

$I_{OUT\_MIN} = \frac{P_{O\_MIN}}{V_{OUT}}$ Because it is an expression, it can also be obtained from I_{OUT_MIN} .

If the rise in the secondary output voltage becomes a problem, connect a secondary output zener diode to suppress the rise in the voltage. It is also necessary to suppress the rise in the output voltage by adding a resistor to the secondary output to provide a constant loss. The output resistor R_{OUT} to be connected to the secondary side should be as follows. The resistor-loss P_{LOSS} is calculated as follows.

$$P_{loss} = \frac{{V_{OUT}}^2}{R_{OUT}} \quad [W]$$

$$R_{out} \leqq \frac{{V_{OUT}}^2}{P_{O\_MIN}} = \frac{{V_{OUT}}^2}{\frac{{V_{IN(Max)}}^2}{2 \times L_P} \times {t_{ON\_MIN(Max)}}^2 \times \frac{1}{t_{ON\_MIN(Max)} + t_{OFF\_MAX(Min)}}}$$

In practice, even if R_{OUT} loads calculated by the above equation are used, the output voltage rises transiently during secondary discharging. Therefore, it should be set lower enough than this R_{OUT}. Adjust this resistance value in the actual evaluation. When selecting a resistor, pay attention to the rated power of the resistor.

Application Design Examples-continued

7. Snubber circuit

Excessive on the SW pin at turn-off when the degree of coupling of the transformer is low or the large current line of the board is long, etc.

Voltage may be applied.

To suppress this, use the snubber circuitry indicated by Figure 34.

This snubber circuit clamps the voltage when the flyback voltage + surge voltage exceeds this snubber voltage.

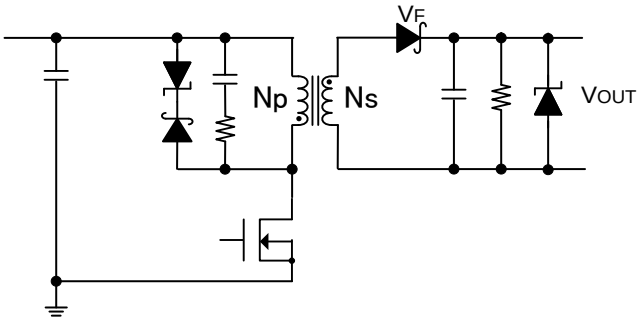


Figure 36. Snubber Circuit

The clamping voltage is determined by the following equation.

$$V_{CLAMP} = V_{F2} + V_z \quad [\mathrm{V}]$$

V_{CLAMP} : Clamp setting voltage of snubber

V_{F2} : Forward voltage of the Schottky diode

V_z : Zener voltage of the zener diode

At turn-off if the clamp setting voltage is lower than the flyback voltage $\frac{N_P}{N_S} \times (V_{OUT} + V_F)$

A current flows through the zener. Therefore, be sure to set a voltage higher than the flyback voltage.

In addition, the snubber circuit may not be clamped at the set clamping voltage because of its operational responsiveness.

Therefore, be sure to check the clamp voltage in actual operation.

8. SDX/EN terminal resistor

8.1 Setting Enable Voltage

After releasing VIN UVLO, Enable voltage V_{IN_ENABLE} can be set by the following equation.

$$V_{IN\_ENABLE} = V_{EN1} \times \frac{R_1 + (R_2 // R_{SDX/EN})}{R_2 // R_{SDX/EN}} \quad [\mathrm{V}]$$

V_{IN_ENABLE} : Target operations start VIN voltage

V_{EN1} : Enable volt1

$R_2 // R_{SDX/EN}$: Partial pressure resistance between R_2 and $R_{SDX/EN}$ inside the ICs

Application Design Examples-continued

8.2 Setting Disable Voltage

Disable voltage $V_{IN\_DISABLE}$ when the VIN pin voltage falls can be set by the following equation.

$$V_{IN\_DISABLE} = V_{EN2} \times \frac{R_1 + (R_2 // R_{SDX/EN})}{R_2 // R_{SDX/EN}} \quad [V]$$

$V_{IN\_DISABLE}$: Intended operation stop VIN voltage

V_{EN2} : Enable volt2

9 Output voltage compensation function using L_COMP pin resistor

The IC can compensate for the voltage drop in the output voltage V_{OUT} in response to the increase in I_P of the primary transformer peak current.

V_{OUT} changes can be caused by V_F variations in the secondary diodes or by leaking magnetic fluxes in the transformer.

An example of the output voltage compensation function is shown in Figure 35.

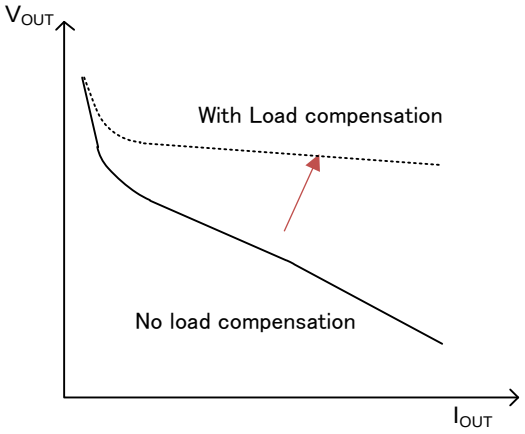


Figure 37. L_COMP voltage compensation example

This function compensates the output voltage by adding a $I_{REFCOMP}$ current to the REF current that determines the output voltage.

$$V_{OUT} = R_{FB} \times \frac{N_S}{N_P} \times \left(\frac{V_{INTREF}}{R_{REF}} + I_{REFCOMP}\right) - V_F \quad [V]$$

$\frac{V_{INTREF}}{R_{REF}} = 200\ \mu A\ (Typ)$ *Fixed value. $I_{REFCOMP}$ is incremented relative to the primary current.*

As a result, the output voltage is compensated according to the load current on the secondary side.

$I_{REFCOMP}$ is determined by the following equation.

$$I_{REFCOMP} = R_{L\_COMP} \times K_{L\_COMP} \times I_{SW(Ave)} \quad [\mu A]$$

R_{L_COMP} : Resistor connected to the L_COMP pin

$I_{SW(Ave)}$: Average current flowing through the SW pin

K_{L_COMP}: Fixed value inside the IC

9 Output Voltage Compensation by L_COMP Pin Resistor-continued

The mean current $I_{SW(Ave)}$ of the SW pin can be converted into the following equation.

$$I_{SW(Ave)} = I_{S(Ave)} \times \frac{N_S}{N_P} = I_{OUT} \times \frac{1}{\eta} \times \frac{N_S}{N_P} \quad [\mathrm{A}]$$

η: Efficiency (Designed at about 70% and adjust R_{L_COMP} in the application assessment.)

As shown in this equation, $I_{SW(Ave)}$ is proportional to I_{OUT}, so you can compensate for the above.
The compensation amount can be adjusted by the resistance value of the L_COMP pin.
Since I_{SW} is a triangle-wave current, always use a capacitor of 0.1 μF or more at the L_COMP pin to smooth this.
Please connect.

The resistor of the L_COMP pin is calculated by the following equation.

$$R_{L\_COMP} = \frac{I_{REFCOMP}}{I_{SW(Ave)}} \times \frac{1}{K_{L\_COMP}} \quad [\mathrm{k\Omega}]$$

Be sure to check the output voltage characteristics in the application evaluation and adjust the L_COMP terminal resistor as necessary.
When compensation is not performed, short the L_COMP pin to GND.

Revision history

Date	Plate	Content of change
1st.Aug.2022	001	New