ROHM Switching Regulator Solutions

Evaluation Board: Synchronous Buck Converter Integrated FET

BD9109FVMEVK-101 (3.3V | 0.8A Output)

No.000000000

- **Introduction**

  This application note will provide the steps necessary to operate and evaluate ROHM's synchronous buck DC/DC converter using the BD9109FVM evaluation boards. Component selection, board layout recommendations, operation procedures and application data is provided.

- **Description**

  This evaluation board has been developed for ROHM's synchronous buck DC/DC converter customers evaluating BD9109FVM. While accepting a power supply of 4.5-5.5V, an output of 3.3V can be produced. The IC has internal 350mohm Pch MOSFET and 250mohm Nch MOSFET and a fixed synchronization frequency of 1 MHz. A Soft Start circuit prevents in-rush current during startup along with UVLO (low voltage error prevention circuit) and TSD (thermal shutdown detection) protection circuits. An EN pin allows for simple ON/OFF control of the IC to reduce standby current consumption. Employs a current mode control system to provide faster transient response to sudden change in load.

- **Applications**

  Power supply for LSI including DSP, Microcomputer and ASIC

- **Evaluation Board Operating Limits and Absolute Maximum Ratings**

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Supply Voltage							
	BD9109FVM	V_{CC}	4.5	5	5.5	V	
Output Voltage / Current							
	BD9109FVM	V_{OUT}	3.234	3.300	3.366	V	
		I_{OUT}	-	-	0.8	A	

- **Evaluation Board**

  Below is evaluation board with the BD9109FVM.

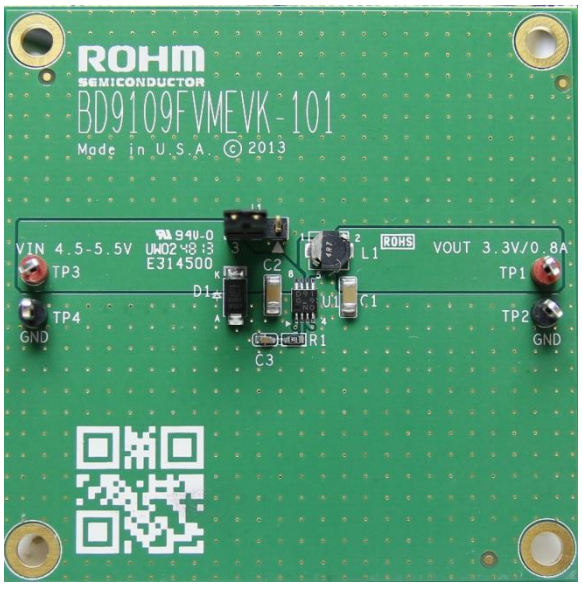

Fig 1: BD9109FVM Evaluation Board

- **Evaluation Board Schematic**

  Below is evaluation board schematic for BD9109FVM.

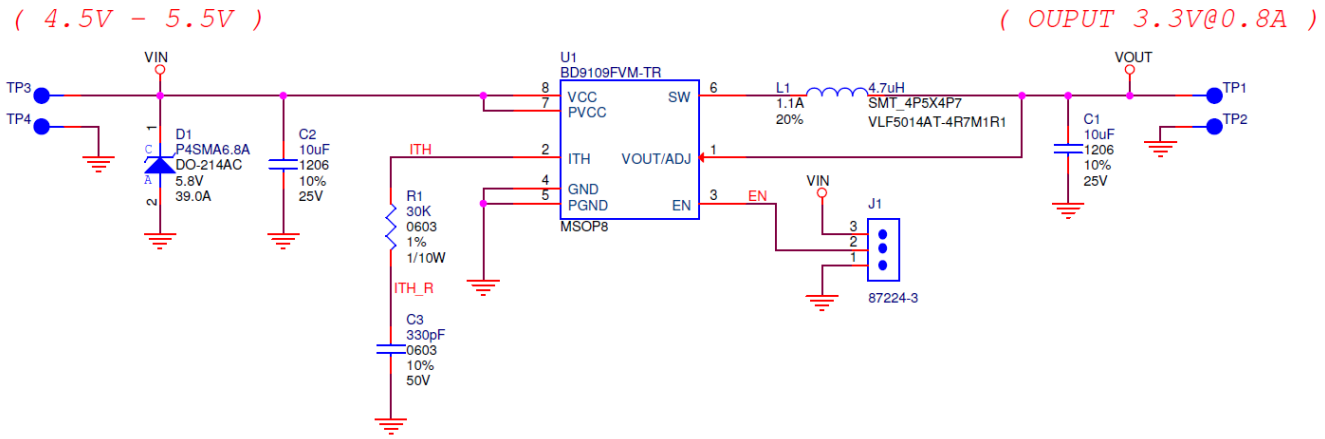

Fig 2: BD9109FVM Evaluation Board Schematic

- **Evaluation Board I/O**

  Below is reference application circuit that shows the inputs (V_{IN}, EN) and the output (V_{OUT}).

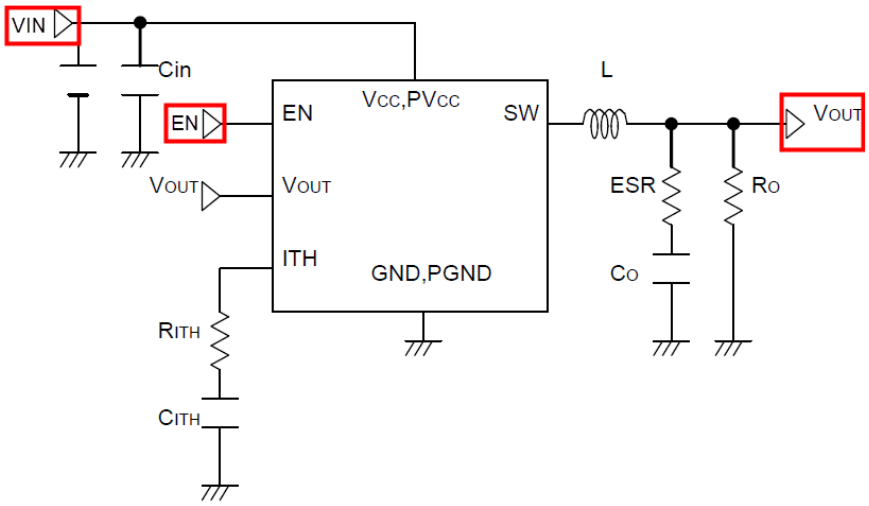

Fig 3: BD9109FVM Evaluation Board I/O

- **Evaluation Board Operation Procedures**

  Below is the procedure to operate the evaluation board.

  1. Connect power supply's GND terminal to GND test point TP4 on the evaluation board.
  2. Connect power supply's V_{CC} terminal to V_{IN} test point TP3 on the evaluation board. This will provide V_{IN} to the IC U1. Please note that the V_{CC} should be in range of 4.5V to 5.5V.
  3. Check if shunt jumper of J1 is at position ON (Pin2 connect to Pin3, EN pin of IC U1 is pulled high as default).
  4. Now the output voltage V_{OUT} (+3.3V) can be measured at the test point TP1 on the evaluation board with a load attached. The load can be increased up to 0.8A MAX.

- **Reference Application Data for BD9109FVMEVK-101**

  Following graphs show hot plugging test, quiescent current, efficiency, load response, output voltage ripple response of the BD9109FVM evaluation board.

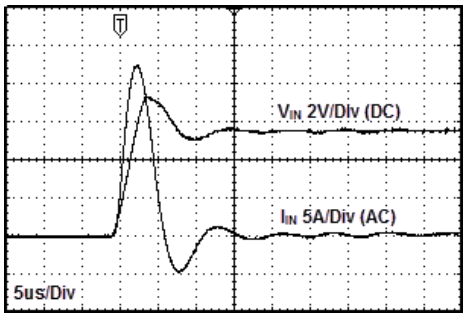

Fig 4: Hot Plug-in Test with Zener Diode SMAJ5.0A, V_{IN}=5.5V, V_{OUT}=3.3V, I_{OUT}=0.8A

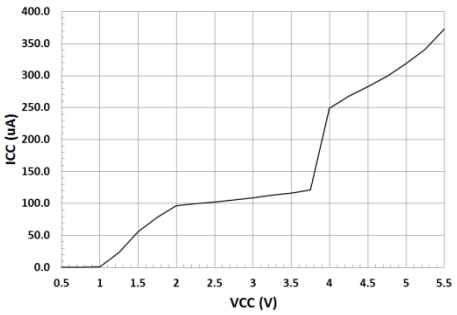

Fig 5: Circuit Current vs. Power supply Voltage Characteristics (Temp=25°C)

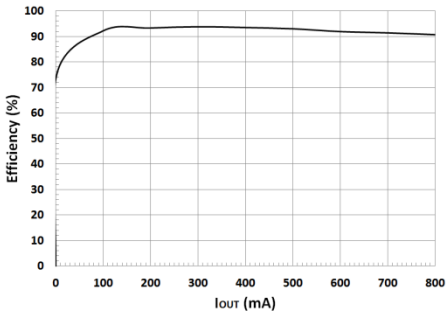

Fig 6: Electric Power Conversion Rate (V_{OUT}=3.3V)

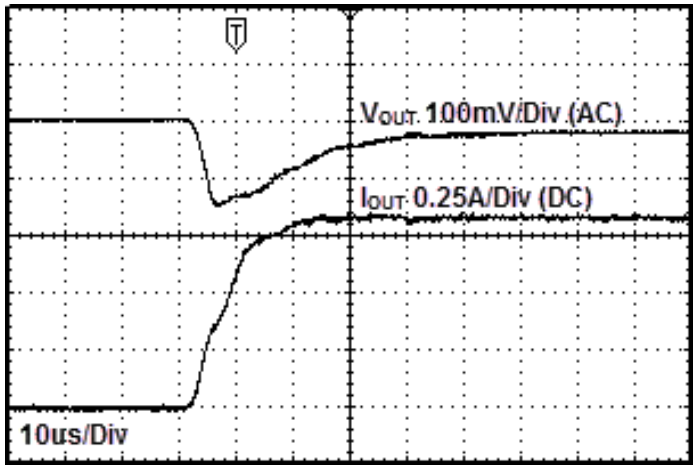

Fig 7: Load Response Characteristics (V_{IN}=5V, V_{OUT}=3.3V, L=4.7uH, C_{OUT}=10uF, I_{OUT}=0A→0.8A)

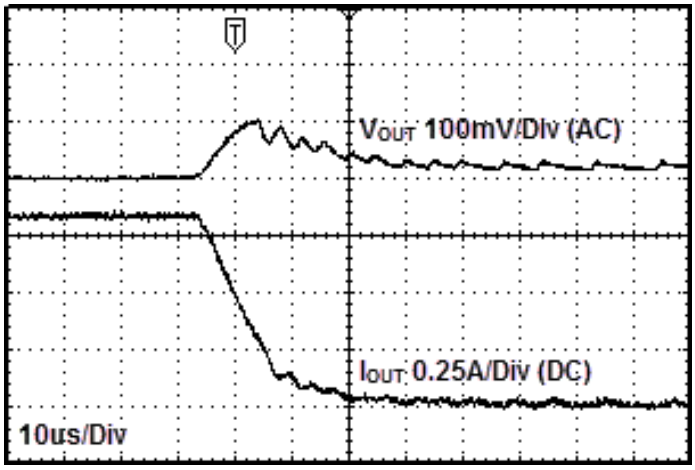

Fig 8: Load Response Characteristics (V_{IN}=5V, V_{OUT}=3.3V, L=4.7uH, C_{OUT}=10uF, I_{OUT}=0.8A→0A)

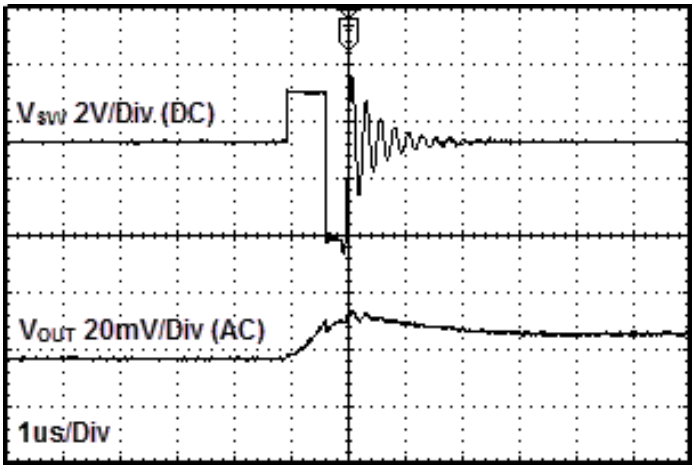

Fig 9: Output Voltage Ripple Response Characteristics (V_{IN}=5V, V_{OUT}=3.3V, L=4.7uH, C_{OUT}=10uF, I_{OUT}=0A)

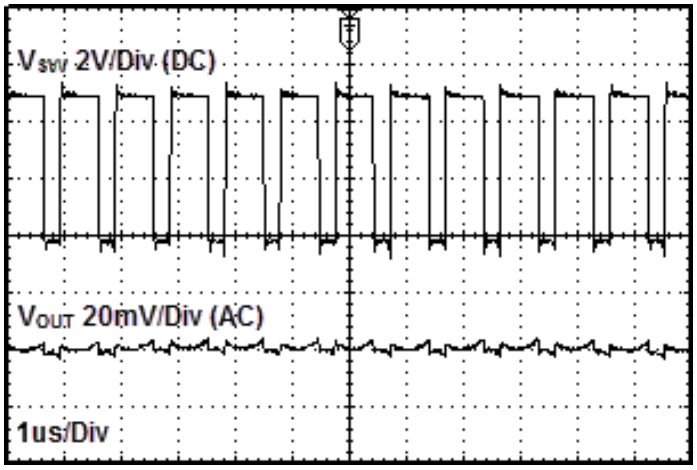

Fig 10: Output Voltage Ripple Response Characteristics (V_{IN}=5V, V_{OUT}=3.3V, L=4.7uH, C_{OUT}=10uF, I_{OUT}=0.8A)

- **Evaluation Board Layout Guidelines**

Below are the guidelines that have been followed and recommended for BD9109FVM designs.
Layout is a critical portion of good power supply design. There are several signals path that conduct fast changing currents or voltage that can interact with stray inductance or parasitic capacitance to generate nose or degrade the power supplies performance. To help eliminate these problems, the V_{CC} pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric.

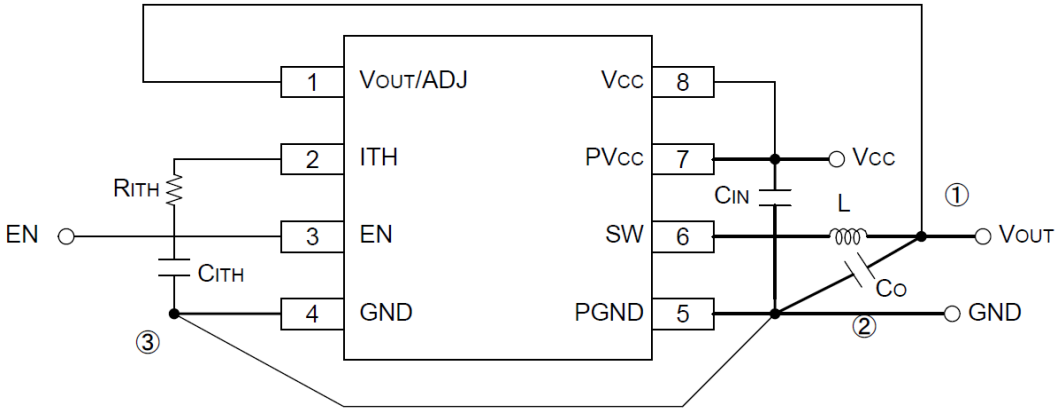

Fig 11: BD9109FVM Layout diagram

① For the sections drawn with heavy line, use thick conductor pattern as short as possible.
② Lay out the input ceramic capacitor C_{IN} closer to the pins PVCC and PGND, and the output capacitor C_O closer to the pin PGND.
③ Layout C_{ITH} and R_{ITH} between the pins ITH and GND as neat as possible with least necessary wiring.

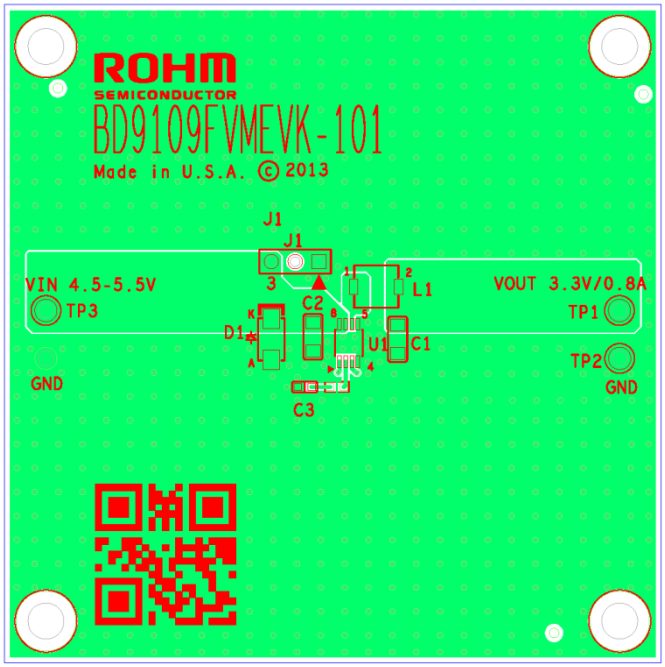

Fig 12: BD9109FVMEVK-101 PCB layout

- **Calculation of Application Circuit Components**

1. Selection of inductor (L)

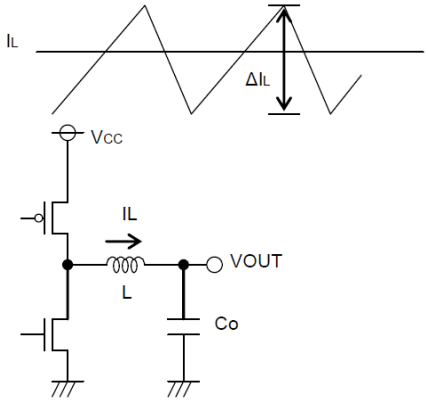

Fig 13: Output ripple current

The inductance significantly depends on output ripple current.
As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{L\times V_{CC}\times f}\ [A] \qquad (1)$$

Appropriate ripple current at output should be 30% more or less of the maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT\ MAX}\ [A] \qquad (2)$$

$$L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{\Delta I_L\times V_{CC}\times f}\ [H] \qquad (3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

* Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=5V, V_{OUT}=3.3V, f=1MHz, ΔI_L=0.3×0.8A=0.24A, for example

$$L = \frac{(5-3.3)\times 3.3}{0.24\times 5\times 1M} = 4.675[uH] \rightarrow 4.7[uH]$$

* Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

2. Selection of output capacitor (C_O)

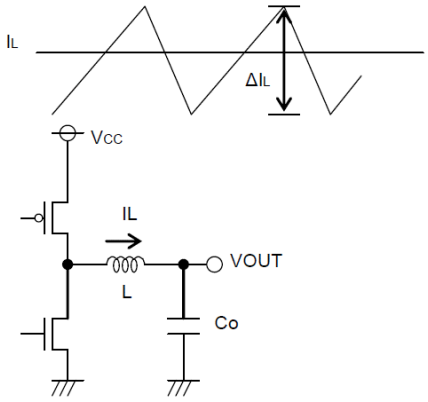

Fig 14: Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage. Output ripple voltage is determined by the equation (4):

$$\Delta V_{OUT} = \Delta I_L \times ESR\ [V] \qquad (4)$$

(ΔI_L: Output ripple current, and ESR: Equivalent series resistance of output capacitor)

* Rating of the capacitor should be determined allowing sufficient margin against output voltage. Less ESR allows reduction in output ripple voltage.

As the output rise time must be designed to fall within the soft-start time, the capacitance of output capacitor should be determined with consideration on the requirements of equation (5)

$$C_O \le \frac{T_{SS}\times(I_{LIMIT}-I_{OUT})}{V_{OUT}}\ [F] \qquad (5)$$

(T_{SS}: Soft-start time, I_{LIMIT}: Over current detection level, 2A [Typ])

For instance, and if V_{OUT}=3.3V, I_{OUT}=0.8A, and T_{SS}=1ms

$$C_O \le \frac{1m\times(2-0.8)}{3.3} = 364[uF]$$

Inappropriate capacitance may cause problem in startup. A 10uF to 100uF ceramic capacitor is recommended.

3. Selection of input capacitor (C_{IN})

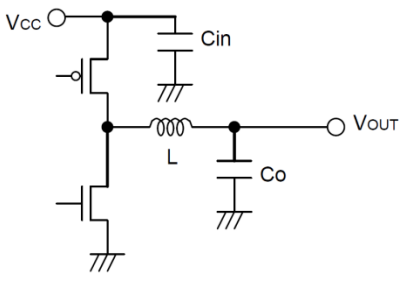

Fig 15: Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (6):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{CC}-V_{OUT})}}{V_{CC}}\ [A] \qquad (6)$$

< Worst case > $I_{RMS(max.)}$

When VCC is twice the V_{OUT}, $I_{RMS} = \frac{I_{OUT}}{2}$

If V_{CC}=5V, V_{OUT}=3.3V, and $I_{OUT\ max}$=0.8A,

$$I_{RMS} = 0.8 \times \frac{\sqrt{3.3(5-3.3)}}{5} = 0.38[A]$$

A low ESR 10uF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

4. Determination of R_{ITH}, C_{ITH} that works as a phase compensator

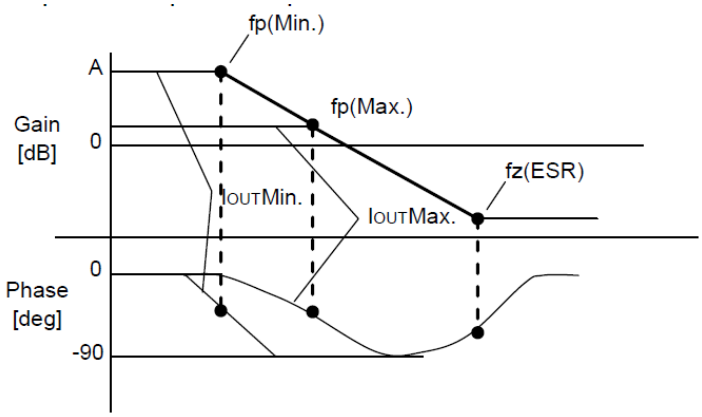

Fig 16: Open loop gain characteristics

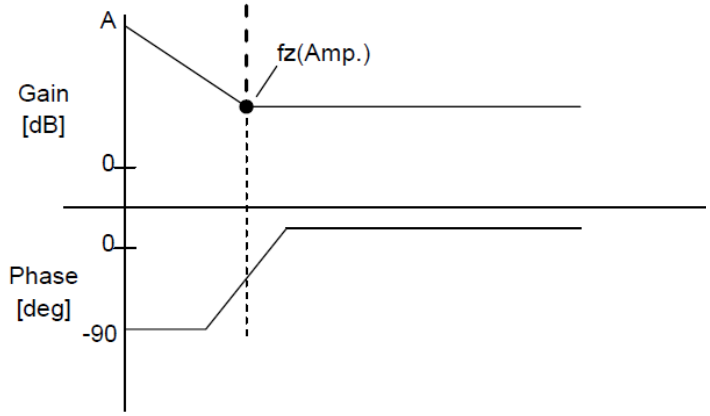

Fig 17: Error amp phase compensation characteristics

As the Current Mode Control is designed to limit a inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of a output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

$$\mathbf{fp} = \frac{1}{2\pi \times Ro \times Co}$$

$$\mathbf{fz(ESR)} = \frac{1}{2\pi \times ESR \times Co}$$

Pole at power amplifier

When the output current decreases, the load resistance R_O increases and the pole frequency lowers.

$$\mathbf{fp(Min.)} = \frac{1}{2\pi \times Romax \times Co}$$ [Hz] ← with lighter load

$$\mathbf{fp(Max.)} = \frac{1}{2\pi \times Romin \times Co}$$ [Hz] ←with heavier load

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$\mathbf{fz(Amp)} = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

Stable feedback loop may be achieved by canceling the pole fp (Min.) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

fx(Amp) = fp(Min)

$$\rightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times Romax \times Co}$$

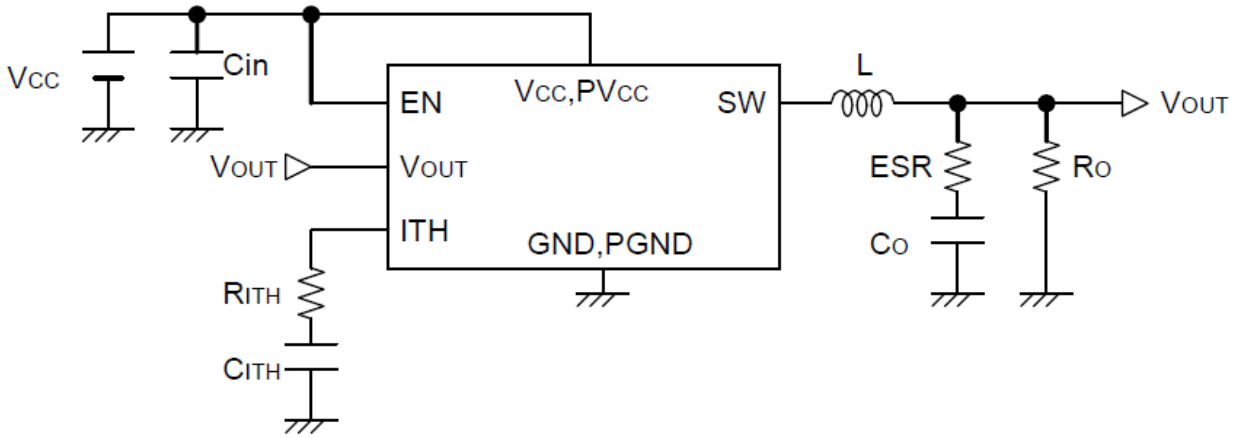

Fig 18: Typical application

- **Evaluation Board BOM**
  Below is a table with the build of materials. Part numbers and supplier references are provided.

Item	Qty.	Ref	Description	Manufacturer	Part Number
1	2	C1,C2	CAP CER 10UF 25V 20% X5R 1206	Murata	GRM31CR61E106MA12L
2	1	C3	CAP CER 330PF 50V 10% X7R 0603	Murata	GRM188R71H331KA01D
3	1	D1	DIODE TVS 400W 6.8V UNI 5% SMD	Littelfuse	P4SMA6.8A
4	1	J1	CONN HEADER VERT .100 3POS 15AU	TE Connectivity	87224-3
5	1	L1	INDUCTOR POWER 4.7UF 1.1A SMD	TDK Corporation	VLF5014AT-4R7M1R1
6	1	R1	RES 30K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF3002
7	2	TP1,TP3	TEST POINT PC MULTI PURPOSE RED	Keystone Electronics	5010
8	2	TP2,TP4	TEST POINT PC MULTI PURPOSE BLK	Keystone Electronics	5011
9	1	U1	IC REG BUCK SYNC 3.3V 0.8A 8MSOP	ROHM	BD9109FVM-TR
10	1		Shunt jumper for header J1 (item #4), CONN SHUNT 2POS GOLD W/HANDLE	TE Connectivity	881545-1