Automotive LED Driver Series

24-channel Constant Current Drivers and 8-line Switch Controllers Embedded Backlight LED Driver

BD94130MUF-M BD94130EFV-M

General Description

BD94130MUF-M/BD94130EFV-M are embedded 24-channel constant current drivers with 12bit PWM dimming and max 8-line switch controllers. This device can set LED constant current value by setting external ISET resistor. Communication with µ-controller via SPI is feasible.

Key Specification

- Power Supply Voltage Range: 3.0 V to 5.5 V
- LEDCHn Pin Voltage (n = 1 to 24): 20 V
- Maximum LED Output Current: 80 mA
- Operating Temperature Range: -40 °C to +125 °C

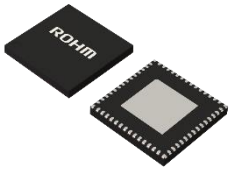
Features

- AEC-Q100 Qualified*(Note 1)*
- Functional Safety Supportive Automotive Products
- Integrated 24-channel LED Constant Current Drivers
- Integrated 4/6/8-line Switch Controllers
- SPI Interface (Cascade Connection Feasible)
- 12bit PWM Dimming
- LED Constant Current Setting by ISET Resistor
- Phase Shift Function
- 6bit Dot Correct (50 % to 100 %)
- LED Open Detection and LED Short Detection
- Adjacent LEDCH Short Detection
- PGATE Short Protection
- VINSW Over Voltage Protection
- Slew Rate Control for PMOS Gate Driver
- Abnormality Output FAILB Pin

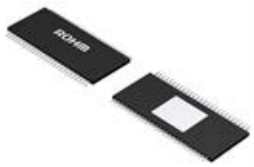
(Note 1) Grade 1

Package

	W (Typ) x D (Typ) x H (Max)
(BD94130MUF-M) VQFN56FCV080	8.0 mm x 8.0 mm x 1.0 mm
(BD94130EFV-M) HTSSOP-B54	18.5 mm x 9.5 mm x 1.0 mm



VQFN56FCV080

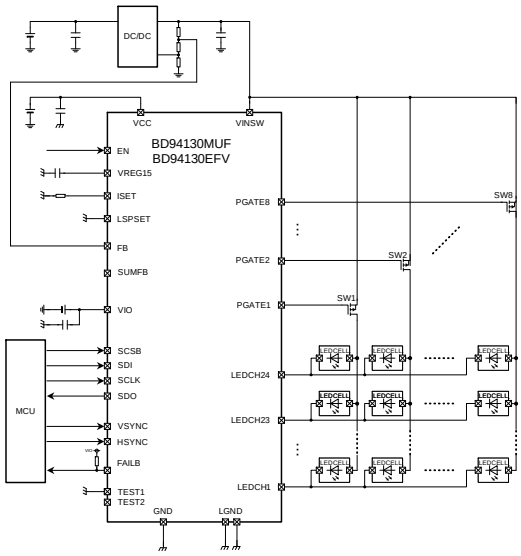


HTSSOP-B54

Application

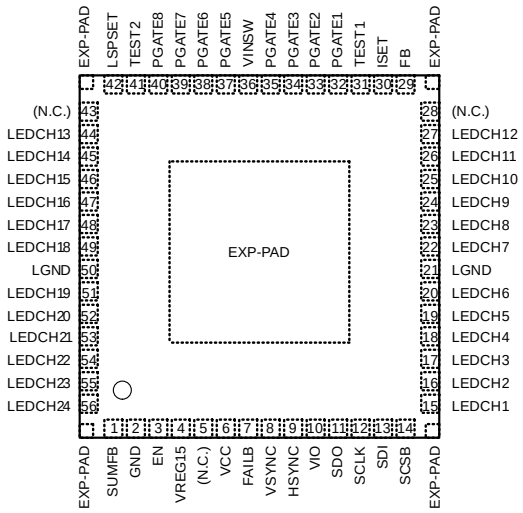
- Cluster, Center Infotainment Display
- Other Automotive Backlights

Typical Application Circuit

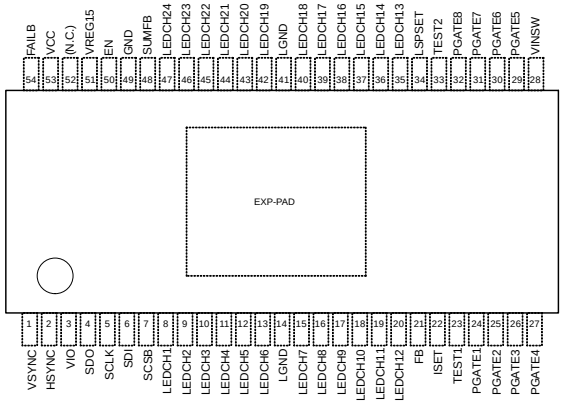


Pin Configuration

VQFN56FCV080 (TOP VIEW)



HTSSOP-B54 (TOP VIEW)



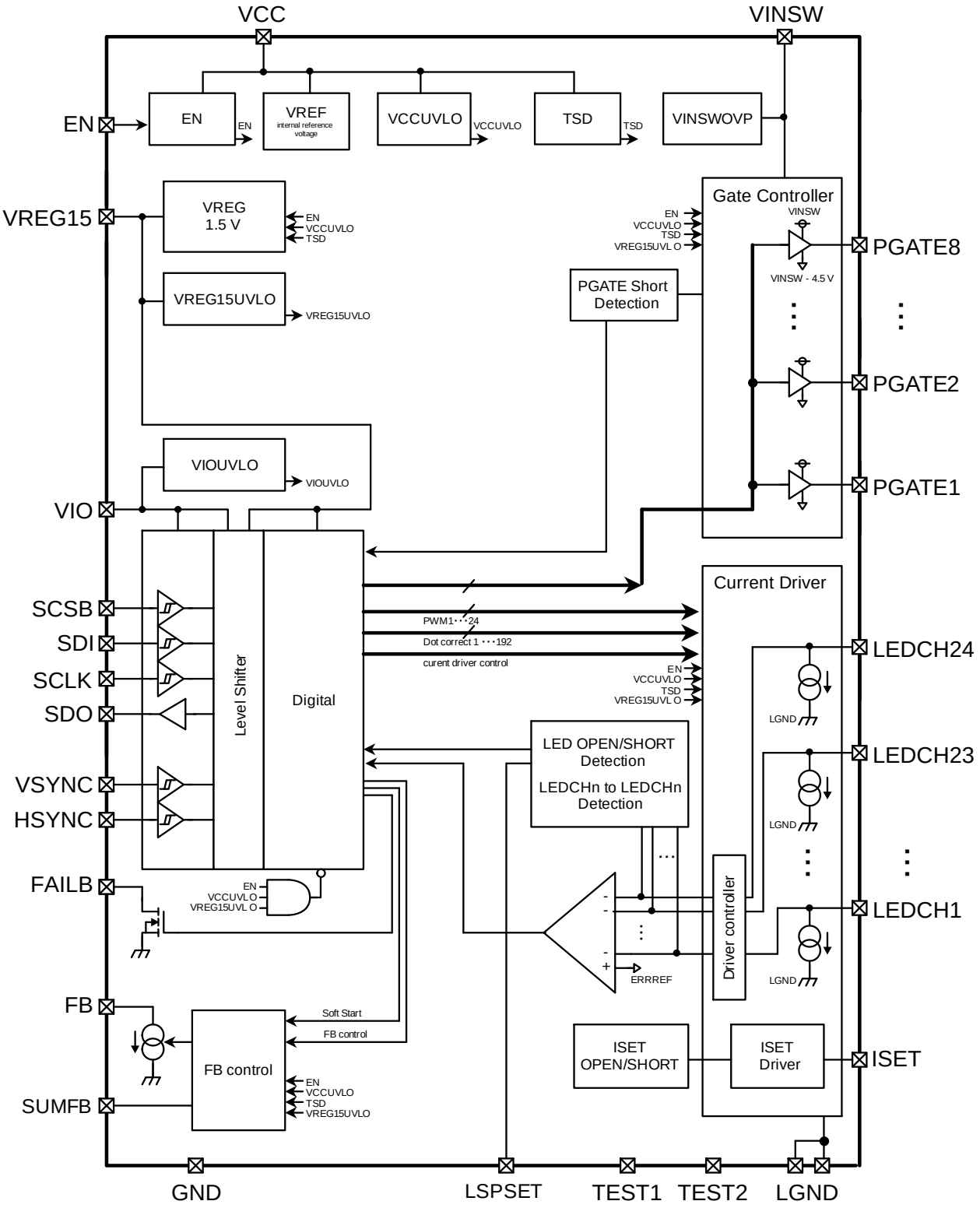
Pin Description

VQFN56FCV080	HTSSOP-B54	Pin Name	Function
1	48	SUMFB	Control DCDC feedback voltage
2	49	GND	Common GND
3	50	EN	Enable input pin
4	51	VREG15	Output of 1.5 V voltage regulator for digital block
6	53	VCC	Power supply pin
7	54	FAILB	Abnormal operation detection output pin
8	1	VSYNC	VSYNC signal input pin
9	2	HSYNC	HSYNC signal input pin
10	3	VIO	Power supply pin for I/O
11	4	SDO	SPI data output pin
12	5	SCLK	SPI CLK input pin
13	6	SDI	SPI data input pin
14	7	SCSB	SPI device select setting pin
15	8	LEDCH1	Output constant current channel 1
16	9	LEDCH2	Output constant current channel 2
17	10	LEDCH3	Output constant current channel 3
18	11	LEDCH4	Output constant current channel 4
19	12	LEDCH5	Output constant current channel 5
20	13	LEDCH6	Output constant current channel 6
21	14	LGND	Analog GND for constant current driver block
22	15	LEDCH7	Output constant current channel 7
23	16	LEDCH8	Output constant current channel 8
24	17	LEDCH9	Output constant current channel 9
25	18	LEDCH10	Output constant current channel 10

Pin Description – continued

VQFN56FCV080	HTSSOP-B54	Pin Name	Function
26	19	LEDCH11	Output constant current channel 11
27	20	LEDCH12	Output constant current channel 12
29	21	FB	Control external DCDC feedback voltage
30	22	ISET	LED constant current setting pin
31	23	TEST1	Test pin 1
32	24	PGATE1	Gate control 1 of external PMOS FET
33	25	PGATE2	Gate control 2 of external PMOS FET
34	26	PGATE3	Gate control 3 of external PMOS FET
35	27	PGATE4	Gate control 4 of external PMOS FET
36	28	VINSW	Power supply for gate controller block
37	29	PGATE5	Gate control 5 of external PMOS FET
38	30	PGATE6	Gate control 6 of external PMOS FET
39	31	PGATE7	Gate control 7 of external PMOS FET
40	32	PGATE8	Gate control 8 of external PMOS FET
41	33	TEST2	Test pin 2. Use this pin as an open pin.
42	34	LSPSET	LED short protection voltage setting for external adjustable
44	35	LEDCH13	Output constant current channel 13
45	36	LEDCH14	Output constant current channel 14
46	37	LEDCH15	Output constant current channel 15
47	38	LEDCH16	Output constant current channel 16
48	39	LEDCH17	Output constant current channel 17
49	40	LEDCH18	Output constant current channel 18
50	41	LGND	Analog GND for constant current driver block
51	42	LEDCH19	Output constant current channel 19
52	43	LEDCH20	Output constant current channel 20
53	44	LEDCH21	Output constant current channel 21
54	45	LEDCH22	Output constant current channel 22
55	46	LEDCH23	Output constant current channel 23
56	47	LEDCH24	Output constant current channel 24
-	-	EXP-PAD	The EXP-PAD is connected to GND

Block Diagram



Description of Blocks

If there is no description, the mentioned values are typical value.
The suffixes m of the symbol represent the number of gate control (m = 1 to 8), and the suffixes n represent the number of current driver (n = 1 to 24), respectively. For example, LEDCHn means LEDCH1, LEDCH2,,,LEDCH24. PGATEm means PGATE1, PGATE2,,,PGATE8. This expression is applicable to the whole of this datasheet.

1. Power Supply (VCC)

The VCC pin has UVLO function (VCCUVLO), and it starts operation at VCC ≥ 2.65 V (Typ) and stops operation at VCC ≤ 2.55 V (Typ). About the condition to release/detect VCC UVLO, refer to Table 53. Connect a ceramic capacitor (C_{VCC}) to the VCC pin for stable operation. C_{VCC} range is 1 µF to 22 µF and recommended value is 2.2 µF. If the C_{VCC} is not connected, unstable operation might occur e.g. oscillation.

2. Power Supply (VIO)

It supplies power to FAILB, SCSB, SCLK, SDI, SDO, VSYNC, and HSYNC input / output from the VIO pin. Connect a ceramic capacitor (C_{VIO}) to the VIO pin for stable operation. C_{VIO} range is 1 µF to 4.7 µF and recommended value is 2.2 µF. If the C_{VIO} is not connected, unstable operation might occur e.g. oscillation.

3. Power Supply (VINSW)

It supplies power to the output of PGATE1 to PGATE8 from the VINSW pin. Connect a ceramic capacitor (C_{VINSW}) to the VINSW pin to ensure stability of LED anode voltage. C_{VINSW} range is 1 µF to 100 µF and recommended value is 10 µF. If the C_{VINSW} value is not enough, the LED output might become unstable e.g. flicker.

4. Reference Voltage (VREG15)

VREG15 block generates 1.5 V from VCC, and outputs 1.5 V to the VREG15 pin. It supplies this power (V_{VREG15}) to the internal digital circuit. The VREG15 pin has UVLO function (VREG15UVLO), and it starts operation at V_{VREG15} ≥ 1.35 V (Typ) and stops operation at V_{VREG15} ≤ 1.30 V (Typ). It cannot be used to supply power to external components from this IC. About the condition to release/detect VREG15 UVLO, refer to Table 53. Connect a ceramic capacitor (C_{VREG15}) to the VREG15 pin for phase margin. C_{VREG15} range is 1 µF to 4.7 µF and recommended value is 2.2 µF. If the C_{VREG15} is not connected, unstable operation might occur e.g. oscillation.

5. Gate Controller

PGATEm pins connect to the gate of external PMOS transistors and this block controls power source timing to LED array. Each PGATEm pin turns on in order from PGATE1 to PGATE8 in one period of VSYNC. The number of PGATEm's ON in one period of VSYNC can be set by PWMFREQ register, refer to PWMFREQ register. PGATEm output HIGH level is V_{VINSW} (Typ) and its LOW level is V_{VINSW} – 4.5 V (Typ).

6. Current Driver

This device has integrated 24-channel constant current driver. Maximum LED current level I_{LEDMAX} (<80 mA) of all channels is set by the external resistor R_{ISET} of the ISET pin. The dot corrected current I_{LEDCHn} (50 % to 100 %) is set by the register IREVmn[5:0]. And the PWM dimming is set by the register DTYmn[11:0]. (m = 1 to 8, n = 1 to 24)

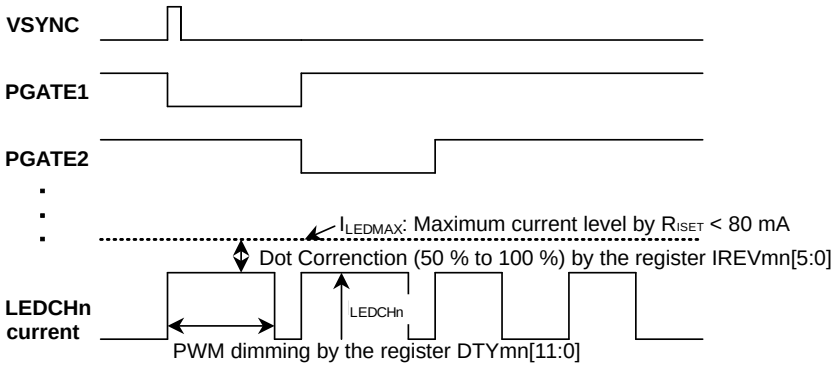


Figure 1. LED Current Setting Method for Dimming

6. Current Driver – continued

(1) Output Current Setting

I_{LEDMAX} and I_{LEDCHn} can be calculated by the following equation.
Recommended I_{LEDMAX} setting range is from 8.5 mA to 80 mA.

$$I_{LEDMAX} = \frac{1440k}{R_{ISET}} \qquad [mA]$$

where R_{ISET} is the external resistor value of the ISET pin.

$$I_{LEDCHn} = I_{LEDMAX} \times \frac{(IREVmn[5:0] + 64)}{127} \qquad [mA]$$

(2) Local PWM Dimming Control

PWM dimming frequency and pulse width are set by SPI commands. Constant current driver can be controlled synchronized to the internal signal PWMn (n = 1 to 24) for each channel set by SPI.
However, the constant current driver's minimum pulse width is limited to 0.6 µs. For example, in Matrix application with HSYNC frequency 8 MHz, 12bit resolution is minimum 125 ns in 8-line controller. The controllable range is from 5 to 4095.

The accurate average current of LEDCHn is expressed as follows, considering the deadtime of line controller.

$$I_{LED\_ave} = I_{LEDCHn} \times \sum_{m=1}^{8} (DTYmn + 1)/\{(4{,}096 + 32 \times 2^{NOOVLAP1} + 32 \times 2^{NOOVLAP2}) \times 8\} \qquad [mA]$$

where NOOVLAP1 = 0 to 3, NOOVLAP2 = 0 to 3, MULSEL = 0

(3) Delay Control

This IC integrates 12bit global delay function and 12bit local (each channel) delay function. In case HSYNC frequency is 8 MHz, the shift rate (global) can be set by 1.0 µs steps in 8-line controller.
If the length of the local delay and duty is more than the period, the remaining "ON" width is output at the next VSYNC period as shown on LEDCH24 of Figure 2. Refer to Delay Setting for details of this function.

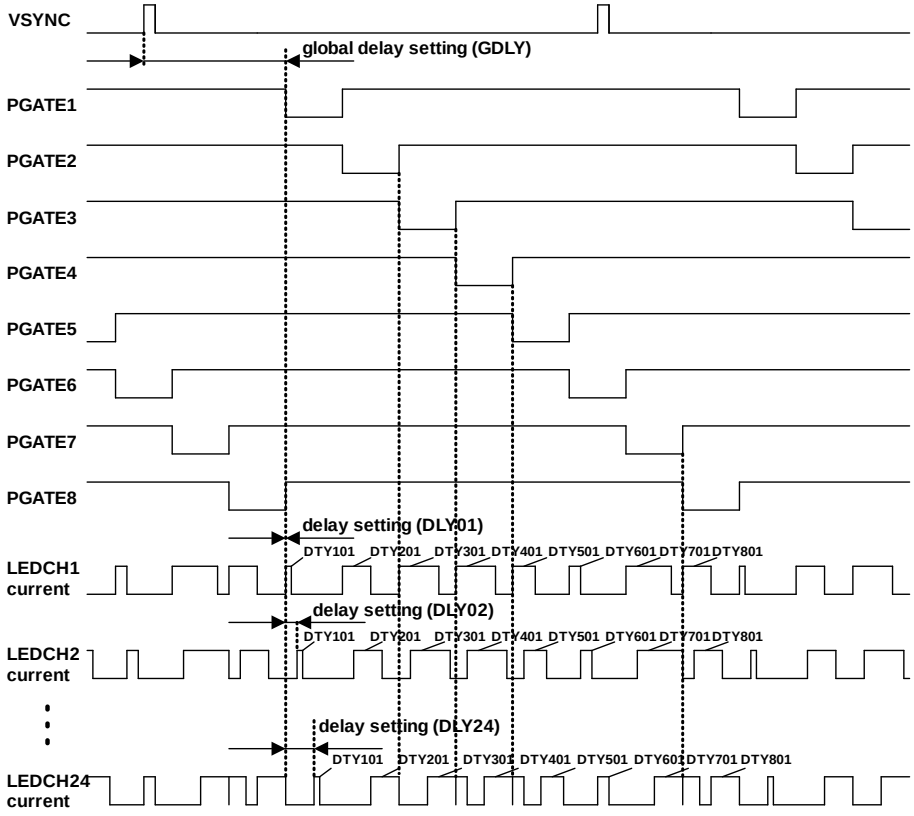


Figure 2. Delay Control

6. Current Driver - continued

(4) LED Open Detection, LED Short Detection

This IC has LED Open Detection and LED Short Detection.
When LED Open/Short is detected and PWM = HIGH, it outputs FAILB = LOW and the status of LED Open/Short Detection is updated.

LED Open Detection Voltage = V_{OPDET}
LED Short Detection Voltage = V_{SHDET}

(LED Short Detection Voltage can be set with SPI or the external resistor of the LSPSET pin. Refer to LEDSH resister)
This IC can automatically detect or release Error condition (FAILB output, Error register) during PWMn = HIGH. The error condition is retained during PWMn = LOW.

7. FB Control

DC/DC output and LEDCHn voltage is controlled by the FB pin. If the minimum LEDCHn voltage is lower than the Feedback Reference Voltage, the FB sink current increases. If the minimum LEDCHn voltage is higher than the Feedback Reference Voltage, the FB sink current decreases.
FB sink current is controlled by FBDAC[7:0]. The output is updated at the PGATE1 = ON in every VSYNC period indicated by Figure 4. The minimum step current is 0.78 µA (Typ) and maximum sink current is 200 µA (Typ). The resistor network between this device and DC/DC should be set appropriately by considering the current ability.
During the boot interval, the soft start function works. Please refer the register SSTIM[2:0] (Address 0x000: SRSST).

Table 1. Feedback Reference Voltage

LED Current Setting	FBREF[2:0] Register	Feedback Reference Voltage
8.5 mA to 20 mA	0x0	0.45 V
20 mA to 30 mA	0x1	0.53 V
30 mA to 40 mA	0x2	0.60 V
40 mA to 60 mA	0x3	0.75 V
60 mA to 80 mA	0x4 to 0x7	0.90 V

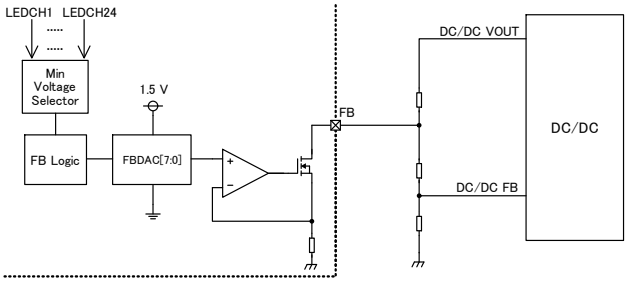


Figure 3. FB Control Block Diagram

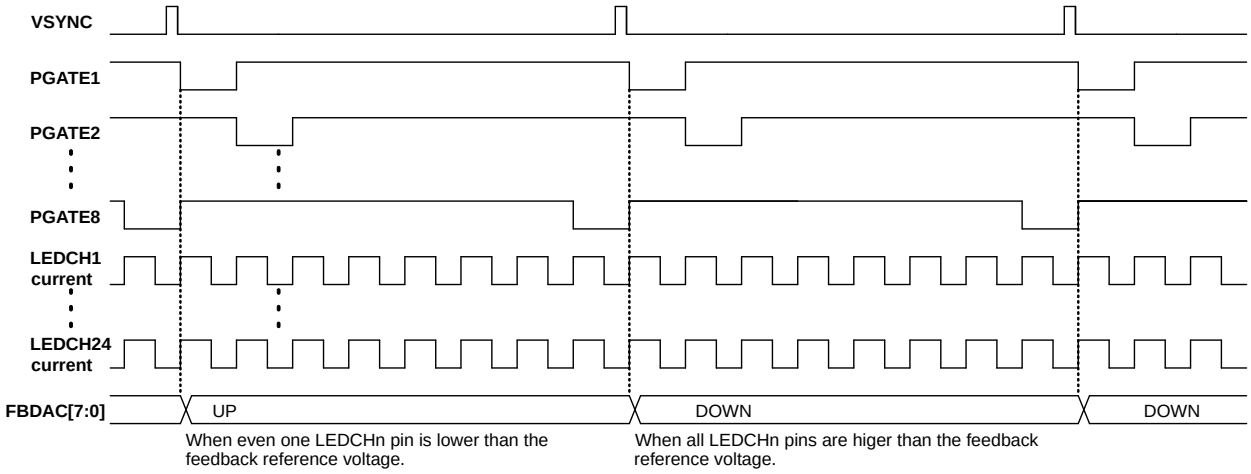


Figure 4. FB Control Timing

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage Range 1	V_{CC}	-0.3 to +7	V
Power Supply Voltage Range 2	V_{VIO}	-0.3 to +4	V
Power Supply Voltage Range 3	V_{VINSW}	-0.3 to +20	V
VREG15 Pin Voltage Range	V_{VREG15}	-0.3 to +1.65	V
LEDCHn Pin Voltage Range	V_{LEDCHn}	-0.3 to +20	V
PGATEm Pin Voltage Range	V_{PGATEm}	-0.3 to V_{VINSW}+0.3 ≤ +20	V
FAILB, ISET Pin Voltage Range	V_{FAILB}, V_{ISET}	-0.3 to +7	V
FB, TEST2 Pin Voltage Range	V_{FB}, V_{TEST2}	-0.3 to +20	V
EN, LSPSET, TEST1 Pin Voltage Range	V_{EN}, V_{LSPSET}, V_{TEST1}	-0.3 to V_{CC}+0.3	V
SCSB, SCLK, SDI, SDO, VSYNC, HSYNC, SUMFB Pin Voltage Range	V_{SCSB}, V_{SCLK}, V_{SDI}, V_{SDO}, V_{VSYNC}, V_{HSYNC}, V_{SUMFB}	-0.3 to V_{VIO}+0.3 ≤ +4	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum LED Output Current	I_{LEDCHn}	85*(Note 1)(Note 2)*	mA

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Wide VF variation of LED increases loss at the driver, which results in rise in package temperature. Therefore, the board needs to be designed with attention paid to heat radiation.

(Note 2) This current value is per 1ch. It needs be used within a range not exceeding power dissipation.

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN56FCV080				
Junction to Ambient	θ_{JA}	72.7	24.3	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	4.0	3.0	°C/W
HTSSOP-B54				
Junction to Ambient	θ_{JA}	55.8	20.6	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	4.0	2.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating Temperature	Topr	-40	-	+125	°C	
Power Supply Voltage 1	V_{CC}	3.0	5.0	5.5	V	
Power Supply Voltage 2	V_{VIO}	1.6	-	3.5	V	
Power Supply Voltage 3	V_{VINSW}	3	-	20	V	
VCC Pin Connection Capacitance	C_{VCC}	1.0	2.2	22.0	µF	
VIO Pin Connection Capacitance	C_{VIO}	1.0	2.2	4.7	µF	
VINSW Pin Connection Capacitance	C_{VINSW}	1	10	100	µF	
FB Pin Operation Voltage	V_{FB}	0	-	16	V	
VREG15 Pin Connection Capacitance	C_{VREG15}	1.0	2.2	4.7	µF	
ISET Resistance	R_{ISET}	18	-	170	kΩ	
HSYNC Frequency	f_{HSYNC}	-	-	20	MHz	
HSYNC Duty	$f_{HSYNCDUTY}$	40	-	60	%	
VSYNC Frequency (8-line switch controller)	f_{VSYNC1}	50	-	500	Hz	MULSEL = 0x0 PWMFREQ = 0
VSYNC Frequency (6-line switch controller)	f_{VSYNC2}	50	-	750	Hz	MULSEL = 0x2 PWMFREQ = 0
VSYNC Frequency (4-line switch controller)	f_{VSYNC3}	50	-	1000	Hz	MULSEL = 0x1 PWMFREQ = 0
VSYNC Minimum Pulse Width	$t_{VSYNCMIN}$	50	-	-	µs	
PWM Minimum Pulse Width	t_{PWMMIN}	0.6	-	-	µs	
LED Output Current 1	$I_{LEDMAX1}$	8.5	-	70.0	mA	3.0 V ≤ VCC < 5.5 V
LED Output Current 2	$I_{LEDMAX2}$	8.5	-	80.0	mA	3.5 V ≤ VCC < 5.5 V
LEDCHn Pin Connection Capacitance	C_{LEDCH}	0	-	0.1	µF	*(Note 1)*
LSPSET Pin Voltage	$V_{LSPSETDET}$	0.5	-	1.8	V	LSHEXT = 1
FAILB Pin Pull Up Resistance	R_{FAILB}	10	-	500	kΩ	

(Note 1) C_{LEDCH} affects the transient response of LEDCHn pin. Please check the LED current waveform of the narrow PWM duty, the time margin of the LED short detection, the short check of the adjacent LEDCHn pin, the pull up charge. Please refer the register ERRMASK (0x003), PRCEN (0x005), LEDSH (0x006), LSHEXE (0x006)

Electrical Characteristics
(Unless otherwise specified V_{CC} = 3.0 V to 5.5 V, V_{VINSW} = 10 V, V_{VIO} = 1.8 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Device Overview]						
VCC Circuit Current 1	I_{CCVCC1}	-	0	20	µA	EN = LOW HSYNC = LOW All Current driver OFF
VCC Circuit Current 2	I_{CCVCC2}	-	10.5	18.0	mA	VSYNC = 240 Hz HSYNC = 7,987,200 Hz MULSEL = 0 Duty = 50 %
VINSW Circuit Current 1	$I_{CCVINSW1}$	-	35	60	µA	EN = LOW
VINSW Circuit Current 2	$I_{CCVINSW2}$	-	220	400	µA	EN = HIGH, PGATEm = HIGH
VIO Circuit Current	I_{CCVIO}	-	0	5	µA	SCSB = HIGH, SDI = SCLK = VSYNC = HSYNC = LOW, EN = LOW
[VREG15 Block]						
VREG15 Pin Output Voltage	V_{VREG15}	1.400	1.470	1.540	V	I_{VREG15} = 0 mA
[PROTECT LOGIC Block]						
VCCUVLO Detection Voltage	$V_{VCCUVLO1}$	2.40	2.55	2.70	V	V_{CC} = SWEEP DOWN
VCCUVLO Release Voltage	$V_{VCCUVLO2}$	-	2.65	-	V	
VCCUVLO Hysteresis Voltage	$V_{VCCUHYS}$	50	100	200	mV	
VIOUVLO Detection Voltage	$V_{VIOUVLO1}$	1.31	1.41	1.51	V	V_{VIO} = SWEEP DOWN
VIOUVLO Release Voltage	$V_{VIOUVLO2}$	-	1.46	-	V	
VIOUVLO Hysteresis Voltage	$V_{VIOUHYS}$	30	50	90	mV	
VREG15UVLO Detection Voltage	$V_{VREG15UVLO}$	1.22	1.30	1.38	V	V_{VREG15} = SWEEP DOWN
LED Open Detection Voltage	V_{OPDET}	0.05	0.15	0.25	V	V_{LEDCHn} = SWEEP DOWN
LED Short Detection Voltage 1	V_{SHDET1}	2.6	3.0	3.4	V	V_{LEDCHn} = SWEEP UP LEDSH[1:0] = 0x0
LED Short Detection Voltage 2	V_{SHDET2}	5.6	6.0	6.4	V	V_{LEDCHn} = SWEEP UP LEDSH[1:0] = 0x1
LED Short Detection Voltage 3	V_{SHDET3}	8.6	9.0	9.4	V	V_{LEDCHn} = SWEEP UP LEDSH[1:0] = 0x2
LED Short Detection Voltage 4	V_{SHDET4}	11.6	12.0	12.4	V	V_{LEDCHn} = SWEEP UP LEDSH[1:0] = 0x3
LED Short Detection Voltage 5	$V_{LSPSETDET}$	7.6	8.0	8.4	V	V_{LSPSET} = 0.8 V LSHEXT = 1
LSPSET Pin Leak Current	$I_{LSPSETLEAK}$	-	0	1	µA	V_{LSPSET} = 0.8 V
ISET Pin GND Short Detection Resistance	R_{ISETSP}	-	-	16	kΩ	
ISET Pin Open Detection Resistance	$R_{ISETOPEN}$	340	-	-	kΩ	
VINSW Over Voltage Detection 1	$V_{VINSWOVP1}$	7.5	8.0	8.5	V	VINSWOVPREF[1:0] = 0x0
VINSW Over Voltage Detection 2	$V_{VINSWOVP2}$	11.4	12.0	12.6	V	VINSWOVPREF[1:0] = 0x1
VINSW Over Voltage Detection 3	$V_{VINSWOVP3}$	15.2	16.0	16.8	V	VINSWOVPREF[1:0] = 0x2
VINSW Over Voltage Detection 4	$V_{VINSWOVP4}$	17.1	18.0	18.9	V	VINSWOVPREF[1:0] = 0x3

Electrical Characteristics – continued
(Unless otherwise specified V_{CC} = 3.0 V to 5.5 V, V_{VINSW} = 10 V, V_{VIO} = 1.8 V, Ta = -40 °C to +125 °C)

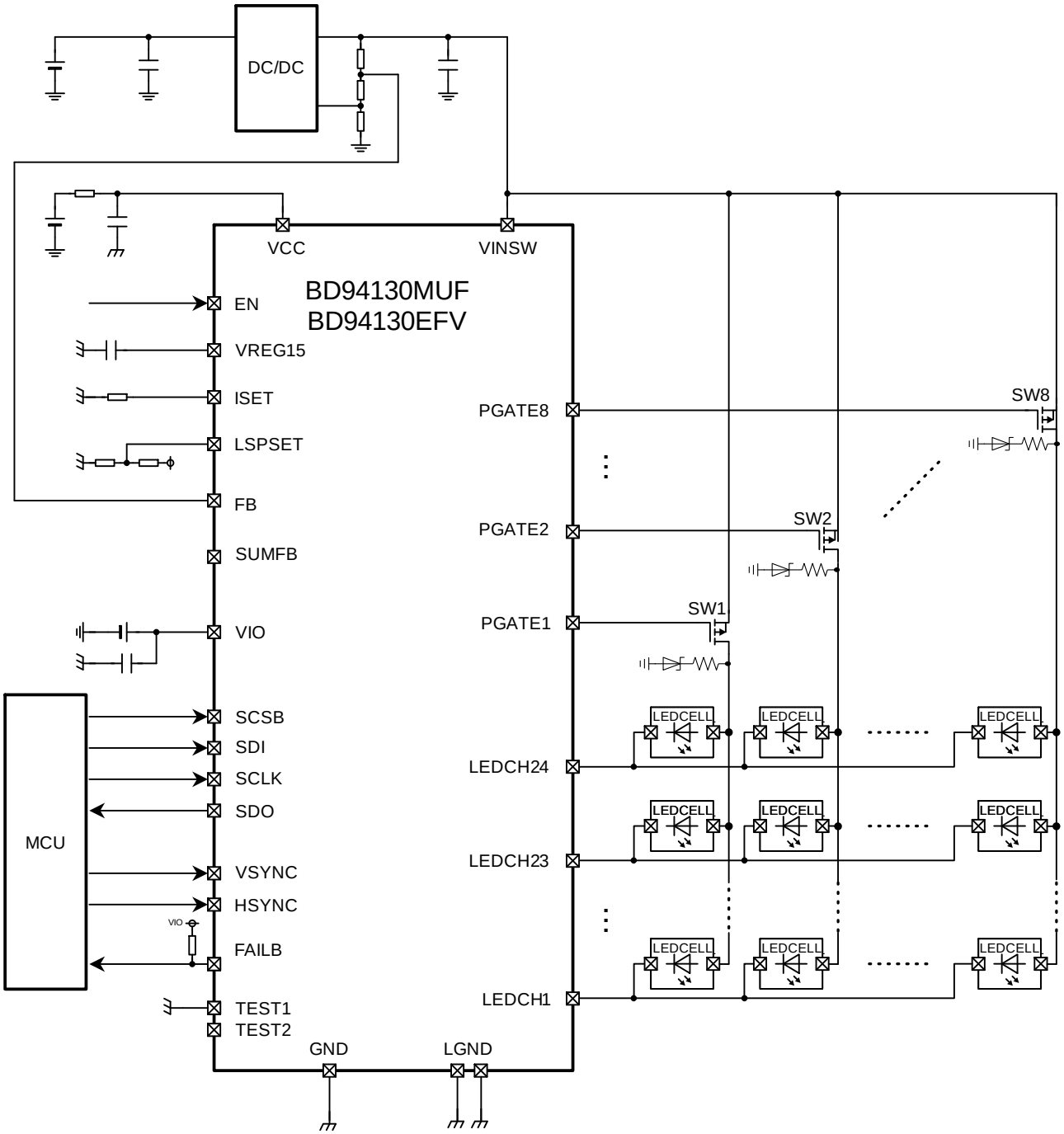
Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Constant Current Driver Block]						
ISET Voltage	V_{ISET}	1.38	1.50	1.62	V	
LEDCHn Pin ON Resistance	R_{LEDCHn}	-	4.5	9.0	Ω	
LED Output Current	I_{LEDCHn}	-	30	-	mA	ISET resistor = 48 kΩ PWM = 100 %
LED Output Current Error	ΔI_{LEDCHn}	-6	-	+6	%	ISET resistor = 48 kΩ PWM = 100 %
LED Constant Current Error1 (channel to channel)*(Note 1)*	ΔI_{LEDC1}	-6	-	+6	%	ISET resistor = 48 kΩ PWM = 100 %
Pull Up Voltage	V_{PULLUP}	VINSW-1.4	VINSW-1.2	VINSW-1.0	V	LED = OFF I_{LEDCHn} = -100 µA 3.5 V ≤ VINSW
[Feedback Control Block]						
Feedback Reference Voltage 1	V_{FB1}	0.36	0.45	0.54	V	FBREF[2:0] = 0x0
Feedback Reference Voltage 2	V_{FB2}	0.44	0.53	0.62	V	FBREF[2:0] = 0x1
Feedback Reference Voltage 3	V_{FB3}	0.50	0.60	0.70	V	FBREF[2:0] = 0x2
Feedback Reference Voltage 4	V_{FB4}	0.64	0.75	0.86	V	FBREF[2:0] = 0x3
Feedback Reference Voltage 5	V_{FB5}	0.78	0.90	1.02	V	FBREF[2:0] = 0x4 to 0x7
FB Maximum Sink Current	I_{FBMAX}	170	200	230	µA	FBDAC[7:0] = 0xFF V_{FB} = 2.0 V V_{LEDCHn} = 0.5 V
FB OFF Current	I_{FBOFF}	-	0	1	µA	V_{LEDCHn} = 1.2 V, EN = LOW
FB ON Resistance	R_{FB}	-	5.5	9.0	kΩ	
SUMFB ON Resistance	R_{SUMFBL}	10	160	290	Ω	I_{FAILB} = +1 mA
SUMFB Pull-up Resistance to VIO	R_{SUMFBH}	50	100	150	kΩ	
[Gate Controller Block]						
PGATEm PMOS ON Resistance	R_{PONR}	10	40	130	Ω	I_{PGATEm} = -1 mA to -5 mA
PGATEm NMOS ON Resistance 1	R_{NONR1}	50	100	200	Ω	I_{PGATEm} = +1 mA to +5 mA PGSRCNT[1:0] = 0x0
PGATEm NMOS ON Resistance 2	R_{NONR2}	1.0	1.4	2.5	kΩ	I_{PGATEm} = +10 µA to +500 µA PGSRCNT[1:0] = 0x1
PGATEm NMOS ON Resistance 3	R_{NONR3}	5	10	15	kΩ	I_{PGATEm} = +10 µA to +120 µA PGSRCNT[1:0] = 0x2
PGATEm NMOS ON Resistance 4	R_{NONR4}	50	100	200	kΩ	I_{PGATEm} = +1 µA to +12 µA PGSRCNT[1:0] = 0x3
PGATEm to VSINSW Short Detection Voltage 1	$V_{PGATEVIN1}$	VINSW-2.2	VINSW-1.5	-	V	VINSW = 10 V
PGATEm to GND Short Detection Voltage 1	$V_{PGATEGND1}$	-	VINSW-2.5	VINSW-0.8	V	VINSW = 10 V
PGATEm to VSINSW Short Detection Voltage 2	$V_{PGATEVIN2}$	VINSW-1.3	VINSW-1.0	-	V	VINSW = 3.5 V
PGATEm to GND Short Detection Voltage 2	$V_{PGATEGND2}$	-	VINSW-1.3	VINSW-0.8	V	VINSW = 3.5 V
PGATEm LOW Level	V_{LGATEm}	3.8	5.6	7.4	V	VINSW = 10 V
[LOGIC Input Block (SCSB, SCLK, SDI, VSYNC, HSYNC)]						
Input HIGH Voltage	V_{INH}	0.75 ×V_{VIO}	-	V_{VIO} +0.2	V	
Input LOW Voltage	V_{INL}	-0.2	-	0.2 ×V_{VIO}	V	
LOGIC Pins Input Current	I_{IN}	-	0	1	µA	V_{VIO} = 3.3 V LOGIC Input = 3.3 V

(Note 1)
$\Delta I_{LEDC1} = (I_{LEDn} / I_{LED\_AVE} - 1) \times 100$
I_{LEDn} is either pin of LED1 to LED24 current.
I_{LED_AVE} is the average current of LED1 to LED24.

Electrical Characteristics – continued
(Unless otherwise specified V_{CC} = 3.0 V to 5.5 V, V_{VINSW} = 10 V, V_{VIO} = 1.8 V, Ta = -40 °C to +125 °C)

[Input Pin (EN)]						
Input Pin HIGH Voltage	V_{ENH}	1.6	-	V_{CC}	V	
Input Pin LOW Voltage	V_{ENL}	-0.2	-	+0.4	V	
Pin Input Current	I_{EN}	-	33	60	µA	V_{EN} = 3.3 V
[Input Pin (TEST1)] Typical Condition						
Input Pin HIGH Voltage	V_{TEST1H}	1.6	-	V_{CC}	V	
Input Pin LOW Voltage	V_{TEST1L}	-0.2	-	+0.4	V	
[LOGIC Output Block (SDO)]						
Output HIGH Voltage	V_{OUTH}	V_{VIO} -0.2	-	V_{VIO}	V	I_{OL} = -1 mA
Output LOW Voltage	V_{OUTL}	-	-	0.2	V	I_{OL} = +1 mA
[FAILB Output Block]						
FAILB Pin ON Resistance	R_{FAILB}	10	110	230	Ω	I_{FAILB} = +1 mA
FAILB Pin Leak Current	$I_{LEAKFAILB}$	-	0	1	µA	V_{FAILB} = 5.0 V

Application Example



Functions of Logic Block

1. Serial Interface and AC Electrical Characteristics

Serial Peripheral Interface (SPI) controls the IC with SCSB, SCLK, SDI, and SDO signals.
Start the SPI communication with the initial value of SCSB is HIGH, and that of SCLK and SDI is LOW.
When using several devices, connect the SDO pin to the SDI pin of the next device to make cascade connection. SDO signal outputs the SDI input after 16 SCLK pulses. Example of the N address write is shown in the following.
The initial value of SDO is LOW, until it is used to output the signal.

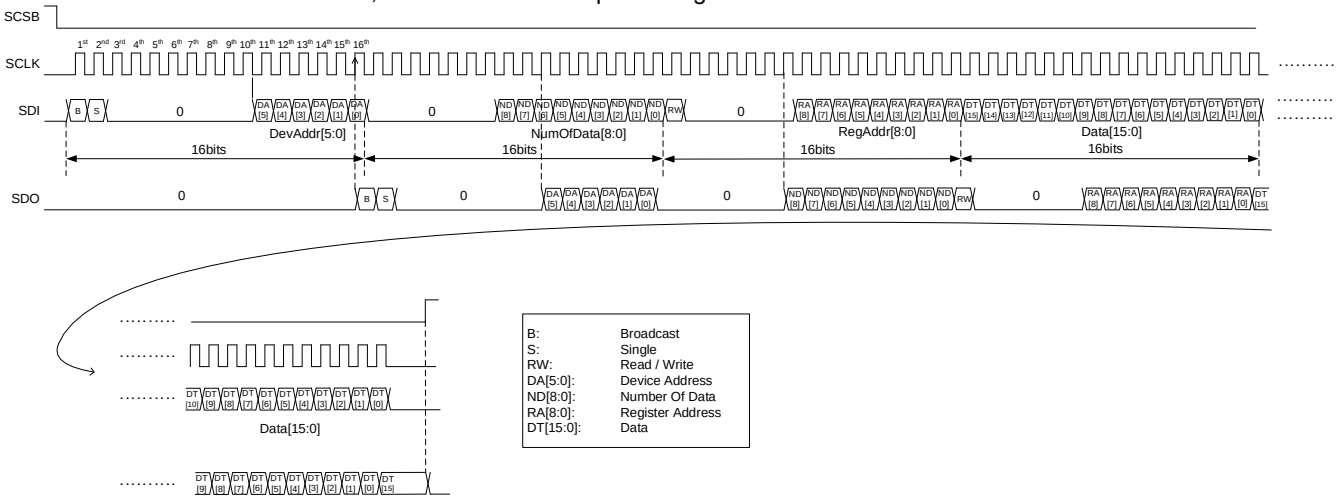


Figure 5. SPI Protocol (Write)

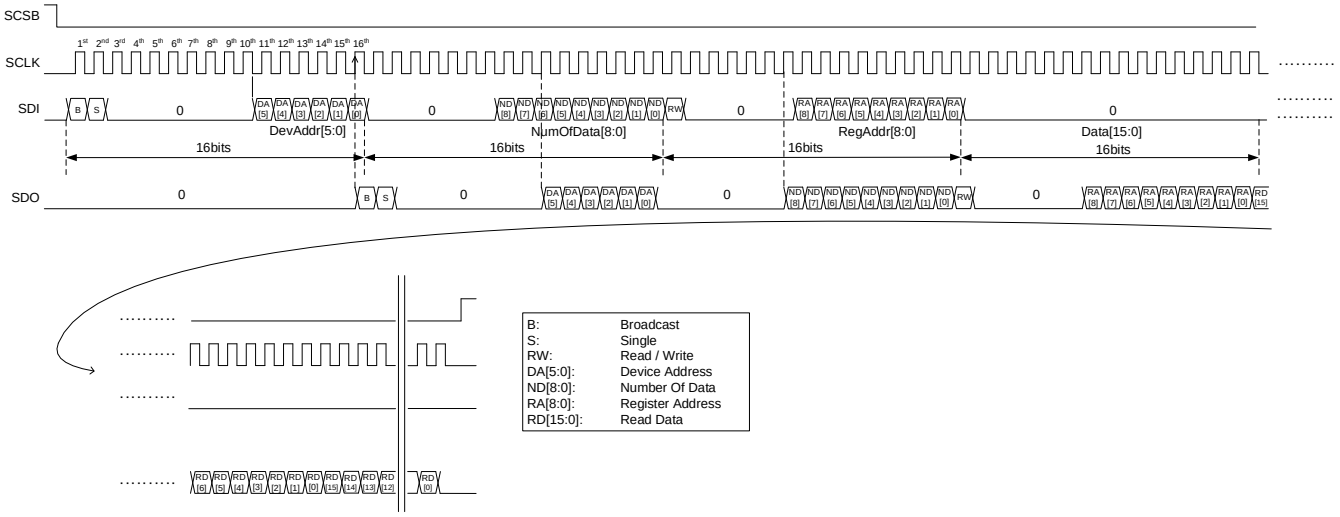
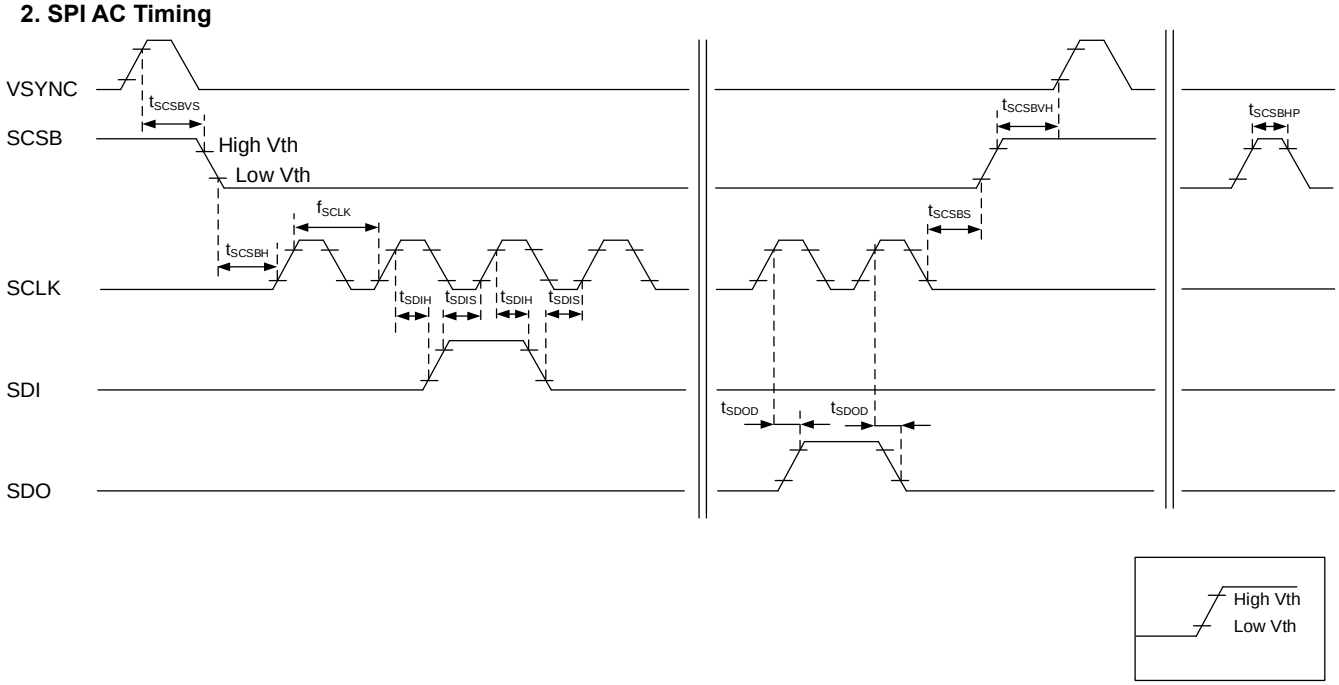


Figure 6. SPI Protocol (Read)

Functions of Logic Block – continued

2. SPI AC Timing



SPI Recommended Operation Condition
(Unless otherwise specified Ta = -40 °C to +125 °C, V_{VIO} = 1.8 V, V_{CC} = 3.0 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SCLK}	0.1	-	20	MHz
SCLK Duty	$f_{SCLKDUTY}$	45	-	55	%
SDI Input Setup Time	t_{SDIS}	10	-	-	ns
SDI Input Hold Time	t_{SDIH}	10	-	-	ns
SCSB Input Setup Time	t_{SCSBS}	100	-	-	ns
SCSB Input Hold Time	t_{SCSBH}	100	-	-	ns
SDO Output Delay Time	t_{SDOD}	-	-	40	ns
SCSB HIGH Pulse Width	t_{SCSBHP}	1000	-	-	ns
SCSB Setup Time for VSYNC	t_{SCSBVS}	10	-	-	µs
SCSB Hold Time for VSYNC	t_{SCSBVH}	10	-	-	µs
Cascade Connection Number	$N_{CASCADE}$	-	-	20	pcs

(Note) Do not input VSYNC pulse during SCSB = LOW (Output load capacitance: 15 pF)

The maximum frequency of the HSYNC and VSYNC is described in the previous section “Recommended Operating Conditions”.

Functions of Logic Block – continued

3. SPI Connection

(1) Cascade Connection

Each device can be controlled by connecting the SCLK and the SCSB pins to all devices in parallel, and by connecting each SDO to the SDI of the next device in series. The maximum number of devices that can be cascaded is 20.

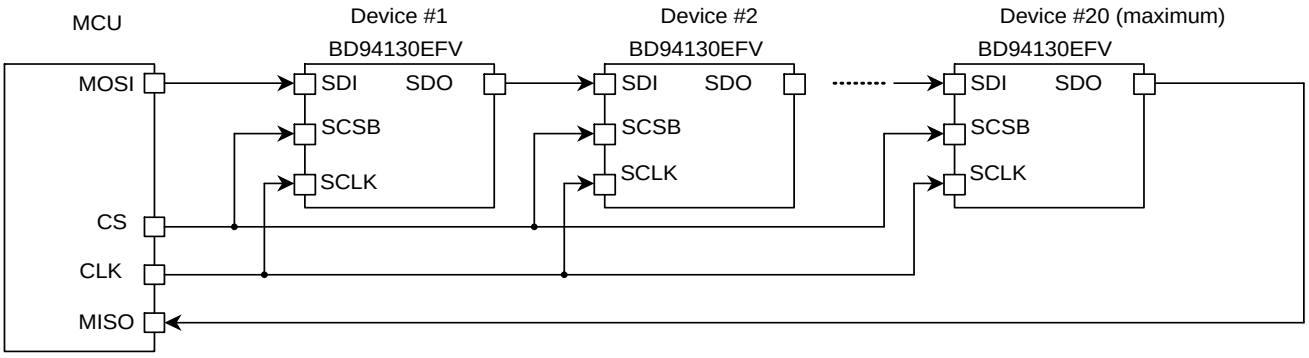


Figure 7. Image of Cascade Connection

(2) Individual Connection

Each device can be controlled by connecting the SCLK and the SDI pins to all devices in parallel, and by connecting each SCSB.

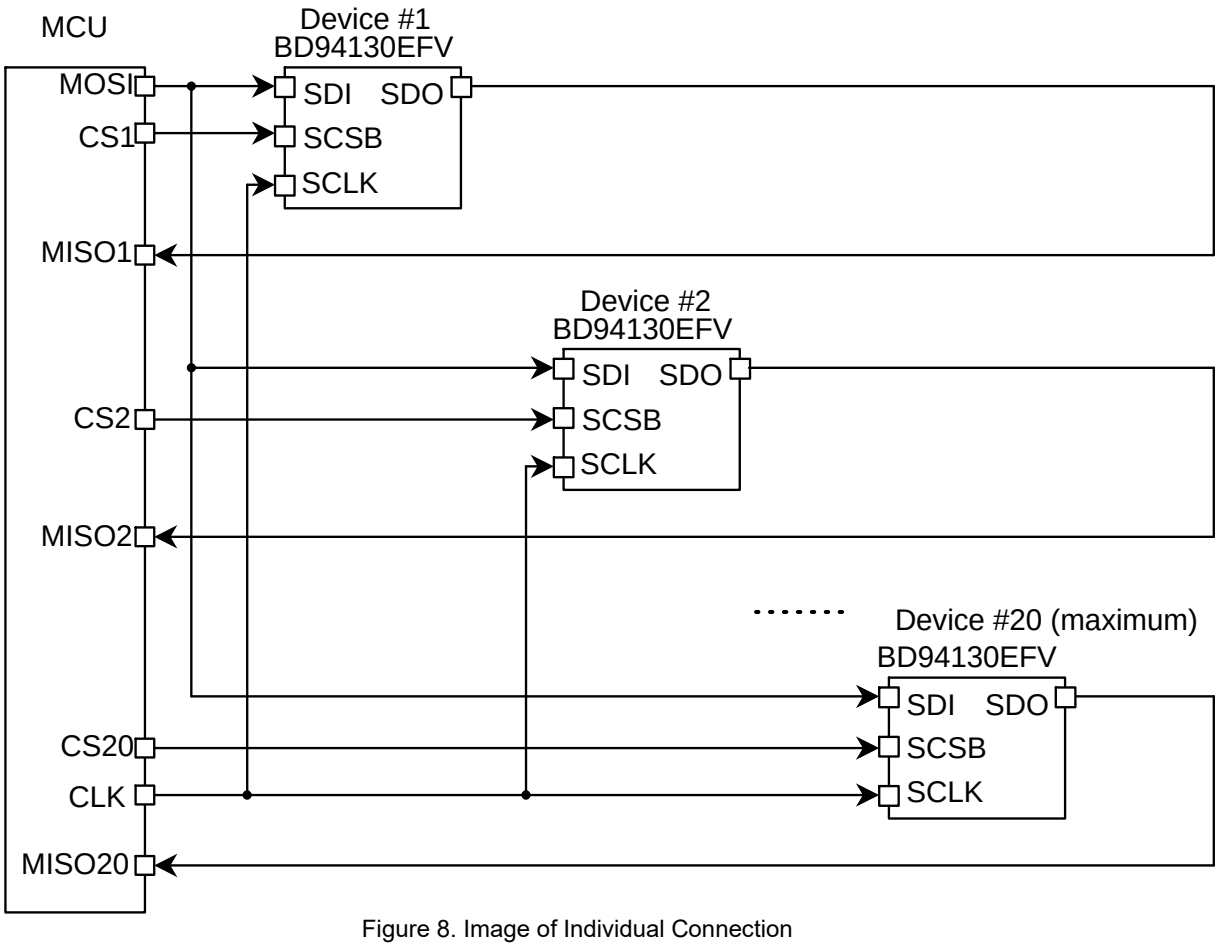


Figure 8. Image of Individual Connection

Functions of Logic Block – continued

4. SPI Data Flow

MCU Write and Read flow is shown as follow. This IC has 4 timing schemes for updating the analog control data.

Type 1 (immediately): Data is updated after SPI access.
Type 2 (VSYNC): Data is updated after SPI access and VSYNC rising edge.
Type 3 (VSYNC+GDLY): Data is updated after SPI access and VSYNC rising edge and GDLY.
Type 4 (PWM): Data is updated after SPI access and VSYNC rising edge and PWM timing.

So there is mismatch between Read data and Control data.

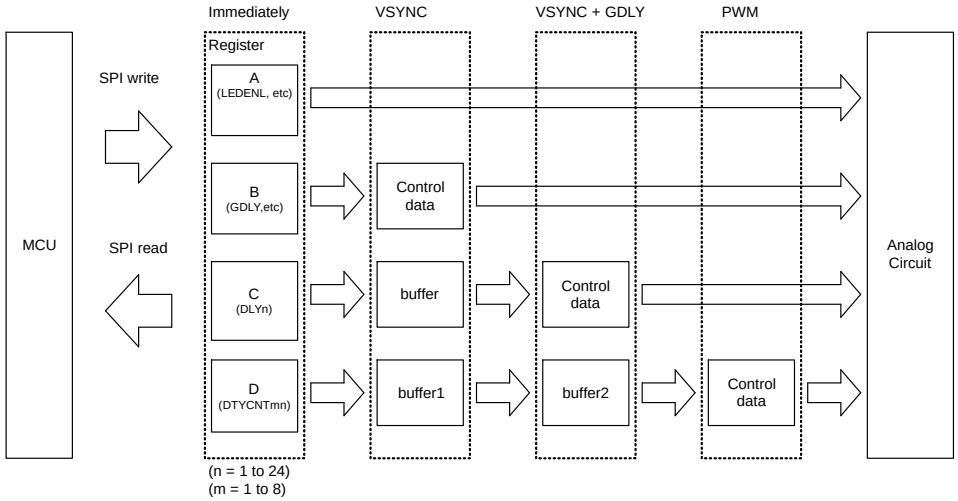


Figure 9. SPI Data Flow

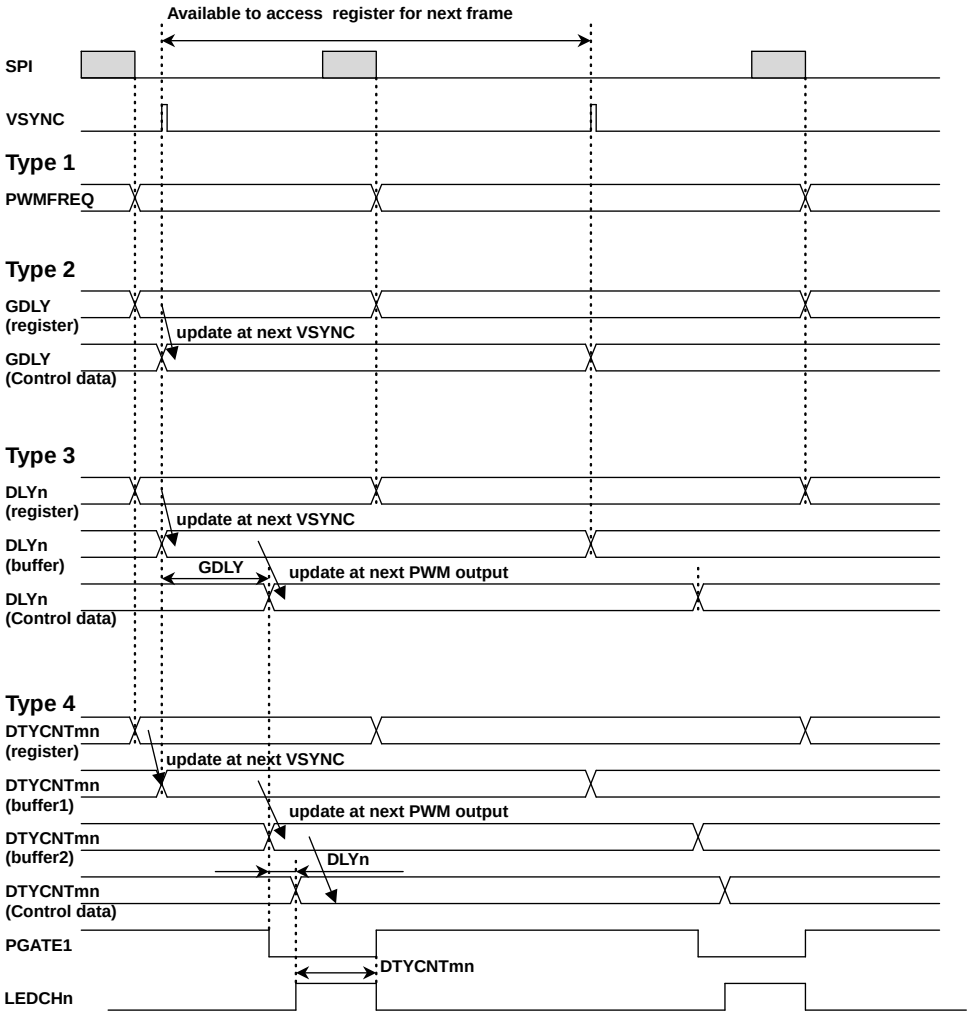


Figure 10. SPI Data Flow Timing

Functions of Logic Block – continued

5. SPI Protocol

(1) Device Address

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B	S	0								DevAddr[5:0]					

Bit	Parameter	Value
B	Broadcast	B = 1: All devices receive the data (Write only / No Read) B = 0: Write / Read to the Device that assigned by DevAddr[5:0]
S	Single	S = 1: 1 address Write / Read mode S = 0: Block Write / Read mode
DevAddr[5:0]	Device Address	0x00: Write the same data to the same RegAddr[8:0] of all devices (provided, B = 1) 0x01 to 0x14: Device Address 0x3F: Write the different data to the same RegAddr[8:0] of all devices (provided, B = 1)

DevAddr[5:0] of each device is calculated by counting the number of byte of 0x0000 data after the fall-edge of SCSB. When the received DevAddr[5:0] matches with the calculated DevAddr[5:0] of the device, Write/Read function occurs. When the received DevAddr[5:0] does not match the calculated DevAddr[5:0] of the device, the data is not received and is output to SDO. Refer to each protocol for the details.

(2) Number of Transferred Byte when Block Write/Read

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0							NumOfData[8:0]								

Bit	Parameter	Value
NumOfData[8:0]	Number of transferred data	0x002 to 0x16B

Transferred byte number = NumOfData[8:0]

5. SPI Protocol – continued

When S = 0 (Block Write / Read) of DevAddr[5:0], set the number of transferred byte (NumOfData) after DevAddr[5:0].
When S = 1, it skip this packet. (“Device Address” -> “Register Address” -> ….)
Please access this IC using the settings as shown in Table 2 and Table 3.

Table 2. Access Table for Write (RW = 0)

SPI Setting				Access to Devices			Acceptable *(Note)*
B	S	DevAddr[5:0]	NumOfData[8:0]	For Single Device	For All Device		
					Same Data	Different Data	
0	0	0x00	0x002 to 0x147	-	-	-	X
		0x01 to 0x14		O	-	-	O
		0x15 to 0x3F		-	-	-	X
	1	0x00	Not sending this data	-	-	-	X
		0x01 to 0x14		O	-	-	O
		0x15 to 0x3F		-	-	-	X
1	0	0x00	0x002 to 0x147	-	O	-	O
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	O	O
	1	0x00	Not sending this data	-	O	-	O
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	O	O

(Note) X: This setting is not acceptable. Do not set this condition

Table 3. Access Table for Read (RW = 1)

SPI Setting				Access to Devices			Acceptable *(Note)*
B	S	DevAddr[5:0]	NumOfData[8:0]	For Single Device	For All Device		
					Same Data	Different Data	
0	0	0x00	0x002 to 0x16B	-	-	-	X
		0x01 to 0x14		O	-	-	O
		0x15 to 0x3F		-	-	-	X
	1	0x00	Not sending this data	-	-	-	X
		0x01 to 0x14		O	-	-	O
		0x15 to 0x3F		-	-	-	X
1	0 / 1	0x00	0x002 to 0x16B	-	-	-	X
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	-	X

(Note) X: This setting is not acceptable. Do not set this condition.

5. SPI Protocol – continued

(3) Register Address

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RW	0						RegAddr[8:0]								

Bit	Parameter	Value
RW	Read / Write	RW = 0: Write the registers RW = 1: Read the registers
RegAddr[8:0]	Register Address	0x000 to 0x16B

(4) Data

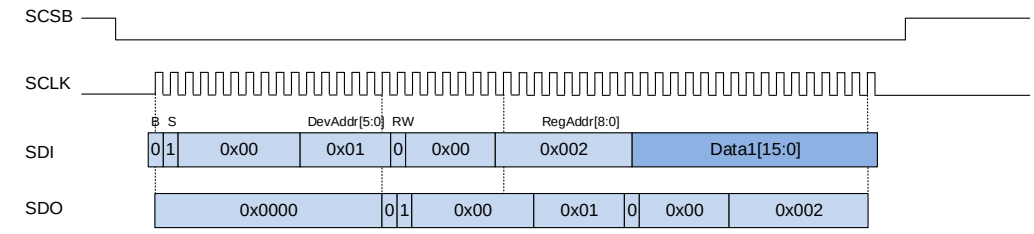
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data[15:0]															

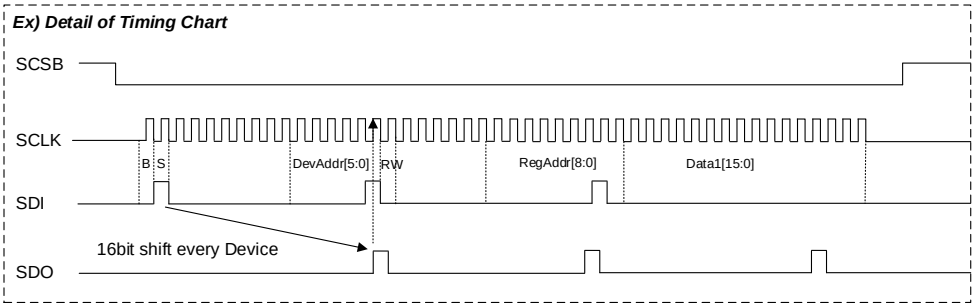
Bit	Parameter	Value
Data[15:0]	Data	0x0000 to 0xFFFF

(5) Single Device, 1 Address Write (Write to Device #1)

B = 0: Target device receives the data
S = 1: Single
DevAddr[5:0] = 0x01: Target device address
NumOfData[8:0] = -: 1 address access
RW = 0: Write
RegAddr[8:0] = 0x002: Address

SDI: Transfer in the order of DevAddr[5:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.





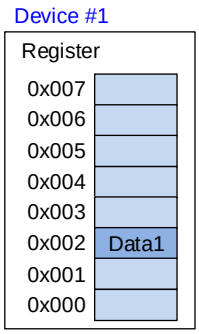


Figure 11. SPI Protocol for 1 Address Write to Device #1

5. SPI Protocol – continued

(6) Single Device, 1 Address Write (Write to Device #3)

B =	0:	Target device receives the data
S =	1:	Single
DevAddr[5:0] =	0x03:	Target device address
NumOfData[8:0] =	-:	1 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

DevAddr[5:0] of each device is calculated by counting the number of byte of 0x00 data after the falling-edge of SCSB.
DevAddr[5:0] = (Number of byte of 0x00 data) + 1

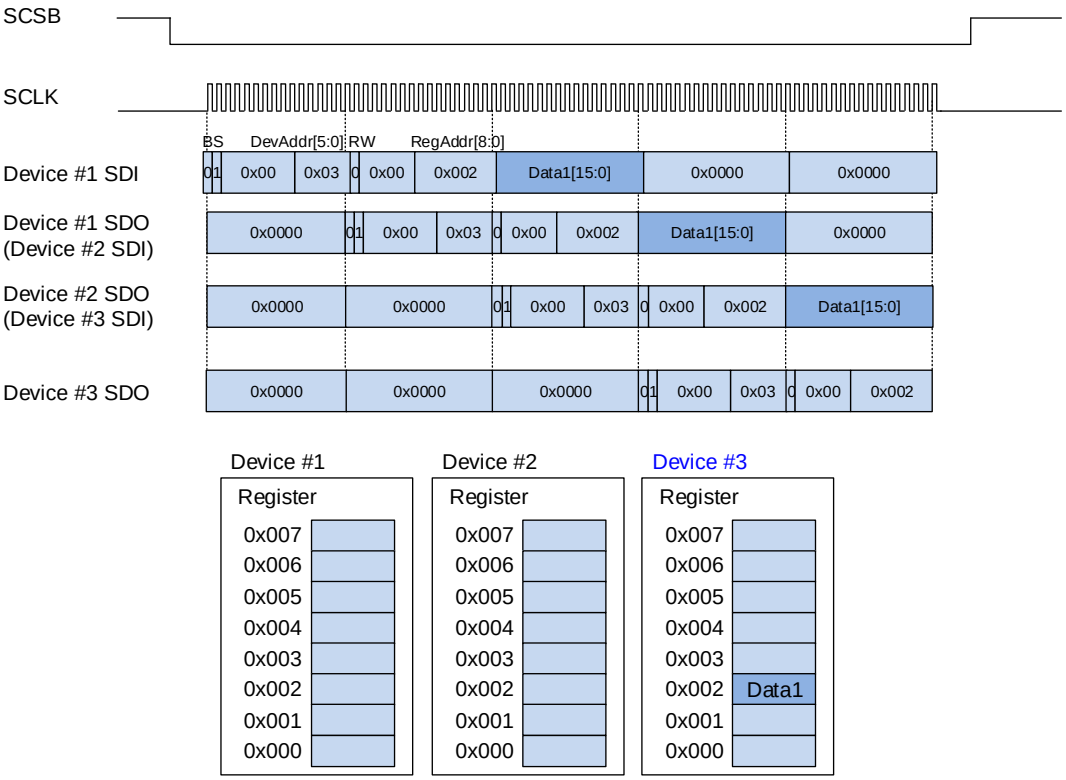


Figure 12. SPI Protocol for 1 Address Write to Device #3

5. SPI Protocol – continued

(7) Single Device, N Address Write (Write to the consecutive register of Device #1)

B =	0:	Target device receives the data
S =	0:	Single
DevAddr[5:0] =	0x01:	Target device address
NumOfData[8:0] =	0x003:	3 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], NumOfData[8:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

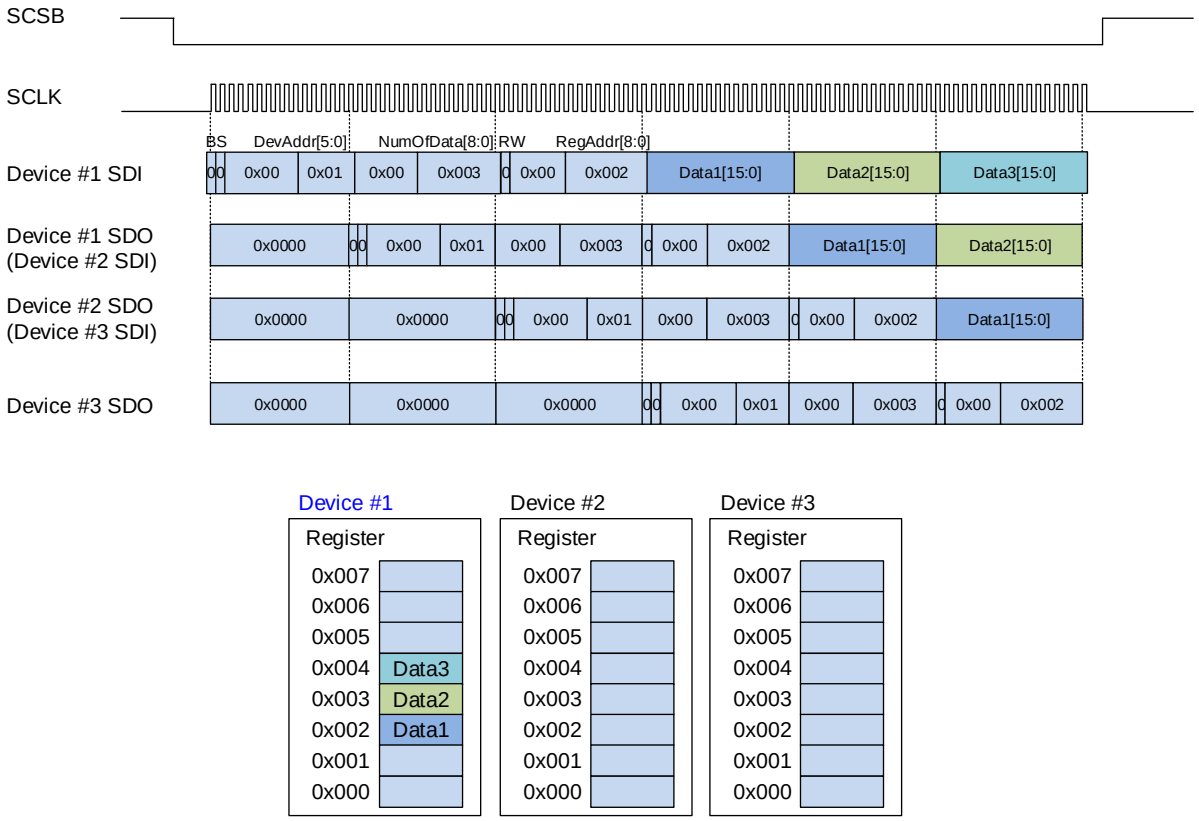


Figure 13. SPI Protocol for N Address Write to Device #1

5. SPI Protocol – continued

(8) All Devices, Different 1 Address Write (Write the same 2 bytes data to the same RegAddr[8:0] of all devices)

B =	1:	All devices receive data
S =	1:	Single
DevAddr[5:0] =	0x3F:	All devices receive different data
NumOfData[8:0] =	-:	1 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

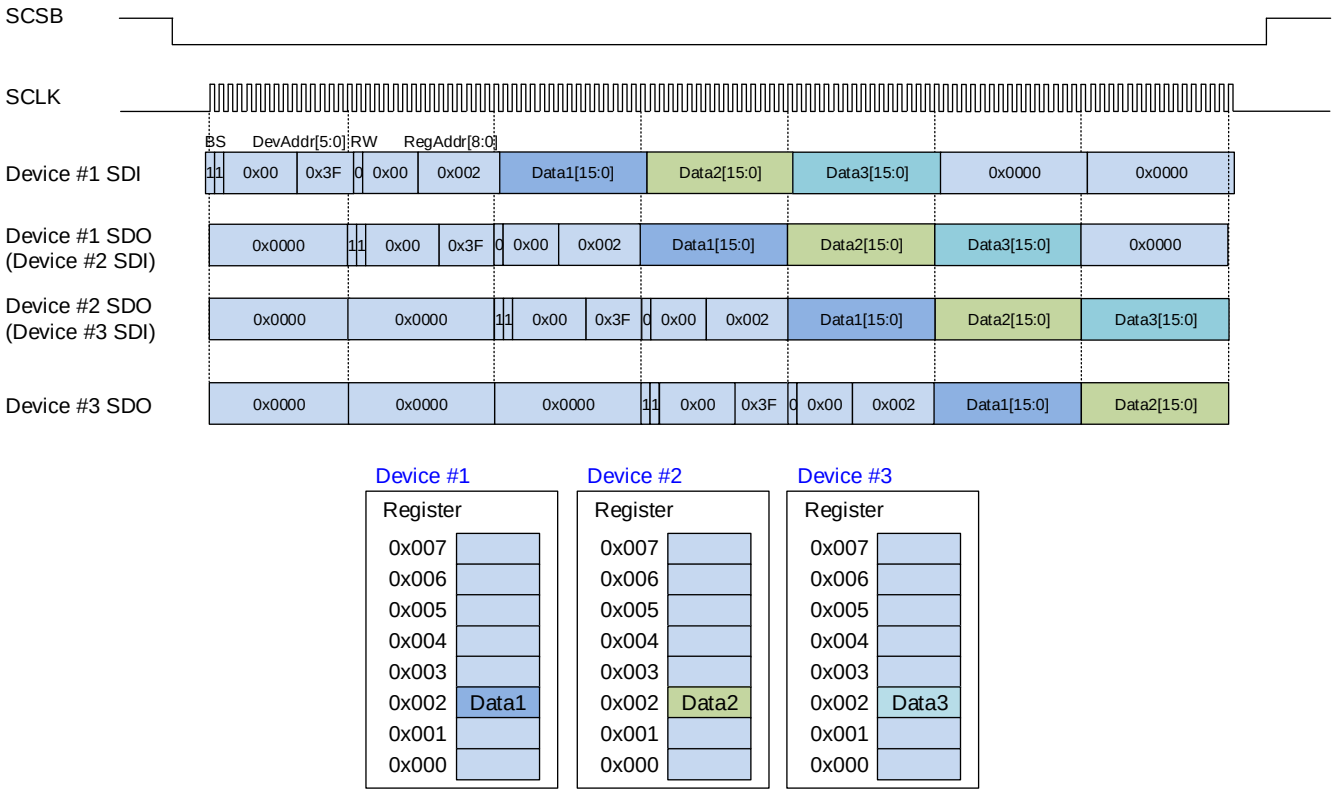


Figure 14. SPI Protocol for 1 Address Distinct Data Write to All Devices

5. SPI Protocol – continued

(9) All Devices, Same 1 Address Write (Write the same 2 bytes data to the same RegAddr[8:0] of all devices)

B =	1:	All devices receive data
S =	1:	Single
DevAddr[5:0] =	0x00:	All devices receive the same data
RW =	0:	Write
NumOfData[8:0] =	-:	1 address access
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

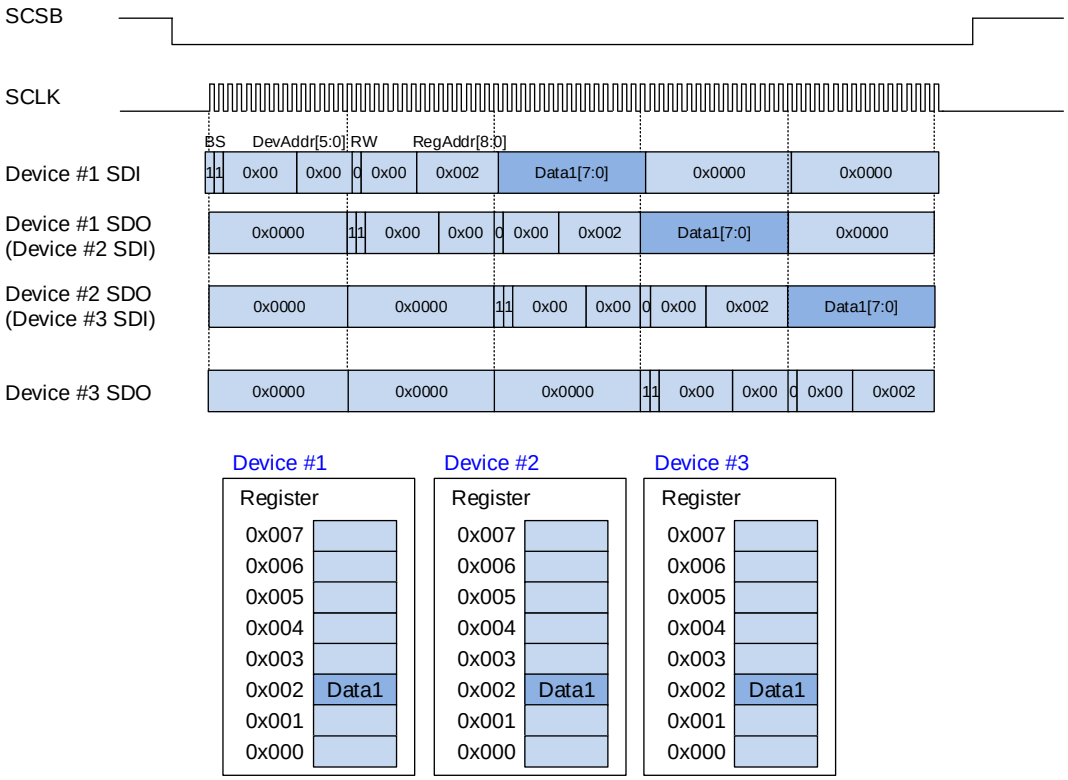


Figure 15. SPI Protocol for 1 Address Distinct Data Write to All Devices

5. SPI Protocol – continued

(10) All Devices, Different N Address Write (Write the different N x 2 bytes data to the same RegAddr[8:0] of all devices)

B =	1:	All devices receive data
S =	0:	Multi
DevAddr[5:0] =	0x3F:	All devices receive different data
NumOfData[8:0] =	0x002:	2 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], NumOfData[8:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

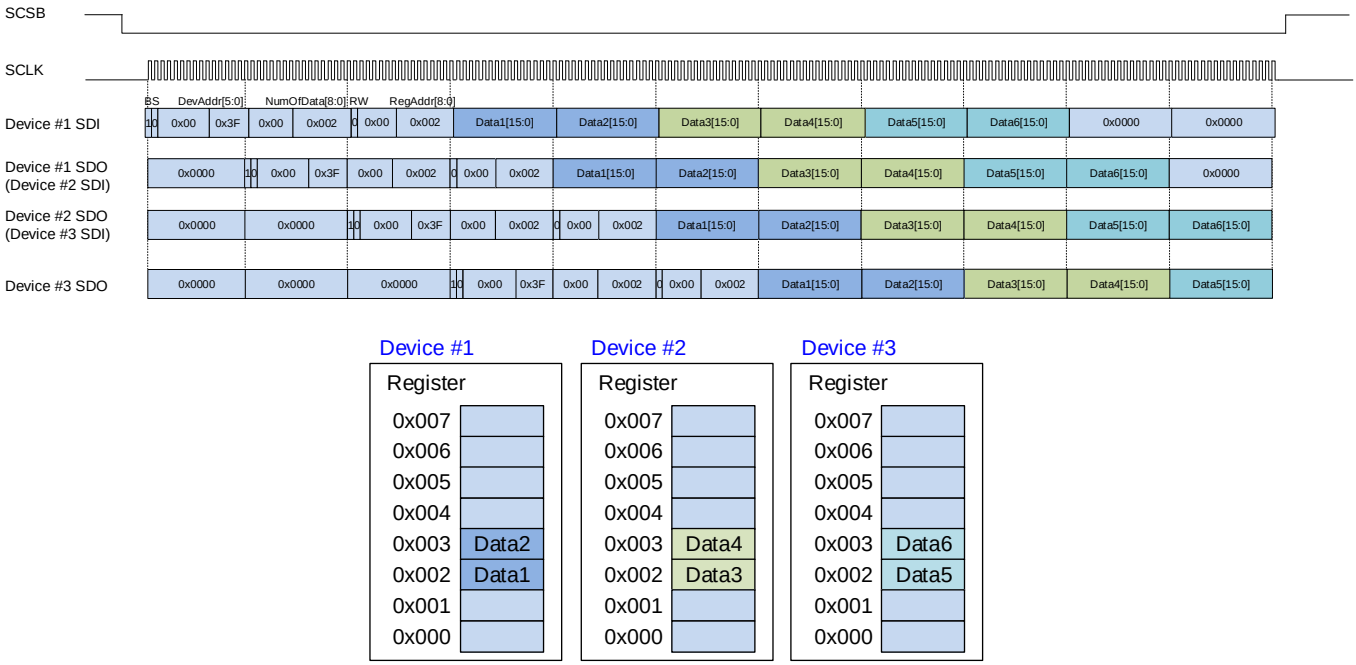


Figure 16. SPI Protocol for N Address Distinct Data Write to All Devices

5. SPI Protocol – continued

(11) All Devices, Same N Address Write (Write the same N x 2 bytes data to the same RegAddr[8:0] of all devices)

B =	1:	All devices receive data
S =	0:	Multi
DevAddr[5:0] =	0x00:	All devices receive the same data
NumOfData[8:0] =	0x003:	3 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], NumOfData[8:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

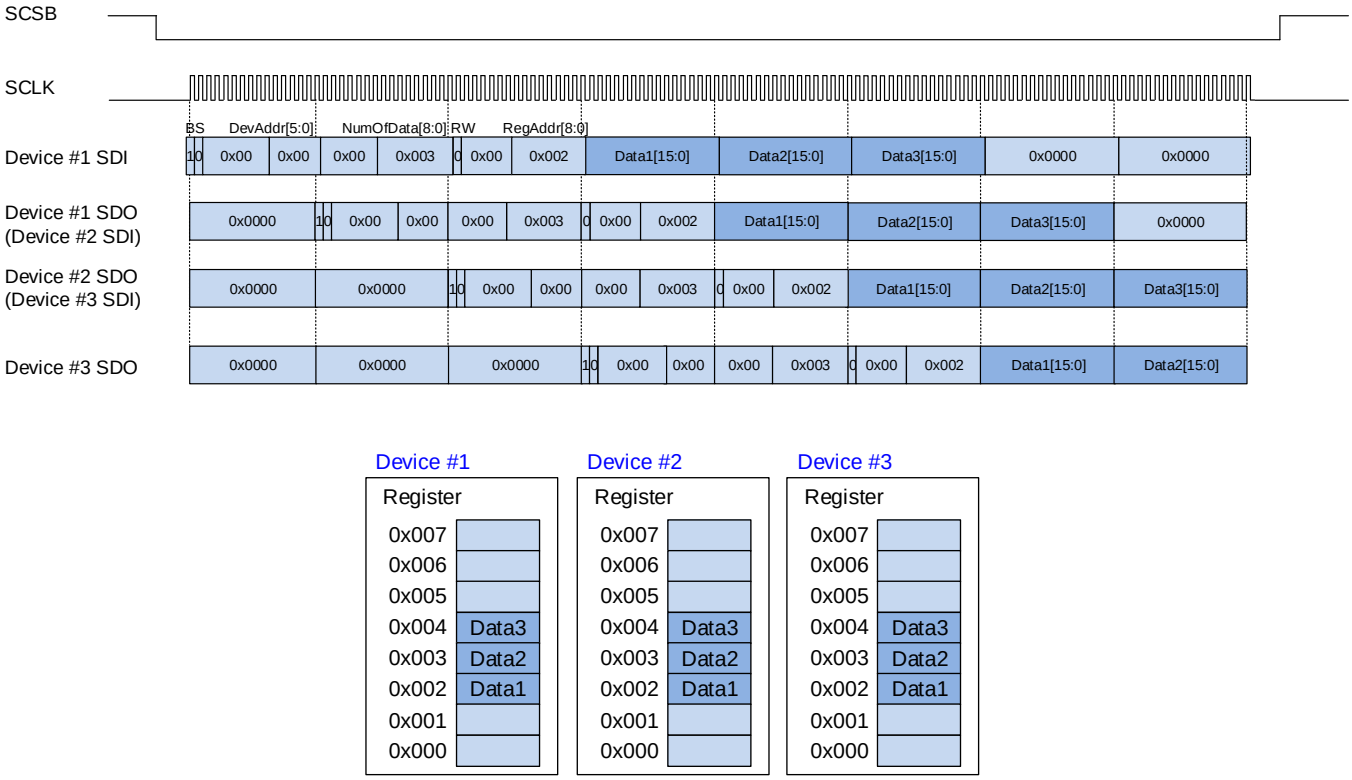


Figure 17. SPI Protocol for N Address Same Data Write to All Devices

5. SPI Protocol – continued

(12) Single Device, 1 Address Read (Read the 2 bytes data from Device #2)

B =	0:	Target device receive the data
S =	1:	Single
DevAddr[5:0] =	0x02:	Target device address
NumOfData[8:0] =	-:	1 address access
RW =	1:	Read
RegAddr[8:0] =	0x003:	Address

SDI: Transfer in the order of DevAddr[5:0] and RegAddr[8:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

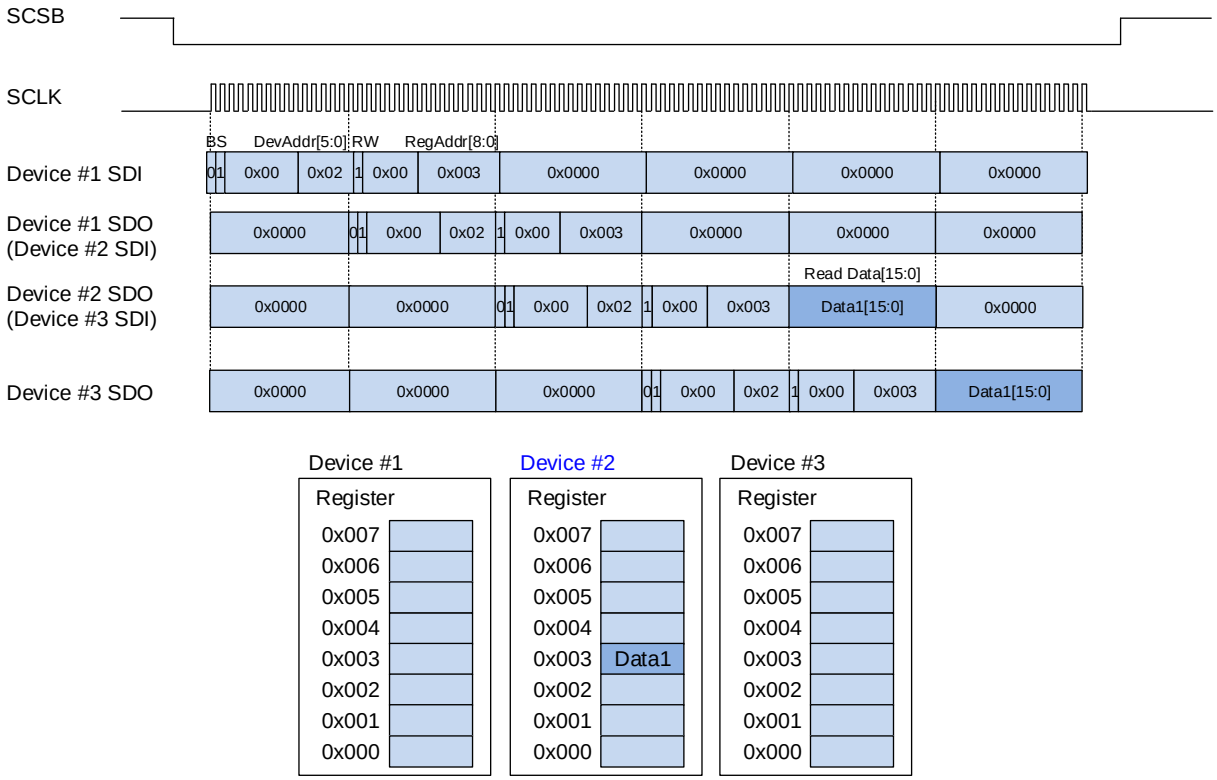


Figure 18. SPI Protocol for 1 Address Read from Device #2

5. SPI Protocol – continued

(13) Single Device, N Address Read (Read the N x 2 bytes data from Device #2)

B =	0:	Target device receives the data
S =	0:	Multi
DevAddr[5:0] =	0x02:	Target device address
NumOfData[8:0] =	0x002:	2 address access
RW =	1:	Read
RegAddr[8:0] =	0x003:	Address

SDI: Transfer in the order of DevAddr[5:0], NumOfData[8:0], and RegAddr[8:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

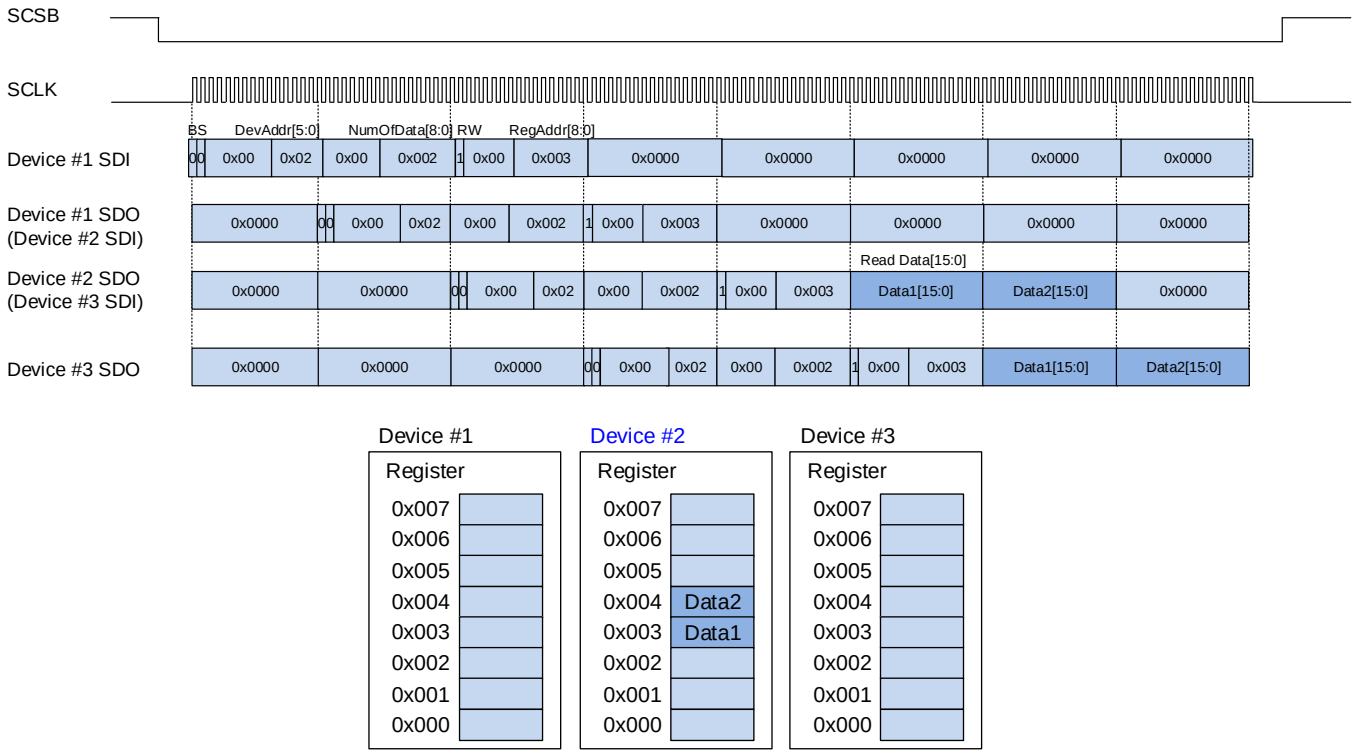


Figure 19. SPI Protocol for N Address Read from Device #2

5. SPI Protocol – continued

(14) Example (Write the data to Device #1 and Device #2)

Example of byte transfer for 2 devices in Cascade Connection.

Table 4. Byte transfer

Transfer setting	B, S, DevAddr[5:0]	2 bytes
	RW, NumOfData[8:0]	2 bytes
	RegAddr[8:0]	2 bytes
Data	Data for the duty setting of Duty	(2 bytes x 24 channels) x 8 matrix switch x 2 devices = 768 bytes
Dummy byte	for multi device transfer	2 bytes
SUM		776 bytes

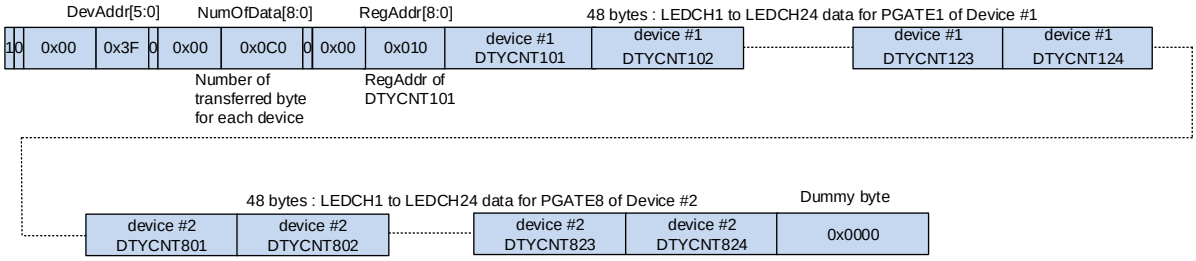


Figure 20. Transfer Byte Number for Multi Access

Functions of Logic Block - continued

6. Register Map

Address	Register Name	Description	Section
0x000	SRSST	Software reset and soft start time	Here
0x001	TURNONWAIT	Wait time after turn on	Here
0x002	SSMASK	Soft start mask time	Here
0x003	ERRMASK	Error output mask time	Here
0x005	SYSCONFIG 1	System config 1	Here
0x006	SYSCONFIG 2	System config 2	Here
0x007	SYSCONFIG 3	System config 3	Here
0x008	SYSCONFIG 4	System config 4	Here
0x009	LEDENL	Enable of LEDCH1 to LEDCH8	Here
0x00A	LEDENM	Enable of LEDCH9 to LEDCH16	Here
0x00B	LEDENU	Enable of LEDCH17 to LEDCH24	Here
0x00C	GDLY	Global delay for all channel	Here
0x010	DTYCNT101	PWM duty setting of LEDCH1 for PGATE1	Here
0x011 to 0x0CD	DTYCNT102 to DTYCNT823	PWM duty setting of LEDCH2 for PGATE1 to PWM duty setting of LEDCH23 for PGATE8	-
0x0CF	DTYCNT824	PWM duty setting of LEDCH24 for PGATE8	-
0x0D0	DLY01	Delay setting of LEDCH1	Here
0x0D1 to 0x0E6	DLY02 to DLY23	Delay setting of LEDCH2 to Delay setting of LEDCH23	-
0x0E7	DLY24	Delay setting of LEDCH24	-
0x0E8	IREV10102	Current revision of LEDCH1 and LEDCH2 for PGATE1	Here
0x0E9 to 0x146	IREV10304 to IREV82122	Current revision of LEDCH3 and LEDCH4 for PGATE1 to Current revision of LEDCH21 and LEDCH22 for PGATE8	-
0x147	IREV82324	Current revision of LEDCH23 and LEDCH24 for PGATE8	-
0x148	ERLSH1L	Error status of LED1 to LED16 short detection for PGATE1	Here
0x149	ERLSH1H	Error status of LED17 to LED24 short detection for PGATE1	Here
0x14A to 0x155	ERLSH2L to ERLSH7H	Error status of LED1 to LED16 short detection for PGATE2 to Error status of LED17 to LED24 short detection for PGATE7	-
0x156	ERLSH8L	Error status of LED1 to LED16 short detection for PGATE8	-
0x157	ERLSH8H	Error status of LED17 to LED24 short detection for PGATE8	-
0x158	ERLOP1L	Error status of LED1 to LED16 open detection for PGATE1	Here
0x159	ERLOP1H	Error status of LED17 to LED24 open detection for PGATE1	Here
0x15A to 0x165	ERLOP2L to ERLOP7H	Error status of LED1 to LED16 open detection for PGATE2 to Error status of LED17 to LED24 open detection for PGATE7	-
0x166	ERLOP8L	Error status of LED1 to LED16 open detection for PGATE8	-
0x167	ERLOP8H	Error status of LED17 to LED24 open detection for PGATE8	-
0x168	EROTHER	Other error status	Here
0x169	ERLEDL	Adjacent LEDCH1 to LEDCH16 short detection	Here
0x16A	ERLEDH	Adjacent LEDCH17 to LEDCH24 short detection	Here
0x16B	ERPGSH	PGATE VIN/GND short detection	Here

As for the register update timing, there are 4 kinds of timing as following.

Type 1. Updated to the newest data immediately when the data is written.

Type 2. Updated to the newest data at the next VSYNC. (Rising edge trigger, after the data is written.)

Type 3. Updated to the newest data at the next VSYNC and GDLY.

Type 4. Updated to the newest data at the next PWM timing. (Rising edge trigger of VSYNC, then rising edge trigger of PWM after the data is written.)

Functions of Logic Block – continued

7. Description of Registers

The writing register annotated "-" is not valid.

Address 0x000: SRSST

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	SSTIM[2:0]			-	-	-	SWRST
Initial value	0	0	1	1	0	0	0	0

[Read / Write] Initial value: 0x0030 Update: Immediately

The register data is updated immediately when the new data is written.
SWRST is Write-only register.

Bit[6:4] SSTIM

SSTIM[2:0] is the register for setting the soft start time. It sets how the FBDAC[7:0] code changes with HSYNC.

Table 5. Soft Start Time / 1 count

SSTIM[2:0]	Count Up Time
0	128 HSYNC
1	256 HSYNC
2	512 HSYNC
3	1024 HSYNC
4	2048 HSYNC
5	4096 HSYNC
6	6144 HSYNC
7	8192 HSYNC

Bit[0] SWRST

SWRST is available when HSYNC is available, because this function uses HSYNC clock.
If SWRST = 1 is written, wait for more than 10 HSYNC pulses before accessing other registers.

Table 6. Software Reset

SWRST	Software Reset
0	Normal
1	Reset (return to '0' automatically)

Address 0x001: TURNONWAIT

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	TURNONWAIT[7:0]							
Initial value	0	0	0	0	0	1	0	0

[Read / Write] Initial value: 0x0004 Update: VSYNC

The register data is updated at the next VSYNC signal rising edge after the data is written.
The mask time of PWM output is set by counting the number of VSYNC pulses.
This register value is updated at the 3rd VSYNC pulse after reset is released (UVLO, SWRST). If this register needs to be updated, update this register before the 3rd VSYNC pulse. Write data higher than 0x04.

$$t_{TURNONWAIT} = TURNONWAIT[7:0]/f_{VSYNC} \quad [s]$$ (Except for waiting time until 1st VSYNC pulse)

Table 7. Maximum Turn on Wait Time

f_{VSYNC}[Hz]	60	120	240	480
Maximum TURNONWAIT Time [ms]	4,250	2,125	1,062.5	531.3

7. Description of Registers – continued

Address 0x002: SSMASK

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	SSMASK[7:0]							
Initial value	0	0	1	1	1	1	0	0

[Read / Write] Initial value: 0x003C Update: VSYNC

The register data is updated at the next VSYNC signal rising edge after the data is written. Set the value higher than 0x02. The mask time of ERROR detection is set by counting the number of VSYNC pulses after TURNONWAIT time.

$t_{SSMASK} = SSMASK[7:0]/f_{VSYNC}$ $[s]$ after TURNONWAIT time
(Except for waiting time until 1st VSYNC pulse)

Table 8. Maximum Soft Start Mask Time

f_{VSYNC}[Hz]	60	120	240	480
Maximum SSMASK Time [ms]	4,250	2,125	1,062.5	531.3

Address 0x003: ERRMASK

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERRMASK[7:0]							
Initial value	0	0	1	0	1	0	0	1

[Read / Write] Initial value: 0x0029 Update: VSYNC

The register data is updated at the next VSYNC signal rising edge after the data is written.

Range: over 0x03 (Set for 0x00 to 0x02 also lead to 0x03, register value = writing value)
ERROR mask time is set by counting the number of HSYNC pulses.

$t_{ERRMASK} = ERRMASK[7:0]/f_{HSYNC}$ $[s]$

If the capacitance of LEDCHn pin C_{LEDCH} is connected, the transient response is affected. Please set the value considering the time margin of LED short detection.
(Example) ERRMASK = 3: mask 3 or 4 clock (PWMn = HIGH and error signal)
It reset ERRMASK counter when PWMn = LOW. Refer to HSYNC equation about the relationship between HSYNC frequency and VSYNC frequency.

Table 9. Maximum Error Mask Time

f_{HSYNC}[Hz]	1,996,800	3,993,600	7,987,200	15,974,400
Maximum ERRMASK Time [µs]	127.7	63.8	31.9	15.9

7. Description of Registers – continued

Address 0x005: SYSCONFIG1

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	MULSEL[1:0]	
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	PGSRCNT[1:0]		-	-	-	-	PRCEN	PRCSEL
Initial value	0	0	0	0	0	0	0	0

[Read / Write] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the new data is written.

Bit[9:8] MULSEL[1:0]

Line Switch Controller setting of external PMOS gate. Refer to PWM Delay and ON Duty setting procedure each dimming mode. As for the HSYNC frequency for MULSEL, Refer to the register PWMFREQ. This register prohibits changing the setting during dimming.

Table 10. Line Switch Controller of External PMOS Gate

MULSEL[1:0]	Line Switch Controller
0x0	8-line switch controller
0x1	4-line switch controller
0x2	6-line switch controller
0x3	6-line switch controller

Bit[7:6] PGSRCNT[1:0]

Fall Slew Rate Control of external PMOS gate.

Table 11. Fall Slew Rate of External PMOS Gate

PGSRCNT[1:0]	Slew Rate
0x0	100 Ω pull down
0x1	1.4 kΩ pull down
0x2	10 kΩ pull down
0x3	100 kΩ pull down

Bit[1] PRCEN

According to setting of PRCSEL, pull up charge ‘VINSW – 1.2 V’ to the LEDCHn pin.

Table 12. Pull up charge Enable Setting

PRCEN	Pull up charge Enable Setting
0	Pull up charge disable
1	Pull up charge enable

(Note) It is necessary to be careful about reverse pressure resistance.

Bit[0] PRCSEL

Pull up charge period setting of the LEDCHn pin.

Table 13. Pull up charge Period

PRCSEL	Pull up charge Period Setting
0	Pull up charge during PWM OFF
1	Pull up charge during all PGATE OFF

7. Description of Registers – continued

Address 0x006: SYSCONFIG2

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	LSHEXE	FBREF[2:0]			SMPTIM[1:0]	
Initial value	0	0	0	0	0	0	0	1

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	PWMFREQ[1:0]		-	LSHEXT	LOPEN	LSHEN	LEDSH[1:0]	
Initial value	0	0	0	0	0	0	0	0

[Read / Write] Initial value: 0x0100 Update: Immediately

The register data is updated immediately when the new data is written.
This register should be set before PWM dimming. Do not change this register value during dimming.

Bit[13] LSHEXE

Short check sequence of adjacent LEDCHn pin is executed after TURNONWAIT time if LSHEXE = 1 is written before TURNONWAIT time.

Table 14. Short Check of Adjacent LEDCHn Pin

LSHEXE	Short Check Execution
0	No operation
1	Execute short check sequence (return to ‘0’ automatically)

Bit[12:10] FBREF

Feedback reference voltage of FB control block.

Table 15. Error Reference of FB Control Block

FBREF[2:0]	Feedback Reference Voltage
0x0	0.45 V
0x1	0.53 V
0x2	0.60 V
0x3	0.75 V
other	0.90 V

Bit[9:8] SMPTIM

The LED channel voltage sampling timing, after PWMn goes from LOW to HIGH. It is necessary to set PWM duty register more than 8 at the dimming.

Table 16. Sampling Time

SMPTIM[1:0]	LED Channel Voltage Sampling Time
0x0	8 HSYNC
0x1	16 HSYNC
0x2	32 HSYNC
0x3	64 HSYNC

Address 0x006: SYSCONFIG2 – continued

Bit[7:6] PWMFREQ (Please update this register until the 4th VSYNC pulse from RESET release.)

The register PWMFREQ defines the number of times PWM turns on during a VSYNC pulse. So the proper HSYNC pulse number is almost proportional to the PWMFREQ. More specifically, considering the NOOVLAP1 and NOOVLAP2 timing, which is the deadtime of PMOSm (m = 1 to 8), the necessary HSYNC pulse number is expressed by the following equation.

$$f_{HSYNC} = f_{VSYNC} \times (4096 + a + b) \times c \times 2^{(PWMFREQ[1:0])}$$

NOOVLAP1 register 0: a = 32, 1: a = 64, 2: a = 128, 3: a = 256
NOOVLAP2 register 0: b = 32, 1: b = 64, 2: b = 128, 3: b = 256
MULSEL register 0: c = 8, 1: c = 4, 2: c = 6, 3: c = 6

The ratio f_{HSYNC}/f_{VSYNC} is noted in the Table 17. Here is the example of the register MULSEL = 0 (the case c = 8 is substituted in the above formula)

Table 17. The example of the ratio f_{HSYNC}/f_{VSYNC} (the register MULSEL = 0)

PWMFREQ[1:0]	NOOVLAP1	NOOVLAP2			
		0	1	2	3
0	0	33,280	33,536	34,048	35,072
	1	33,536	33,792	34,304	35,328
	2	34,048	34,304	34,816	35,840
	3	35,072	35,328	35,840	36,864
1	0	66,560	67,072	68,096	70,144
	1	67,072	67,584	68,608	70,656
	2	68,096	68,608	69,632	71,680
	3	70,144	70,656	71,680	73,728
2	0	133,120	134,144	136,192	140,288
	1	134,144	135,168	137,216	141,312
	2	136,192	137,216	139,264	143,360
	3	140,288	141,312	143,360	147,456
3	0	266,240	268,288	272,384	280,576
	1	268,288	270,336	274,432	282,624
	2	272,384	274,432	278,528	286,720
	3	280,576	282,624	286,720	294,912

The example of HSYNC pulse number is shown as VSYNC is 60 Hz, 120 Hz, 240 Hz and 480 Hz.
The maximum HSYNC frequency is 20 MHz. (Refer to frequency range of electric characteristics)

Table 18. HSYNC Frequency and PWM Frequency (NOOVLAP1 = NOOVLAP2 = 0, MULSEL = 0) (Example)

PWMFREQ [1:0]	VSYNC Frequency [Hz]			
	60	120	240	480
0	60	120	240	480
	1,996,800	3,993,600	7,987,200	15,974,400
1	120	240	480	960
	3,993,600	7,987,200	15,974,400	-
2	240	480	960	1,920
	7,987,200	15,974,400	-	-
3	480	960	1,920	3,840
	15,974,400	-	-	-

(Note) Upper: PWM frequency Lower: HSYNC frequency "-" is not acceptable to set this value in PWMFREQ register

Address 0x006: SYSCONFIG2 – continued

Bit[4] LSHEXT
External pin or internal register setting for LED short protection voltage.

Table 19. Setting for LED Short Protection Voltage

LSHEXT	Setting for LED Short Protection
0	Internal register LEDSH[1:0] setting
1	External LSPSET pin setting

As LSHEXT = 0, please connect the LSPSET pin to GND.
As LSHEXT = 1, please set the LED short protection voltage $V_{LSPSETDET}$ by the following equation.

$$V_{LSPSETDET} = 10 \times V_{LSPSET}$$

Where V_{LSPSET} is the LSPSET pin voltage (0.5 V to 1.8 V)

Bit[3] LOPEN
This register enables/disables LED Open Error detection.

Table 20. Enable Setting for LED Open Error Detection of LEDCHn

LOPEN	Enable Setting
0	LED Open Error detection is not available
1	LED Open Error detection is available

Bit[2] LSHEN
This register enables/disables LED Short Error detection.

Table 21. Enable Setting for LED Short Error Detection of LEDCHn

LSHEN	Enable Setting
0	LED Short Error detection is not available
1	LED Short Error detection is available

Bit[1:0] LEDSH[1:0]
This register controls the detection voltage for LED Short Error.

Table 22. LED Short Error Detection Voltage Setting

LEDSH[1:0]	Detection Voltage[V]
0	3.0 V
1	6.0 V
2	9.0 V
3	12.0 V

7. Description of Registers – continued

Address 0x007: SYSCONFIG3

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	VINSW OVPEN	VINSWOVPREF[1:0]	
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	NOOVLAP1[1:0]		NOOVLAP2[1:0]		AUTOCLR	AUTOOFF	ERRCLR	ERRLAT
Initial value	0	0	0	0	0	0	0	0

[Read / Write] Initial value: 0x0000 Update: Immediately or VSYNC

The data in registers (VINSWOVPEN, VINSWOVPREF, AUTOCLR, AUTOOFF and ERRCLR) are updated immediately when the new data is written.
The data in registers (NOOVLAP1, NOOVLAP2, ERRLAT) are updated at the next VSYNC signal rising edge after the data is written. The data in registers (NOOVLAP1, NOOVLAP2) should be set before PWM dimming.
AUTOCLR and ERRCLR are Write-only registers.

Bit[10] VINSWOVPEN

This register enables/disables Over Voltage Detection of the VINSW pin.

Table 23. Enable Setting for Over Voltage Detection of the VINSW pin

VINSWOVPEN	Enable Setting
0	VINSW Over Voltage detection is not available
1	VINSW Over Voltage detection is available

Bit[9:8] VINSWOVPREF[1:0]

Detection voltage for over voltage of the VINSW pin.

Table 24. Detection Voltage Setting of the VINSW pin

VINSWOVPREF[1:0]	Detection Voltage[V]
0	8.0 V
1	12.0 V
2	16.0 V
3	18.0 V

Bit[7:6] NOOVLAP1 (Update this register until 4th VSYNC pulse from RESET release.)

None overlap time setting 1. Refer to None overlap function.
As for the HSYNC frequency for NOOVLAP1, please refer to the register PWMFREQ.

Table 25. None Overlap Time Setting1

NOOVLAP1[1:0]	None Overlap Time Setting 1
0	32 HSYNC
1	64 HSYNC
2	128 HSYNC
3	256 HSYNC

Bit[5:4] NOOVLAP2 (Update this register until 4th VSYNC pulse from RESET release.)

None overlap time setting 2. Refer to None overlap function.
As for the HSYNC frequency for NOOVLAP2, please refer to the register PWMFREQ.

Table 26. None Overlap Time Setting2

NOOVLAP2[1:0]	None Overlap Time Setting 2
0	32 HSYNC
1	64 HSYNC
2	128 HSYNC
3	256 HSYNC

Address 0x007: SYSCONFIG3 – continued

Bit[3] AUTOCLR

AUTOCLR is available in AUTOOFF = 1 setting.

Table 27. AUTOOFF Condition

AUTOCLR	AUTOOFF Condition
0	No Operation
1	AUTOOFF condition in LEDCHn output is released (return to '0' automatically)

Bit[2] AUTOOFF

Control ON/OFF condition in LEDCHn output. AUTOOFF condition is latched until released by UVLO or AUTOCLR.

Table 28. ON/OFF Condition of LEDCHn Output

AUTOOFF	ON/OFF Condition
0	LEDCHn does not turn OFF automatically after error is detected
1	LEDCHn turn OFF automatically after error is detected

Bit[1] ERRCLR

ERRCLR is available in ERRLAT = 1 setting.

Table 29. Clear Error Register

ERRCLR	Clear Error Register
0	No Operation
1	Clear error register and return Hi-z in FAILB output when ERRLAT = 1 (returns to '0' automatically)

Bit[0] ERRLAT

Control error register and FAILB output when error is detected.

Table 30. Error Detection Function

ERRLAT	Error Detection Function
0	Error register and FAILB output return to initial condition when error is released
1	Error register and FAILB output is retained until ERRCLR = 1 is written

7. Description of Registers – continued

Address 0x008: SYSCONFIG4

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	DACUP[2:0]			DACDN[1:0]		-	MSMODE
Initial value	0	0	0	1	0	0	0	0

[Read / Write] Initial value: 0x0010 Update: Immediately

The register data is updated immediately when the new data is written.

Bit[6:4] DACUP[2:0]

DACUP[2:0] is register for setting the FB DAC's count up step after soft start.

Table 31. FB DAC Code Count Up Step

DACUP[2:0]	FB DAC Code Count Up Step
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8

Bit[3:2] DACDN[1:0]

DACDN[1:0] is register for setting the FB DAC's count down step after soft start.

Table 32. FB DAC Code Count Down Step

DACDN[1:0]	FB DAC Code Count Down Step
0	-1
1	-2
2	-3
3	-4

Bit[0] MSMODE

MSMODE is register for setting of FB DAC’s controller mode or target mode.

Table 33. FB DAC Mode Setting

MSMODE	FB DAC Mode Setting
0	Controller mode
1	Target mode

7. Description of Registers – continued

Address 0x009: LEDENL

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	LEDEN[7:0]							
Initial value	1	1	1	1	1	1	1	1

[Read / Write] Initial value: 0x00FF Update: Immediately

Address 0x00A: LEDENM

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	LEDEN[15:8]							
Initial value	1	1	1	1	1	1	1	1

[Read / Write] Initial value: 0x00FF Update: Immediately

Address 0x00B: LEDENU

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	LEDEN[23:16]							
Initial value	1	1	1	1	1	1	1	1

[Read / Write] Initial value: 0x00FF Update: Immediately

The register data is updated immediately when the new data is written.

These registers (0x009, 0x00A, 0x00B) enable or disable each LED channel. If ‘0’ is set in LEDEN[n-1] (n = 1 to 24), the channel n is not available. LEDCHn current is turned off, and the status of LED Open/Short Detection and FAILB output are not affected by LEDCHn since disabled channels do not detect LED Open/Short Error.

Table 34. LEDCHn Enable Setting

LEDEN[n-1]	LEDCHn current control, LED Open/Short Detection, FAILB output for LEDCHn
0	Disable
1	Enable

7. Description of Registers – continued

Address 0x00C: GDLY

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	GDLY[11:8]			
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	GDLY[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read / Write] Initial value: 0x0000 Update: VSYNC

GDLY is the delay time counted from VSYNC rising edge to PGATE1 fall-edge.
The register data is updated at the next VSYNC signal rising edge after the data is written.

MULSEL register 0: c = 8, 1: c = 4, 2: c = 6, 3: c = 6

Table 35. Global Delay Setting

GDLY[11:0]	GDLY Total Clock Number (clock width @HSYNC)
0x000	N_{GDLYa} = 5 clock to 6 clock from rise-edge of VSYNC
0x001	N_{GDLYa} + 1 x c x $2^{(PWMFREQ[1:0])}$
0x002	N_{GDLYa} + 2 x c x $2^{(PWMFREQ[1:0])}$
0x003	N_{GDLYa} + 3 x c x $2^{(PWMFREQ[1:0])}$
to	to
0xFFC	N_{GDLYa} + 4092 x c x $2^{(PWMFREQ[1:0])}$
0xFFD	N_{GDLYa} + 4093 x c x $2^{(PWMFREQ[1:0])}$
0xFFE	N_{GDLYa} + 4094 x c x $2^{(PWMFREQ[1:0])}$
0xFFF	N_{GDLYa} + 4095 x c x $2^{(PWMFREQ[1:0])}$

(Note) This count starts from VSYNC rising edge.

7. Description of Registers – continued

Address 0x010: DTYCNT101

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	DTY101[11:8]			
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	DTY101[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read / Write] Initial value: 0x0000 Update: PWM

The register data is updated at the next PWM signal rising edge after the data is written.

Table 36. PWM Duty Setting

DTYmn[11:0]	LED Pulse Width
0x000	0 HSYNC clock width
0x001	1 HSYNC clock width
0x002	2 HSYNC clock width
0x003	3 HSYNC clock width
0x004	4 HSYNC clock width
to	to
0xFFC	4,092 HSYNC clock width
0xFFD	4,093 HSYNC clock width
0xFFE	4,094 HSYNC clock width
0xFFF	4,095 HSYNC clock width

Address 0x011 to 0x0CF: DTYCNT102 to DTYCNT824

These registers are used to set the PWM pulse width. The setting procedure is the same as that for LEDCH1 with Address set to 0x010.

Address	Description
0x010 to 0x027	PWM duty register for PGATE1
0x028 to 0x03F	PWM duty register for PGATE2
0x040 to 0x057	PWM duty register for PGATE3
0x058 to 0x06F	PWM duty register for PGATE4
0x070 to 0x087	PWM duty register for PGATE5
0x088 to 0x09F	PWM duty register for PGATE6
0x0A0 to 0x0B7	PWM duty register for PGATE7
0x0B8 to 0x0CF	PWM duty register for PGATE8

Address 0x0D0: DLY01

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	DLY01[11:8]			
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	DLY01[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read / Write] Initial value: 0x0000 Update: VSYNC+GDLY

The register data is updated at the next VSYNC+GDLY timing after the data is written.
DLY01 is the delay time which starts to count after NOOVLAP2.

Address 0x0D0: DLY01 (PWM Delay setting register) – continued

Table 37. Delay Setting of PWM Output

DLY01[11:0]	DLY01 Total Clock Number (clock width @HSYNC)
0x000	0
0x001	1
0x002	2
0x003	3
to	to
0xFFC	4092
0xFFD	4093
0xFFE	4094
0xFFF	4095

(Note) This count starts from NOOVLAP2 finish point.

Address 0x0D1 to 0x0E7: DLY02 to DLY24
These registers are used to set the delay width of PWM for LEDCH2 to LEDCH24. The setting procedure is the same as that for LEDCH1 with address set to 0x0D0.

Address 0x0E8: IREV10102

Bit No	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	IREV102[5:0]					
Initial value	0	0	1	1	1	1	1	1

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	IREV101[5:0]					
Initial value	0	0	1	1	1	1	1	1

[Read / Write] Initial value: 0x3F3F Update: immediately

IREV101 is used with current revision of LEDCH1 of PGATE1 from 50 % to 100 %.
IREV102 is used with current revision of LEDCH2 of PGATE1 from 50 % to 100 %.
IREV register prohibit changing the setting during dimming.

These LED current registers should be updated before LED turns on. The dynamic update during the dimming may affect to the DCDC feedback.

Table 38. Current Revision Setting of LEDCHn

IREV101[5:0]	Current Revision Setting
0x3F	I_{LEDDC} x 100 %
0x3E	I_{LEDDC} x 99.2 %
0x3D	I_{LEDDC} x 98.4 %
0x3C	I_{LEDDC} x 97.6 %
to	to
0x03	I_{LEDDC} x 52.8 %
0x02	I_{LEDDC} x 52.0 %
0x01	I_{LEDDC} x 51.2 %
0x00	I_{LEDDC} x 50.4 %

$$I_{LEDALL} = I_{LEDDC} \times \frac{(IREV_{mn}[5:0] + 64)}{127} \qquad [mA]$$

Address 0x0E9 to 0x147: IREVmn
This register is used to make setting of current revision for LEDCH3 to LEDCH24 of PGATE1 and LEDCH1 to LEDCH24 of PGATE2 to PGATE8. The setting procedure is the same as that for LEDCH1 of PGATE1 with address set to 0x0E8.

7. Description of Registers – continued

Address 0x148: ERLSH1L

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSH1 [15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSH1 [7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x149: ERLSH1H

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSH1 [23:16]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the data is written.
These registers (0x148, 0x149) correspond to the status of LED Short Detection of PGATE1 of LED1 to LED24.

Table 39. Status of LED Short Detection

ERLSH1[n-1]	Status
0	Normal
1	Detected LED Short Error*(Note 1)*

(Note 1) ERRLAT = 0: ERLSHm[n-1] (m = 1 to 8, n = 1 to 24) turns 0, if LED Short Error is released or LEDEN[n-1] = 0 is set or LSHEN = 0 is set.
ERRLAT = 1: ERLSHm[n-1] turns 0, if ERRCLR = 1 is set.

Address 0x14A to 0x157: ERLSHm[n-1]

These registers (0x14A to 0x157) correspond to the status of LED Short Detection of PGATE2 to PGATE8 of LED1 to LED24. The setting procedure is the same as that for LED1 to LED24 of PGATE1 with address set to 0x148 and 0x149.

7. Description of Registers – continued

Address 0x158: ERLOP1L

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLOP1[15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLOP1[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x159: ERLOP1H

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLOP1[23:16]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the data is written.
These registers (0x158, 0x159) correspond to the status of LED Open Detection of PGATE1 of LED1 to LED24.

Table 40. Status of LED Open Detection

ERLOP1 [n-1]	Status
0	Normal
1	Detected LED Open Error*(Note 2)*

(Note 2) ERRLAT = 0: ERLOPm[n-1] (m = 1 to 8, n = 1 to 24) turns 0,if LED Open Error is released or LEDEN[n-1] = 0 is set or LOPEN = 0 is set.
ERRLAT = 1: ERLOPm[n-1] turns 0, if ERRCLR = 1 is set.

Address 0x15A to 0x167: ERLOPm[n-1]

These registers (0x15A to 0x167) correspond to the status of LED Short Detection of PGATE2 to PGATE8 of LED1 to LED24. The setting procedure is the same as that for LED1 to LED24 of PGATE1 with Address set to 0x158 and 0x159.

7. Description of Registers – continued

Address 0x168: EROTHER

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	EXENG	EXEOK	ERISET OPEN	ERISET OCP	-	ERVINSW OVP
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the new data is written.

Bit[5]: EXENG

EXENG register correspond to the status that short check sequence of adjacent LEDCHn is not executed.

Table 41. Status of Short Check Sequence NG

EXENG	Status
0	Normal
1	Short check sequence of adjacent LEDCHn is not executed

Bit[4]: EXEOK

EXEOK register correspond to the status that short check sequence of adjacent LEDCHn is executed.

Table 42. Status of Short Check Sequence OK

EXEOK	Status
0	Normal
1	Short check sequence of adjacent LEDCHn is executed

Bit[3]: ERISETOPEN

ERISETOPEN register correspond to the status of ISET Open Detection.

Table 43. Status of ISET Open Detection

ERISETOPEN	Status
0	Normal
1	Detected ISET Open Error*(Note 3)*

Bit[2]: ERISETOCP

ERISETOCP register correspond to the status of ISET Over Current Detection.

Table 44. Status of ISET Over Current Detection

ERISETOCP	Status
0	Normal
1	Detected ISET Over Current Error*(Note 3)*

Bit[0]: ERVINSWOVP

ERVINSWOVP register correspond to the status of VINSW Over Voltage Detection.

Table 45. Status of VINSW Over Voltage Detection

ERVINSWOVP	Status
0	Normal
1	Detected VINSW Over Voltage Error*(Note 3)*

(Note 3) ERRLAT = 0: ERISETOPEN, ERISETOCP and ERVINSWOVP turns 0, if error condition is released. ERRLAT = 1: ERISETOPEN, ERISETOCP and ERVINSWOVP turns 0, if ERRCLR = 1 is set.

7. Description of Registers – continued

Address 0x169: ERLEDL

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLED[15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLED[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x16A: ERLEDH

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLED[23:16]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the data is written.
These registers (0x169, 0x16A) correspond to the status of Short Detection of adjacent LEDCHn.

Table 46. Status of Short Detection of Adjacent LEDCHn

ERLED[n-1] (n = 1 to 24))	Status
0	Normal
1	Detected Short Detection Error of Adjacent LEDCHn*(Note 4)*

Address 0x16B: ERPGSH

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERPGVINSH[7:0]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERPGGSH[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the data is written.

Bit[15:8]: ERPGVINSH[7:0]
This register correspond to the status of Short Detection between the PGATEm pin and the VINSW pin.

Table 47. Status of Short Detection between the PGATEm pin and the VINSW pin

ERPGVINSH[m-1] (m = 1 to 8)	Status
0	Normal
1	Detected Short Error to the VINSW pin*(Note 4)*

Bit[7:0]: ERPGGSH[7:0]
This register correspond to the status of Short Detection between the PGATEm pin and the GND.

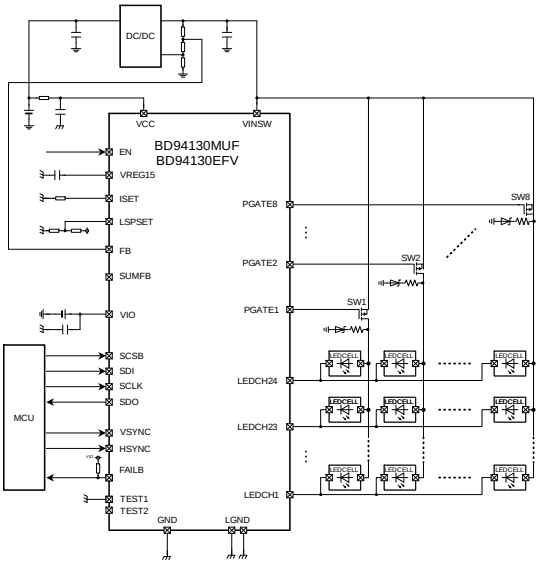
Table 48. Status of Short Detection between the PGATEm pin and GND

ERPGGSH[m-1] (m = 1 to 8)	Status
0	Normal
1	Detected Short Error to GND*(Note 4)*

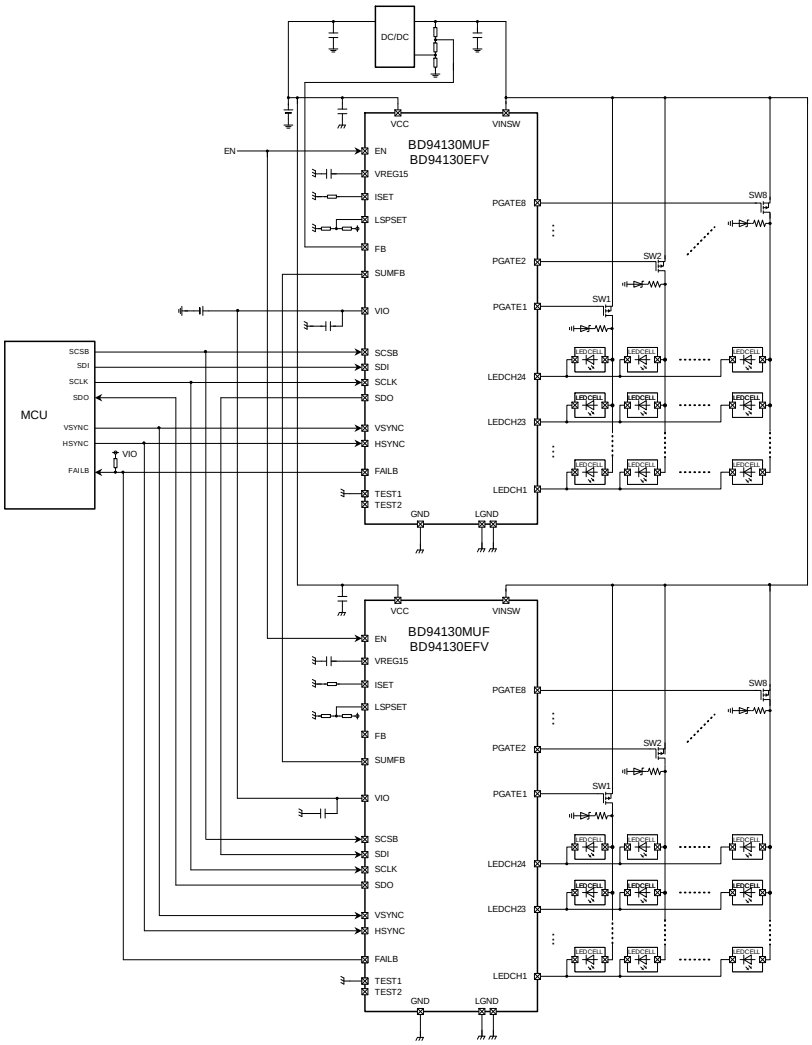
(Note 4) ERLED[n-1], ERPGVINSH[m-1] and ERPGGSH[m-1] turn 0, if ERRCLR = 1 is set.

Application Circuit Diagram

1. The Example of Basic Application



2. The Plural BD94130 Usage (the common SPI and the common DCDC)



Timing Chart

1. Boot Sequence

(1) SPI Command Mode

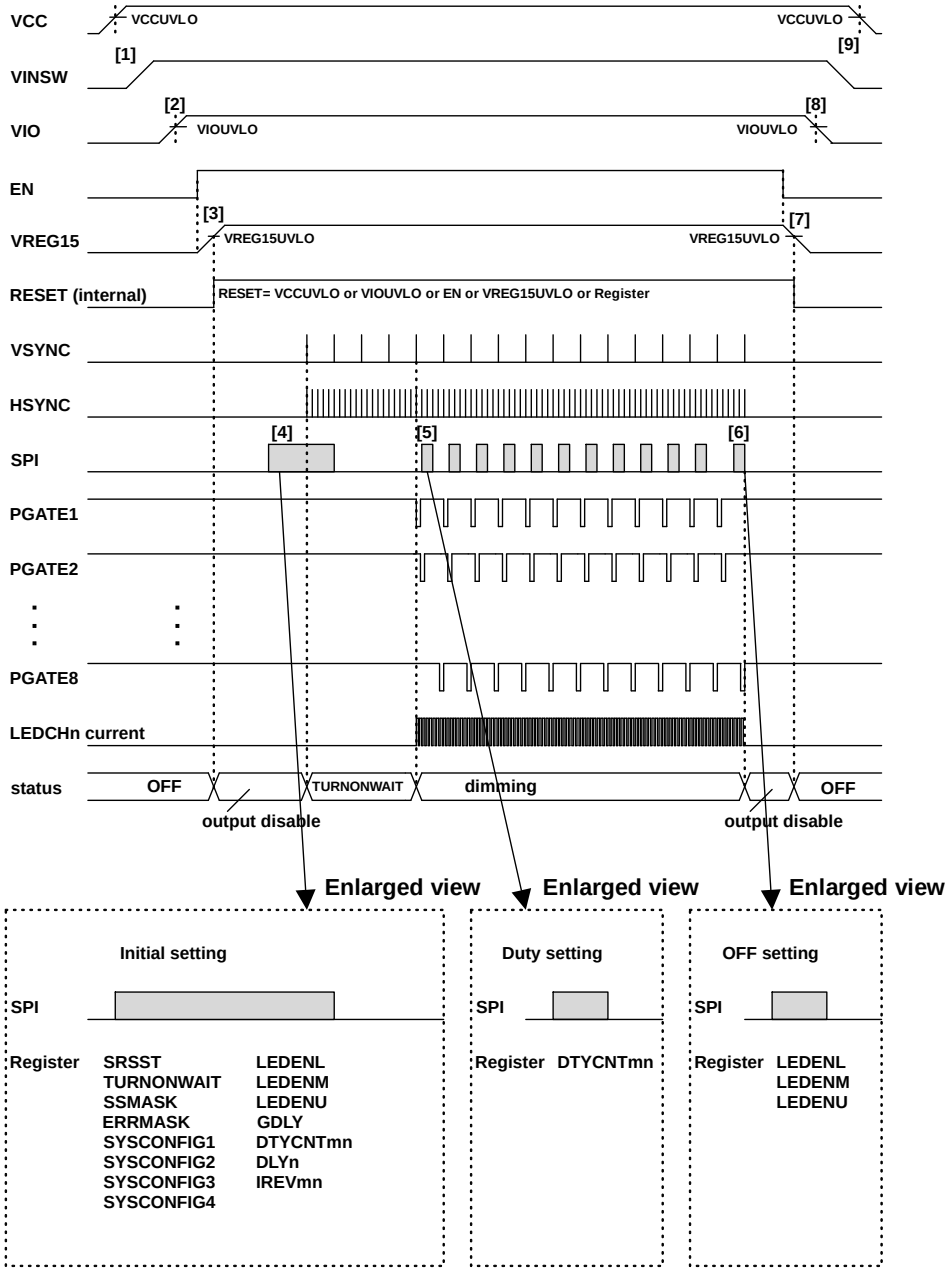


Figure 21. The Boot Sequence for SPI Command Mode

Turn ON Sequence

[1] Power on VCC and VCCUVLO is released. And power on VINSW.
[2] Power on VIO and VIOUVLO is released.
[3] After the EN pin is H, VREG15 turn on. The signal RESET is expressed by the following equation. After RESET is released, the registers can be accessed.
RESET = VCCULVO or VIOUVLO or EN or VREG15UVLO or Register
[4] Set the initial registers until 4th VSYNC period from RESET release. 4th VSYNC period is adjustable by the register TURNONWAIT[7:0]. During the state TURNONWAIT, the IC keeps LEDs off.
[5] The duty register DTYCNTmn are updated in every VSYNC period for dimming.

Turn OFF Sequence

[6] Set the register LEDENL, LEDENM and LEDENU registers to 0.
[7] VREG15 turn off after the EN pin is L. The registers cannot be accessed during RESET = L.
[8] Power off VIO and VIOUVLO is detected.
[9] Power off VINSW and VCC.

The first turn on and the last turn off are VCC. And the order of the VIO, EN can be exchanged.

1. Boot Sequence – continued

(2) PWM Direct Control Mode (without SPI command)

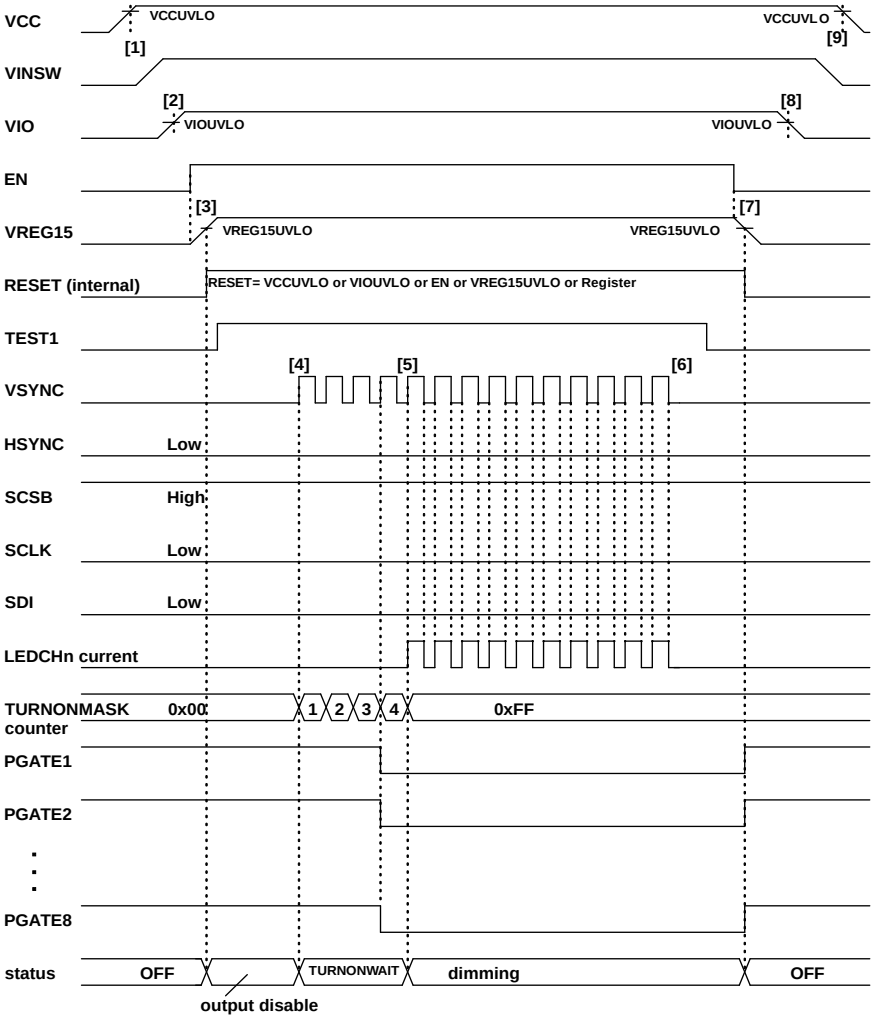


Figure 22. The boot Sequence for PWM Direct Control Mode

Turn ON Sequence

[1] Power on VCC and VCCUVLO is released. And power on VINSW.
[2] Power on VIO and VIOUVLO is released.
[3] After the EN pin is H, VREG15 turn on. The signal RESET is expressed by the following equation. After RESET is released, the VSYNC signal becomes valid. And the TEST1 pin must be H.

RESET = VCCULVO or VIOUVLO or EN or VREG15UVLO or Register

[4] Until 4th VSYNC period from RESET release, the IC keeps LEDs off, as TURNONWAIT.
[5] Input PWM pulse to VSYNC for dimming. VSYNC signal can control LED current directly. PGATEm are all on.

Turn OFF Sequence

[6] Stop PWM dimming pulse input to VSYNC.
[7] VREG15 turn off after the EN pin is L.
[8] Power off VIO and VIOUVLO is detected.
[9] Power off VINSW and VCC.

The first turn on and the last turn off are VCC. And the order of the VIO, EN can be exchanged.

About PWM Direct Control Mode

If 8 HSYNC clocks counts, PWM Direct Control Mode is shifted to SPI Command Mode.
Even if error is detected, LED keeps ON, and FAILB signal is still HIGH.

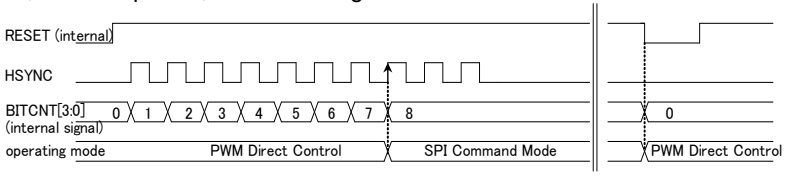


Figure 23. SPI Command Mode / PWM Direct Control Mode

Timing Chart – continued

2. Matrix Operation and PWM Dimming Setting

(1) Matrix Operation Setting (the line number of gate controller)

The register MULSEL[1:0] controls the number of active PGATE as shown in Figure 24. The unused PGATE5 to PGATE8 asserts always OFF. The selectable gate number is 4, 6, and 8. The necessary HSYNC clock number is depend on the register MULSEL[1:0].

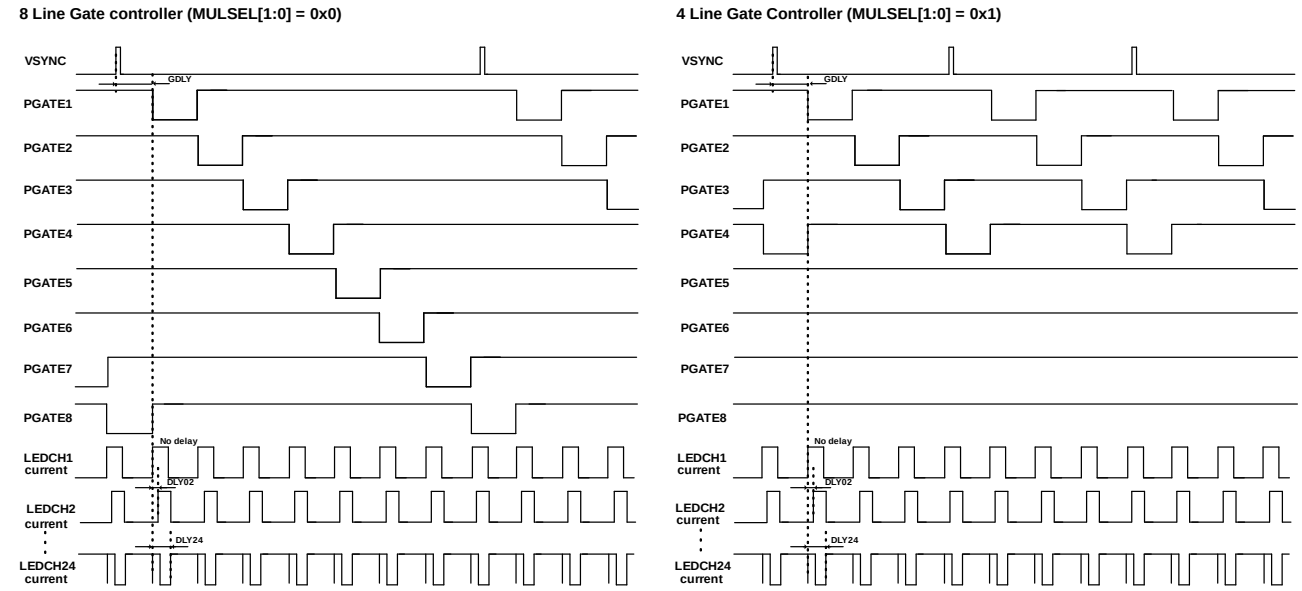


Figure 24. Dimming Mode

(2) Matrix Operation Setting (PWM frequency)

The register PWMFREQ[1:0] controls the repeated number of active PGATE for VSYNC period. The figure 25 show the example of the one repeat and two repeats. The selectable repeated number is 1, 2, 4, and 8. The necessary HSYNC clock number is depend on the register PWMFREQ[1:0].

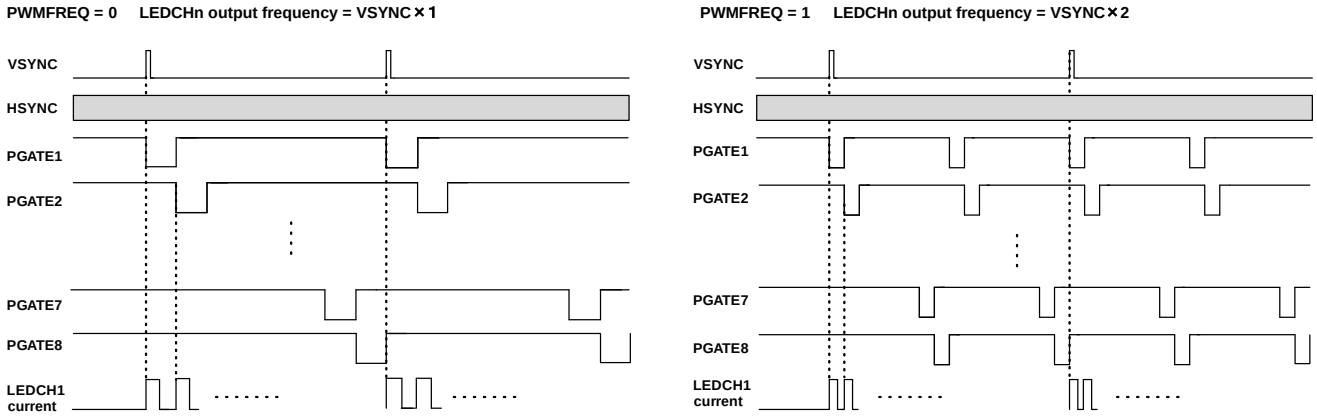


Figure 25. PWMFREQ vs LEDCHn output

2. Matrix Operation and PWM Dimming Setting – continued
(3) PWM Delay Setting

There are 2 kinds of delay setting.
The register GDLY set the interval from VSYNC to PGATE1, and the GDLY delay affects all PGATEm accordingly.
The register DLYn (n = 1 to 24) set the interval from PGATE = ON to the current rising of LEDCHn. (That interval is expressed NOOVLAP2 + DLYn in detail.)
By shifting the starting timing of each LED current, the transient response of the total current is averaged.

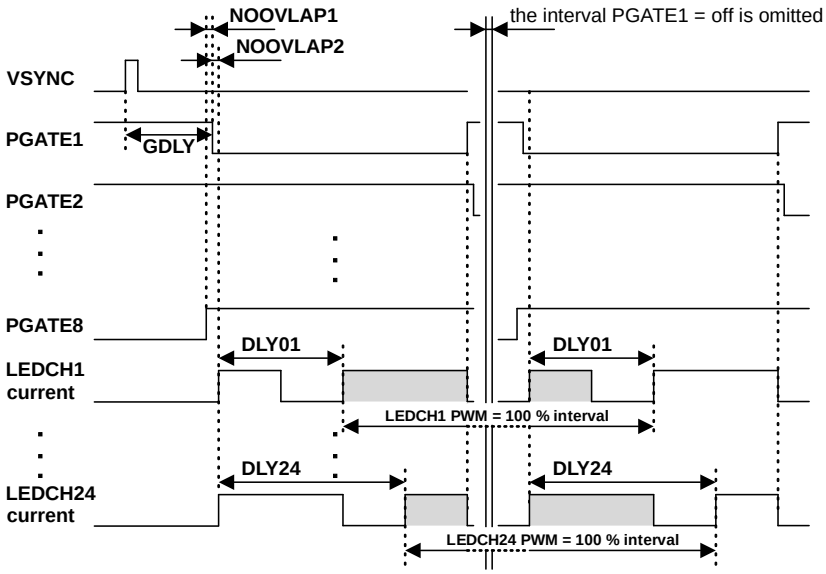


Figure 26. PWM delay setting

Figure 26 shows the delay setting over 1 PGATE in 8 Line Gate Controller. The setting in the figure is 75 % Duty and 50 % Delay for LEDCH1.
If the LED current is finished within the single period of PGATE = ON, the delay setting of DTYmn is expressed as following.

$$0 \leq DLY_n < 4095$$
$$DTY_{mn} + DLY_n \leq 4095$$

2. Matrix Operation and PWM Dimming Setting – continued
(4) PWM Duty Setting

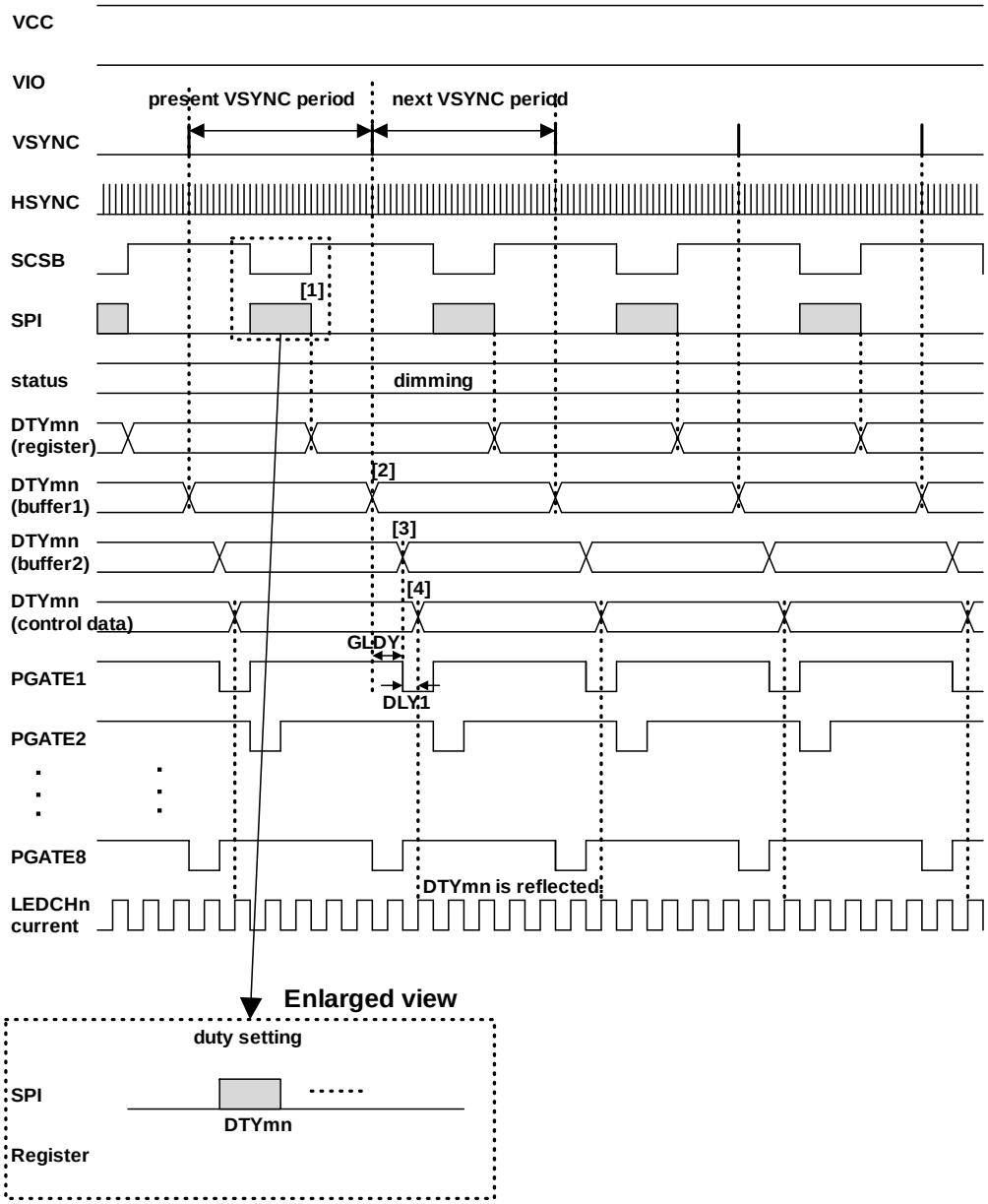


Figure 27. Dimming Sequence for Normal Operation

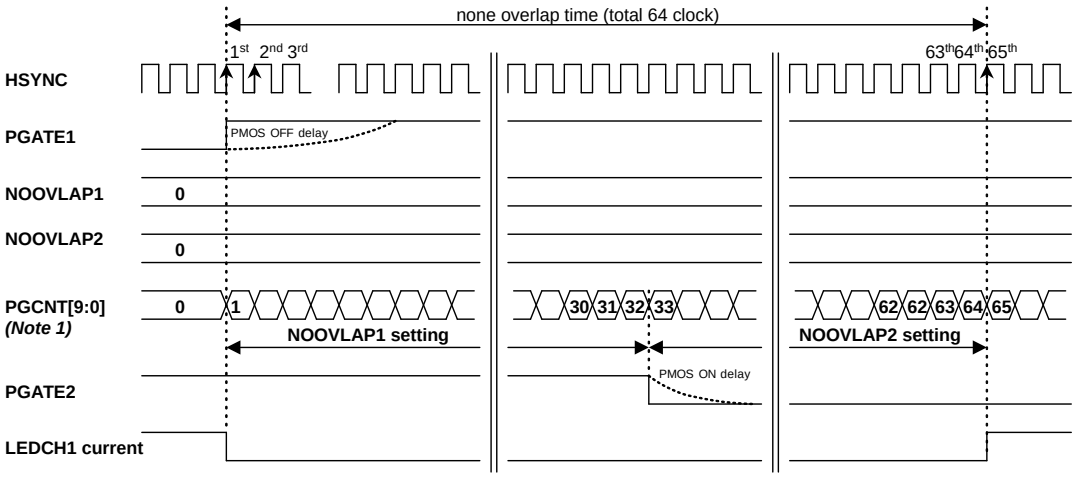
[1] The register DTYmn access is finished within the present VSYNC period to reflect in the next VSYNC period. If that access is not finished by the VSYNC, the register is not reflected correctly.
[2] Buffer1 data is updated at VSYNC timing.
[3] Buffer2 data is updated at VSYNC+GDLY timing.
[4] Control data (DTYmn) is updated after the delay setting DLYn in the next VSYNC period, DTYmn is reflected to the LEDCHn current.

Timing Chart – continued

3. None Overlap Function

None overlap time between PMOSm can be adjustable by the register NOOVLAP1, NOOVLAP2.
NOOVLAP1 is the interval from PMOSm = OFF to PMOS(m+1) = ON. This is set longer than the PMOS off delay not to cause PMOS = ON simultaneously.
NOOVLAP2 is the interval from PMOS = ON to the beginning of LEDCHn current. This is set longer than the PMOS on delay.
These register adjustable such as 32 clock, 64 clock, 128 clock, 256 clock by HSYNC.
The necessary clock of HSYNC is changed accordingly. Please refer the section of Description of PWMFREQ[1:0] (Address 0x006).

(Example) NOOVLAP1 = 0, NOOVLAP2 = 0 (DTY101, DTY201 = 0xFFF, DLY1 = 0)



(Note 1) Internal signal for counting PGATE ON timing and LEDCH1 current ON timing.

Figure 28. PGATE1, PGATE2 None Overlap Timing

Timing Chart – continued

4. PWM Behavior at Close VSYNC Intervals

In this section, PWM dimming behavior is shown if HSYNC is not equal to ideal frequency.
The ideal frequency of HSYNC is 33280 times of VSYNC below example.

(1) HSYNC Frequency less than Ideal Frequency

Example: Delay = 0, Duty = 75 %, PWMFREQ = 0, NOOVLAP1 = NOOVLAP2 = 0, MULSEL = 0

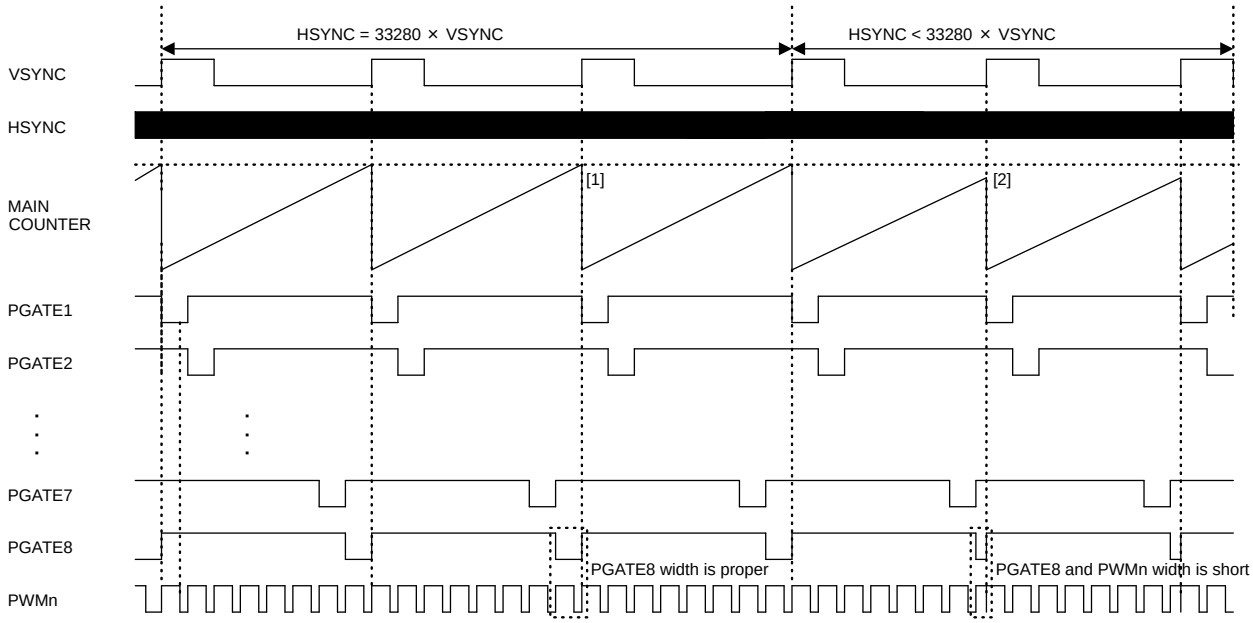


Figure 29. HSYNC Frequency Less than Ideal Frequency

The main counter is reset at the rising edge of VSYNC. The main counter starts counting up by HSYNC and proceed the line control from PGATE1 to PGATE8.

[1] As HSYNC is equal to the ideal frequency, the main counter reaches the full value 33280. The ON interval of PGATE8 and PWMn are proper.

[2] As HSYNC is smaller than the ideal frequency, the main counter does not reach the full value. The ON interval of PGATE8 and PWMn are short.

(2) HSYNC Frequency more than Ideal Frequency

Example: Delay = 0, Duty = 50 %, PWMFREQ = 0, NOOVLAP1 = NOOVLAP2 = 0, MULSEL = 0

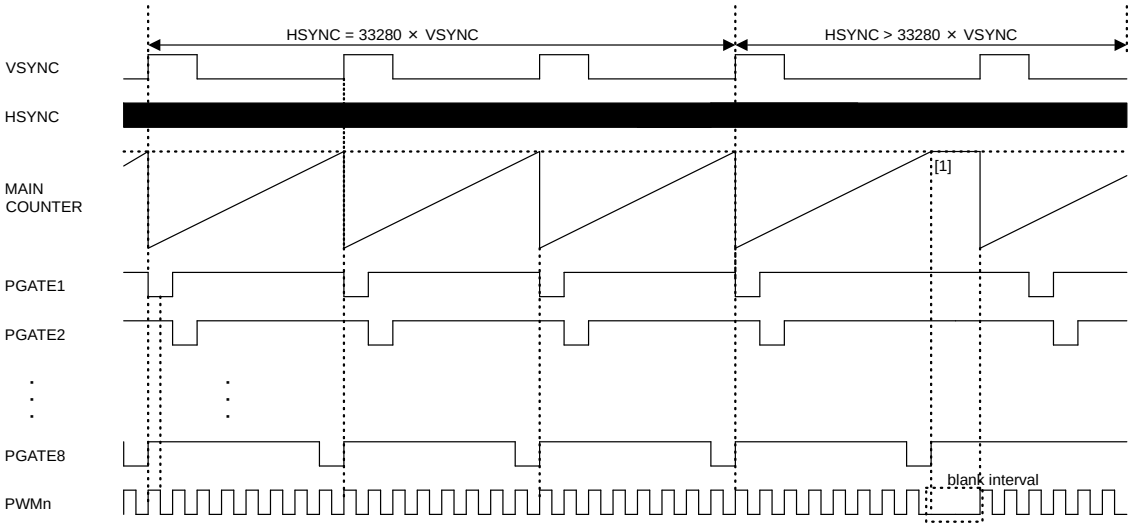


Figure 30. HSYNC Frequency More than Ideal Frequency

[1] As HSYNC is more than the ideal frequency, the main counter continues the full value 33280 without reset. In this blank interval after PGATE8 = OFF, all LEDs turn off. The ON interval of PGATE8 and PWMn are almost proper, but all LEDs brightness is LOW.

Timing Chart – continued

5. ERROR Detection and Release

The following are the internal signals on the timing chart:

PWM_OH[1]	PWM signal for channel 2 control
LOPDET_IL[n-1]	LED Open Error signal (HIGH: normal, LOW: error)
LSHDET_IL[n-1]	LED Short Error signal (HIGH: normal, LOW: error)
VINSWOVP_IL	VINSW pin Over Voltage Error signal (HIGH: normal, LOW: error)
ISETOCP_IL	ISET pin Over Current Error signal (HIGH: normal, LOW: error)
ISETOPEN_IL	ISET pin OPEN Error signal (HIGH: normal, LOW: error)
PGGSH_IL[m-1]	PGATEm Comparator signal
SSEND	Soft start mask signal (HIGH: normal, LOW: mask)
R_LOPDET, R_LSHDET, R_VSYNC	retiming signal
ERR_MASKCNTmn	error mask counter for PGATEm
R_SSCNT	counter for soft start
(m = 1 to 8, n = 1 to 24)	

(1) LED Open Detection

LED Open Error is detected after ERRMASK, and LED Open Error is released as shown in Figure 31.
Here ERRMASK[7:0] = 0x03

If PWM_OH[n-1] is shorter than ERR_MSKCNTmn[7:0], the LED OPEN is not detected.

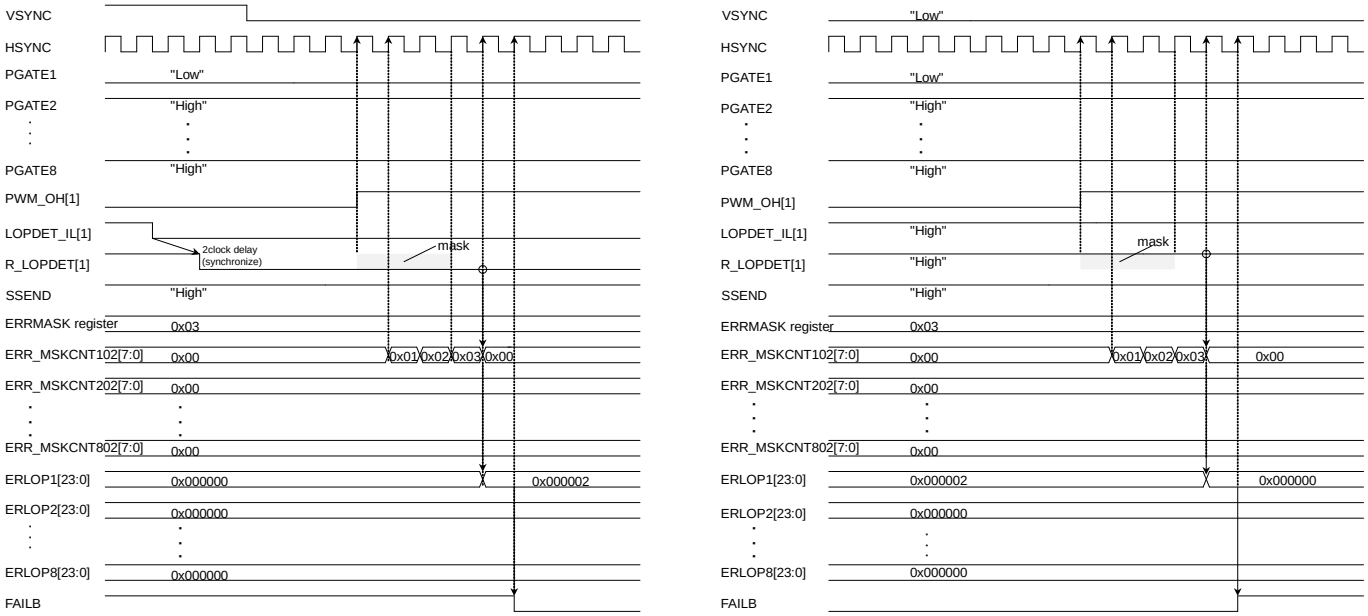


Figure 31. LED Open Detection and Release

(1) LED Open Detection - continued

[Case: LED Open Error signal is LOW width]

While PWM_OH[1] = HIGH and LOPDET_IL[1] = LOW with SSEND = HIGH (Soft Start end), if ERR_MSKCNT does not counts up until the ERRMASK, FAILB remains HIGH.
In the same condition, if ERR_MSKCNT counts up until the ERRMASK, FAILB asserts LOW.

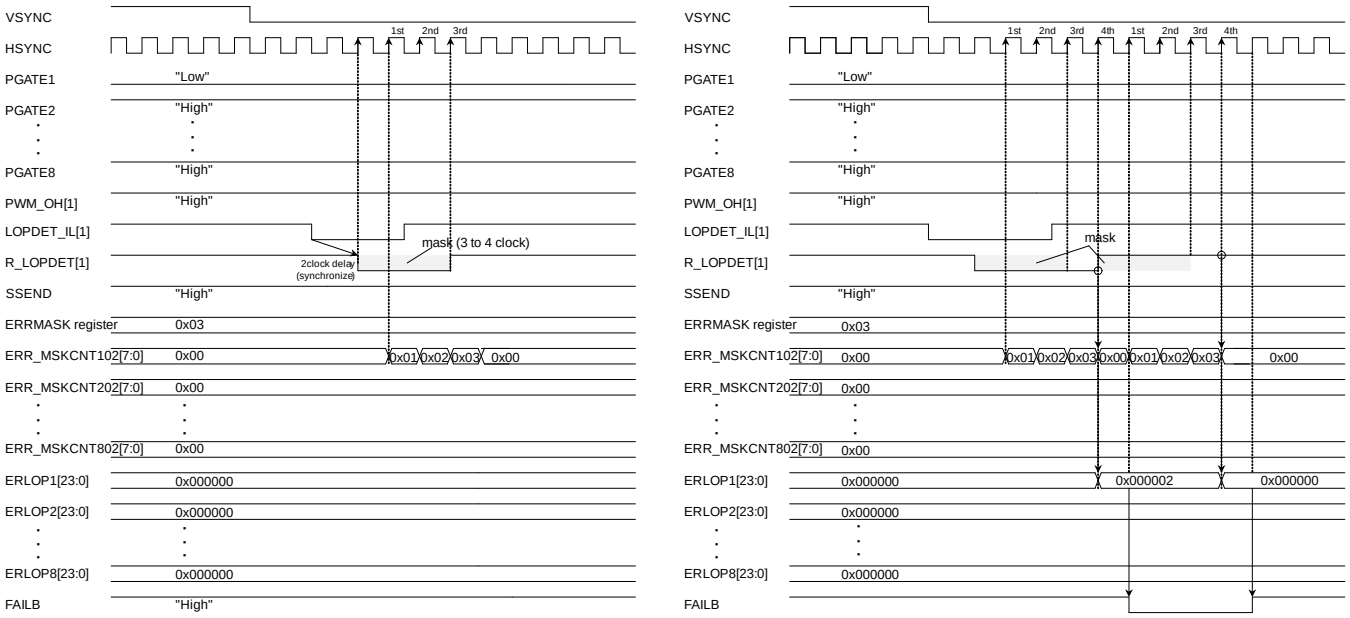


Figure 32. LED Open Detection (the error signal is LOW width)

(2) LED Short Detection

(Example) ERRMASK[7:0] = 0x03
LED Short Error is detected after ERRMASK, and LED Short Error is released as shown in Figure 33.
If the capacitance of LEDCHn pin C_{LEDCH} is connected, the transient response is affected. Please set the ERRMASK value considering the time margin of LED short detection.

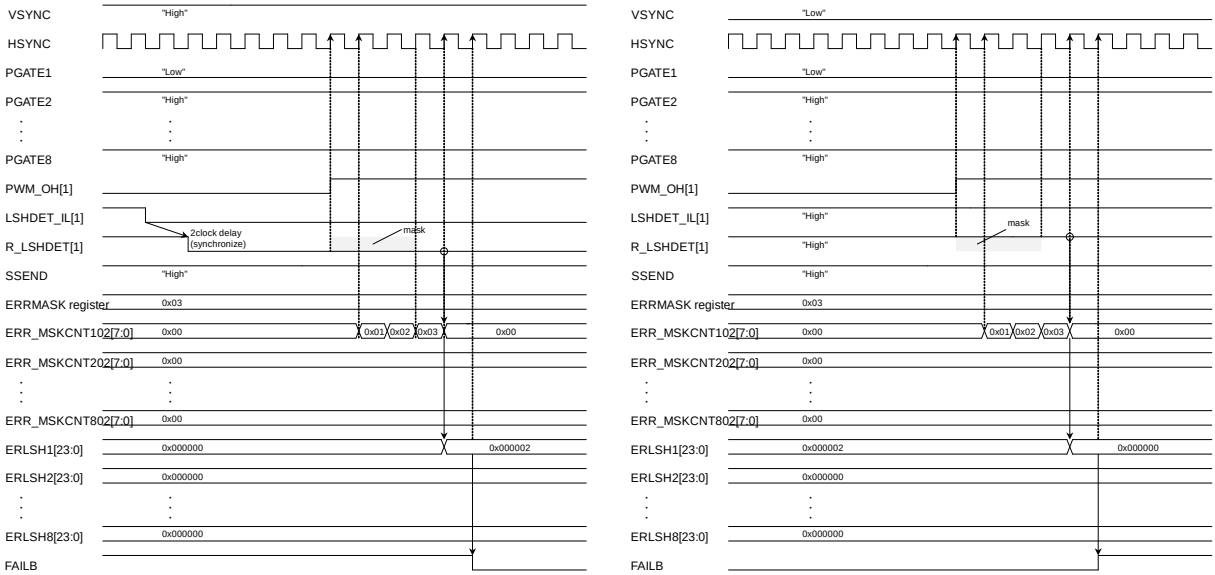


Figure 33. LED Short Detection and Release

5. ERROR Detection and Release - continued

(3) VINSW Over Voltage Detection

(Example) VINSWOVPEN = 1, ERRLAT = 0

VINSW Over Voltage is detected after SSEND, and VINSW Over Voltage Error is released as shown in Figure 34.
LEDCHn output is not turned off by VINSW Over Voltage Error.

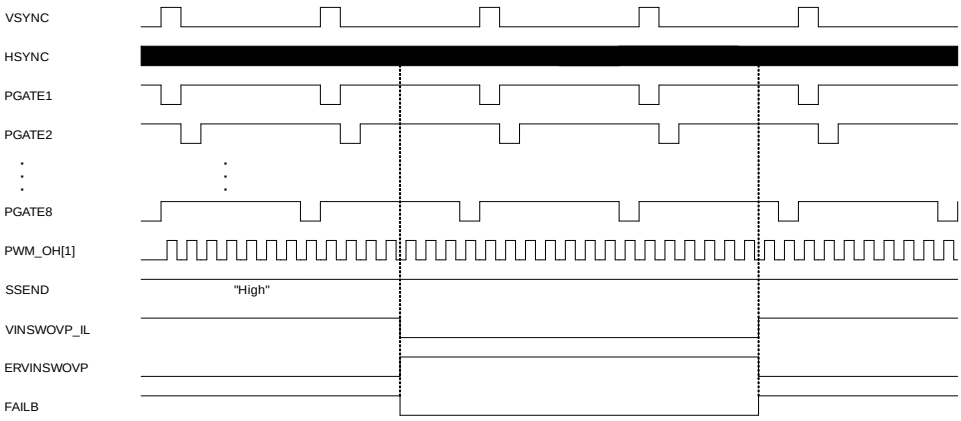


Figure 34. VINSW Over Voltage Detection

(4) ISET Over Current Detection

(Example) ERRLAT = 0

ISET Over Current is detected after SSEND, and ISET Over Current Error is released as shown in Figure 35.
LEDCHn output is turned off by ISET Over Current Error.

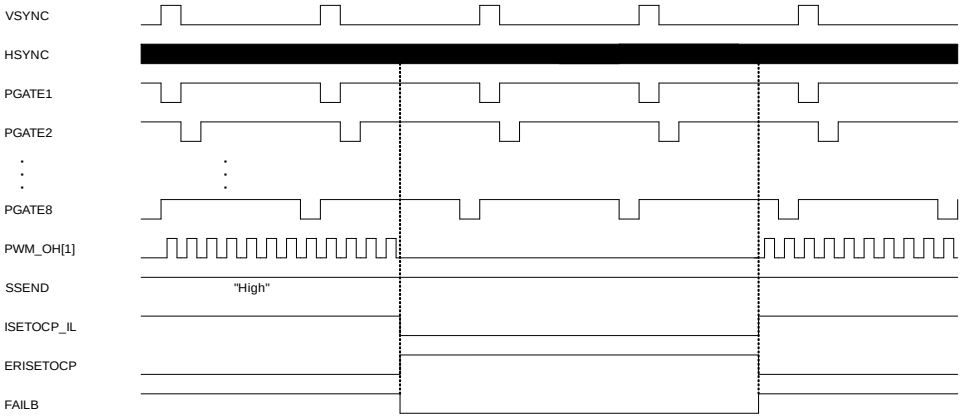


Figure 35. ISET Over Current Detection

(5) ISET Open Detection

(Example) ERRLAT = 0

ISET Open is detected after SSEND, and ISET Open Error is released as shown in Figure 36.
LEDCHn output is not turned off by ISET Open Error.

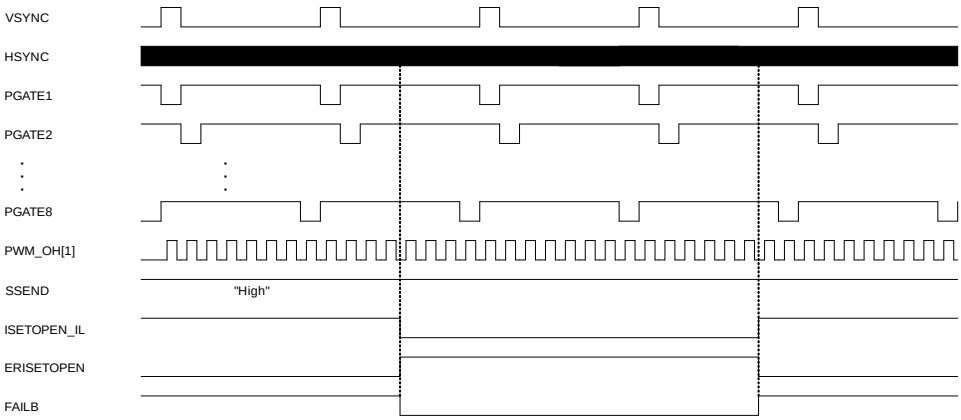


Figure 36. ISET Open Detection

5. ERROR Detection and Release – continued

(6) Short PGATEm to VINSW Detection

(Example) MULSEL = 0

Short PGATEm to VINSW is detected the timing that PGATEm goes from LOW to HIGH during dimming mode. Detected PGATEm becomes Hi-z output. Short Error can release by ERRCLR.

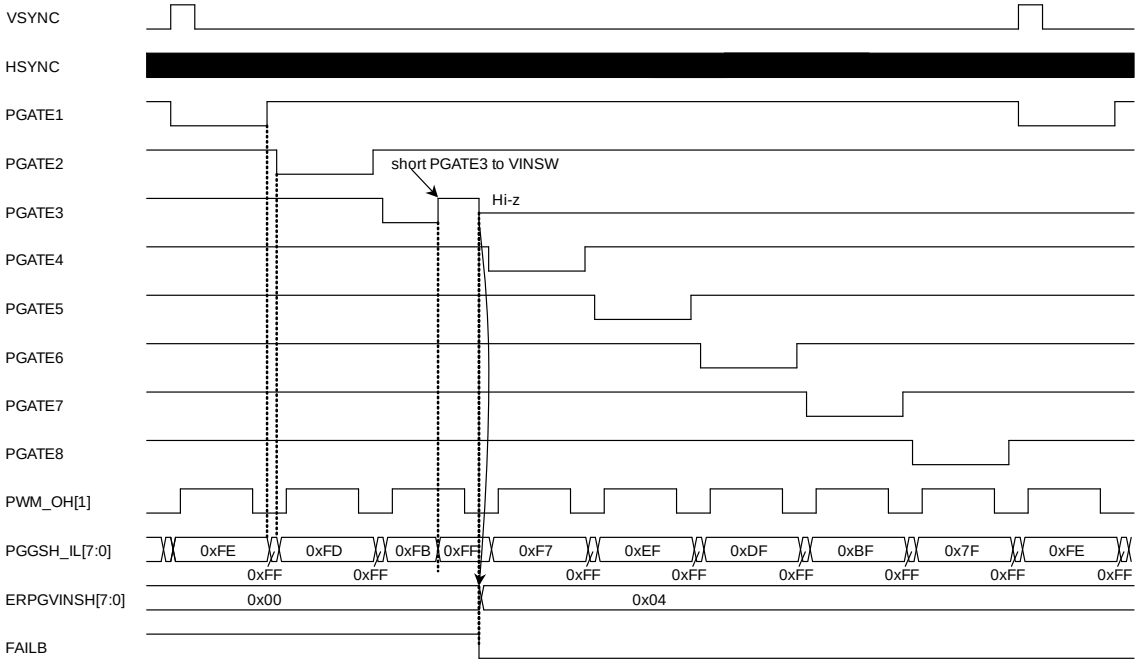


Figure 37. Short PGATEm to VINSW Detection

5. ERROR Detection and Release – continued

(7) Short PGATEm to GND Detection

(Example) MULSEL = 0

Short PGATEm to GND is detected the timing that PGATEm goes from HIGH to LOW during dimming mode. Detected PGATEm becomes Hi-z output. Short Error can release by ERRCLR.

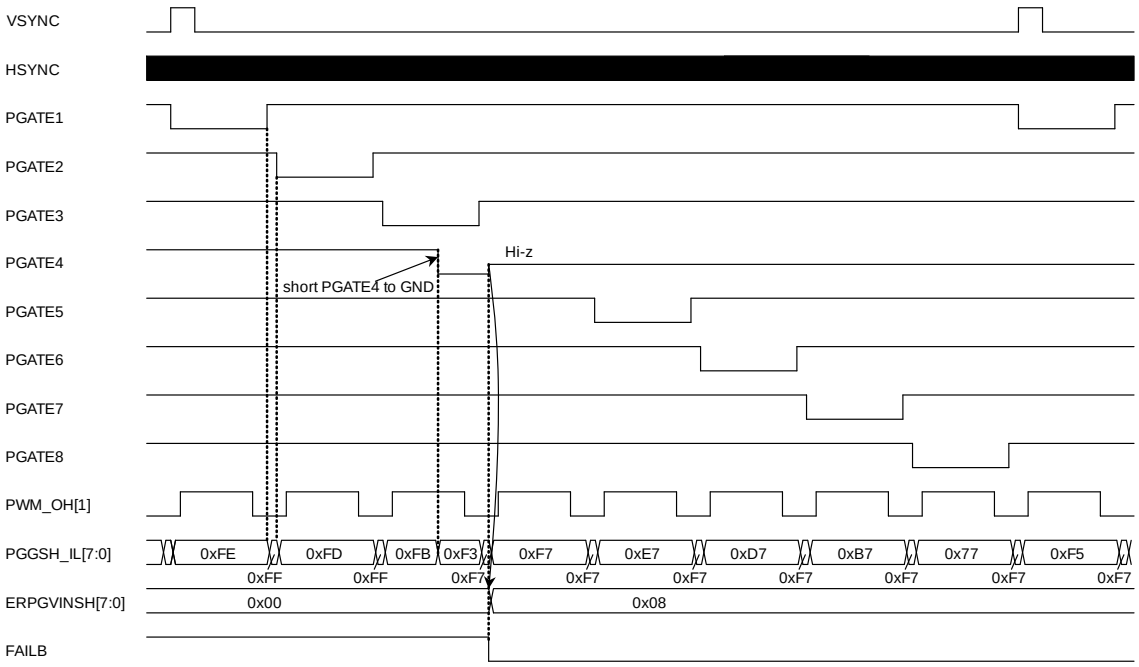


Figure 38. Short PGATEm to GND Detection

5. ERROR Detection and Release – continued

(8) Short Check Detection of Adjacent LEDCHn

The short check sequence of adjacent the LEDCHn pin is executed at the end of TURNONWAIT interval, if the register LSHEXE = 1 is written by the end of TURNONWAIT interval, where EXEOK status is HIGH. If LSHEXE = 1 is written after TURNONWAIT interval, the short check sequence is not executed and the register EXENG = 1.
The short check result can be read from the register ERLED[23:0]. Example both ERLED[5] and ERLED[6] is HIGH, the LEDCH6 pin and the LEDCH7 pin can be judged as short pin.

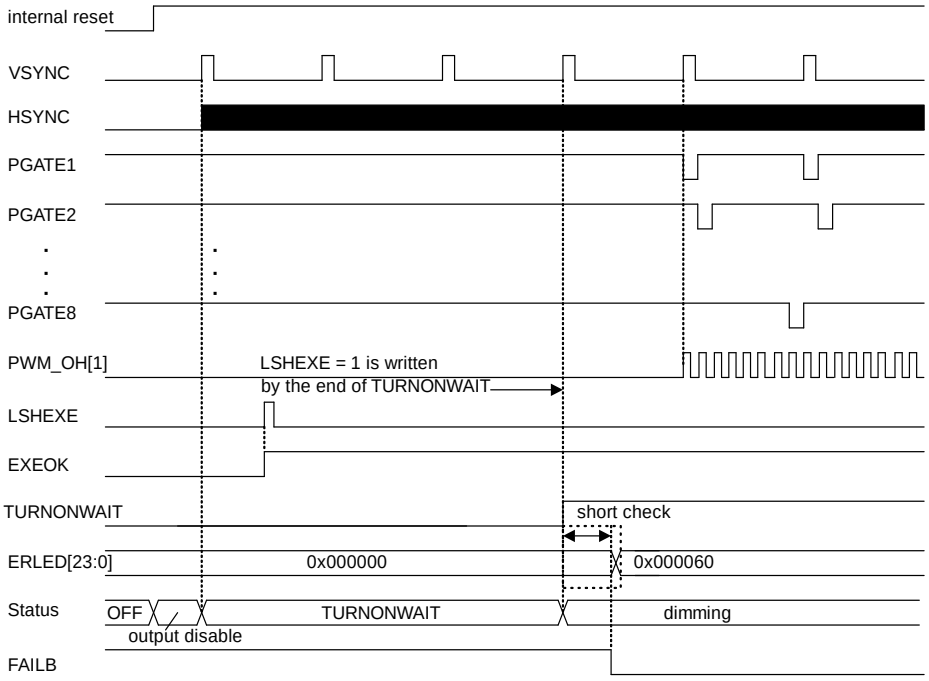


Figure 39. Short Check Detection of Adjacent LEDCHn

(9) Soft-start Masking Function

LED Open Error cannot be detected during Soft Start (SSEND = LOW). Soft start counter counts up every VSYNC period until the SSMASK setting (SSEND = HIGH) as shown Figure 40 below. LED Open Error can be detected when SSEND = HIGH. It is also the same when LED Short Error is detected.

Time of mask = (TURNONWAIT register + SSMASK register) x VSYNC
(Example) SSMASK = 0x3C

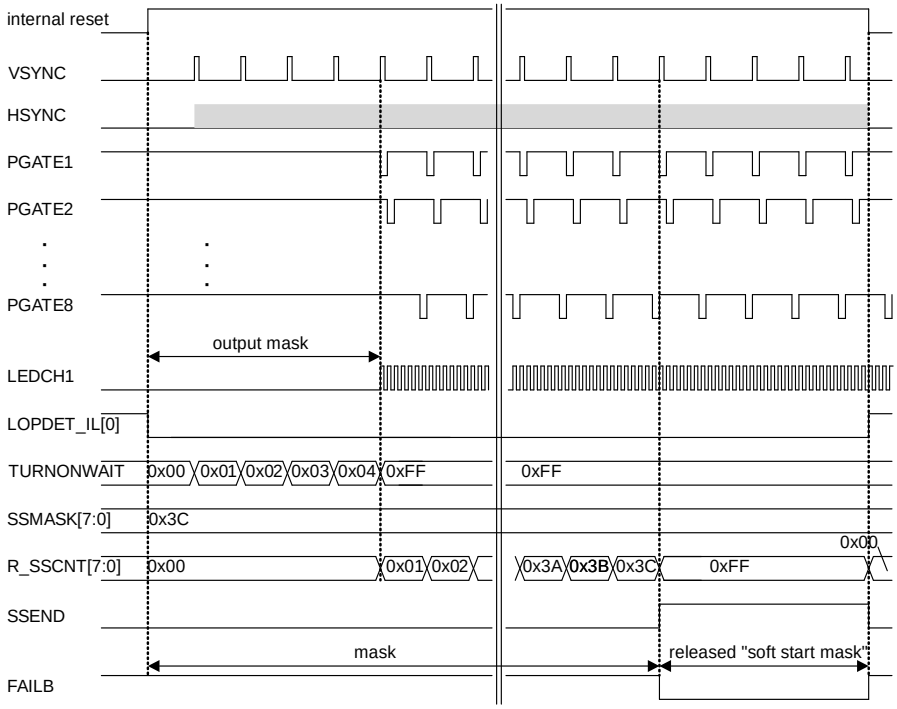


Figure 40. Setting for Soft Start Mask

5. ERROR Detection and Release – continued

(10) Error Sequence for the Register AUTOOFF

AUTOOFF set the abnormal LED = OFF automatically.

(Case) the register ERRLAT = 0 and AUTOOFF = 1

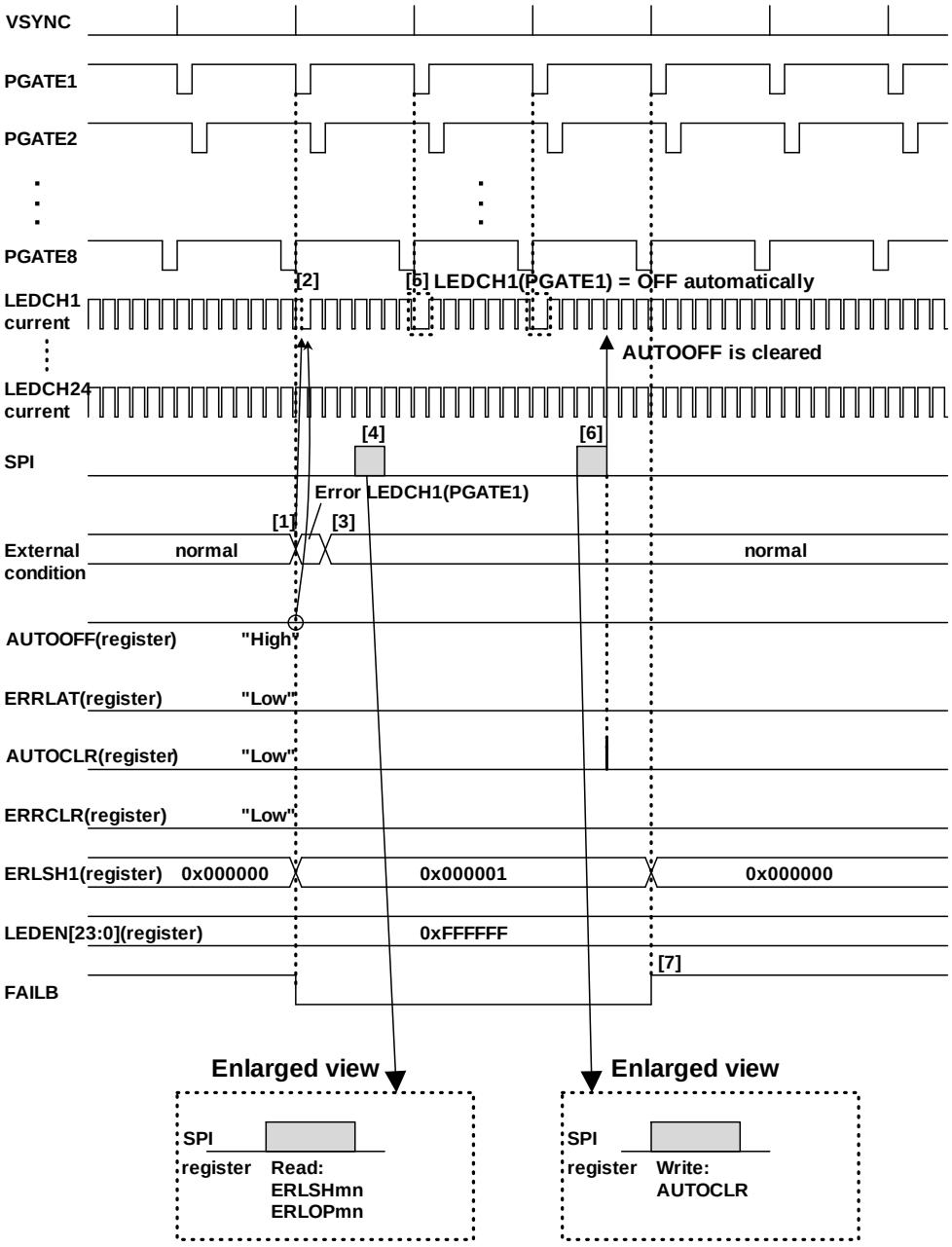


Figure 41. Error Sequence for the register AUTOOFF = 1

[1] If LED Short Error is detected, FAILB asserts LOW.
[2] LEDCH1 output is turned off automatically. (Only target timing (PGATE1))
[3] The external condition turns to normal. The LEDCH1 = OFF continues, and FAILB keeps LOW.
[4] By reading the register ERLSHmn, ERLOPmn, the abnormal LED component can be distinguished.
[5] Once LEDCH1(PGATE1) is off automatically, IC does not judge the LED Short Error status. The LED keeps off.
[6] The register AUTOCLR = 1 is written, The automatical off status is cleared.
[7] IC judges LED Short Error. As the external condition is normal, LED turns on and ERLSH1 = 0x000000 and FAILB = HIGH.

(Case) the register ERRLAT = 0 and AUTOOFF = 0
[2] When the abnormal is detected, LED does not turn off automatically.
[3] If the abnormal state is released, LED turn on again.

5. ERROR Detection and Release – continued

(11) Error Sequence for the Register ERRLAT

ERRLAT keeps the abnormal state as latch state, even if that is released.

(Case) the register ERRLAT = 1 and AUTOOFF = 0

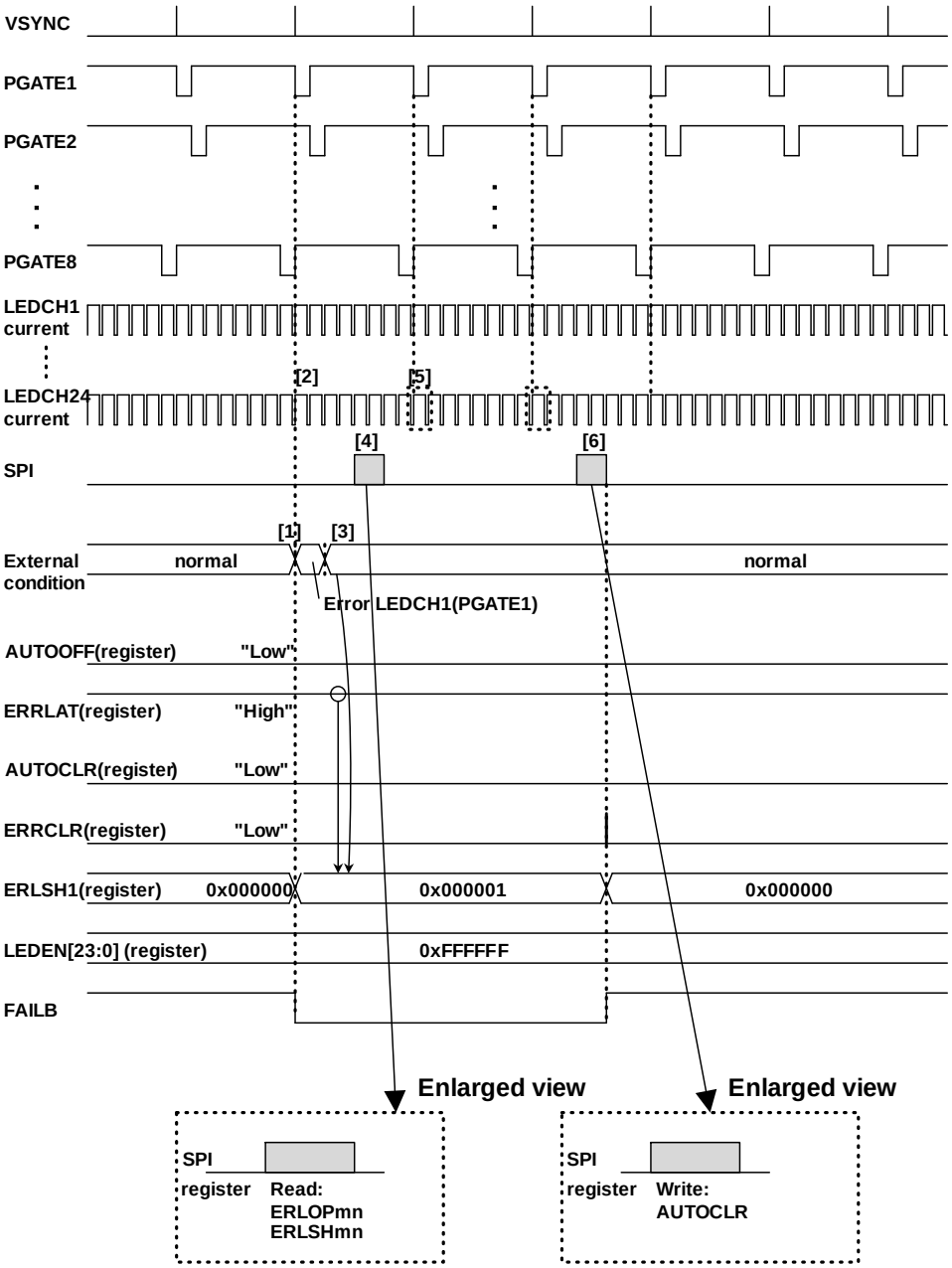


Figure 42. Error Sequence for the register ERRLAT = 1

[1] If LED Short Error is detected, FAILB asserts LOW.
[2] LEDCH1 output is still turned on, because AUTOOFF is 0.
[3] The external condition turns to normal. The register ERLSH1 keeps 0x000001 and FAILB asserts LOW.
[4] By reading the register ERLSHmn, ERLOPmn, the abnormal LED component can be distinguished.
[5] LEDCH1 output is still turned on, because AUTOOFF is 0.
[6] The register ERRCLR = 1 is written, The register ERLSH1 is cleared to 0x000000 and FAILB asserts HIGH.

Condition for Protections

Table 49. Protection Table 1

		LED OPEN		LED SHORT	
		ERRLAT = 0	ERRLAT = 1	ERRLAT = 0	ERRLAT = 1
Protection	Pin	LEDCHn in every PGATEm			
	Detection Condition	LEDEN[n-1] = 1 and DTYmn > 0 and LOPEN = 1 and LEDCHn ON and $V_{LEDCHn} \leq 0.15$ V		LEDEN[n-1] = 1 and DTYmn > 0 and LSHEN = 1 and LEDCHn ON and $V_{LEDCHn} \geq V_{SHDET}$	
	Release Condition	LEDEN[n-1] = 0 or LOPEN = 0 or LEDCHn ON and $V_{LEDCHn} > 0.15$ V		LEDEN[n-1] = 0 or LSHEN = 0 or LEDCHn ON and $V_{LEDCHn} < V_{SHDET}$	
Error Setting	Error Enable	LOPEN		LSHEN	
	SSMASK	O		O	
	ERRMASK	O		O	
	ERRLAT	O		O	
	AUTOOFF	O		O	
Error Flag	Error Register	ERLOP[n-1]		ERLSH[n-1]	
	FAILB *(Note 1)*	LOW		LOW	
	Clear Condition	Protection released	ERRCLR = 1	Protection released	ERRCLR = 1
Error Channel	AUTOOFF = 0	OFF by LEDEN[n-1] = 0 *(Note 2)*		OFF by LEDEN[n-1] = 0 *(Note 2)*	
	AUTOOFF = 1	OFF automatically		OFF automatically	

'O': It has the function.

(Note 1) When the IC detects VCCUVLO or VREG15UVLO or TSD or EN, it cannot detect other protection.
(Note 2) Write LEDEN[n-1] = 0 when the error channel is turned off.
(Note) m = 1 to 8, n = 1 to 24

Table 50. Protection Table 2

		ISET OCP		ISET OPEN	
		ERRLAT = 0	ERRLAT = 1	ERRLAT = 0	ERRLAT = 1
Protection	Pin	ISET			
	Detection Condition	$R_{ISETSP} \leq$ max 16 kΩ		$R_{ISETOPEN} \geq$ min 340 kΩ	
	Release Condition	$R_{ISETSP} >$ max 16 kΩ		$R_{ISETOPEN} <$ min 340 kΩ	
Error Setting	Error Enable	-		-	
	SSMASK	O		O	
	ERRMASK	-		-	
	ERRLAT	O		O	
	AUTOOFF	-		-	
Error Flag	Error Register	ERISETOCP		ERISETOPEN	
	FAILB *(Note 1)*	LOW		LOW	
	Clear Condition	Protection released	ERRCLR = 1	Protection released	ERRCLR = 1
Error Channel	AUTOOFF = 0	-		-	
	AUTOOFF = 1	-		-	

'-': It does not have the function.

(Note 1) When the IC detects VCCUVLO or VREG15UVLO or TSD or EN, it cannot detect other protection.

Condition for Protections – continued

Table 51. Protection Table 3

		PGATEm to VINSW SHORT	PGATEm to GND SHORT
Protection	Pin	PGATEm	
	Detection Condition	PGATEm Rise edge and V_{PGATEm} > VINSW-1.5 V	PGATEm Fall edge and V_{PGATEm} ≤ VINSW-2.5 V
	Release Condition	ERRCLR = 1	ERRCLR = 1
Error Setting	Error Enable	-	-
	SSMASK	-	-
	ERRMASK	-	-
	ERRLAT	-	-
	AUTOOFF	-	-
Error Flag	Error Register	ERPGVINSH[m-1]	ERPGGSH[m-1]
	FAILB*(Note 1)*	LOW	LOW
	Clear Condition	ERRCLR = 1	ERRCLR = 1
Error Channel	AUTOOFF = 0	-	-
	AUTOOFF = 1	-	-

'-': It does not have the function.

(Note 1) When the IC detects VCCUVLO or VREG15UVLO or TSD or EN, it cannot detect other protection.
(Note) m = 1 to 8

Table 52. Protection Table 4

		VINSW OVP		Short of Adjacent LEDCHn
		ERRLAT = 0	ERRLAT = 1	
Protection	Pin	VINSW		LEDCHn
	Detection Condition	V_{VINSW} > $V_{VINSWOVPREF}$		LSHEXE = 1 before TURNONWAIT time and LEDCHn OFF and V_{LEDCHn} < V_{SHDET} during short check sequence
	Release Condition	V_{VINSW} ≤ $V_{VINSWOVPREF}$ × 0.9		ERRCLR = 1
Error Setting	Error Enable	VINSWOVPEN		-
	SSMASK	O		-
	ERRMASK	-		-
	ERRLAT	O		-
	AUTOOFF	-		-
Error Flag	Error Register	ERVINSWOVP		ERLED[n-1]
	FAILB*(Note 1)*	LOW		LOW
	Clear Condition	Protection released	ERRCLR = 1	ERRCLR = 1
Error Channel	AUTOOFF = 0	-		-
	AUTOOFF = 1	-		-

'-': It does not have the function.

(Note 1) When the IC detects VCCUVLO or VREG15UVLO or TSD or EN, it cannot detect other protection.
(Note) n = 1 to 24

Condition for Protections – continued

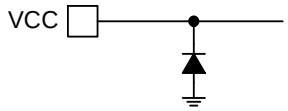
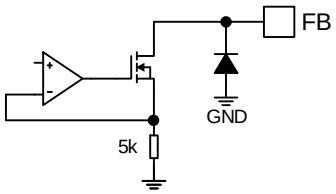
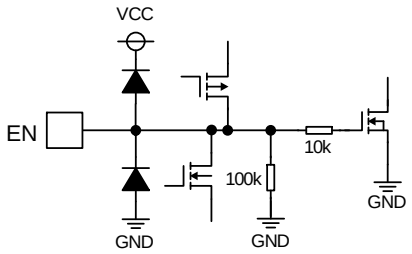
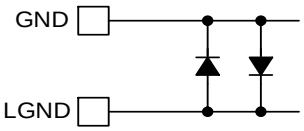
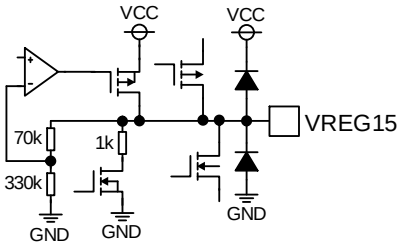
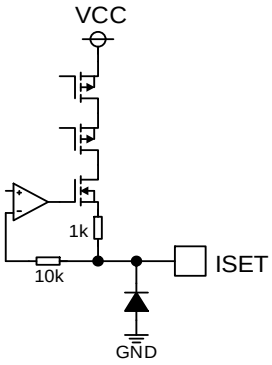
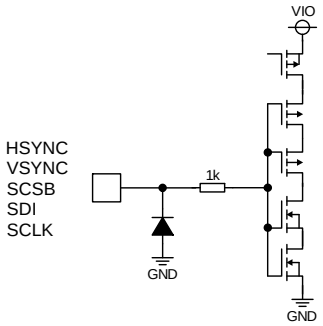
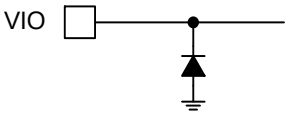
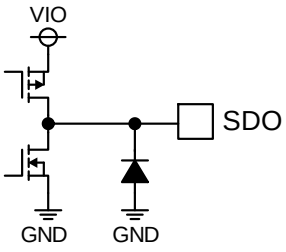
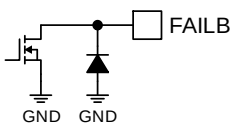
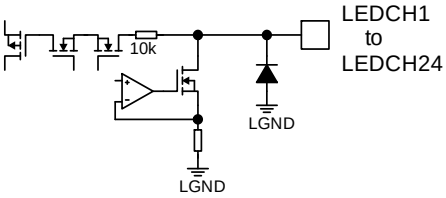
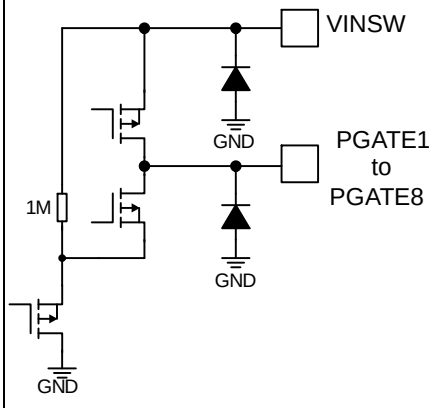
Table 53. Protection Table 5

		VCCUVLO	VREG15UVLO	VIOUVLO
Protection	Pin	VCC	VREG15	VIO
	Detection Condition	V_{CC} ≤ 2.55 V	V_{VREG15} ≤ 1.3 V	V_{VIO} ≤ 1.41 V
	Release Condition	V_{CC} ≥ 2.65 V	V_{VREG15} ≥ 1.35 V	V_{VIO} ≥ 1.46 V
Error Setting	Error Enable	-	-	-
	SSMASK	-	-	-
	ERRMASK	-	-	-
	ERRLAT	-	-	-
	AUTOOFF	-	-	-
Error Flag	Error Register	-	-	-
	FAILB*(Note 1)*	-	-	-
	Clear Condition	-	-	-
Error Channel	AUTOOFF = 0	-	-	-
	AUTOOFF = 1	-	-	-

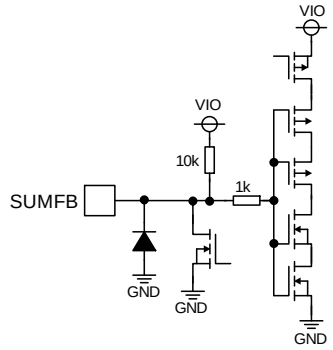
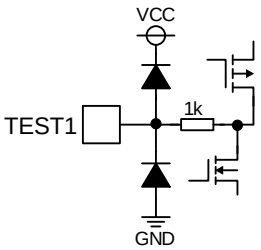
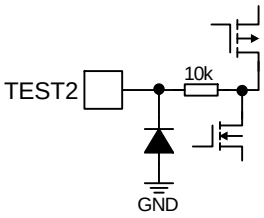
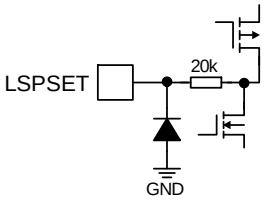
'-': It does not have the function.

(Note 1) When the IC detects VCCUVLO or VREG15UVLO or TSD or EN, it cannot detect other protection.

I/O Equivalence Circuit

VCC	FB	EN
		
GND / LGND	**VREG15**	**ISET**
		
HSYNC / VSYNC / SCSB / SDI / SCLK	**VIO**	**SDO**
		
FAILB	**LEDCH1 to LEDCH24**	**PGATE1 to PGATE8 / VINSW**
		

I/O Equivalence Circuit – continued

SUMFB	TEST1	TEST2
		
LSPSET		
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

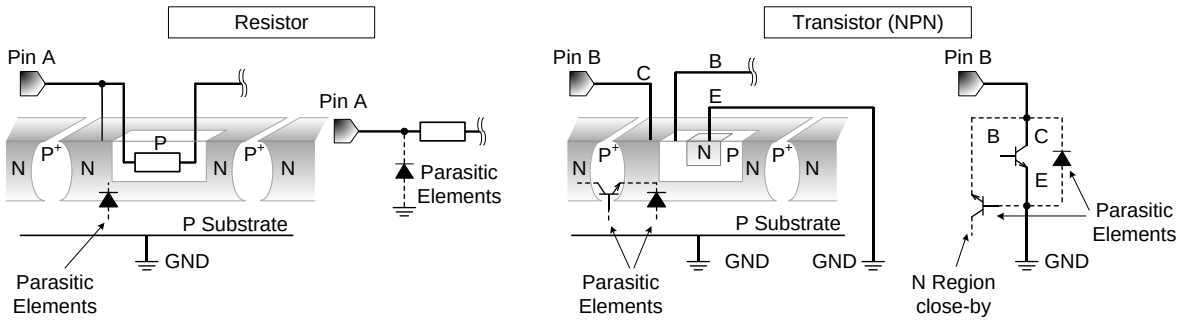


Figure 43. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.
"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.
"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

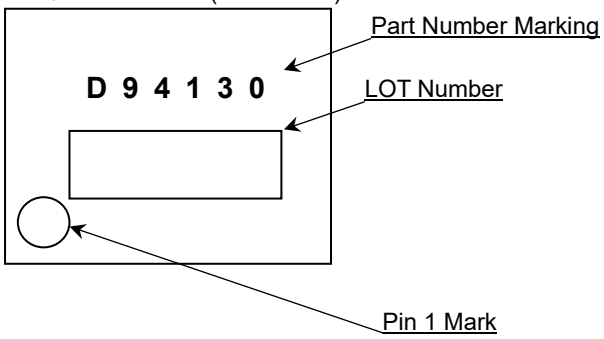
B	D	9	4	1	3	0	x	x	x	-	ME2

Package
MUF: VQFN56FCV080
EFV: HTSSOP-B54

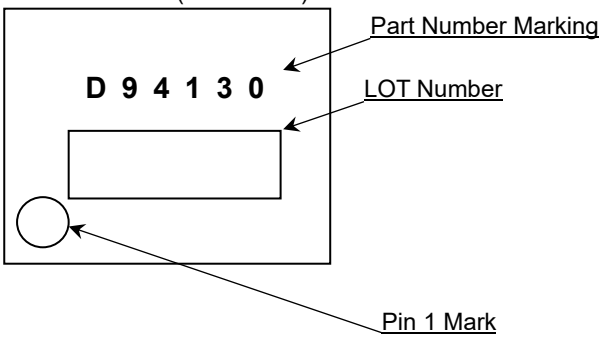
Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram

VQFN56FCV080 (TOP VIEW)

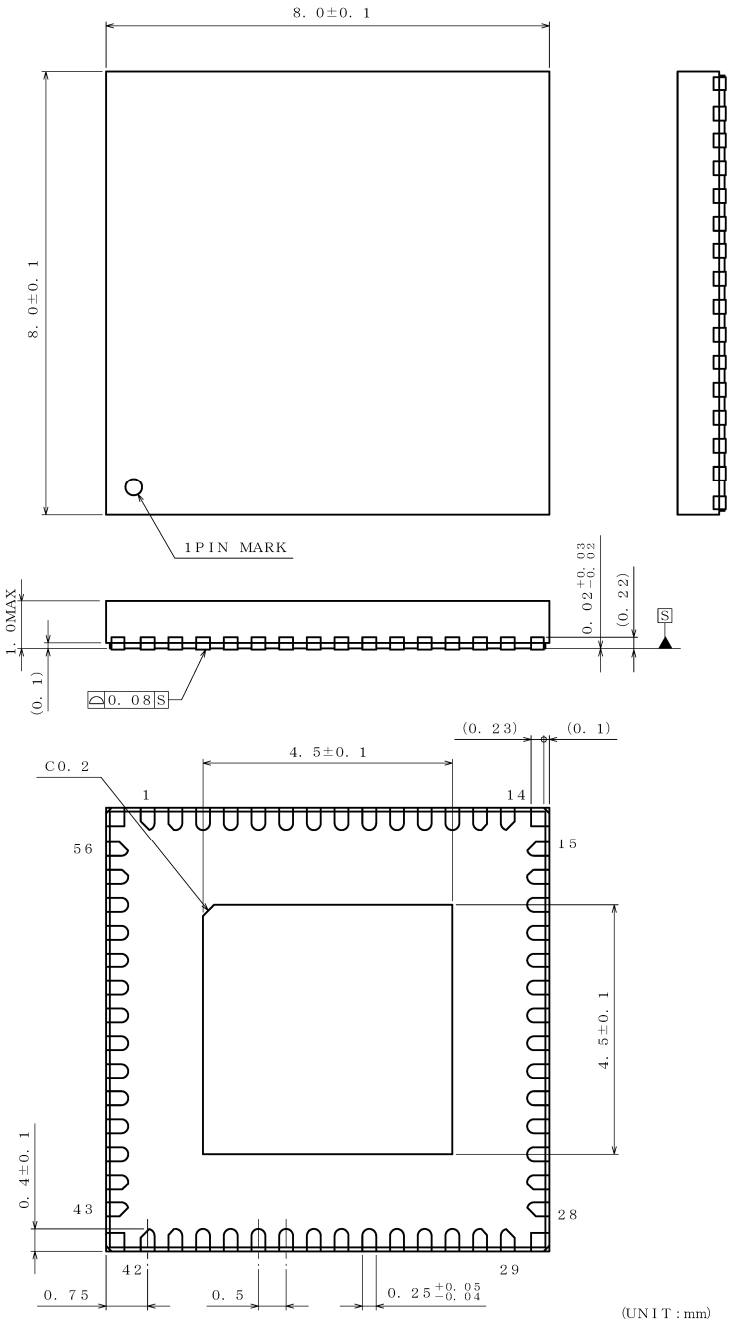


HTSSOP-B54 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN56FCV080



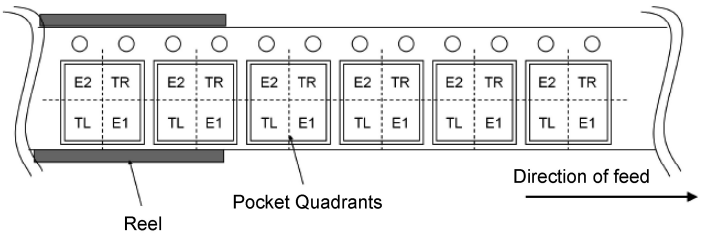
(UNIT:mm)

PKG:VQFN56FCV080
Drawing No. EX433-5001

NOTE: Dimensions in ( ) for reference only.

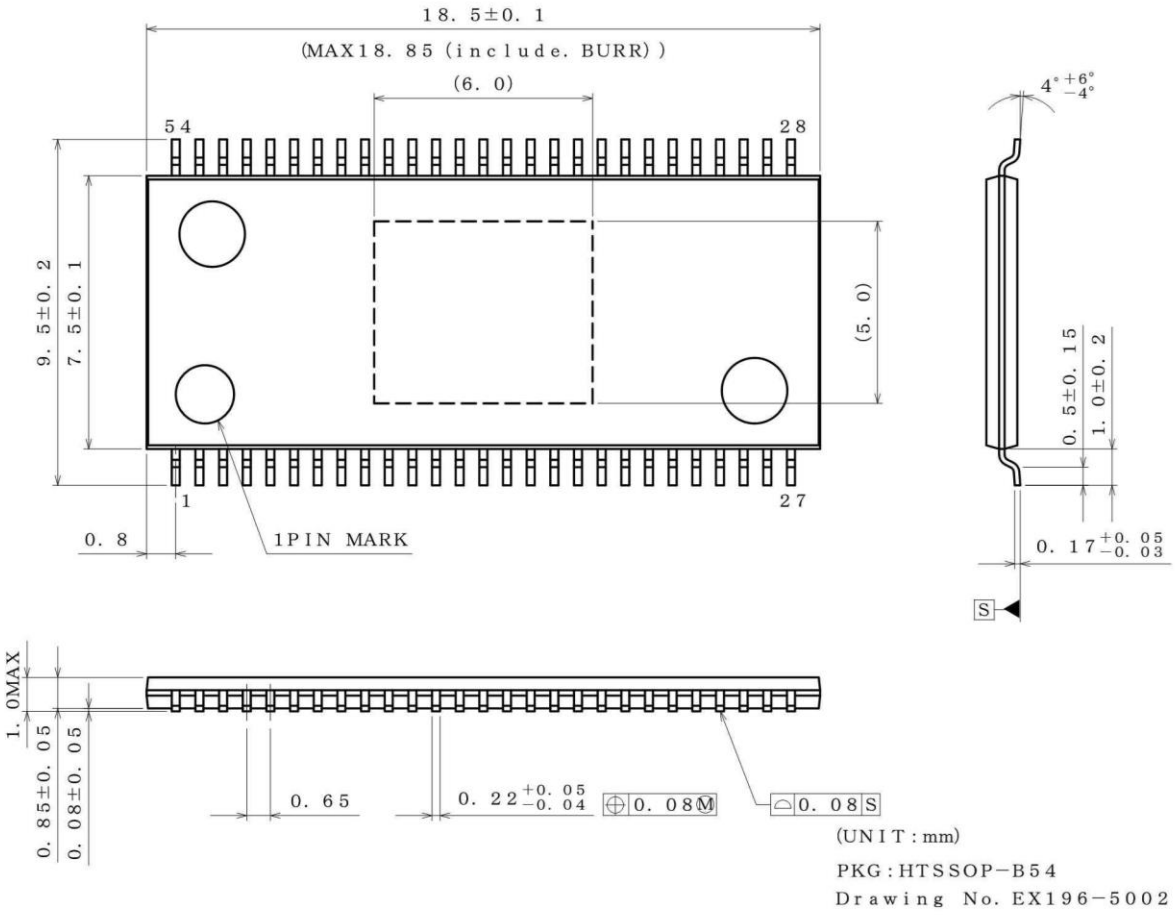
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



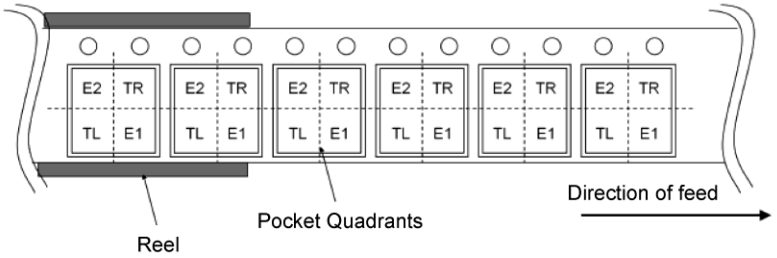
Physical Dimension and Packing Information - continued

Package Name	HTSSOP-B54



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Data	Revision	Changes
17.Aug.2022	001	New release
02.Dec.2022	002	(1) Page 39 Modified description of MSMODE register. (2) Page 49, 50 Added VINSW pin to the timing chart.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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