# BlueNRG-2N

Datasheet

## Bluetooth® Low Energy wireless network coprocessor

WLCSP34


QFN32

| Product status link |
|---|
| BlueNRG-2N |

| Product summary | |
|---|---|
| Order codes | BlueNRG-232N |
| | BlueNRG-234N |

## Features

- Low-power radio performance
  - Sleep current consumption down to 900 nA
  - TX current consumption 6.8 mA (@ -2 dBm, 3.0 V)
  - RX current consumption 6.2 mA (@ sensitivity level, 3.0 V)
  - Up to +8 dBm programmable output power level (@ antenna connector)
  - Excellent RF link budget (up to 96 dB)
  - Integrated DC-DC step-down converter and LDO regulators
- Bluetooth® 5.2 certified
  - Multi-master to multi-slave communication guaranteed
  - 2 masters to 6 slaves simultaneously
  - Up to 8 simultaneous connections handled
  - LE data length extension (up to 700 kbps at application level)
  - Over-the-air firmware update is 2.5 times faster
  - LE Privacy 1.2
  - Reduces the ability to be tracked over a period of time by changing the address on a frequent basis without involving the HOST and saving battery life
  - LE secure connections
  - The pairing mechanism is established with the elliptic curve Diffie-Hellman (ECDH) key agreement protocol enabling a secure key exchange mechanism preventing eavesdropping

## Applications

- Watches
- Fitness, wellness and sports
- Consumer medical
- Security/proximity
- Remote control
- Home and industrial automation
- Assisted living
- Mobile phone peripherals
- Lighting
- PC peripherals

## Description

The BlueNRG-2N is an ultra low power (ULP) network coprocessor solution for Bluetooth® low energy applications.

It embeds the STMicroelectronics's state-of-the-art RF radio IPs combining unparalleled performance with extremely long battery lifetime.

It is fully compliant with Bluetooth core specification version 5.2 and supports enhanced features such as state-of-the-art security, privacy, and extended packet length for faster data transfer up to 700 kbps at application level.

The BlueNRG-2N is Bluetooth® 5.2 certified ensuring interoperability with the latest generation of smartphones and other host devices.

The Bluetooth low energy stack runs on the embedded ARM Cortex-M0 core. The STMicroelectronics BLE stack is stored into the on-chip non-volatile Flash memory and it can be easily upgraded via SPI/UART as well through the dedicated STMicroelectronics software tools.

# 1 High performance and benefits

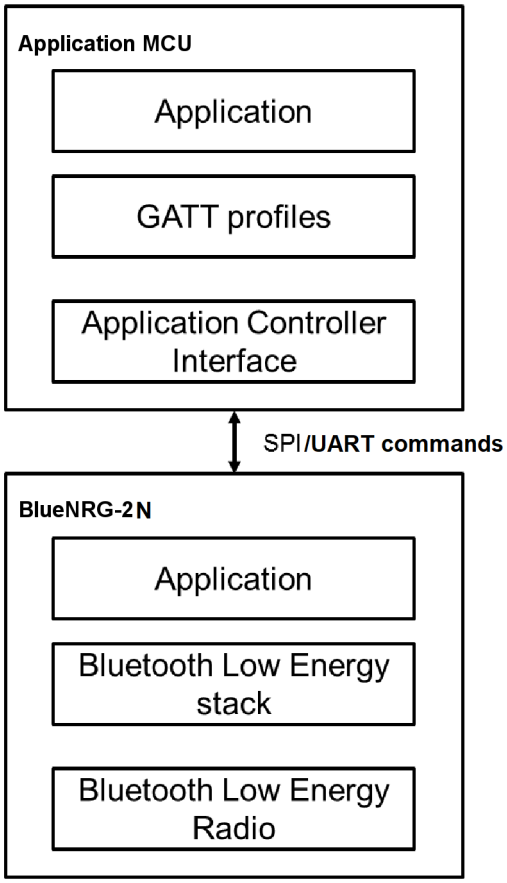
The BlueNRG-2N shows a reliable communication thanks to the best-in-class output power level assuring a robust communication even in a noisy corrupted scenario without compromising the overall power consumption.

The BLUENRG-2N collaterals include comprehensive tools for developers such as a full featured SDK including:

- Templates
- High-level abstraction layer APIs (no BLE expertise required)
- Real-time debug capabilities

A dedicated firmware is provided to support the interface with an external application processor. The whole Bluetooth low energy stack runs in the BlueNRG-2N; the GATT profiles are provided to run in the application processor together with the application code. The figure below shows the network processor RF software layers.

**Figure 1. BlueNRG-2N network processor RF software layers**



# 2 Functional details

The BlueNRG-2N integrates:

- ARM Cortex-M0 core
- Power management
- Clocks
- Bluetooth low energy radio
- Random number generator (RNG) (reserved for Bluetooth low energy protocol stack, but user applications can read it)
- External microcontroller interface (SPI/UART)
- Public key cryptography (PKA) (reserved for Bluetooth low energy protocol stack)

## 2.1 Core

The ARM® Cortex®-M0 processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8-bit and 16-bit devices.

The BlueNRG-2N has an embedded ARM core and is therefore compatible with all ARM tools and software. The ARM Cortex M0 processor is reserved for internal operations and it is not open to customer application developments.

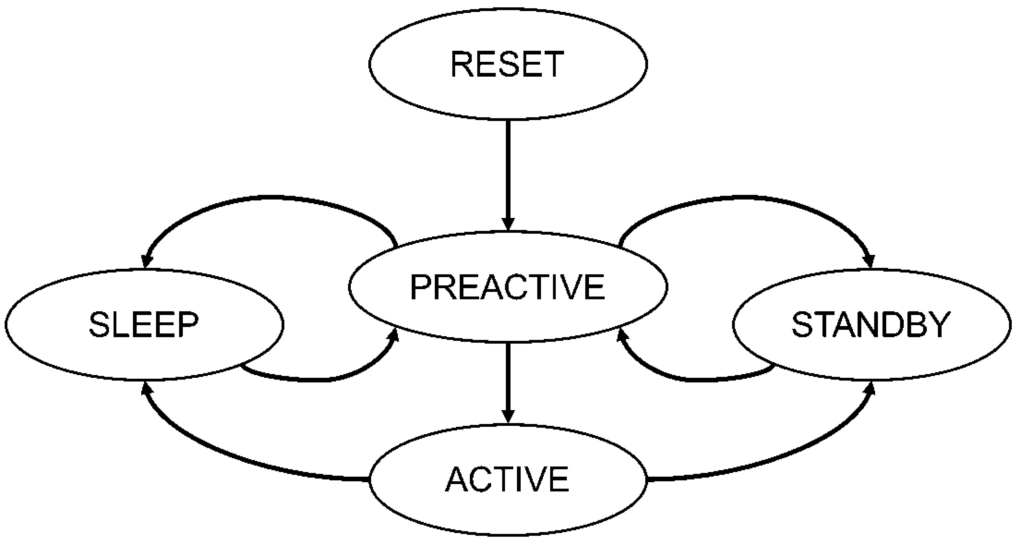
## 2.2 Power management

The BlueNRG-2N integrates both a low dropout voltage regulator (LDO) and a step-down DC-DC converter to supply the internal BlueNRG-2N circuitry.

The BlueNRG-2N most efficient power management configuration is with DC-DC converter active where best power consumption is obtained without compromising performances. Nevertheless, a configuration based on LDO can also be used, if needed.

A simplified version of the state machine is shown below.

**Figure 2. BlueNRG-2N power management state machine**



### 2.2.1 State description

#### 2.2.1.1 *Preactive state*

The preactive state is the default state after a POR event.

In this state:

- All the digital power supplies are stable.
- The high frequency clock runs on internal fast clock RC oscillator (16 MHz).
- The low frequency clock runs on internal RC oscillator (32.768 kHz).

#### 2.2.1.2 *Active state*

In this state:

- The high frequency runs on the accurate clock (32 MHz ±50 ppm) provided by the external XO. The internal fast clock RO oscillator is switched off.

#### 2.2.1.3 *Standby state*

In this state:

- Only the digital power supplies necessary to keep the RAM in retention are used.

#### 2.2.1.4 *Sleep state*

In this state:

- Only the digital power supplies necessary to keep the RAM in retention are used
- The low frequency oscillator is switched on

The wake-up from this low power state is driven by the following sources:

- Internal timers
- SPI CS (SPI mode only)

#### 2.2.1.5 *Power saving strategy*

The application power saving strategy is based on clock stopping, dynamic clock gating, digital power supply switch-off and analog current consumption minimization.

A summary of functional blocks versus the BlueNRG-2N states is provided below.

**Table 1. Relationship between the BlueNRG-2N states and functional blocks**

| Functional blocks | RESET | STANDBY | SLEEP | Preactive | Active | LOCK RX/ LOCK TX | RX | TX |
|---|---|---|---|---|---|---|---|---|
| LDO_SOFT_1V2 or LDO_SOFT_0V9 | OFF | ON | ON | ON | ON | ON | ON | ON |
| LDO_STRONG_1V2 | OFF | OFF | OFF | ON | ON | ON | ON | ON |
| LDO_DIG_1V8 | OFF | OFF | OFF | ON | ON | ON | ON | ON |
| SMPS | OFF | OFF | OFF | ON | ON | ON | ON | ON |
| LDO_DIG_1V2 | OFF | OFF | OFF | ON | ON | ON | ON | ON |
| BOR | OFF | OFF | OFF | ON | ON | ON | ON | ON |
| 16 MHz RO | OFF | OFF | OFF | ON | OFF | OFF | OFF | OFF |
| 32 MHz XO | OFF | OFF | OFF | OFF | ON | ON | ON | ON |
| 32 kHz RO or XO | OFF | OFF | ON | ON | ON | ON | ON | ON |

## 2.3 Clocks and reset management

The BlueNRG-2N embeds an RC low-speed frequency oscillator at 32 kHz and an RO high-speed frequency oscillator at 16 MHz.

The low-frequency clock is used in low power mode and can be supplied either by a 32.7 kHz oscillator that uses an external crystal and guarantees up to ±50 ppm frequency tolerance, or by a ring oscillator, which does not require any external components.

The primary high-speed frequency clock is a 32 MHz crystal oscillator. A fast-starting 16 MHz ring oscillator provides the clock while the crystal oscillator is starting up. Frequency tolerance of the high-speed crystal oscillator is ±50 ppm.

Usage of the high-speed crystal usage is strictly necessary for RF communications.

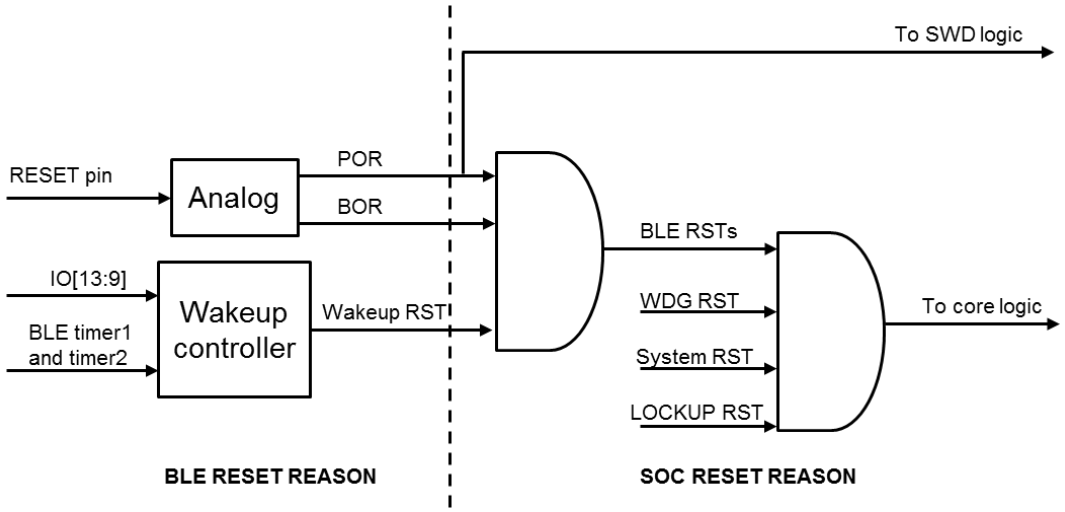
### 2.3.1 Reset management

Figure 3. Reset and wake-up generation shows the general principle of reset. Releasing the reset pin takes the chip out of shutdown state. The wake-up logic is powered and receives the POR. Each time the wake-up controller decides to exit sleep or standby modes, it generates a reset for the core logic. The core logic can also be reset by:

- Watchdog
- Reset request from the processor (system reset)
- LOCKUP state of the Cortex-M0

The SWD logic is reset by the POR. It is important to highlight that the reset pin actually powers down the chip, so it is not possible to perform debug access with system under reset.

**Figure 3. Reset and wake-up generation**




If, for any reason, the user would like to power off the device there are two options:

1. Force RESETN pin to ground, keeping VBAT level
2. To put VBAT pins to ground (e.g. via a transistor)

In the second option, care must be taken to ensure that no voltage is applied to any of the other pins as the device can be powered and have an anomalous power consumption. The ST recommendation is to use RESETN whenever it is possible.

#### 2.3.1.1 *Power-on-Reset*

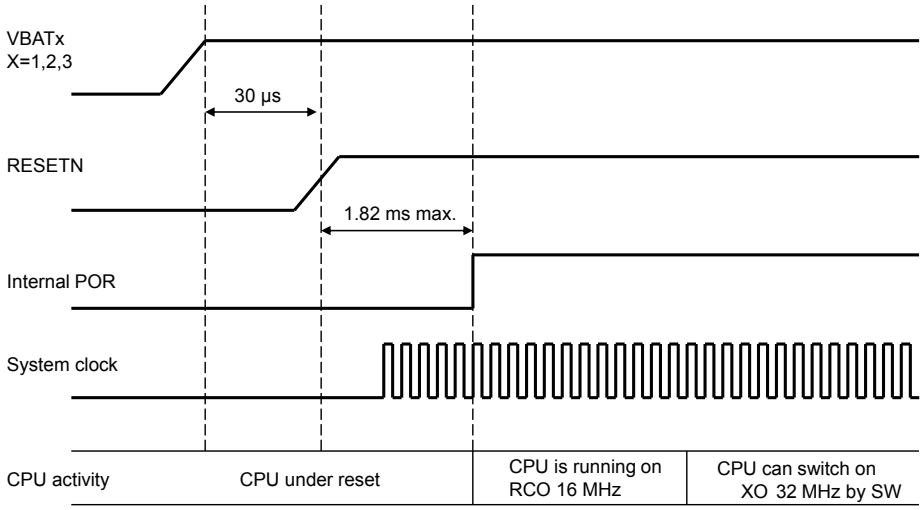
The Power-on-Reset (POR) signal is the combination of the POR signal and the BOR signal generated by the analog circuitry contained in the BlueNRG-2N device. The combination of these signals is used to generate the input to the Cortex-M0, which is used to reset the debug access port (DAP) of the processor. It is also used to generate the signal, which resets the debug logic of the Cortex-M0. The POR signal also resets the TAP controller of the BlueNRG-2N and a part of the Flash controller (managing the Flash memory boot, which does not need to be impacted by system resets).

The BOR reset is enabled by default. At software level, it can be decided to change the default values after reset.

#### 2.3.1.2 *Power-up sequence*

The starting sequence of the BlueNRG-2N supply and reset signal is shown below.

**Figure 4. BlueNRG-2N power-up sequence**

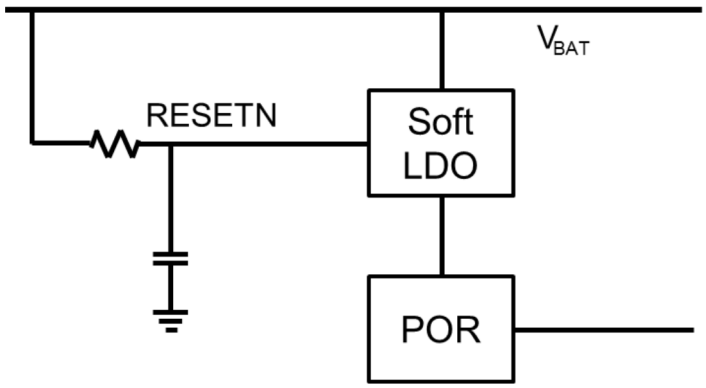



- The VBATx power must only be raised when RESETN pin is low.
- The different VBATx (x=1,2,3) power can be raised separately or together.
- Once the VBATx (x=1,2,3) reaches the nominal value, the RESETN pin could be driven high after a 30 us.
- The internal POR is released once internal LDOs are established and RCO clock is ready.
- The system starts on RCO 16 MHz clock system. The software is responsible for configuring the XO 32 MHz when necessary.

*Note: The minimum negative pulse to reset the system must be at least 30 µs.*

The POR circuit is powered by a 1.2 V regulator, which must also be powered up with the correct startup sequence. Before VBAT has reached the nominal value, RESETN line must be kept low. An external RC circuit on RESETN pin adds a delay that can prevent RESETN signal from going high before VBAT has reached the nominal value.

**Figure 5. Reset circuit**



If the above conditions are not satisfied, ST cannot guarantee the correct operation of the device.

The BlueNRG-2N could inform the external microcontroller via the host interface protocol on the internal reset reason, which includes: POR, BOR, watchdog, lockup.

## 2.4 TX/RX event alert

The BlueNRG-2N is provided with the ANATEST1 (pin 14 for QFN32 package, pin D4 for WCSP34 package) signal which alerts forthcoming transmission or reception event. The ANATEST1 pin switches to high level about 18 µs before transmission before reception. Then, it switches to low level at the end of the event. The signal can be used for controlling external antenna switching and supporting coexistence with other wireless technologies.

## 2.5 SWD debug feature

The BlueNRG-2N embeds the ARM serial wire debug (SWD) port. It is two pins (clock and single bi-directional data) debug interface, providing all the debug functionality plus real-time access to system memory without halting the processor or requiring any target resident code.

The SWD interface is provided to allow firmware upgrade on the device in the production lines.

**Table 2. SWD port**

| Pin functionality | Pin name | Pin description |
|---|---|---|
| SWCLK | IO9 | SWD clock signal |
| SWDIO | IO10 | SWD data signal |

The Cortex-M0 subsystem of the BlueNRG-2N embeds four breakpoints and two watchpoints.

## 2.6 Bluetooth low energy radio

The BlueNRG-2N integrates an RF transceiver compliant to the Bluetooth specification and to the standard national regulations in the unlicensed 2.4 GHz ISM band.

The RF transceiver requires very few external discrete components. It provides 96 dB link budgets with excellent link reliability, keeping the maximum peak current below 15 mA.

In transmit mode, the power amplifier (PA) drives the signal generated by the frequency synthesizer out to the antenna terminal through a very simple external network. The power delivered as well as the harmonic content depends on the external impedance seen by the PA.

### 2.6.1 Radio operating modes

Several operating modes are defined for the BlueNRG-2N radio:

- Reset mode
- Sleep mode
- Active mode
- Radio mode
  - RX mode
  - TX mode

In Reset mode, the BlueNRG-2N is in ultra-low power consumption: all voltage regulators, clocks and the RF interface are not powered. The BlueNRG-2N enters Reset mode by asserting the external Reset signal. As soon as it is de-asserted, the device follows the normal activation sequence to transit to active mode.

In sleep mode either the low speed crystal oscillator or the low speed ring oscillator are running, whereas the high speed oscillators are powered down as well as the RF interface. The state of the BlueNRG-2N is retained and the content of the RAM is preserved.

While in sleep mode, the BlueNRG-2N waits until an internal timer expires and then it goes into active mode.

In active mode the BlueNRG-2N is fully operational: all interfaces, including RF, are active as well as all internal power supplies together with the high speed frequency oscillator. The MCU core is also running.

Radio mode differs from active mode as the RF transceiver is also active and is capable of either transmitting or receiving.

## 2.7 Firmware image

The Bluetooth Low Energy stack runs on the embedded ARM Cortex-M0 core. The stack is stored on the on-chip non-volatile Flash memory at a specific offset (0x2000) and can be easily upgraded through a dedicated pre-programmed device updater FW stored at device Flash base address, and using the selected hardware interface to external microcontroller. If DIO3 is high at power-up or hardware reset the device updater FW is activated.

The device comes pre-programmed with a production-ready stack image (version may change at any time without notice). A different or more up-to-date stack image can be downloaded from the ST website and programmed on the device through the ST provided software tools.

*Note: Only the BlueNRG-2N Bluetooth LE stack images provided by ST are allowed to run on the BlueNRG-2N device.*

## 2.8 Pre-programmed bootloader

The BlueNRG-2N device has also a pre-programmed bootloader supporting UART protocol with automatic baud rate detection. The main features of the embedded bootloader are:

- Auto baud rate detection up to 460 kbps
- Flash sector erase
- Flash programming
- Flash readout protection enable

The pre-programmed bootloader is an application which is stored on the BlueNRG-2N internal ROM at manufacturing time by STMicroelectronics. This application allows upgrading the device Flash with an authorized user application based on offset 0x2000, using a serial communication channel (UART).

Bootloader is activated by hardware by forcing DIO7 high during power-up or hardware reset, otherwise, the application residing in Flash is launched.

*Note: The customer application must ensure that DIO7 is forced low during power-up. Bootloader protocol is described in a separate application note.*

## 2.9 Unique device serial number

The BlueNRG-2N device has a unique six-byte serial number stored at address 0x100007F4: it is stored as two words (8 bytes) at addresses 0x100007F4 and 0x100007F8 with unique serial number padded with 0xAA55.

Specific API allows such locations to get access.

# 3 Pin description

The BlueNRG-2N comes in two package versions: WCSP34 offering 14 GPIOs, QFN32 offering 15 GPIOs. Figure 6. BlueNRG-2N pinout top view (QFN32) shows the QFN32 pinout, and Figure 7. BlueNRG-2N ball out top view (WCSP34) shows the WCSP34 ball out.

**Figure 6. BlueNRG-2N pinout top view (QFN32)**

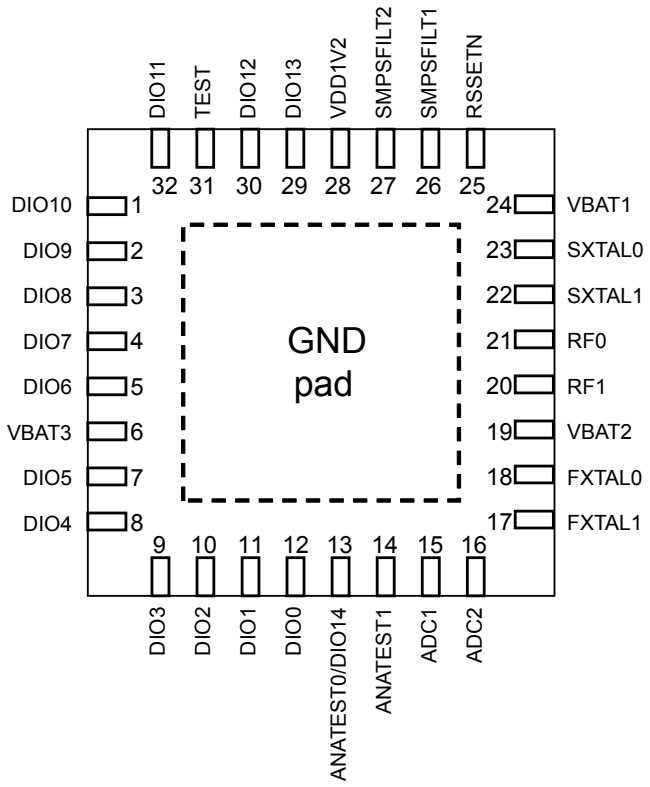


Figure 7. **BlueNRG-2N ball out top view (WCSP34)**

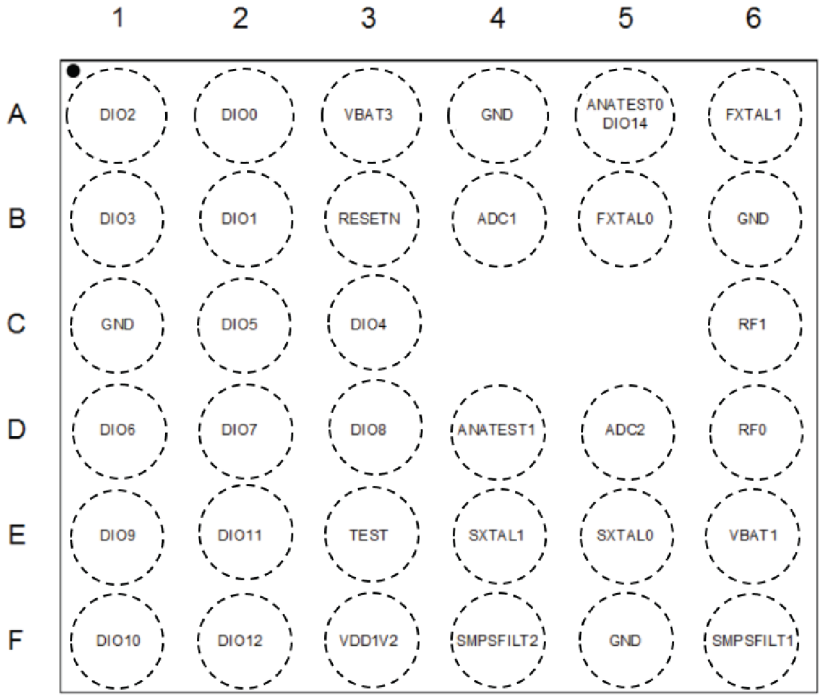


Figure 8. **BlueNRG-2N ball out bottom view (WCSP34)**

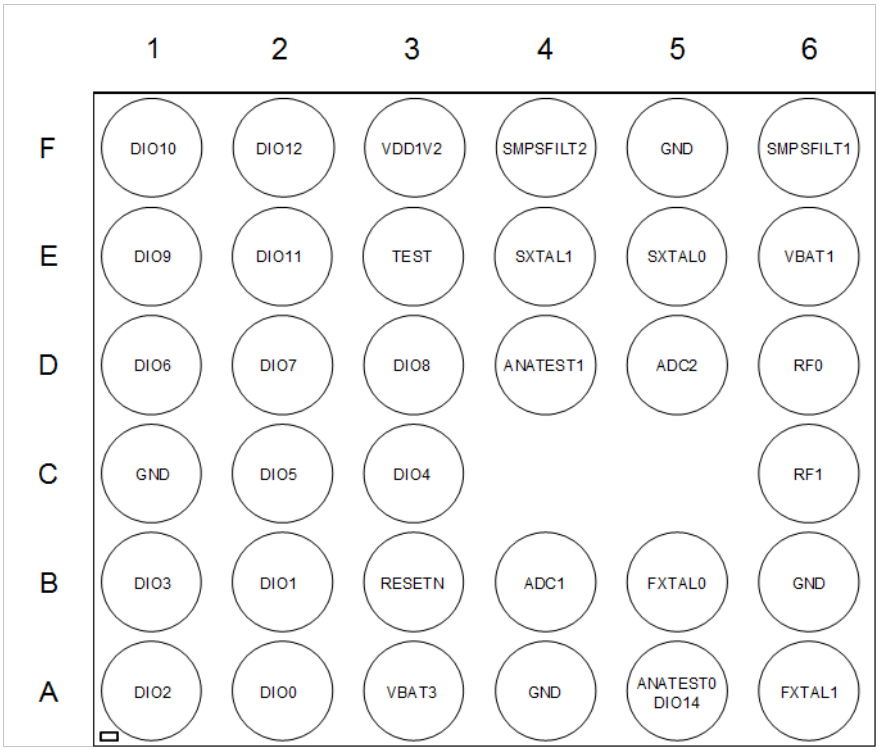



Table 3. **Pinout description**

| Pins | | Name | I/O | Description |
|---|---|---|---|---|
| QFN32 | WCSP34 | | | |
| 1 | F1 | DIO10 | I/O | SWDIO, not connected |
| 2 | E1 | DIO9 | I/O | SWCLK, not connected |
| 3 | D3 | DIO8 | I/O | UART_TXD |
| 4 | D2 | DIO7/BOOT(1) | I/O | Bootloader pin |
| | | | | SPI_IRQ |
| 5 | D1 | DIO6 | I/O | Reserved, put to ground |
| 6 | A3 | VBAT3 | VDD | Battery voltage input |
| - | - | | | |
| 7 | C2 | DIO5 | I/O | Reserved, put to ground |
| 8 | C3 | DIO4 | I/O | Reserved, put to ground |
| 9 | B1 | DIO3(2) | I/O | SPI_IN |
| 10 | A1 | DIO2 | I/O | SPI_OUT |
| 11 | B2 | DIO1 | I/O | Reserved, put to ground |
| 12 | A2 | DIO0 | I/O | SPI_CLK |
| 13 | A5 | DIO14 | I/O | Reserved, not connected |
| | | ANATEST0 | O | Analog output |
| 14 | D4 | ANATEST1 | O | Analog output, not connected |

| Pins | | Name | I/O | Description |
|---|---|---|---|---|
| QFN32 | WCSP34 | | | |
| 15 | B4 | ADC1 | I | Connect to ground |
| 16 | D5 | ADC2 | I | Connect to ground |
| 17 | A6 | FXTAL1 | I | 32 MHz crystal |
| 18 | B5 | FXTAL0 | I | 32 MHz crystal |
| 19 | - | VBAT2 | VDD | Battery voltage input |
| 20 | C6 | RF1 | I/O | Antenna + matching circuit connection |
| 21 | D6 | RF0 | I/O | Antenna + matching circuit connection |
| 22 | E4 | SXTAL1 | I | 32 kHz crystal |
| 23 | E5 | SXTAL0 | I | 32 kHz crystal |
| 24 | E6 | VBAT1 | VDD | Battery voltage input |
| 25 | B3 | RESETN | I | System reset |
| 26 | F6 | SMPSFILT1 | I | SMPS output to external filter |
| 27 | F4 | SMPSFILT2 | I/O | SMPS output to external filter/battery voltage input |
| 28 | F3 | VDD1V2 | O | 1.2V digital core output |
| 29 | - | DIO13 | I/O | Reserved, put to ground by a pull-down resistor |
| 30 | F2 | DIO12 | I/O | Connect to VDD for UART interface by a pull-up resistor<br>Connect to ground for SPI interface by a pull-down resistor |
| 31 | E3 | TEST | I | Test pin put to GND |
| 32 | E2 | DIO11 | I/O | UART_RXD/SPI_CS |
| - | A4 | GND | GND | Ground |
| - | B6 | | | |
| - | C1 | | | |
| - | F5 | | | |

1. *The pin DIO7/BOOT is monitored by bootloader after power-up or hardware reset and it should be low to prevent unwanted bootloader activation.*
2. *The pin DIO3 is monitored by the device updater FW after power-up or hardware reset and it should be low to prevent unwanted updater FW activation.*

# 4 Application circuit

The schematics below are purely indicative.

**Figure 9. Application circuit: active DC-DC converter QFN32 package**

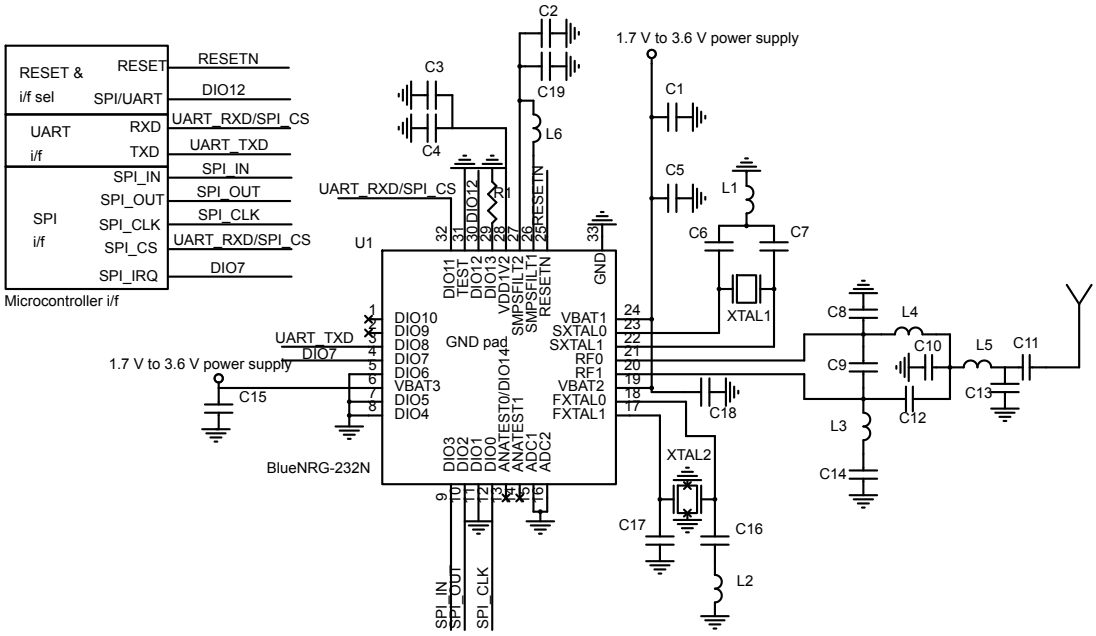



**Figure 10. Application circuit: non-active DC-DC converter QFN32 package**

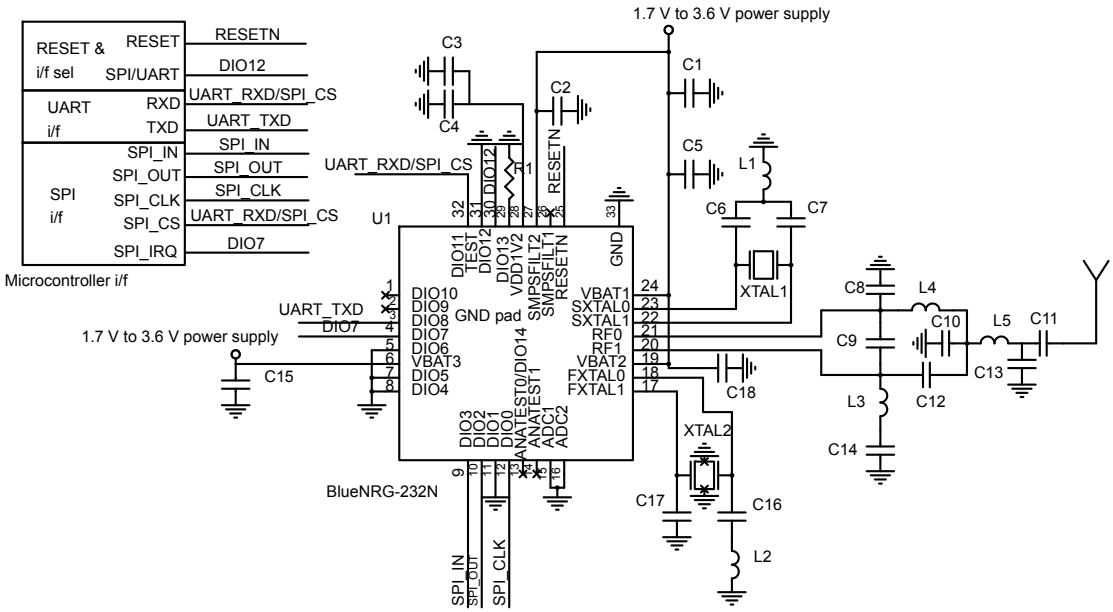


**Figure 11. Application circuit: active DC-DC converter WCSP34 package**

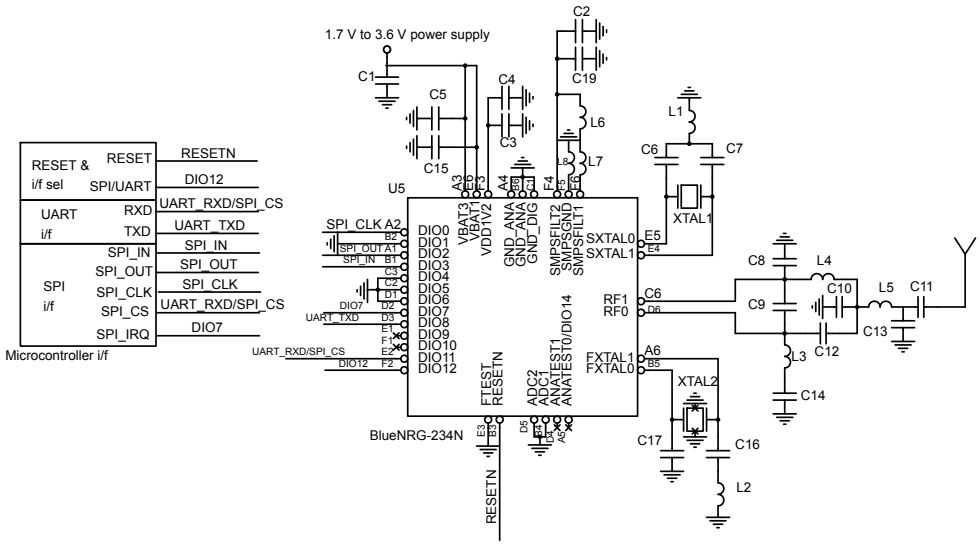



**Figure 12. Application circuit: non active DC-DC converter WCSP34 package**

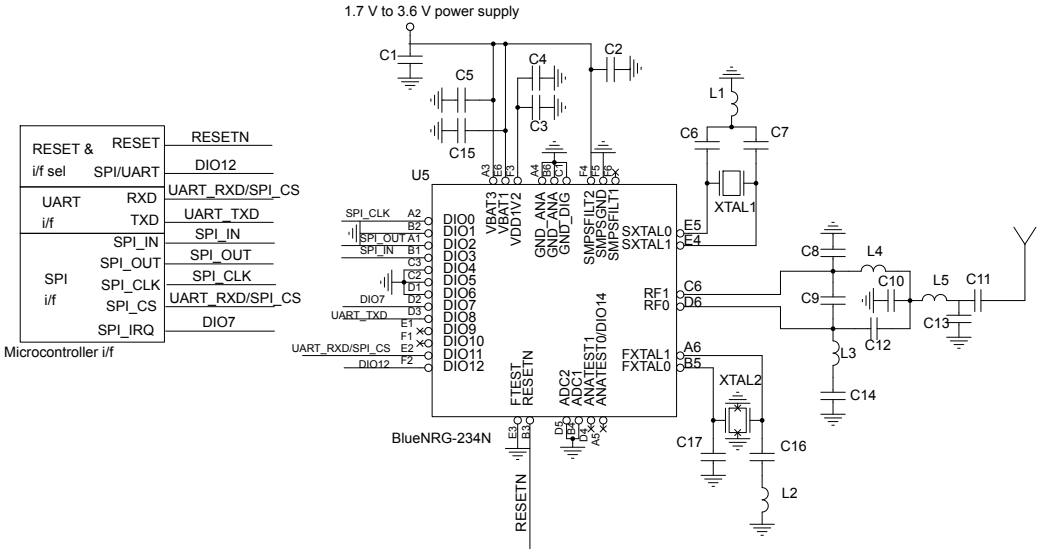


Figure 13. **Application circuit: active DC-DC converter QFN32 package with BALF-NRG-02D3 balun**

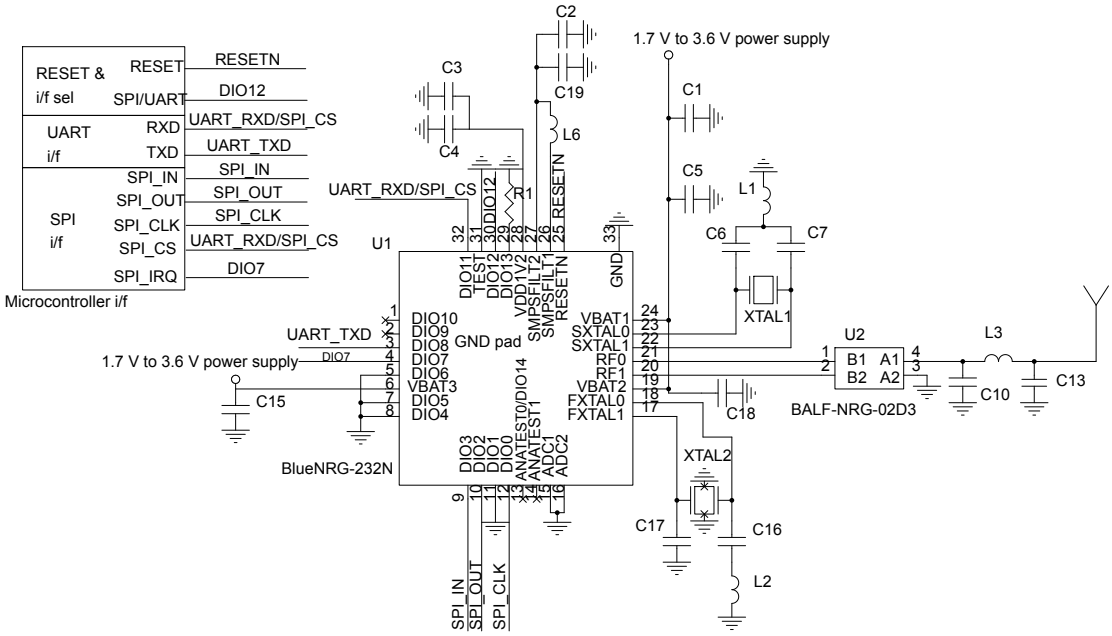



Table 4. **External component list**

| Component | Description |
|---|---|
| C1 | Decoupling capacitor |
| C2 | DC-DC converter output capacitor |
| C3 | Decoupling capacitor for 1.2 V digital regulator |
| C4 | Decoupling capacitor for 1.2 V digital regulator |
| C5 | Decoupling capacitor |
| C6 | 32 kHz crystal loading capacitor |
| C7 | 32 kHz crystal loading capacitor |
| C8 | RF balun/matching network capacitor |
| C9 | RF balun/matching network capacitor |
| C10 | RF balun/matching network capacitor |
| C11 | RF balun/matching network capacitor |
| C12 | RF balun/matching network capacitor |
| C13 | RF balun/matching network capacitor |
| C14 | RF balun/matching network capacitor |
| C15 | Decoupling capacitor |
| C16 | 32 MHz crystal loading capacitor |
| C17 | 32 MHz crystal loading capacitor |
| C18 | Decoupling capacitor |
| C19 | DC-DC converter output capacitor |
| L1 | 32 kHz crystal filter inductor |
| L2 | 32 MHz crystal filter inductor |

| Component | Description |
|---|---|
| L3 | RF balun/matching network inductor |
| L4 | RF balun/matching network inductor |
| L5 | RF balun/matching network inductor |
| L6 | SMPS inductor |
| L7 | SMPS noise filter inductor (15 nH) |
| L8 | SMPS ground noise filter inductor (3.4 nH) |
| XTAL1 | 32 kHz crystal (optional) |
| XTAL2 | 32 MHz crystal |

# 5 Application controller interface

The application controller interface (ACI) is based on a standard UART/SPI module. The ACI defines a protocol providing access to all services offered by the layers of the embedded Bluetooth stack. ACI commands are described in the BlueNRG-232N ACI command interface documentation. In addition, ACI provides a set of commands that allow the BlueNRG-232N firmware to be programmed from an external device connected to SPI or UART.

The complete description of updater commands and procedures is provided in a separate application note.

# 6 External microcontroller interface

The BlueNRG-2N provides a hardware interface to external microcontroller based on two very common protocols:

- SPI slave protocol with interrupt signal
- UART

The selection between SPI or UART mode is done through the DIO12 pin. Refer to Table 3. Pinout description, DIO12 description for UART, SPI selection options.

The physical layer (SPI or UART) is used to transfer commands and events between the external microcontroller and the BlueNRG-2N.

The commands and events are collectively named application control interface (ACI) and they are described in the BlueNRG-2N ACI documentation.

In addition, ACI provides a set of commands that allow the BlueNRG-2N firmware to be programmed/updated from an external device connected to SPI or UART.

## 6.1 UART interface

The characteristics of the UART interface are as follows:

- Baud rate: 115200
- Data bits: 8
- Parity: N
- Stop bits: 1
- Full duplex

The interface operates with logic levels as specified in Table 12. Digital I/O specifications.

The UART interface does not allow the device to go to sleep state.

The pins dedicated to the UART interface are:

- DIO11 (UART RX)
- DIO8 (UART TX)

## 6.2 SPI interface

The characteristics of the SPI interface are the following:

- SPI clock: 1 MHz (max.)
- Data bits: 8
- Polarity: 0 (clock to 0 when idle)
- Phase: second edge
- Full duplex
- Slave mode

A dedicated IRQ pin is used to inform the external microcontroller that an event has occurred and the device needs attention.

The interface operates with logic levels as specified in Table 11. Electrical characteristics.

The SPI interface allows the device to go into sleep state achieving the optimal power consumption.

## 6.3 SPI protocol specificatons

This section describes the features and details of the SPI protocol provided by the BlueNRG-2N network coprocessor.

The features provided by the SPI protocol are:

- Power efficient
- Code efficient
- Fast data transfer

## 6.4 SPI protocol hardware details

The SPI port requires five pins:

- SPI clock
- SPI MOSI
- SPI MISO
- SPI CS
- SPI IRQ

The maximum SPI baud rate supported is 1 MHz. The timing diagram adopted is CPOL 0 and CPHA 1, which means data are captured on the SPI clock falling edge and data are changed on the rising edge. The SPI CS acts also as wake-up pin for the BlueNRG-2N, so that if the SPI CS pin is low (external uC selects the BlueNRG-2N for communication) the BlueNRG-2N is woken up if it was asleep.The BlueNRG-2N notifies event pending to the external uC through the SPI IRQ pin. If the SPI IRQ pin is high, the BlueNRG-2N has at least an event for the external uC.

**Table 5. BlueNRG-2N SPI lines**

| Pin function | Pin name | Pin number | | Information |
|---|---|---|---|---|
| | | QFN32 | WCSP34 | |
| SPI clock | DIO0 | 12 | A2 | SPI clock signal |
| SPI MISO | DIO2 | 10 | A1 | SPI master input slave output signal |
| SPI MOSI | DIO3 | 9 | B1 | SPI master output slave input signal |
| SPI CS | DIO11 | 32 | E2 | SPI chip select signal/ wake-up signal |
| SPI IRQ | DIO7 | 4 | D2 | SPI IRQ request for event pending signal |

## 6.5 SPI communication protocol

To communicate with the BlueNRG-2N, the data on the SPI bus must be formatted as described in this section. An SPI transaction is defined from a falling edge of the SPI CS signal to the next rising edge of the SPI CS signal. Each SPI transaction must contain one data frame only. Each data frame should contain at least five bytes of header, and may have from 0 to N bytes of data.

**Figure 14. Generic SPI transaction**

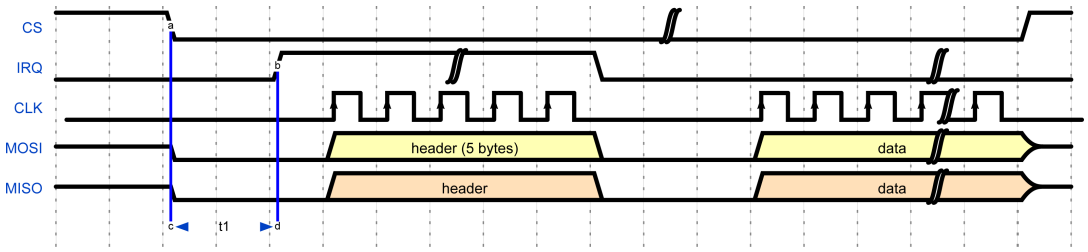



Figure 14. Generic SPI transaction shows a generic SPI transaction. The list of steps is as follows:

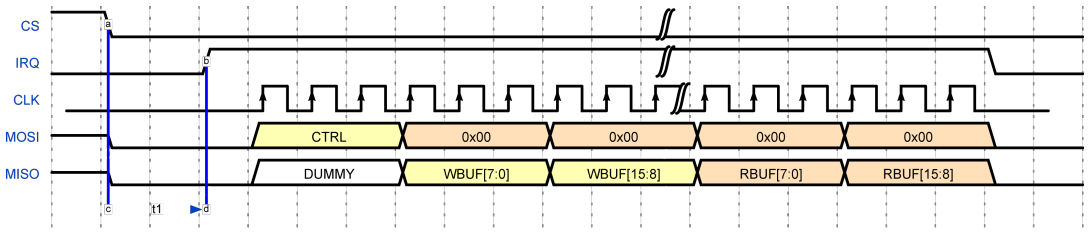
1. The external uC lowers the SPI CS signal to start the communication.
2. The BlueNRG-2N raises the SPI IRQ signal to indicate that it is ready for the communication. The time t1 changes according to the state of the BlueNRG-2N. This time t1 can include wakeup of the BlueNRG-2N and preparation of the header part of the frame.
3. The external uC must wait for the SPI IRQ signal to become high and then start to transfer the five bytes of the header that includes the control field with the intended operation. In addition, the external uC reads five bytes from the BlueNRG-2N, which include information about the actual size of the read and write buffer.

4. The external uC, after checking the five bytes of header, performs data transaction.
5. The BlueNRG-2N lowers SPI IRQ signal after the five byte headers are transferred, but due to internal processing, this could be done also during the data transfer phase.
6. The external uC must wait for the SPI IRQ to be low before raising the SPI CS signal to mark the end of the communication.

Some important notes are:

- Setting the SPI CS signal low wakes up the BlueNRG-2N if the device is asleep
- If the SPI IRQ signal is low before setting the SPI CS signal low, the BlueNRG-2N has no data events for the external uC, so the read buffer size is zero (RBUF=0)
- The time t1 is the time between wake-up (point a in Figure 14. Generic SPI transaction) and the BlueNRG-2N ready to perform the SPI transaction (point b in Figure 14. Generic SPI transaction). The t1 time range is from minimal value (the BlueNRG-2N already awakes when the SPI CS is asserted), to a maximum value that involves wake-up sequence and software boot
- Even if there are events pending after the end of the transaction, the SPI IRQ signal goes low to allow the BlueNRG-2N to update five byte headers and to re-arm the SPI for the next transaction (after this delay the SPI IRQ signal goes high again if events are pending)
- The SPI CS signal marks the beginning and end of the transaction
- The SPI CS high marks the end of the transaction and must be set to high only when IRQ line is low
- The gap between the header and the data is not mandatory, but it is normally required by the external uC to process the header and check if there is enough space in the buffers to perform the wanted transaction
- When the SPI IRQ signal is high, the five byte headers are locked and cannot be modified by the BlueNRG-2N firmware

**Figure 15. SPI header format**



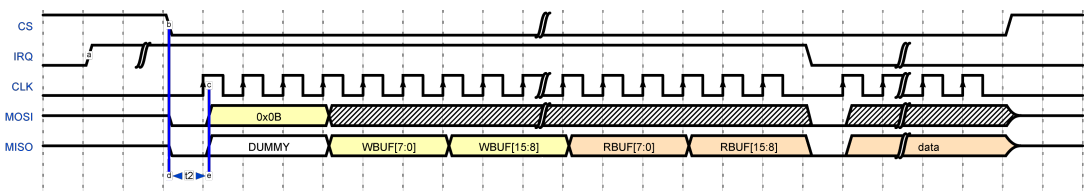

- The header of the external uC (the SPI master) is on the MOSI line, which is composed of one control byte (CTRL) and four bytes 0x00. CTRL field can have only the value of 0x0A (SPI write) or 0x0B (SPI read). The BlueNRG-2N returns the header on the MISO line at the same time. When the BlueNRG-2N asserts the SPI IRQ signal, it is ready. Otherwise, the BlueNRG-2N is still not initialized. The external uC must wait for the IRQ line to become high and perform a five bytes transaction.

  The five bytes in the MISO line gives one byte of starting frame, two bytes with the size of the write buffer (WBUF) and two bytes with the size of the read buffer (RBUF). The endianness for WBUF and RBUF is LSB first. The value in WBUF means how many bytes the master can write to the BlueNRG-2N. The value in RBUF means how many bytes in the BlueNRG-2N are waiting to be read by the external uC

### Read transaction

A read transaction is performed when the BlueNRG-2N raises the SPI IRQ line before the SPI CS signal is lowered by the external uC.

**Figure 16. SPI read transaction**

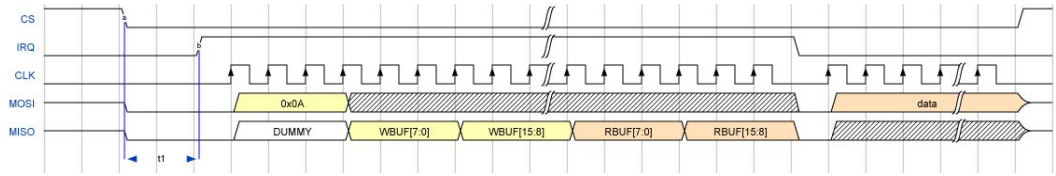


- In this case, the SPI IRQ signal is high indicating the BlueNRG-2N is awake and ready to perform the SPI transaction, after a hardware dependent set-up time t2 (>=0.5 us). The transaction is performed as follows:
  1. An event has been generated by the BlueNRG-2N (point a in Figure 16. SPI read transaction ).
  2. The external uC lowers the SPI CS signal to initiate a transaction (point b in Figure 16. SPI read transaction).
  3. Since the SPI IRQ signal is high, the external uC initiates a data transfer after t2. The external uC transfers five bytes as follows [0x0B, XX, XX, XX, XX]. The WBUF and RBUF sizes are read by the SPI MISO signal.
  4. The external uC performs the read data transaction for RBUF bytes. (Note: if RBUF is 0, this is an unexpected condition since the BlueNRG-2N is indicating that data is available; in any case the transaction needs to be completed by reading no bytes).
  5. The BlueNRG-2N lowers SPI IRQ signal after the five bytes header are transferred, but due to internal processing, this could be done also during the data transfer phase.
  6. The external uC must wait for the SPI IRQ to be low before raising the SPI CS signal to mark the end of the communication.

**Write transaction**

- A write transaction is performed by the external uC to send a command to the BlueNRG-2N. The BlueNRG-2N can be awakened or put to sleep when the SPI CS signal is lowered by the external uC. The assertion of the SPI CS signal wakes up the BlueNRG-2N, if asleep

**Figure 17. SPI write transaction**




- The transaction is performed as follows:
  1. The external uC lowers the SPI CS signal to initiate a transaction.
  2. The BlueNRG-2N raises the SPI IRQ signal to indicate that it is ready with t1 >= 0.
  3. The external uC waits for SPI IRQ signal to become high and start a transfer of five bytes sending the code of the intended operation and reading the read buffer and write buffer size. The external uC transfers five bytes as follows: [0x0A, XX, XX, XX, XX]. The WBUF and RBUF values are sampled in the SPI MISO signal.
  4. The BlueNRG-2N lowers the SPI IRQ after the five byte headers are transferred, but due to internal processing, this could be done also during the data transfer phase.
  5. The external uC checks if the WBUF allows sending the command. If yes, it performs the data transaction, otherwise it performs no data transfer (it would be possible to retry later.)
  6. The external uC must wait for the SPI IRQ signal to be low before the communication is closed
  7. The external uC must raise the SPI CS to mark the end of the transaction.

**Error transaction**

- This section lists the BlueNRG-2N firmware behavior when some error transactions are performed:
  - Incomplete header transaction (0 to 4): the BlueNRG-2N ignores the transaction
  - The external uC does not wait for the SPI IRQ signal to be low before raising the SPI CS signal: the BlueNRG-2N lowers the SPI IRQ signal when the SPI CS signal is high
  - The external uC does not wait for the SPI IRQ signal to be high before SPI clock starts: the result is acquisition of corrupted data both master and slave side
  - Incomplete read transaction: the master loses the event
  - Incomplete write transaction: the BlueNRG-2N stores the bytes written by the external uC. During the next write operation the BlueNRG-2N gets the new bytes trying to get a complete frame according to Bluetooth protocol
  - Two commands in a row without reading event for command: the BlueNRG-2N parses the two commands and then it generates the corresponding events

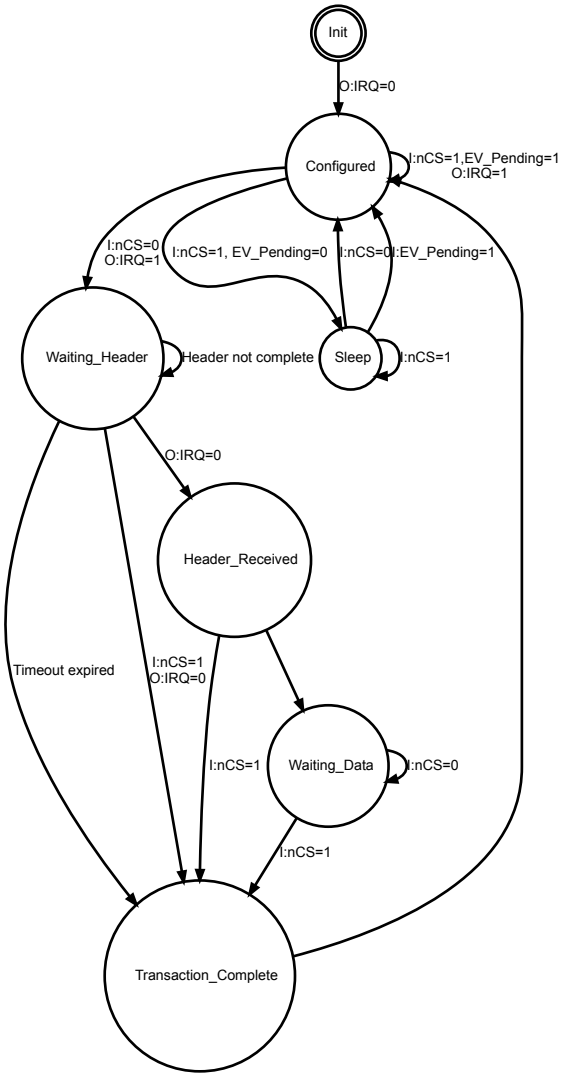
### SPI state machine

- Hereafter the description of the BlueNRG-2N SPI state machine

**Table 6. BlueNRG-2N SPI state machine states**

| State | Description | Input | Output | Next state |
|---|---|---|---|---|
| Init | Boot/transient state<br>Hardware initialization | - | IRQ=0 | Configured |
| Configured | Ready to transfer information, 5 byte header frozen | CS=0 | IRQ=1 | Waiting_Header |
| | | CS=1<br>Event pending=0 | IRQ=0 | Sleep |
| | | CS=1<br>Event pending=1 | IRQ=1 | Configured |
| Sleep | Sleep state with almost all logic off | CS=1<br>Event pending=0 | IRQ=0 | Sleep |
| | | CS=1<br>Event pending=1 | IRQ=0 | Configured |
| | | CS=0 | IRQ=0 | Configured |
| Waiting_Header | Receiving 5 byte header from SPI master | CS=0 | IRQ=1 | When 5-byte are received goes to Header_Received |
| | | CS=1 | IRQ=1 | Transaction_Complete |
| Header_Received | 5 byte header received | CS=0 | IRQ=0 | Waiting_Data |
| | | CS=1 | IRQ=0 | Transaction_Complete |
| Waiting_Data | Receiving payload | CS=0 | IRQ=0 | Waiting_Data |
| | | nCS=1 | IRQ=0 | Transaction_Complete |
| Transaction_Complete | Transitional | nCS=1 | IRQ=0 | Configured |

Figure 18. **SPI protocol state machine**




**External uC behavior**

- The external uC must act according to the information from the BlueNRG-2N:
  - SPI IRQ signal
  - Information from header frame WBUF and RBUF

Table 7. **BlueNRG-2N SPI inputs**

| Input from BlueNRG-1 | Meaning | External uC |
|---|---|---|
| IRQ=1, RBUF is not 0 | Read operation is required, at least one event pending | Read operation can be performed |
| IRQ=0, RBUF is 0 | No event pending | Nothing to do |
| IRQ=0, RBUF is 0, WBUF is N | No event pending | If the number of bytes to write is lesser or equal than N, then write operation is acceptable. Otherwise, the extent uC must wait |

Figure 19. **Expected uC SPI protocol state machine**

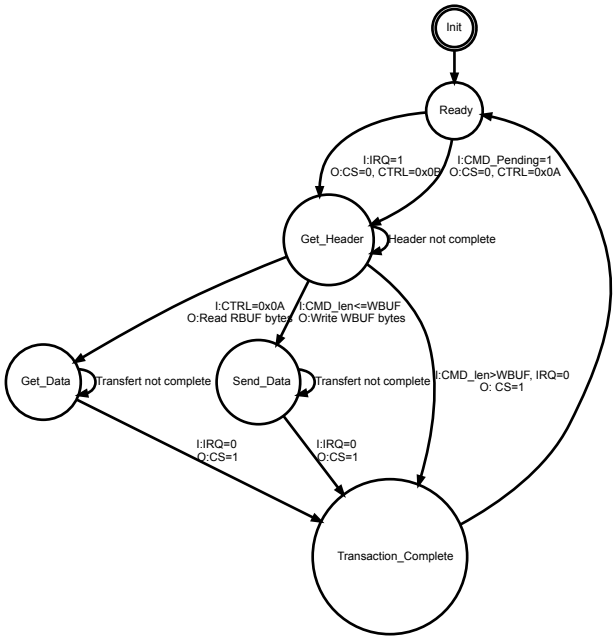



Figure 20. **HCI_READ_LOCAL_VERSION_INFORMATION SPI waveform**

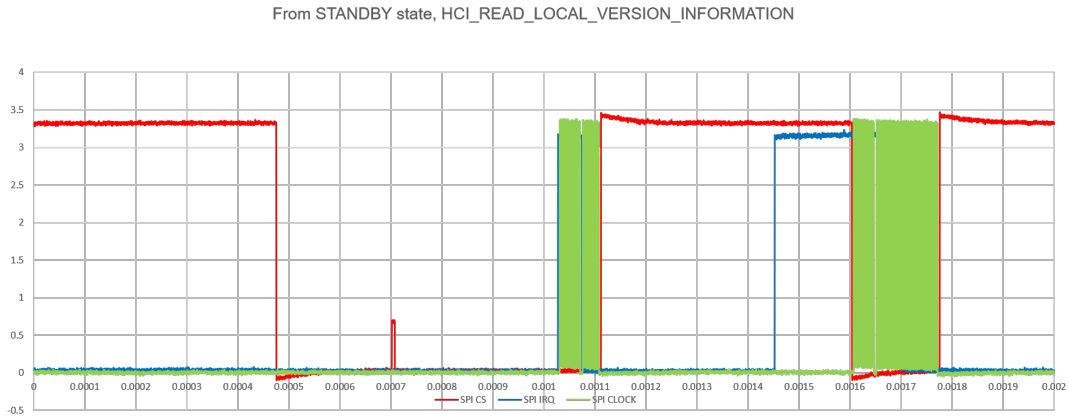



Figure 21. **HCI_READ_LOCAL_VERSION_INFORMATION SPI waveform zoom**

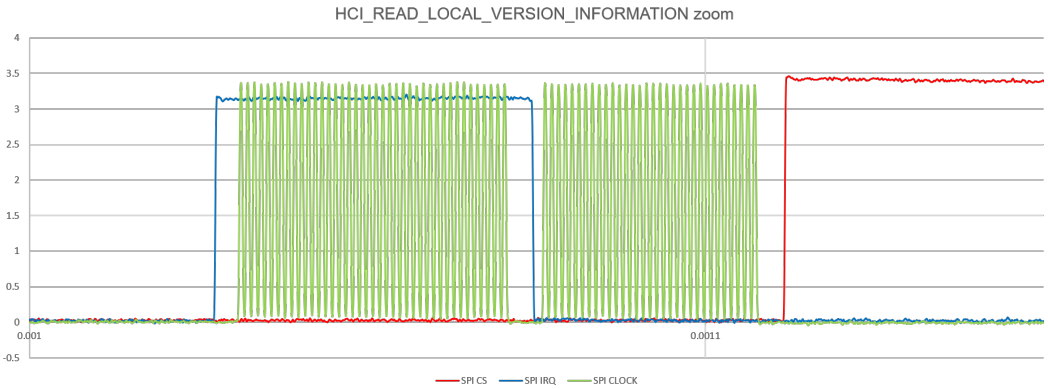
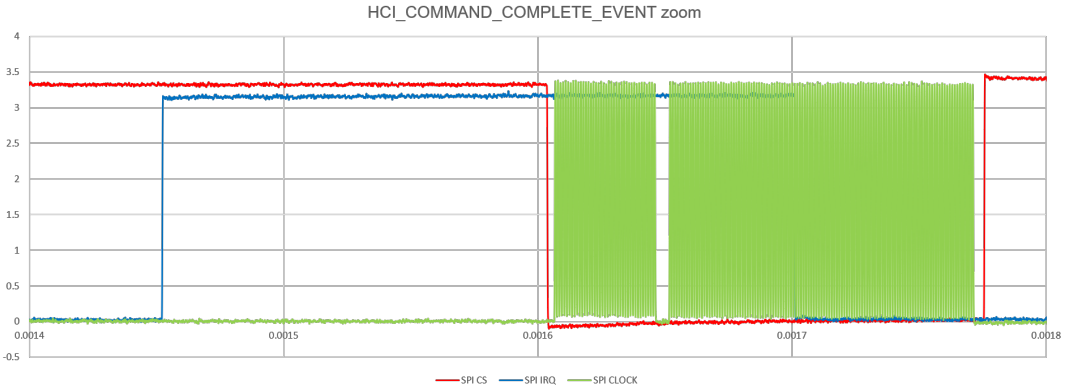


**Figure 22. HCI_COMMAND_COMPLETE_EVENT SPI waveform**



# 7 Absolute maximum ratings and thermal data

**Table 8. Absolute maximum ratings**

| Pin | Parameter | Value | Unit |
|---|---|---|---|
| VBAT3, VBAT2, VBAT1, RESETN, SMPSFILT1, SMPSFILT2 | DC-DC converter supply voltage input and output | -0.3 to +3.9 | V |
| VDD1V2 | DC voltage on linear voltage regulator | -0.3 to +1.3 | V |
| DIO0 to DIO25, TEST | DC voltage on digital input/output pins | -0.3 to +3.9 | V |
| ANATEST0, ANATEST1, ADC1, ADC2 | DC voltage on analog pins | -0.3 to +3.9 | V |
| FXTAL0, FXTAL1, SXTAL0, SXTAL1 | DC voltage on XTAL pins | -0.3 to +1.4 | V |
| RF0, RF1 | DC voltage on RF pins | -0.3 to +1.4 | V |
| TSTG | Storage temperature range | -40 to +125 | °C |
| VESD-HBM | Electrostatic discharge voltage | ±2.0 | kV |

*Note: Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referred to GND.*

**Table 9. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| Rthj-amb | Thermal resistance junction-ambient | 34 (QFN32)<br>50 (WLCSP34) | °C/W |
| Rthj-c | Thermal resistance junction-case | 2.5 (QFN32)<br>25 (WLCSP34) | °C/W |

# 8 General characteristics

**Table 10. Operating conditions**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BAT}$ | Operating battery supply voltage | 1.7 | | 3.6 | V |
| $T_A$ | Operating Ambient temperature range | -40 | | +105 | °C |

# 9 Electrical specifications

## 9.1 Electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$ = 25 °C, $V_{BAT}$ = 3.0 V. All performance data are referred to a 50 Ω antenna connector, via reference design, QFN32 package version.

**Table 11. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power consumption when DC-DC converter active | | | | | | |
| $I_{BAT}$ | Supply current | Reset | – | 5 | – | nA |
| | | Standby | – | 500 | – | nA |
| | | Sleep mode: 32 kHz XO ON (24 KB retention RAM) | – | 0.9 | – | µA |
| | | Sleep mode: 32 kHZ RO ON (24 KB retention RAM) | | 2.1 | | |
| | | Active mode: CPU, Flash and RAM on | – | 1.9 | – | mA |
| | | RX | – | 7.7 | – | mA |
| | | TX +8 dBm | – | 15.1 | – | mA |
| | | TX +4 dBm | | 10.9 | | |
| | | TX +2 dBm | | 9 | | |
| | | TX -2 dBm | | 8.3 | | |
| | | TX -5 dBm | | 7.7 | | |
| | | TX -8 dBm | | 7.1 | | |
| | | TX -11 dBm | | 6.8 | | |
| | | TX -14 dBm | | 6.6 | | |
| Power consumption when DC-DC converter not active | | | | | | |
| $I_{BAT}$ | Supply current | Reset | – | 5 | – | nA |
| | | Standby | – | 500 | – | nA |
| | | Sleep mode: 32 kHz XO ON (24 KB retention RAM) | – | 0.9 | – | µA |
| | | Sleep mode: 32 kHZ RO ON (24 KB retention RAM) | – | 2.1 | – | |
| | | Active mode: CPU, Flash and RAM on | – | 3.3 | – | mA |
| $I_{BAT}$ | Supply current | RX | – | 14.5 | – | mA |
| | | TX +8 dBm | – | 28.8 | – | mA |
| | | TX +4 dBm | | 20.5 | | |
| | | TX +2 dBm | | 17.2 | | |
| | | TX -2 dBm | | 15.3 | | |
| | | TX -5 dBm | | 14 | | |
| | | TX -8 dBm | | 13 | | |
| | | TX -11 dBm | | 12.3 | | |
| | | TX -14 dBm | | 12 | | |

**Table 12. Digital I/O specifications**

| Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| T(RST)L | | | 1.5 | | ms |
| TC | | | 3.3 | | V |
| TC1 | | | 2.5 | | V |
| TC2 | | | 1.8 | | V |
| VIL | | | | 0.3*VDD | V |
| VIH | | 0.65*VDD | | | V |
| VOL | IOL = 3 mA | | | 0.4 | V |
| VOH | IOH = 3 mA | 0.7*VDD | | | V |
| IOL (low drive strength) | TC (VOL = 0.4 V) | | 5.6 | | mA |
| | TC1 (VOL = 0.42 V) | | 6.6 | | mA |
| | TC2 (VOL = 0.45 V) | | 3 | | mA |
| IOL (high drive strength) | TC (VOL = 0.4 V) | | 11.2 | | mA |
| | TC1 (VOL = 0.42 V) | | 13.2 | | mA |
| | TC2 (VOL = 0.45 V) | | 6 | | mA |
| IOL (Very high drive strength) | TC (VOL = 0.4 V) | | 16.9 | | mA |
| | TC1 (VOL = 0.42 V) | | 19.9 | | mA |
| | TC2 (VOL = 0.45 V) | | 9.2 | | mA |
| IOH (low drive strength) | TC (VOH = 2.4 V) | | 10.6 | | mA |
| | TC1 (VOH = 1.72 V) | | 7.2 | | mA |
| | TC2 (VOH = 1.35 V) | | 3 | | mA |
| IOH (high drive strength) | TC (VOH = 2.4 V) | | 19.2 | | mA |
| | TC1 (VOH = 1.72 V) | | 12.9 | | mA |
| | TC2 (VOH = 1.35 V) | | 5.5 | | mA |
| IOH (very high drive strength) | TC (VOH = 2.4 V) | | 29.4 | | mA |
| | TC1 (VOH = 1.72 V) | | 19.8 | | mA |
| | TC2 (VOH = 1.35 V) | | 8.4 | | mA |
| IPUD (current sourced/sinked from IOs with pull enabled) | Static supply 1.7 V | 5 | | 10 | µA |
| | Static supply 3.6 V | 40 | | 60 | µA |

## 9.2 RF general characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$= 25 °C, $V_{BAT}$ = 3.0 V. All performance data are referred to a 50 Ω antenna connector, via reference design, QFN32 package version.

**Table 13. RF general characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| FREQ | Frequency range | | 2400 | – | 2483.5 | MHz |
| FCH | Channel spacing | | – | 2 | – | MHz |
| RFch | RF channel center frequency | | 2402 | – | 2480 | MHz |

## 9.3 RF transmitter characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$ = 25 °C, $V_{BAT}$ = 3.0 V. All performance data are referred to a 50 Ω antenna connector, via reference design, QFN32 package version.

**Table 14. RF transmitter characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| MOD | Modulation scheme | | | GFSK | | |
| BT | Bandwidth-bit period product | | – | 0.5 | – | |
| Mindex | Modulation index | | – | 0.5 | – | |
| DR | Air data rate | | – | 1 | – | Mbps |
| PMAX | Maximum output power | At antenna connector | – | +8 | +10 | dBm |
| PRFC | Minimum output power | | – | -16.5 | – | dBm |
| PBW1M | 6 dB bandwidth for modulated carrier (1 Mbps) | Using resolution bandwidth of 100 kHz | 500 | – | – | kHz |
| PRF1 | 1st adjacent channel transmit power 2 MHz | Using resolution bandwidth of 100 kHz and average detector | – | -35 | – | dBm |
| PRF2 | 2nd Adjacent channel transmit power >3 MHz | Using resolution bandwidth of 100 kHz and average detector | – | -40 | – | dBm |
| ZLOAD | Optimum differential load | @ 2440 MHz | – | 25.4 + j20.8 (1) | – | Ω |

1. *Simulated value.*

## 9.4 RF receiver characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$ = 25 °C, $V_{BAT}$ = 3.0 V. All performance data are referred to a 50 Ω antenna connector, via reference design, QFN32 package version.

**Table 15. RF receiver characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| RXSENS | Sensitivity | BER <0.1% | | -88 | | dBm |
| PSAT | Saturation | BER <0.1% | | 11 | | dBm |
| zIN | Input differential impedance | @ 2440 MHz | | 25.5-j14.2 | | Ω |
| **RF selectivity with BLE equal modulation on interfering signal** | | | | | | |
| C/ICO-channel | Co-channel interference | Wanted signal = -67 dBm, BER ≤ 0.1% | | 6 | | dBc |
| C/I1 MHz | Adjacent (+1 MHz) interference | Wanted signal = -67 dBm, BER≤0.1% | | 0 | | dBc |
| C/I2 MHz | Adjacent (+2 MHz) interference | Wanted signal = -67 dBm, BER ≤ 0.1% | | -40 | | dBc |
| C/I3 MHz | Adjacent (+3 MHz) interference | Wanted signal = -67 dBm, BER ≤ 0.1% | | -47 | | dBc |
| C/I≥4 MHz | Adjacent (≥ ± 4 MHz) interference | Wanted signal = -67 dBm, BER ≤ 0.1% | | -46 | | dBc |
| C/I≥6 MHz | Adjacent (≥ ± 6 MHz) interference | Wanted signal = -67 dBm BER ≤ 0.1% | | -48 | | dBc |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| C/I≥25 MHz | Adjacent (≥ ±25 MHz) interference | Wanted signal = -67 dBm, BER ≤ 0.1% | | -70 | | dBc |
| C/IImage | Image frequency interference<br>-2 MHz | Wanted signal = -67 dBm, BER ≤ 0.1% | | -16 | | dBc |
| C/IImage±1 MHz | Adjacent (±1 MHz) interference to in-band image frequency<br>-1 MHz<br>-3 MHz | Wanted signal = -67 dBm, BER ≤ 0.1% | | 0<br>-23 | | dBc |
| **Intermodulation characteristics (CW signal at $f_1$, BLE interfering signal at $f_2$)** | | | | | | |
| P_IM(3) | Input power of IM interferes at 3 and 6 MHz distance from wanted signal | Wanted signal = -64 dBm, BER ≤ 0.1% | | -34 | | dBm |
| P_IM(-3) | Input power of IM interferes at -3 and -6 MHz distance from wanted signal | Wanted signal = -64 dBm, BER ≤ 0.1% | | -48 | | dBm |
| P_IM(4) | Input power of IM interferes at ±4 and ±8 MHz distance from wanted signal | Wanted signal = -64 dBm, BER ≤ 0.1% | | -34 | | dBm |
| P_IM(5) | Input power of IM interferes at ±5 and ±10 MHz distance from wanted signal | Wanted signal = -64 dBm, BER ≤ 0.1% | | -34 | | dBm |

## 9.5 High speed crystal oscillator characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$ = 25 °C, $V_{BAT}$ = 3.0 V.

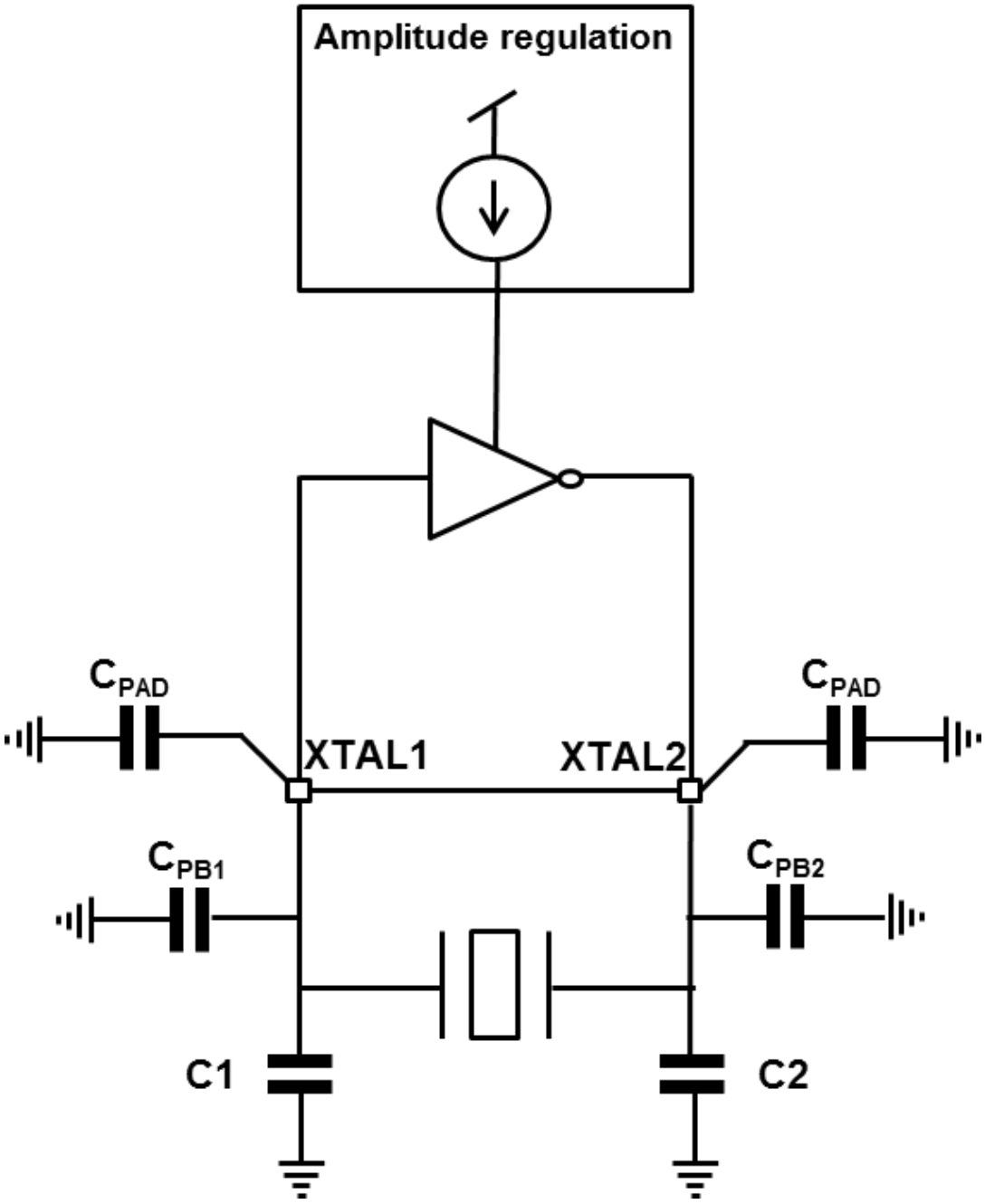
**Table 16. High speed crystal oscillator characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| fNOM | Nominal frequency | | – | 32 | – | MHz |
| fTOL | Frequency tolerance | Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance | – | – | ±50 | ppm |
| ESR | Equivalent series resistance | | – | – | 100 | Ω |
| PD | Drive level | | – | – | 100 | µW |

## 9.6 High speed crystal oscillator

The BlueNRG-2N includes a fully integrated low power 32 MHz Xtal oscillator with an embedded amplitude regulation loop. In order to achieve low power operation and good frequency stability of the XTAL oscillator, certain considerations with respect to the quartz load capacitance C0 need to be taken into account.
Figure 23. High speed oscillator block diagram shows a simplified block diagram of the amplitude regulated oscillator used on the BlueNRG-2N.

Figure 23. **High speed oscillator block diagram**




Low power consumption and fast start-up time is achieved by choosing a quartz crystal with a low load capacitance C0. A reasonable choice for capacitor C0 is 12 pF. To achieve good frequency stability, the following equation needs to be satisfied:

$$C_0 = \frac{C_1' * C_2'}{C_1 + C_2} \quad (1)$$

Where $C_1$'=$C_1$+$C_{PCB1}$+$C_{PAD}$, $C_2$'= $C_2$+$C_{PCB2}$+$C_{PAD}$, where $C_1$ and $C_2$ are external (SMD) components, $C_{PCB1}$ and $C_{PCB2}$ are PCB routing parasites and $C_{PAD}$ is the equivalent small-signal pad-capacitance. The value of $C_{PAD}$ is around 0.5 pF for each pad. The routing parasites should be minimized by placing quartz and $C_1$/$C_2$ capacitors close to the chip, not only for an easier matching of the load capacitance $C_0$, but also to ensure robustness against noise injection. Connect each capacitor of the Xtal oscillator to ground by a separate vias.

## 9.7 Low speed crystal oscillator characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$ = 25 °C, $V_{BAT}$ = 3.0 V.

**Table 17. Low speed crystal oscillator characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| fNOM | Nominal frequency | | – | 32.768 | – | kHz |
| fTOL | Frequency tolerance | Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance. | – | – | ±50 | ppm |
| ESR | Equivalent series resistance | | – | – | 90 | kΩ |
| PD | Drive level | | – | – | 0.1 | µW |

*Note: These values are the correct ones for NX3215SA-32.768 kHz-EXS00A-MU00003.*

## 9.8 High speed ring oscillator characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$= 25 °C, $V_{BAT}$ = 3.0 V.

**Table 18. High speed ring oscillator characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{NOM}$ | Nominal frequency | | – | 14 | – | MHz |

## 9.9 Low speed ring oscillator characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$ = 25 °C, $V_{BAT}$ = 3.0 V, QFN32 package version.

**Table 19. Low speed ring oscillator characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| 32 kHz ring oscillator (LSROSC) | | | | | | |
| $f_{NOM}$ | Nominal frequency | | – | 32 | – | kHz |

## 9.10 N-fractional frequency synthesizer characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to $T_A$ = 25 °C, $V_{BAT}$ = 3.0 V, $f_c$ = 2440 MHz.

**Table 20. N-Fractional frequency synthesizer characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| PNSYNTH | RF carrier phase noise | At ±1 MHz offset from carrier | – | -113 | – | dBc/Hz |
| | | At ±3 MHz offset from carrier | – | -119 | – | dBc/Hz |
| LOCKTIME | PLL lock time | | – | – | 40 | µs |
| TOTIME | PLL turn-on / hop time | Including calibration | – | – | 150 | µs |

# 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 10.1 QFN32 package information

Figure 24. **QFN32 (5 x 5 x 1 pitch 0.5 mm) package outline**

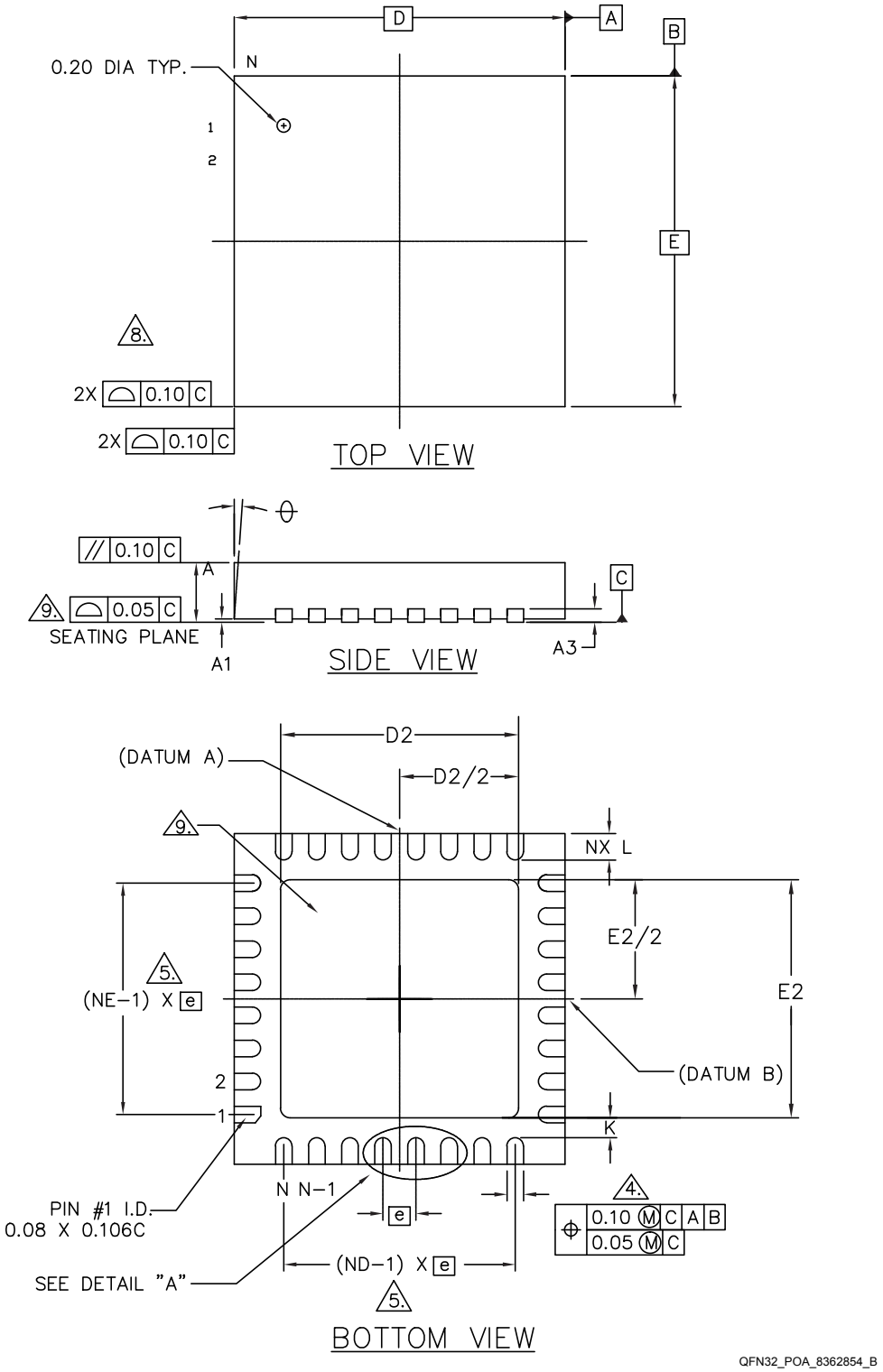
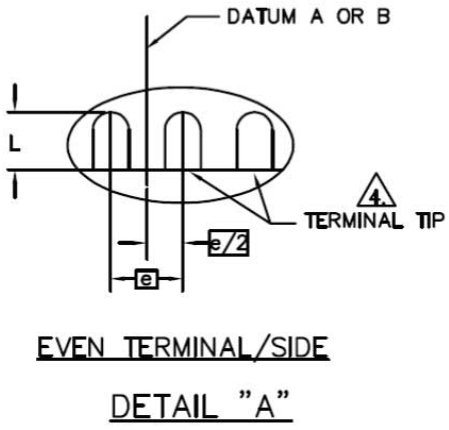


Table 21. **QFN32 (5 x 5 x 1 pitch 0.5 mm) mechanical data**

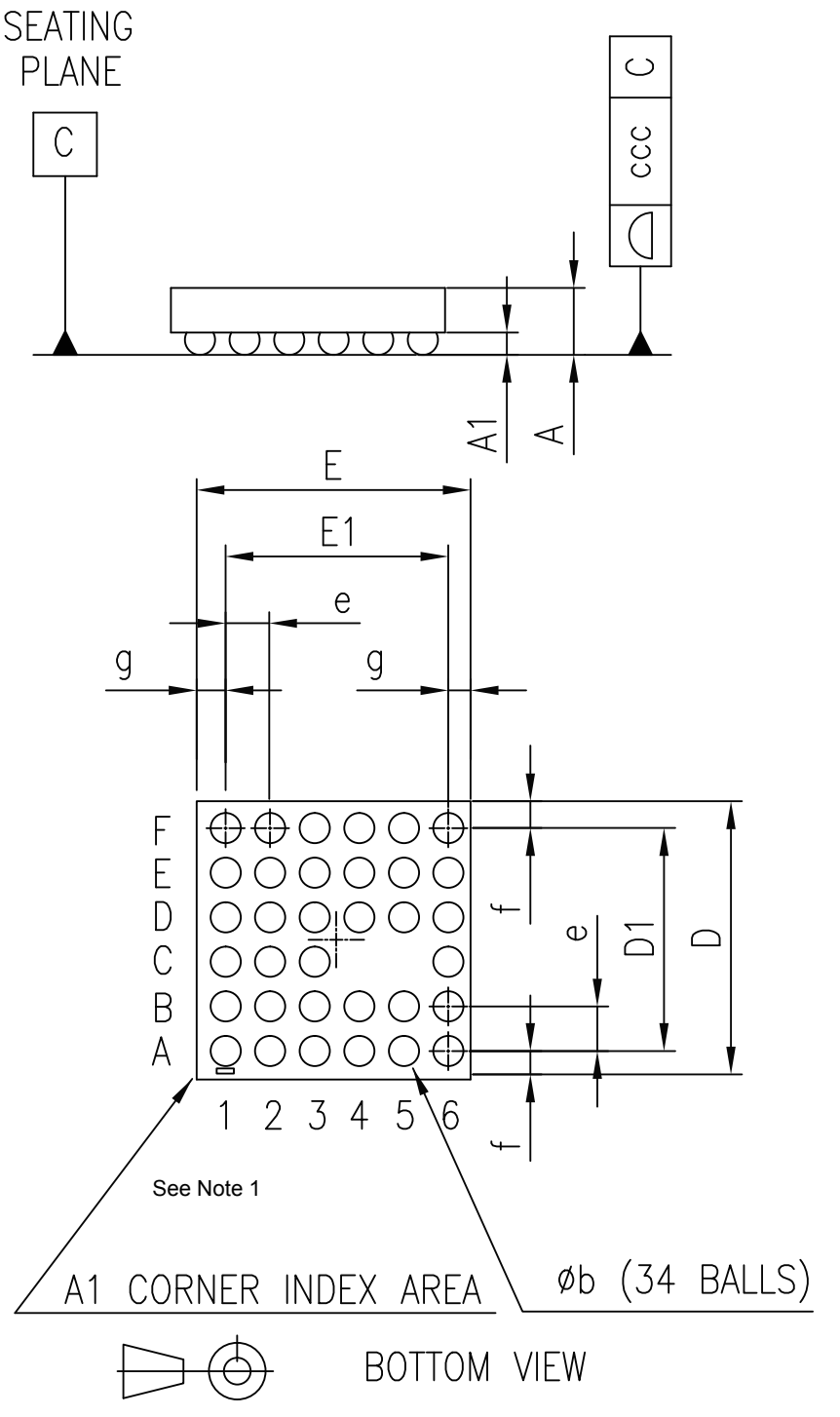
| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 5.00 BSC | |
| E | | 5.00 BSC | |
| D2 | 3.2 | | 3.70 |
| E2 | 3.2 | | 3.70 |
| e | | 0.5 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| Φ | 0° | | 14° |
| K | 0.20 | | |

Figure 25. **QFN32 (5 x 5 x 1 pitch 0.5 mm) package detail "A"**



## 10.2 WLCSP34 package information

Figure 26. **WLCSP34 (2.66 x 2.56 x 0.5 pitch 0.4 mm) package outline**




1. The corner of terminal A1 must be identified on the top surface by using a laser marking dot.

**Table 22. WLCSP34 (2.66 x 2.56 x 0.5 pitch 0.4 mm) mechanical data**

| Dim. | mm. | | | Notes |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| A | | | 0.50 | |
| A1 | | 0.20 | | |
| b | | 0.27 | | (1) |
| D | 2.50 | 2.56 | 2.58 | (2) |
| D1 | | 2.00 | | |
| E | 2.60 | 2.66 | 2.68 | (3) |
| E1 | | 2.00 | | |
| e | | 0.40 | | |
| f | | 0.28 | | |
| g | | 0.33 | | |
| ccc | | | 0.05 | |

1. *The typical ball diameter before mounting is 0.25 mm.*
2. *D = f + D1 + f.*
3. *E = g + E1 + g.*

# 11 PCB assembly guidelines

For Flip Chip mounting on the PCB, STMicroelectronics recommends the use of a solder stencil aperture of 330 x 330 µm maximum and a typical stencil thickness of 125 µm.

Flip Chips are fully compatible with the use of near eutectic 95.8% Sn, 3.5% Ag, 0.7% Cu solder paste with no-clean flux. ST's recommendations for Flip-Chip board mounting are illustrated on the soldering reflow profile shown in Figure 27. Flip Chip CSP (2.71 x 2.58 x 0.5 pitch 0.4 mm) package reflow profile recommendation.

**Figure 27. Flip Chip CSP (2.71 x 2.58 x 0.5 pitch 0.4 mm) package reflow profile recommendation**

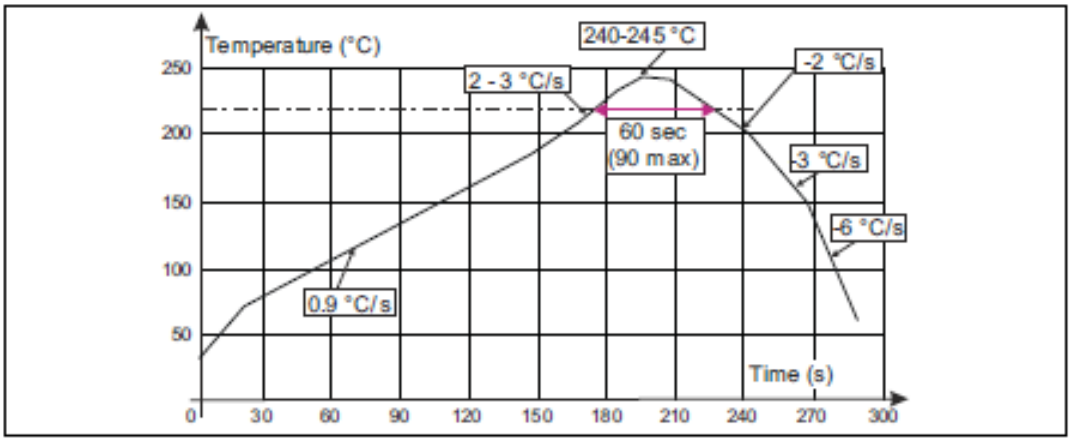



**Table 23. Flip Chip CSP (2.71 x 2.58 x 0.5 pitch 0.4 mm) package reflow profile recommendation**

| Profile | Value | |
|---|---|---|
| | Typ. | Max. |
| Temp. gradient in preheat (T = 70 - 180 °C/s | 0.9 °C/s | 3 °C/s |
| Temp. gradient (T = 200 - 225 °C) | 2 °C/s | 3 °C/s |
| Peak temp. in reflow | 240 - 245 °C | 260 °C |
| Time above 200 °C | 60 s | 90 s |
| Temp. gradient in cooling | -2 to -3 °C | -6 °C/s |
| Time from 50 to 220 °C | 160 to 220 °C | |

Dwell time in the soldering zone (with temperature higher than 220 °C) has to be kept as short as possible to prevent component and substrate damage. Peak temperature must not exceed 260 °C. Controlled atmosphere (N2 or N2H2) is recommended during the whole reflow, especially above 150 °C.

Flip Chips are able to withstand three times the previous recommended reflow profile to be compatible with a double reflow when SMDs are mounted on both sides of the PCB plus one additional repair.

A maximum of three soldering reflows are allowed for these lead-free packages (with repair step included).

The use of a no-clean paste is highly recommended to avoid any cleaning operation. To prevent any bump cracks, ultrasonic cleaning methods are not recommended.

# 12 Ordering information

Table 24. **Ordering information**

| Order code | Package | Packing |
|---|---|---|
| BlueNRG-232N | QFN32 (5x5 mm) | Tape and reel |
| BlueNRG-234N | WLCSP34 (2.66x2.56 mm) | |

# Revision history

Table 25. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 09-Jul-2020 | 1 | Initial release. |
| 17-Sep-2020 | 2 | Updated features in cover page. |
| 18-Jan-2021 | 3 | Updated Section Features and Section Description.<br>Updated Table 1. Relationship between the BlueNRG-2N states and functional blocks, Table 3. Pinout description.<br>Updated Section 2.2.1.2 Active state, Section 2.8 Pre-programmed bootloader, Section 9.5 High speed crystal oscillator characteristics and Section 9.6 High speed crystal oscillator. |
| 23-Nov-2021 | 4 | Updated Table 5. BlueNRG-2N SPI lines. |

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