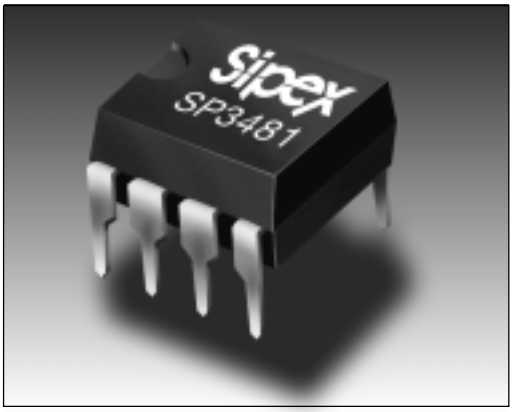
+3.3V Low Power Half-Duplex RS-485 Transceivers with 10Mbps Data Rate

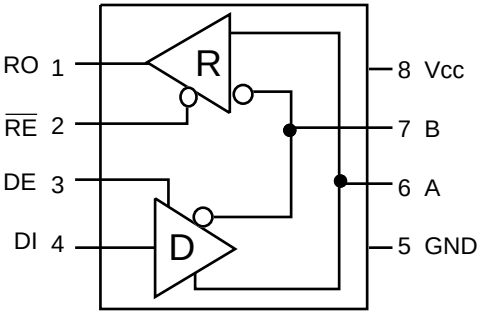
- RS-485 and RS-422 Transceivers
- Operates from a single +3.3V supply
- Interoperable with +5.0V logic
- Driver/Receiver Enable
- Low Power Shutdown Mode (SP3481)
- -7V to +12V Common-Mode Input Voltage Range
- Allows up to 32 transceivers on the serial bus
- Compatibility with the industry standard 75176 pinout
- Driver Output Short-Circuit Protection



Now Available in Lead Free Packaging

DESCRIPTION

The **SP3481** and the **SP3485** are a family of +3.3V low power half-duplex transceivers that meet the specifications of the RS-485 and RS-422 serial protocols. These devices are pin-to-pin compatible with the Sipex SP481, SP483, and SP485 devices as well as popular industry standards. The **SP3481** and the **SP3485** feature Sipex's BiCMOS process, allowing low power operation without sacrificing performance. The **SP3481** and **SP3485** meet the electrical specifications of RS-485 and RS-422 serial protocols up to 10Mbps under load. The **SP3481** is equipped with a low power Shutdown mode.

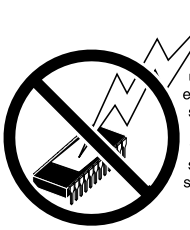


SP3481 and SP3485

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... +6.0V
Input Voltages
Logic ..... -0.3V to +6.0V
Drivers ..... -0.3V to +6.0V
Receivers ..... ±15V
Output Voltages
Drivers ..... ±15V
Receivers ..... -0.3V to +6.0V
Storage Temperature ..... -65°C to +150°C
Power Dissipation per Package
8-pin NSOIC (derate 6.90mW/°C above +70°C) 600mW
8-pin PDIP (derate 11.8mW/°C above +70°C) 1000mW



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

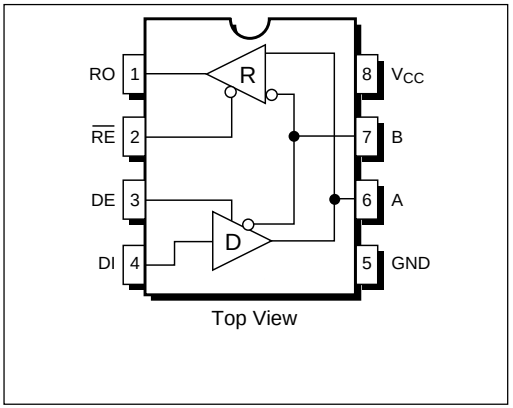
$T_{AMB} = T_{MIN}$ to T_{MAX} and V_{CC} = +3.3V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP3481/SP3485 DRIVER DC Characteristics					
Differential Output Voltage	GND		V_{CC}	Volts	Unloaded; R = ∞; *Figure 1*
Differential Output Voltage	2		V_{CC}	Volts	with load; R = 50Ω; (RS-422); *Figure 1*
Differential Output Voltage	1.5		V_{CC}	Volts	with load; R = 27Ω; (RS-485); *Figure 1*
Change in Magnitude of Driver Differential Output Voltage for Complimentary States			0.2	Volts	R = 27Ω or R = 50Ω; *Figure 1*
Driver Common-Mode Output Voltage			3	Volts	R = 27Ω or R = 50Ω; *Figure 1*
Input High Voltage	2.0			Volts	Applies to DE, DI, $\overline{RE}$
Input Low Voltage			0.8	Volts	Applies to DE, DI, $\overline{RE}$
Input Current			±10	µA	Applies to DE, DI, $\overline{RE}$
Driver Short-Circuit Current					
V_{OUT} = HIGH			±250	mA	-7V ≤ V_O ≤ +12V
V_{OUT} = LOW			±250	mA	-7V ≤ V_O ≤ +12V
SP3481/SP3485 DRIVER AC Characteristics					
Maximum Data Rate	10			Mbps	$\overline{RE}$ = V_{CC}, DE = V_{CC}
Driver Input to Output, t_{PLH}	20	40	60	ns	*Figures 2 and 8*
Driver Input to Output, t_{PHL}	20	40	60	ns	*Figures 2 and 8*
Differential Driver Skew		2	10	ns	$\lvert t_{DO1} - t_{DO2} \rvert$ *Figures 2 and 9*
Driver Rise or Fall Time		5	20	ns	From 10% to 90% ; *Figures 3 and 9*
Driver Enable to Output High		52	120	ns	*Figures 4 and 10*
Driver Enable to Output Low		60	120	ns	*Figures 5 and 10*
Driver Disable Time from Low		40	120	ns	*Figures 5 and 10*
Driver Disable Time from High		60	120	ns	*Figures 4 and 10*
SP3481/SP3485 RECEIVER DC Characteristics					
Differential Input Threshold	-0.2		+0.2	Volts	-7V ≤ V_{CM} ≤ +12V
Input Hysteresis		20		mV	V_{CM} = 0V
Output Voltage High	V_{CC}-0.4			Volts	V_{ID} = +200mV, -1.5mA
Output Voltage Low			0.4	Volts	V_{ID} = -200mV, 2.5mA
Three-State (High Impedance) Output Current			±1	µA	0V ≤ V_O ≤ V_{CC}; $\overline{RE}$ = V_{CC}
Input Resistance	12	15		kΩ	-7V ≤ V_{CM} ≤ +12V
Input Current (A, B); V_{IN} = 12V			1.0	mA	DE = 0V, V_{CC} = 0V or 3.6V, V_{IN} = 12V
Input Current (A, B); V_{IN} = -7V			-0.8	mA	DE = 0V, V_{CC} = 0V or 3.6V, V_{IN} = -7V
Short-Circuit Current	7		60	mA	0V ≤ V_{CM} ≤ V_{CC}

SPECIFICATIONS (continued)

$T_{AMB} = T_{MIN}$ to T_{MAX} and V_{CC} = +3.3V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP3481/SP3485 RECEIVER					
AC Characteristics					
Maximum Data Rate	10			Mbps	$\overline{RE}$ = 0V, DE = 0V
Receiver Input to Output, t_{PLH}	40	70	100	ns	*Figures 6 and 11*
			70	ns	T_{AMB} = +25ºC, V_{CC} = +3.3V, *Figures 6 and 11*
Receiver Input to Output, t_{PHL}	40	70	100	ns	*Figures 6 and 11*
			70	ns	T_{AMB} = +25ºC, V_{CC} = +3.3V, Figures 6 and 11
Differential Receiver Skew		4		ns	$t_{RSKEW} = \lvert t_{RPHL} - t_{RPLH} \rvert$ *Figures 6 and 11*
Receiver Enable to Output Low		35	60	ns	*Figures 7 and 12*; S_1 closed, S_2 open
Receiver Enable to Output High		35	60	ns	*Figures 7 and 12*; S_2 closed, S_1 open
Receiver Disable from Low		35	60	ns	*Figures 7 and 12*; S_1 closed, S_2 open
Receiver Disable from High		35	60	ns	*Figures 7 and 12*; S_2 closed, S_1 open
SP3481 Shutdown Timing					
Time to Shutdown	50	75	200	ns	$\overline{RE}$ = 3.3V, DE = 0V
Driver Enable from Shutdown to Output High		65	150	ns	*Figures 4 and 10*
Driver Enable from Shutdown to Output Low		65	150	ns	*Figures 5 and 10*
Receiver Enable from Shutdown to Output High		50	200	ns	*Figures 7 and 12;* S_2 closed, S_1 open
Receiver Enable from Shutdown to Output Low		50	200	ns	*Figures 7 and 12;* S_1 closed, S_2 open
POWER REQUIREMENTS					
Supply Current					
SP3481/3485					
No Load		1000	2000	µA	$\overline{RE}$, DI = 0V or V_{CC}; DE = V_{CC}
		800	1500	µA	$\overline{RE}$ = 0V, DI = 0V or V_{CC}; DE = 0V
SP3481					
Shutdown Mode			10	µA	DE = 0V, $\overline{RE}$=V_{CC}



SP3481/SP3485
Pinout (Top View)

PIN FUNCTION

Pin 1 – RO – Receiver Output.

Pin 2 – $\overline{RE}$ – Receiver Output Enable Active LOW.

Pin 3 – DE – Driver Output Enable Active HIGH.

Pin 4 – DI – Driver Input.

Pin 5 – GND – Ground Connection.

Pin 6 – A – Driver Output/Receiver Input Non-inverting.

Pin 7 – B – Driver Output/Receiver Input Inverting.

Pin 8 – V_{CC}

DESCRIPTION

The **SP3481** and the **SP3485** are 2 members in the family of +3.3V low power half-duplex transceivers that meet the specifications of the RS-485 and RS-422 serial protocols. These devices are pin-to-pin compatible with the Sipex SP481, SP483, and SP485 devices as well as popular industry standards. The **SP3481** and the **SP3485** feature Sipex's BiCMOS process allowing low power operation without sacrificing performance.

Drivers

The driver outputs of the **SP3481** and **SP3485** are differential outputs meeting the RS-485 and RS-422 standards. The typical voltage output swing with no load will be 0 Volts to +3.3 Volts. With a load of 54Ω across the differential outputs, the drivers maintain greater than 1.5V voltage levels. The drivers of the **SP3481** and **SP3485** have an enable control line which is active HIGH. A logic HIGH on DE (pin 3) will enable the differential driver outputs. A logic LOW on DE (pin 3) will tri-state the driver outputs.

The tranceivers in the **SP3481** and **SP3485** operate up to 10Mbps. The 250mA I_{SC} maximum limit on the driver output allows the **SP3481** and the **SP3485** to withstand an infinite short circuit over the -7.0V to +12.0V common mode range without catastrophic damage to the IC.

Receivers

The **SP3481** and **SP3485** receivers have differential inputs with an input sensitivity as low as ±200mV. Input impedance of the receivers is typically 15kΩ (12kΩ minimum). A wide common mode range of -7V to +12V allows for large ground potential differences between systems. The receivers of the **SP3481** and **SP3485** have a tri-state enable control pin. A logic LOW on $\overline{RE}$ (pin 2) will enable the receiver, a logic HIGH on $\overline{RE}$ (pin 2) will disable the receiver.

The receivers of the **SP3481** and **SP3485** operate up to 10Mbps. The receiver for each of the three devices is equipped with fail-safe. Fail-safe guarantees that the receiver output will be in a HIGH state when the input is left unconnected.

Shutdown Mode for the SP3481

The **SP3481** is equipped with a Shutdown mode. To enable the Shutdown state, both the driver and receiver must be disabled simultaneously. A logic LOW on DE (pin 3) and a logic HIGH on $\overline{RE}$ (pin 2) will put the **SP3481** into Shutdown mode. In Shutdown, supply current will drop to typical 1μA, 10μA maximum.

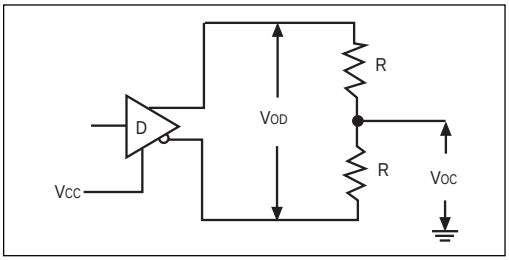


Figure 1. Driver DC Test Load Circuit

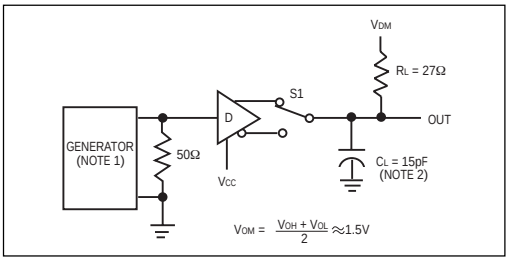


Figure 2. Driver Propagation Delay Test Circuit

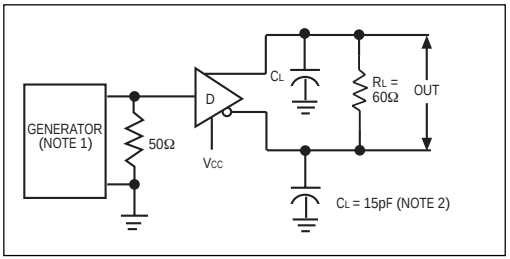


Figure 3. Driver Differential Output Delay and Transition Time Circuit

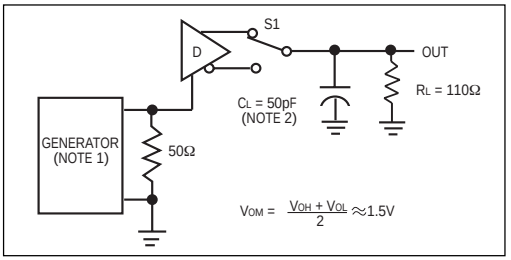


Figure 4. Driver Enable and Disable Timing Circuit, Output HIGH

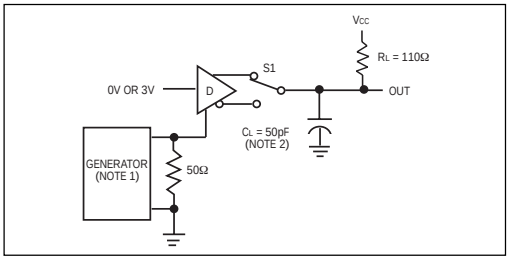


Figure 5. Driver Enable and Disable Timing Circuit, Output LOW

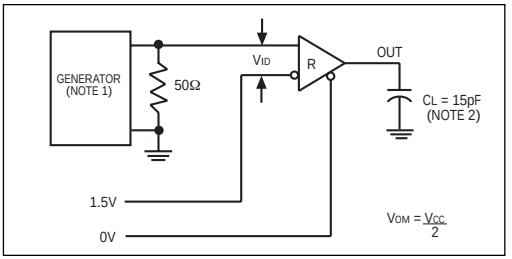


Figure 6. Receiver Propagation Delay Test Circuit

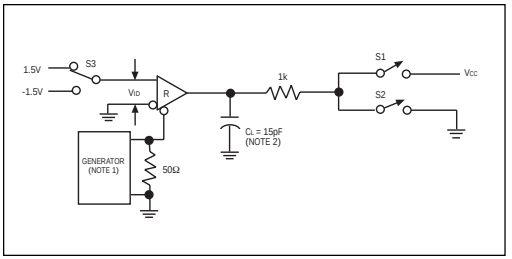


Figure 7. Receiver Enable and Disable Timing Circuit

INPUTS				OUTPUTS	
$\overline{RE}$	DE	DI	LINE CONDITION	B	A
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z

Table 1. Transmit Function Truth Table

INPUTS			OUTPUTS
$\overline{RE}$	DE	A - B	R
0	0	+0.2V	1
0	0	-0.2V	0
0	0	Inputs Open	1
1	0	X	Z

Table 2. Receive Function Truth Table

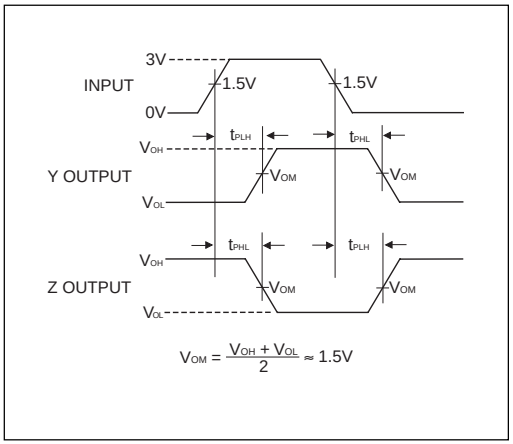


Figure 8. Driver Propagation Delay Waveforms

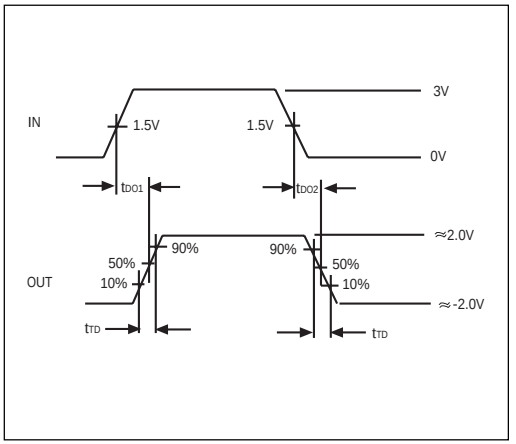


Figure 9. Driver Differential Output Delay and Transition Time Waveforms

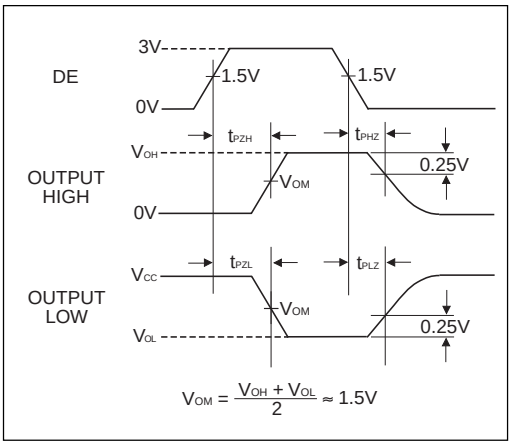


Figure 10. Driver Enable and Disable Timing Waveforms

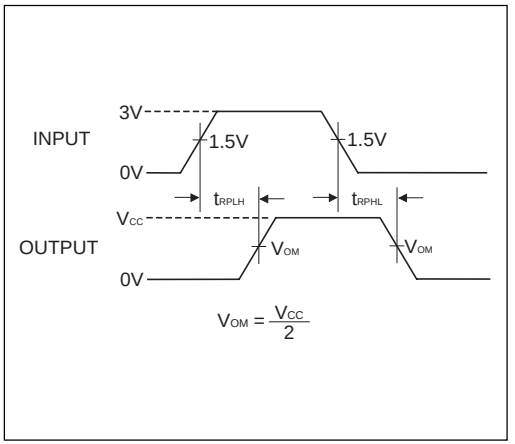


Figure 11. Receiver Propagation Delay Waveforms

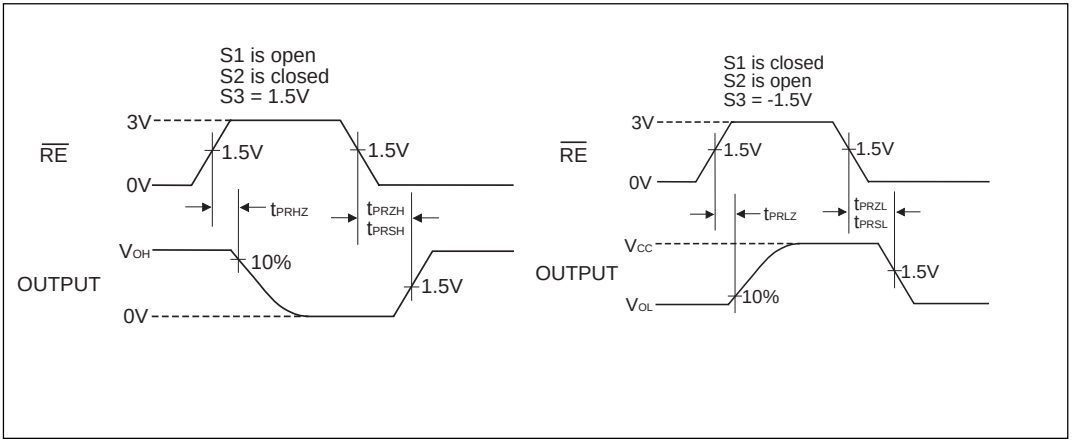
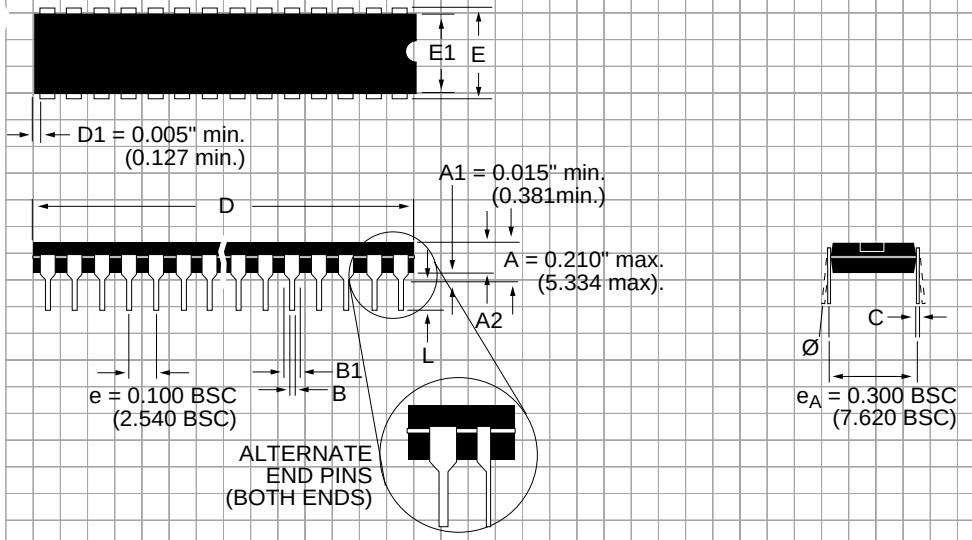


Figure 12. Receiver Enable and Disable Waveforms

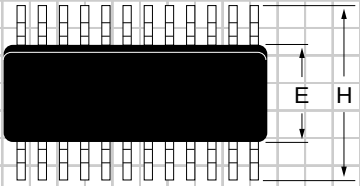
NOTE 1: The input pulse is supplied by a generator with the following characteristics: PRR=250KHz, 50% duty cycle, t_r < 6.0ns, Z_0=50Ω.
NOTE 2: C_L includes probe and stray capacitance.

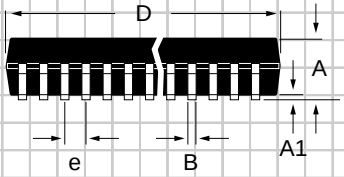
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

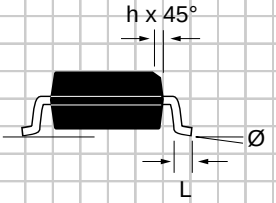


DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A2	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)
E	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)







DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249
B	0.014/0.019 (0.35/0.49)
D	0.189/0.197 (4.80/5.00)
E	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

