

PNP Silicon Darlington Transistor

- High collector current
- Low collector-emitter saturation voltage
- Complementary types: BSP50...BSP52 (NPN)
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101



Type	Marking	Pin Configuration						Package
		1=B	2=C	3=E	4=C	-	-	
BSP60	BSP60	1=B	2=C	3=E	4=C	-	-	SOT223
BSP61	BSP61	1=B	2=C	3=E	4=C	-	-	SOT223
BSP62	BSP62	1=B	2=C	3=E	4=C	-	-	SOT223

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}		V
BSP60		45	
BSP61		60	
BSP62		80	
Collector-base voltage	V_{CBO}		
BSP60		60	
BSP61		80	
BSP62		90	
Emitter-base voltage	V_{EBO}	5	
Collector current	I_C	1	A
Peak collector current, $t_p \leq 10$ ms	I_{CM}	2	
Base current	I_B	100	mA
Total power dissipation- $T_S \leq 124$ °C	P_{tot}	1.5	W
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}	≤ 17	K/W

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Collector-emitter breakdown voltage $I_C = 10 \text{ mA}$, $I_B = 0$, BSP60 $I_C = 10 \text{ mA}$, $I_B = 0$, BSP61 $I_C = 10 \text{ mA}$, $I_B = 0$, BCP62	$V_{(BR)CEO}$	45 60 80	- - -	- - -	V
Collector-base breakdown voltage $I_C = 100 \mu\text{A}$, $I_E = 0$, BSP60 $I_C = 100 \mu\text{A}$, $I_E = 0$, BSP61 $I_C = 100 \mu\text{A}$, $I_E = 0$, BSP62	$V_{(BR)CBO}$	60 80 90	- - -	- - -	
Emitter-base breakdown voltage $I_E = 100 \mu\text{A}$, $I_C = 0$	$V_{(BR)EBO}$	5	-	-	
Collector-emitter cutoff current $V_{CE} = V_{CE0max}$, $V_{BE} = 0$	I_{CES}	-	-	10	μA
Emitter-base cutoff current $V_{EB} = 4 \text{ V}$, $I_C = 0$	I_{EBO}	-	-	10	μA
DC current gain ²⁾ $I_C = 150 \text{ mA}$, $V_{CE} = 10 \text{ V}$ $I_C = 500 \text{ mA}$, $V_{CE} = 10 \text{ V}$	h_{FE}	1000 2000	- -	- -	-
Collector-emitter saturation voltage ²⁾ $I_C = 500 \text{ mA}$, $I_B = 0.55 \text{ mA}$ $I_C = 1 \text{ A}$, $I_B = 1 \text{ mA}$	V_{CEsat}	- -	- -	1.3 1.8	V
Base emitter saturation voltage ²⁾ $I_C = 500 \text{ mA}$, $I_B = 0.5 \text{ mA}$ $I_C = 1 \text{ A}$, $I_B = 1 \text{ mA}$	V_{BEsat}	- -	- -	1.9 2.2	

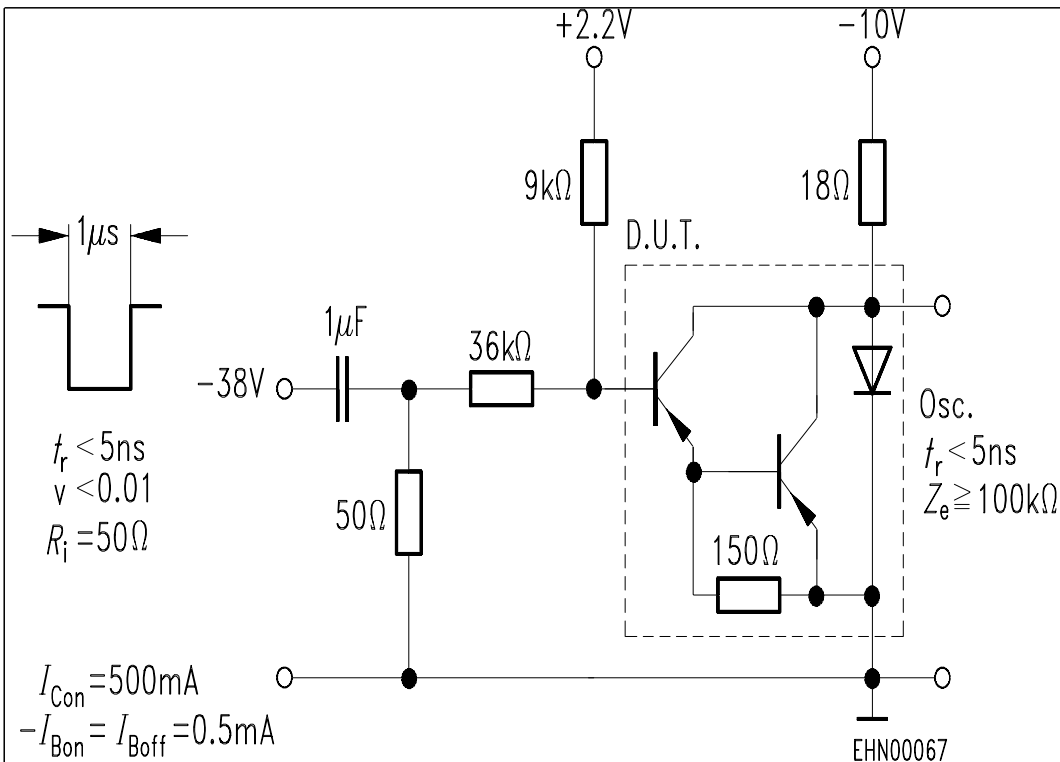
AC Characteristics

Transition frequency $I_C = 100 \text{ mA}$, $V_{CE} = 5 \text{ V}$, $f = 100 \text{ MHz}$	f_T	-	200	-	MHz
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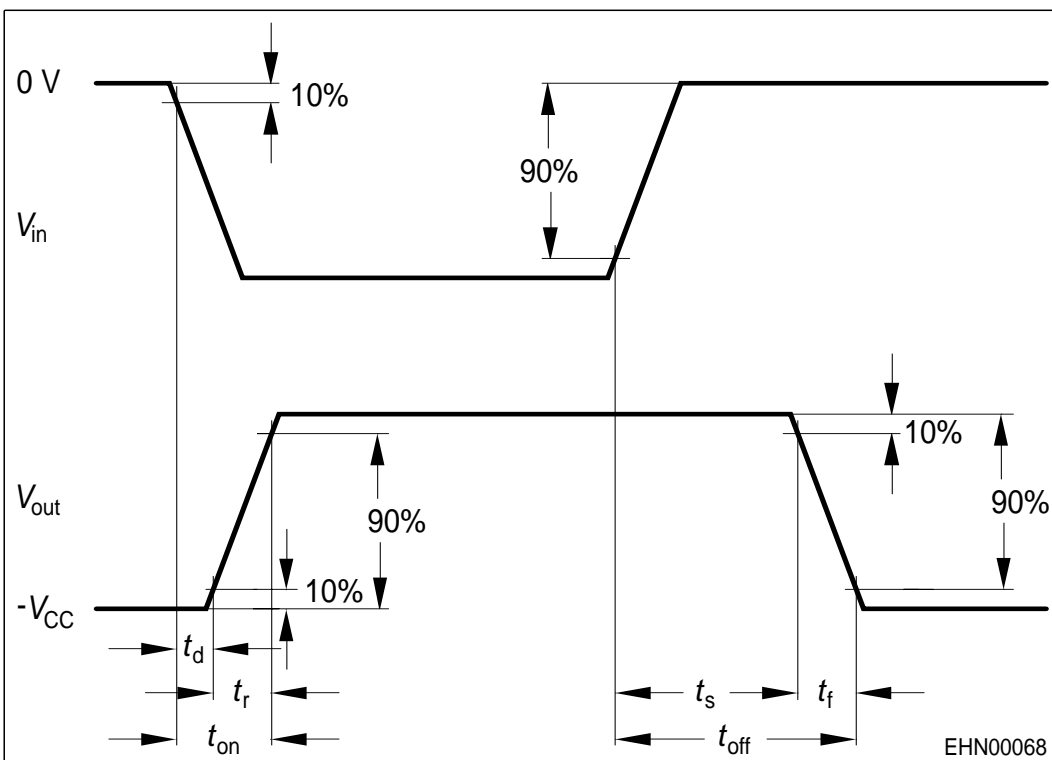
¹⁾For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

²⁾Pulse test: $t < 300 \mu\text{s}$; $D < 2\%$

Switching time test circuit

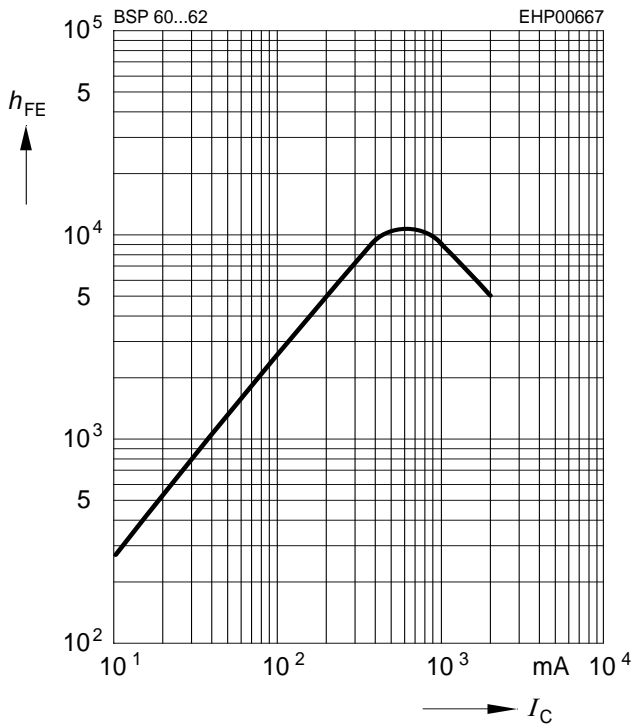


Switching time waveform



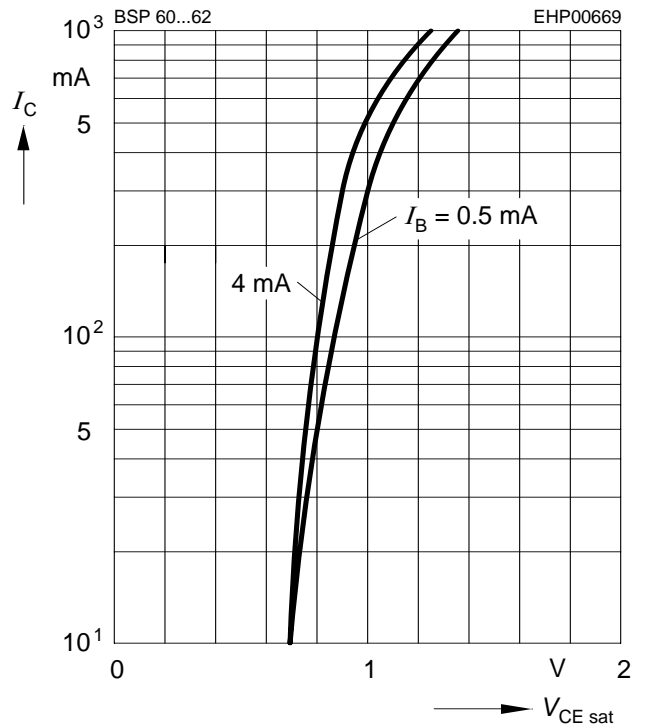
DC current gain $h_{FE} = f(I_C)$

$V_{CE} = 10\text{ V}$



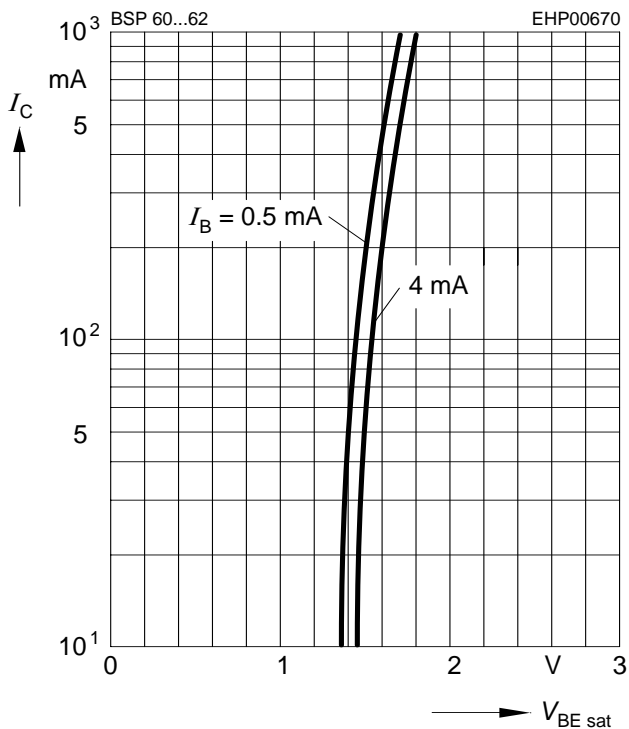
Collector-emitter saturation voltage

$I_C = f(V_{CEsat}), I_B = \text{Parameter}$



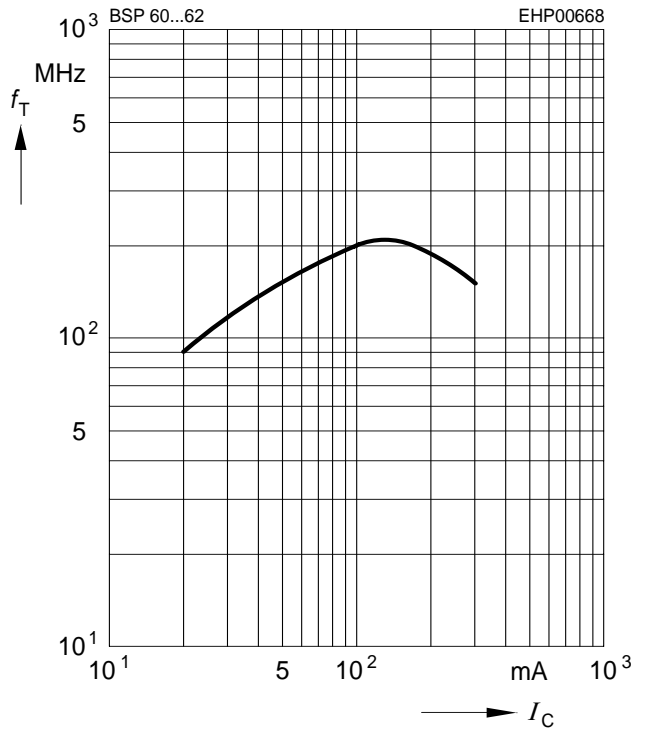
Base-emitter saturation voltage

$I_C = f(V_{BEsat}), I_B = \text{Parameter}$



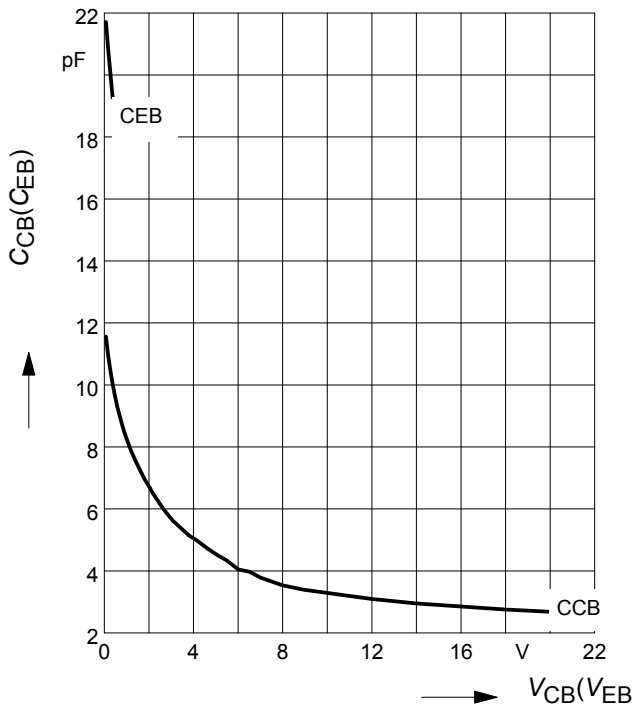
Transition frequency $f_T = f(I_C)$

$V_{CE} = 10\text{ V}, f = 100\text{ MHz}$

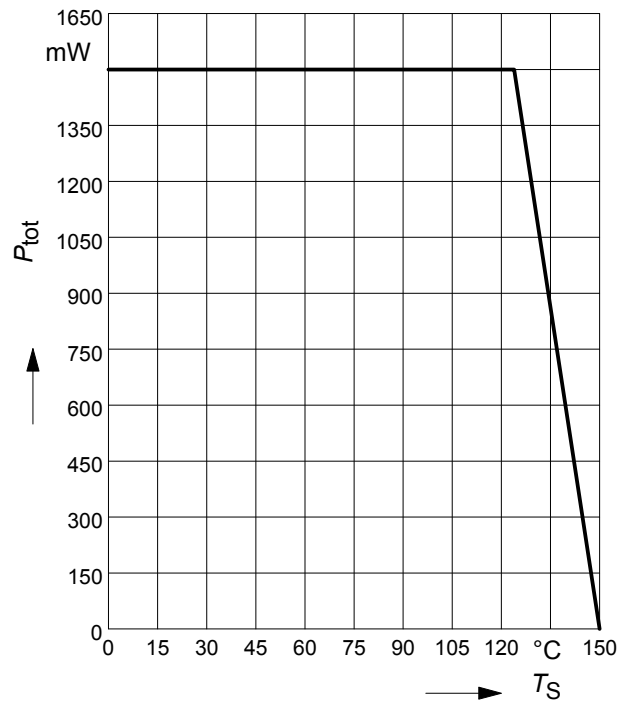


Collector-base capacitance $C_{cb} = f(V_{CB})$

Emitter-base capacitance $C_{eb} = f(V_{EB})$

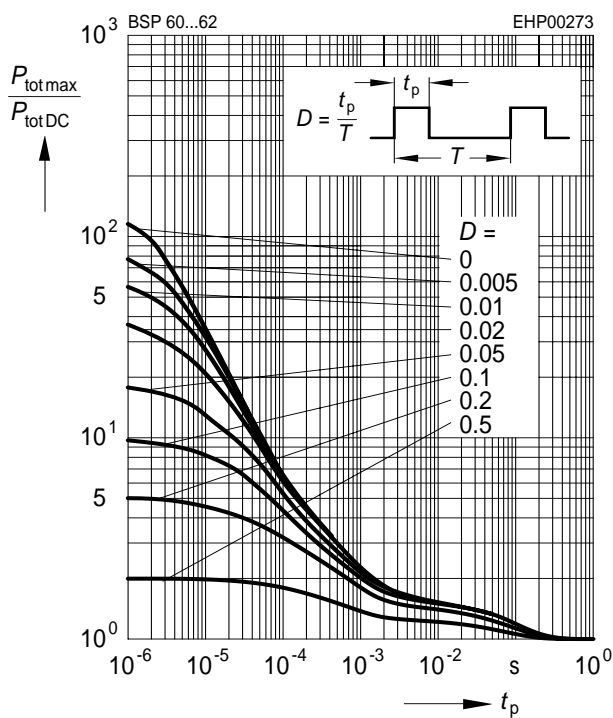


Total power dissipation $P_{tot} = f(T_S)$



Permissible Pulse Load

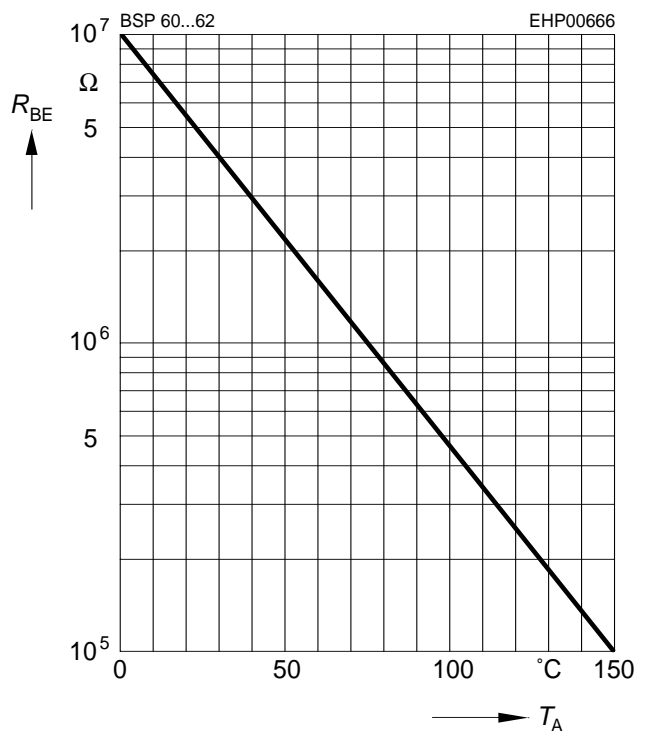
$P_{totmax}/P_{totDC} = f(t_p)$



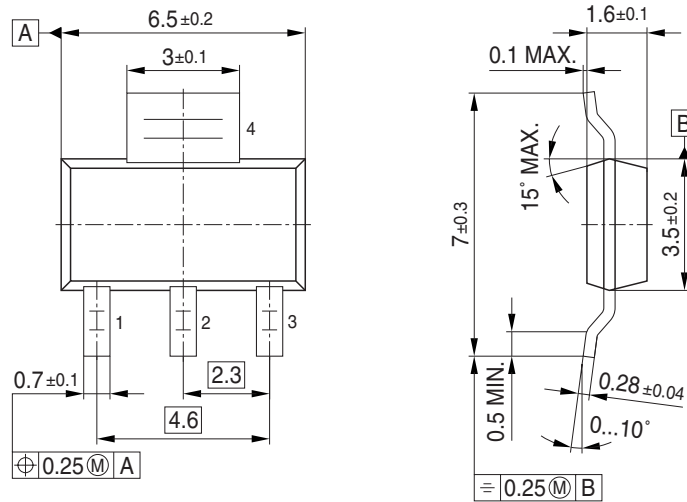
External resistance $R_{BE} = f(T_A)**$

$V_{CB} = V_{CEmax}$

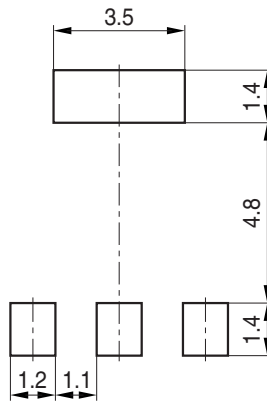
** R_{BEmax} for thermal stability



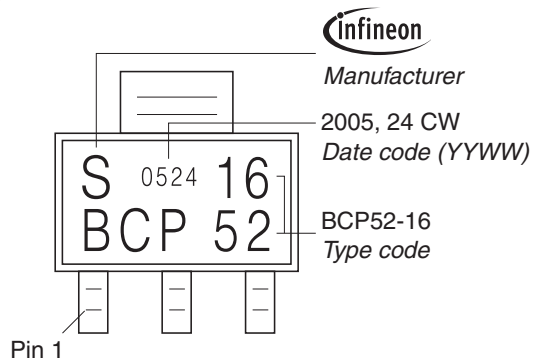
Package Outline



Foot Print



Marking Layout (Example)



Packing

Reel $\varnothing 180 \text{ mm} = 1.000 \text{ Pieces/Reel}$
 Reel $\varnothing 330 \text{ mm} = 4.000 \text{ Pieces/Reel}$

