

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT223 surface-mountable plastic package. This very sensitive gate "series D" triac is intended for interfacing with low power drivers including microcontrollers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drivers and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose low power motor control
- General purpose switching and phase control

4. Quick reference data

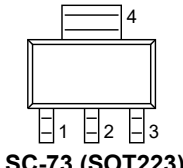
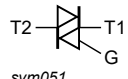
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|--|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 108\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 10 | A |
| | | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | - | 11 | A |
| T_j | junction temperature | | - | - | 125 | °C |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 9 | - | 2 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 9 | - | 2.5 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 9 | - | 2.5 | 5 | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--|-----|-----|-----|------------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 9 | - | 5 | 10 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 11 | - | 1.2 | 10 | mA |
| V_T | on-state voltage | $I_T = 2\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | - | 1.2 | 1.5 | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; $R_{GT1(ext)} = 1\text{ k}\Omega$ | - | 5 | - | V/ μ s |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|--|---|
| 1 | T1 | main terminal 1 |  <p>SC-73 (SOT223)</p> |  <p>sym051</p> |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| 4 | T2 | main terminal 2 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| BT134W-600D | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| BT134W-600D | BT134W-6D |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|--|-----|-----|------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 108\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 10 | A |
| | | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | 11 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 0.5 | A ² s |
| di_T/dt | rate of rise of on-state current | $I_G = 10\text{ mA}$ | - | 50 | A/ μ s |
| | | $I_G = 20\text{ mA}$ | - | 10 | A/ μ s |
| | | $I_G = 10\text{ mA}$ | - | 50 | A/ μ s |
| | | $I_G = 10\text{ mA}$ | - | 50 | A/ μ s |
| I_{GM} | peak gate current | | - | 2 | A |
| P_{GM} | peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.5 | W |
| T_{stg} | storage temperature | | -40 | 150 | °C |
| T_j | junction temperature | | - | 125 | °C |

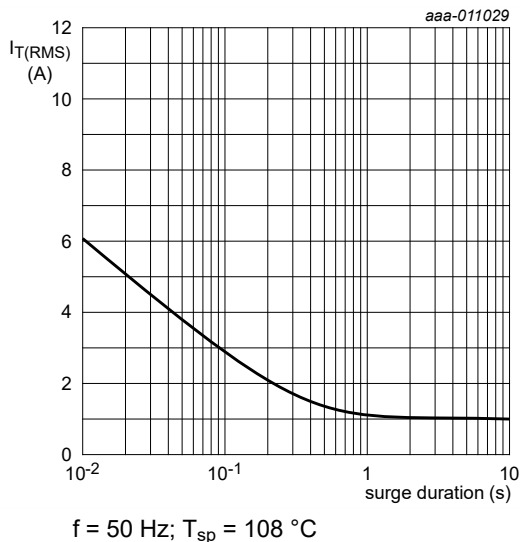


Fig. 1. RMS on-state current as a function of surge duration; maximum values

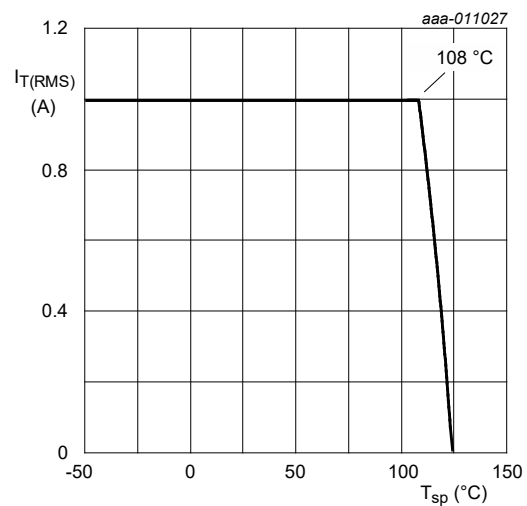


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

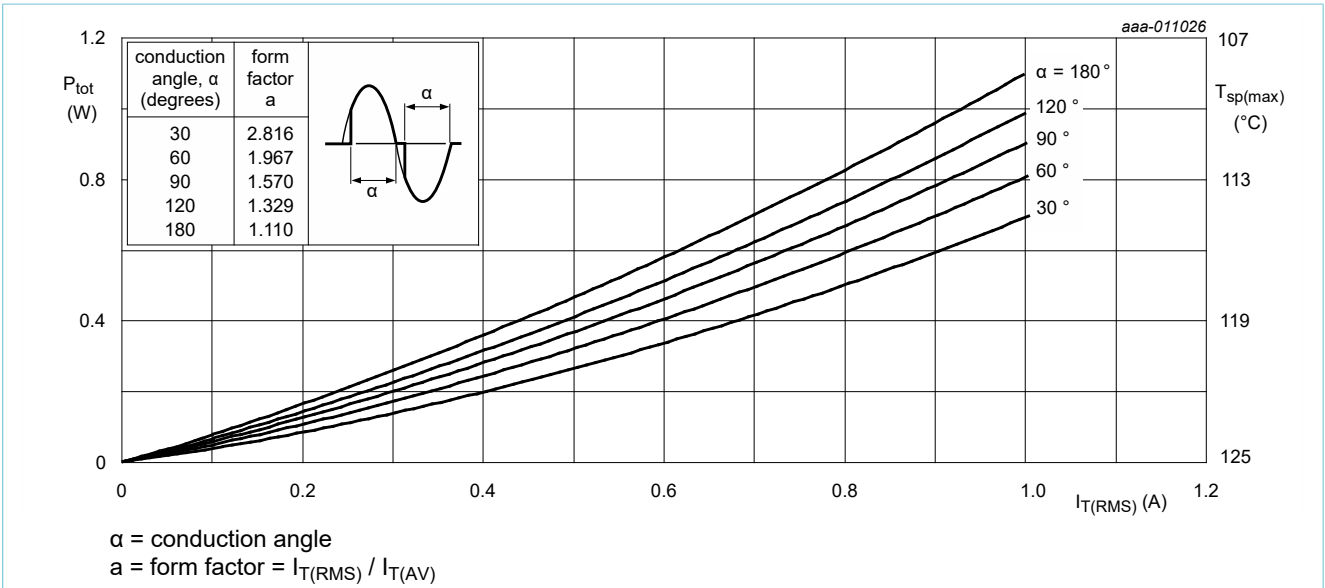


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

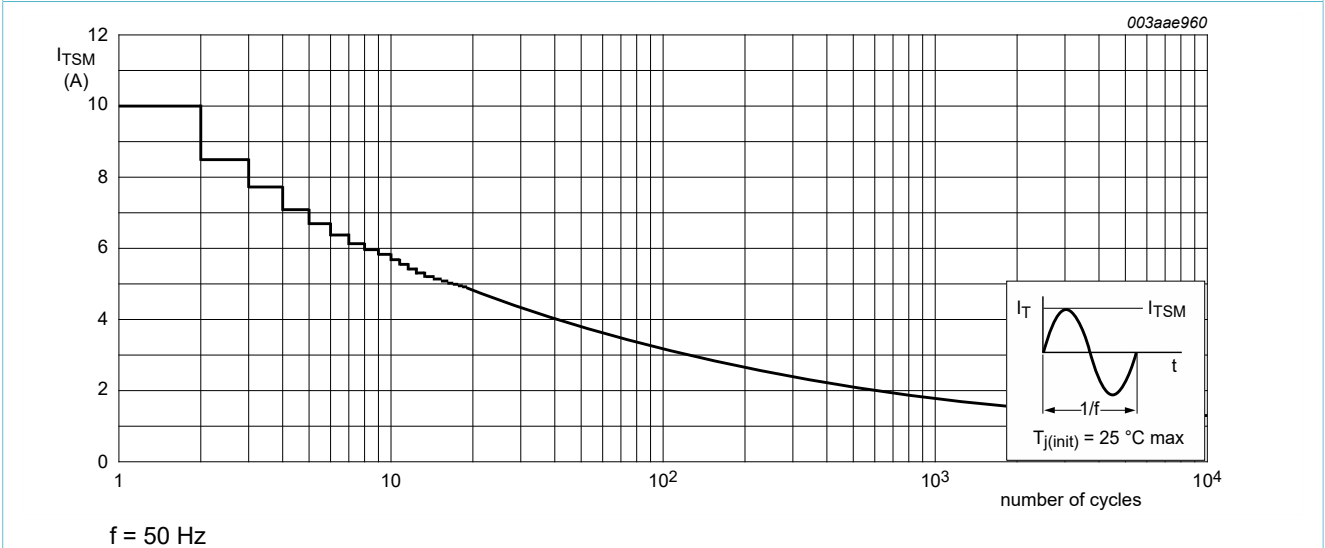
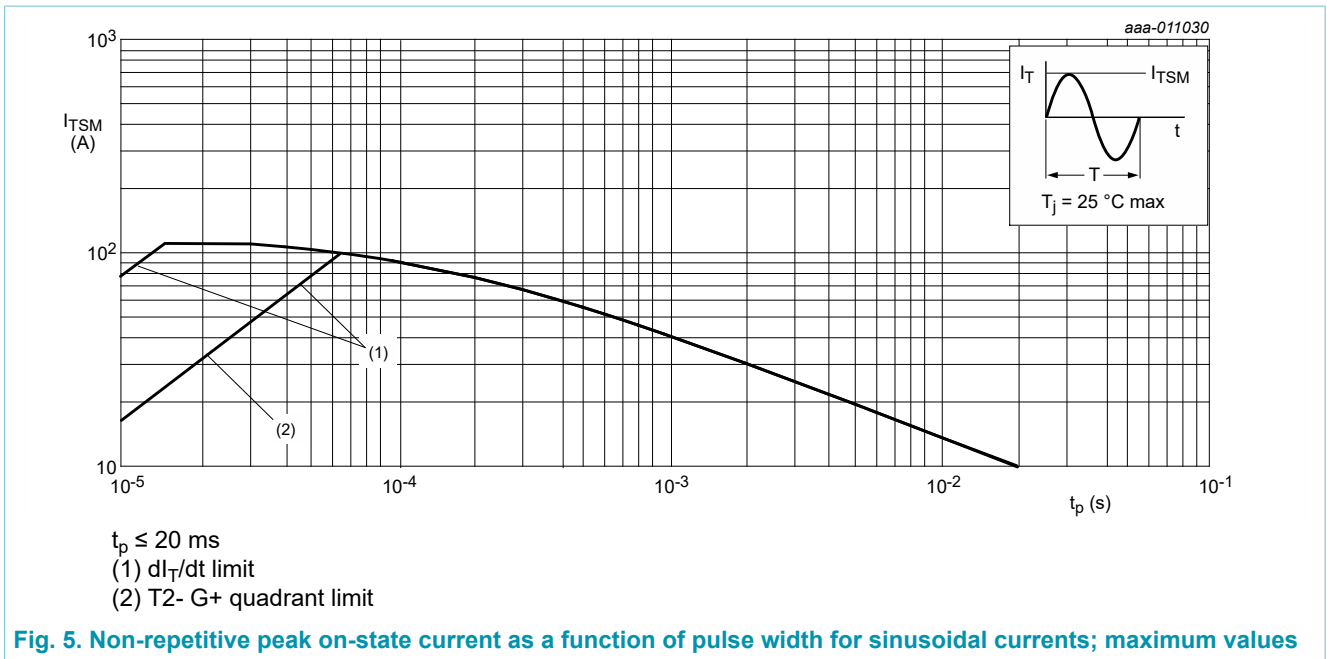


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|---|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | full cycle; Fig. 6 | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air; printed circuit board mounted; minimum footprint; Fig. 7 | - | 156 | - | K/W |
| | | in free air; printed circuit board mounted; pad area; Fig. 8 | - | 70 | - | K/W |

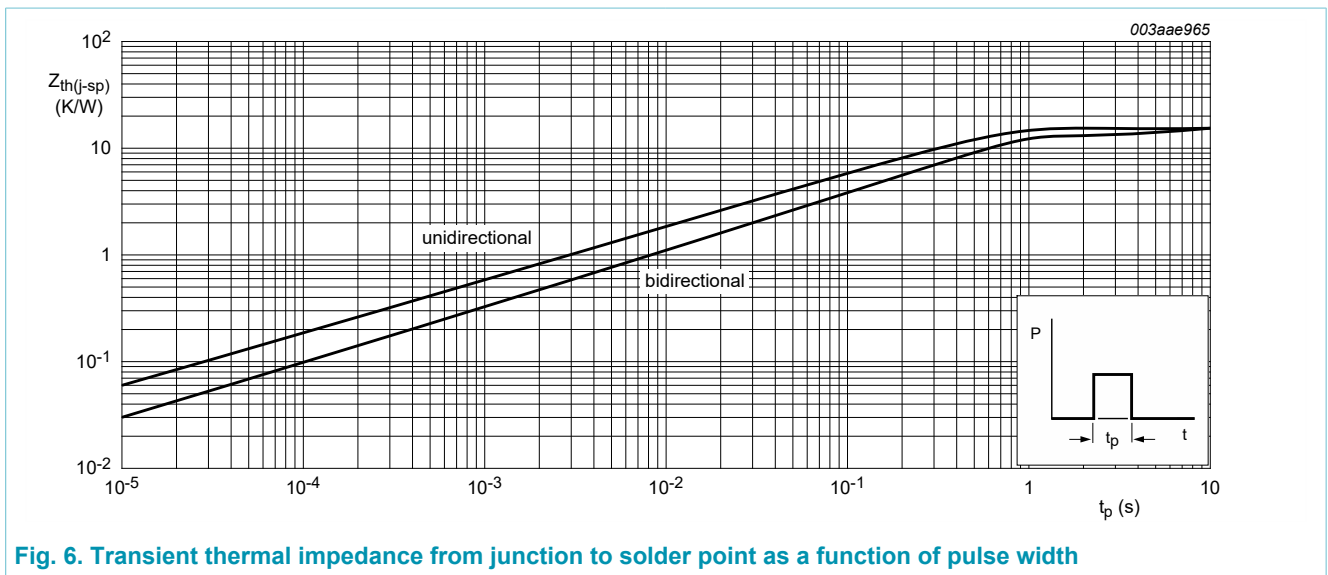
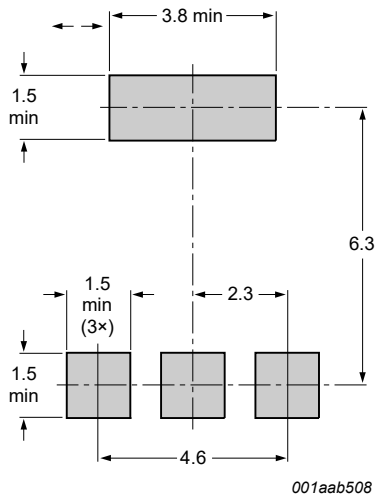
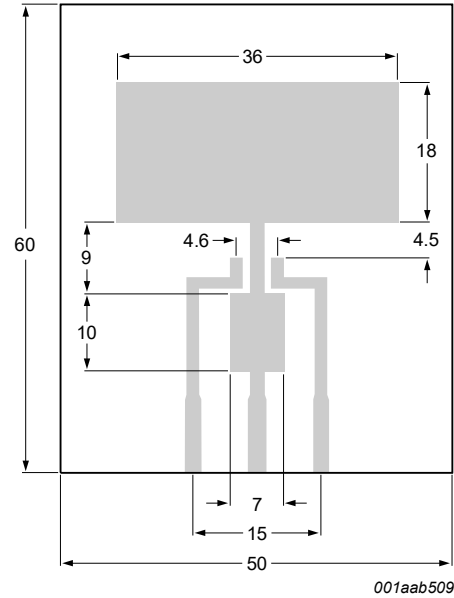


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width



All dimensions are in mm

Fig. 7. Minimum footprint SOT223



All dimensions are in mm

Printed circuit board:

FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 8. Printed circuit board pad area: SOT223

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--|------|-----|-----|------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 9 | - | 2 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 9 | - | 2.5 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 9 | - | 2.5 | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 9 | - | 5 | 10 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 10 | - | 1.6 | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 10 | - | 4.5 | 15 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 10 | - | 1.2 | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 10 | - | 2.2 | 15 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 11 | - | 1.2 | 10 | mA |
| V_T | on-state voltage | $I_T = 2\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | - | 1.2 | 1.5 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 13 | - | 0.7 | 1 | V |
| | | $V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$; Fig. 13 | 0.25 | 0.4 | - | V |
| I_D | off-state current | $V_D = 600\text{ V}$; $T_j = 125\text{ °C}$ | - | 0.1 | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; $R_{GT1(ext)} = 1\text{ k}\Omega$ | - | 5 | - | V/ μ s |
| t_{gt} | gate-controlled turn-on time | $I_{TM} = 1.5\text{ A}$; $V_D = 600\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$ | - | 2 | - | μ s |

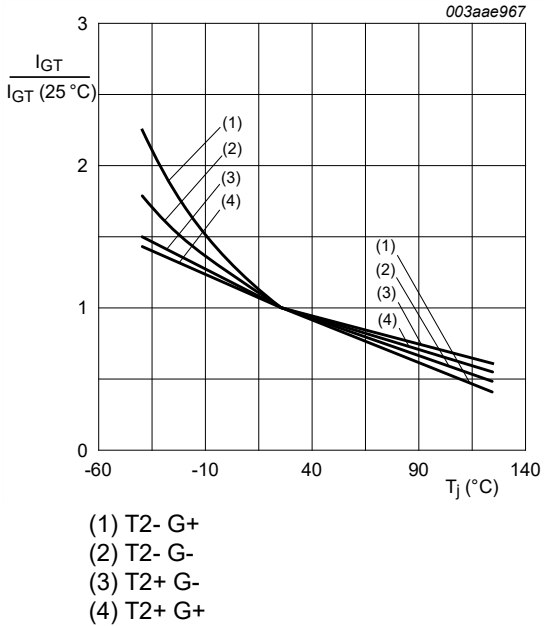


Fig. 9. Normalized gate trigger current as a function of junction temperature

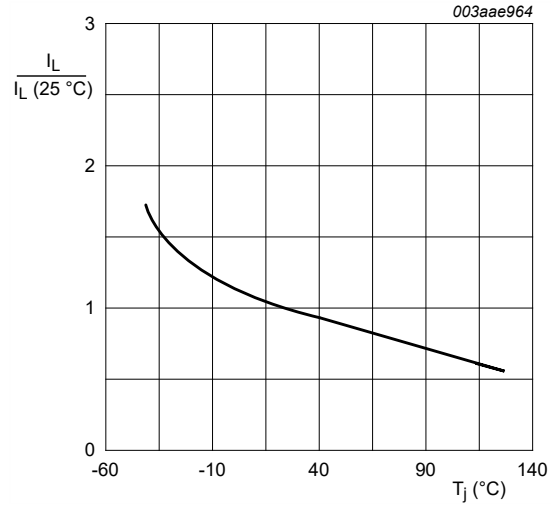


Fig. 10. Normalized latching current as a function of junction temperature

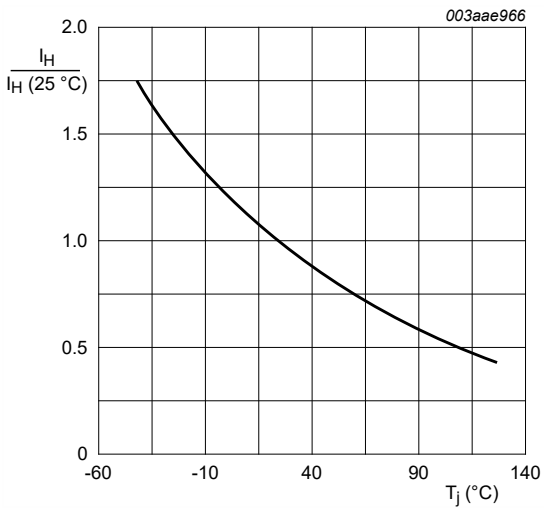


Fig. 11. Normalized holding current as a function of junction temperature

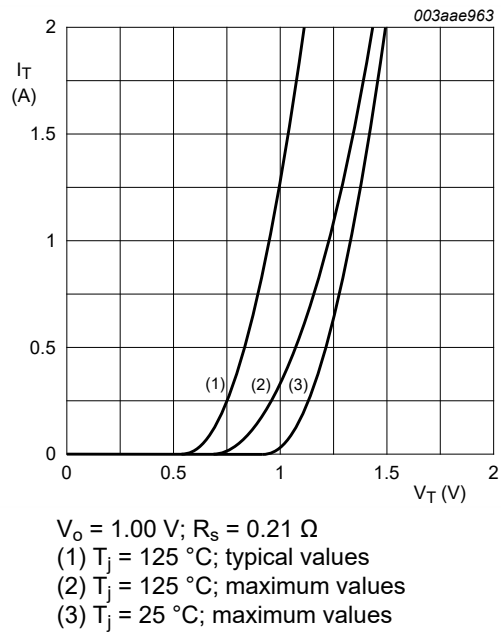


Fig. 12. On-state current as a function of on-state voltage

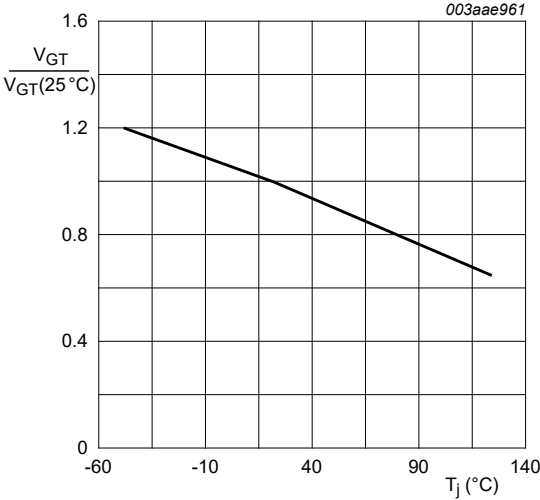


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

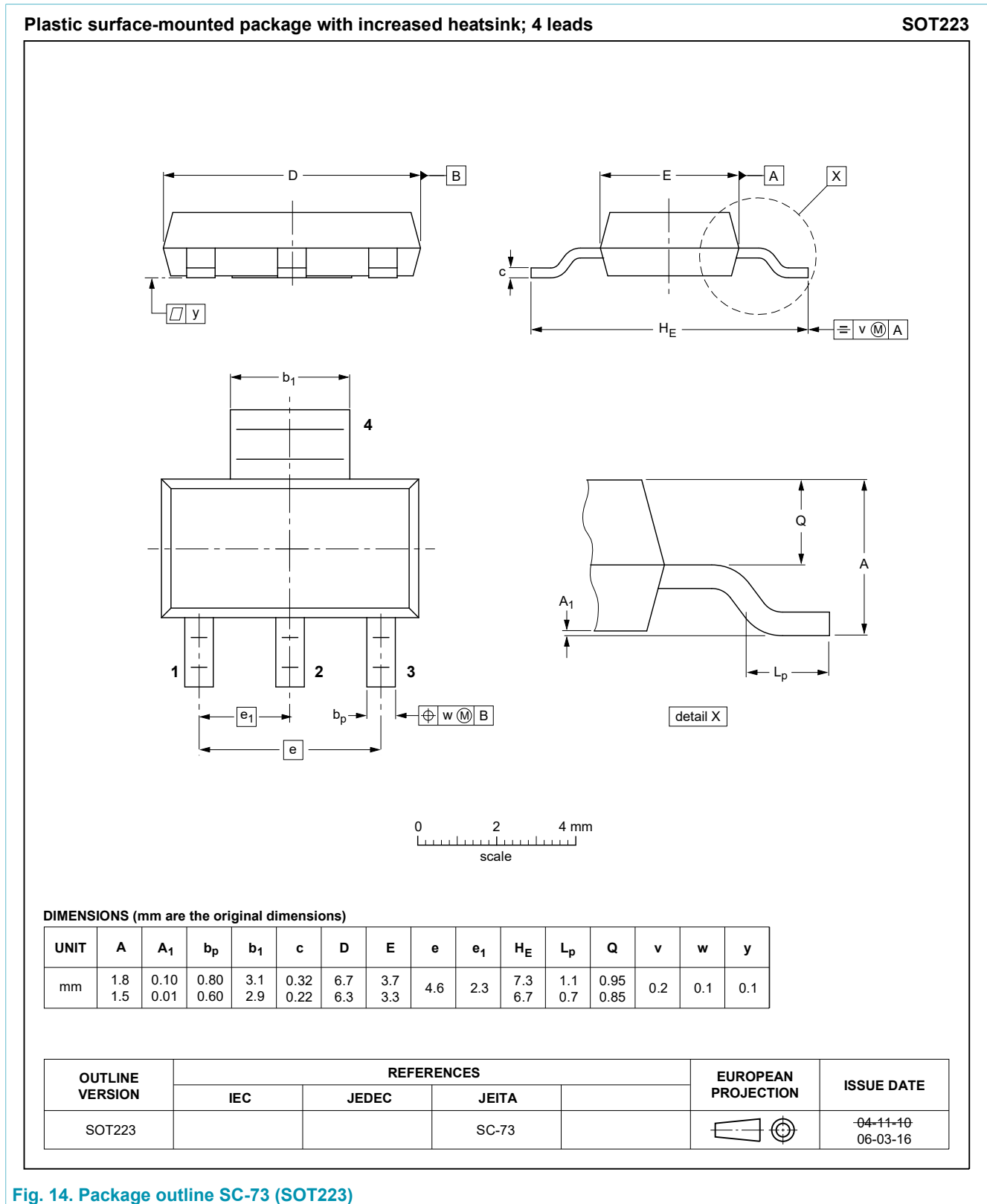


Fig. 14. Package outline SC-73 (SOT223)

12. Package outline (minimized)

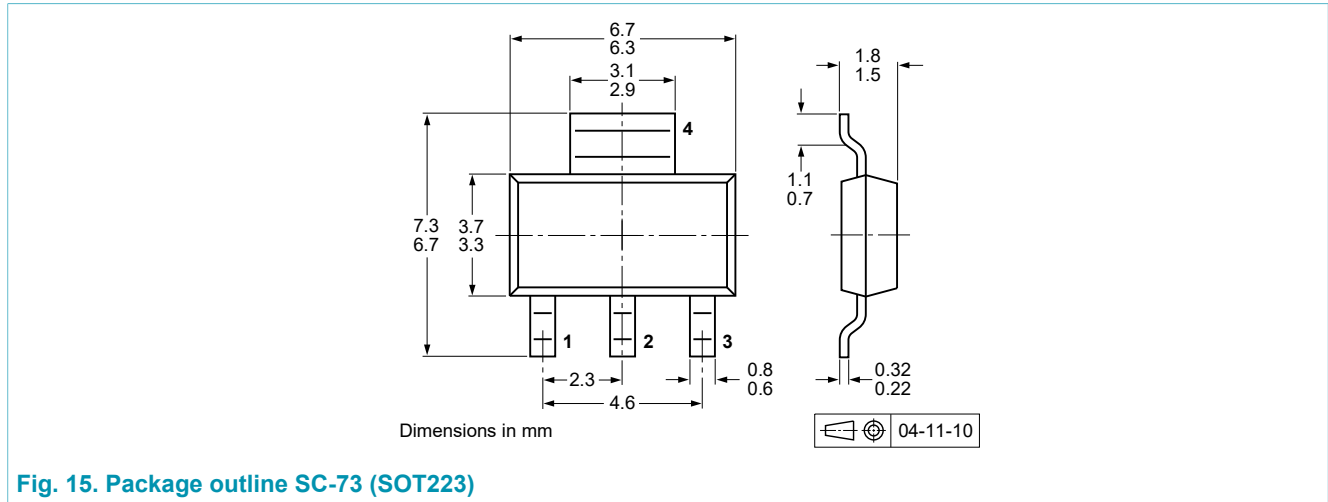


Fig. 15. Package outline SC-73 (SOT223)

13. Soldering

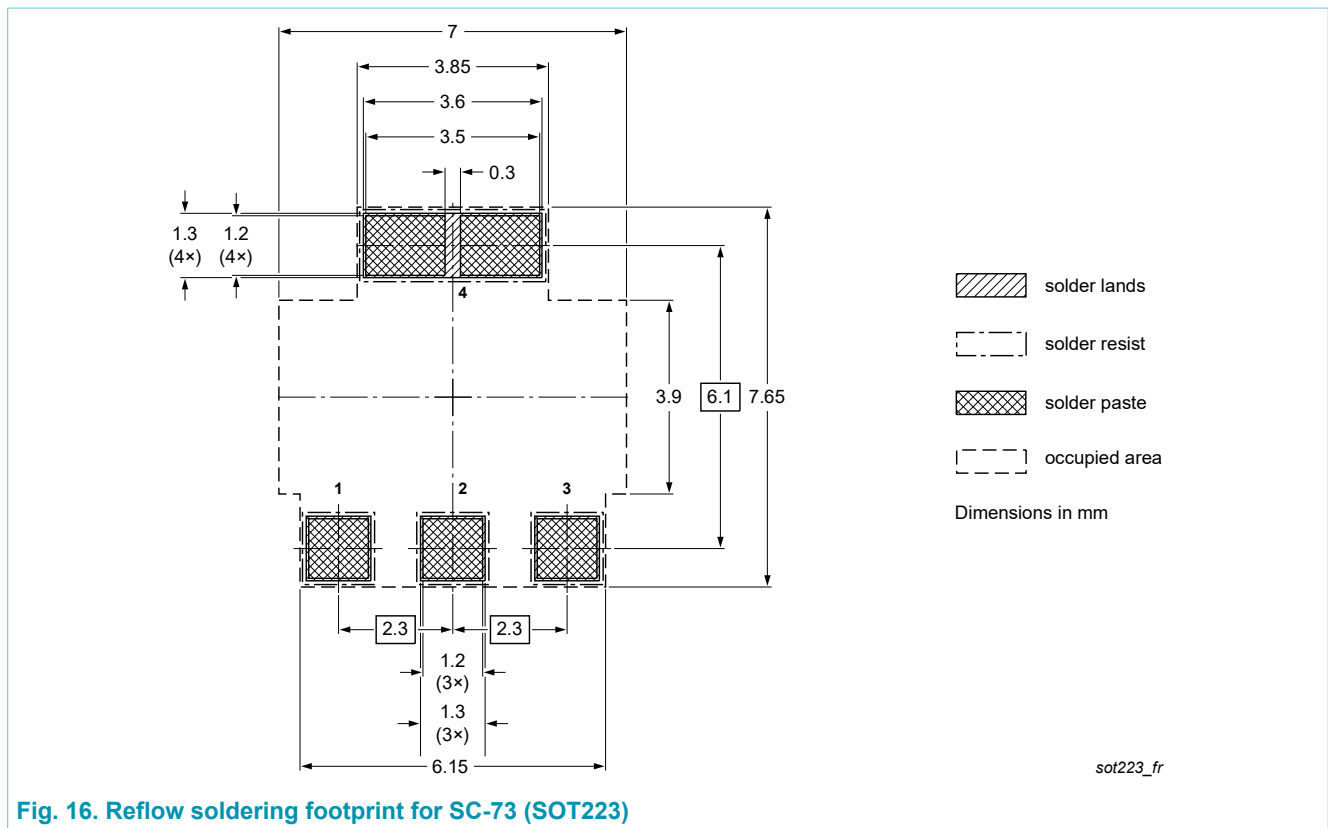
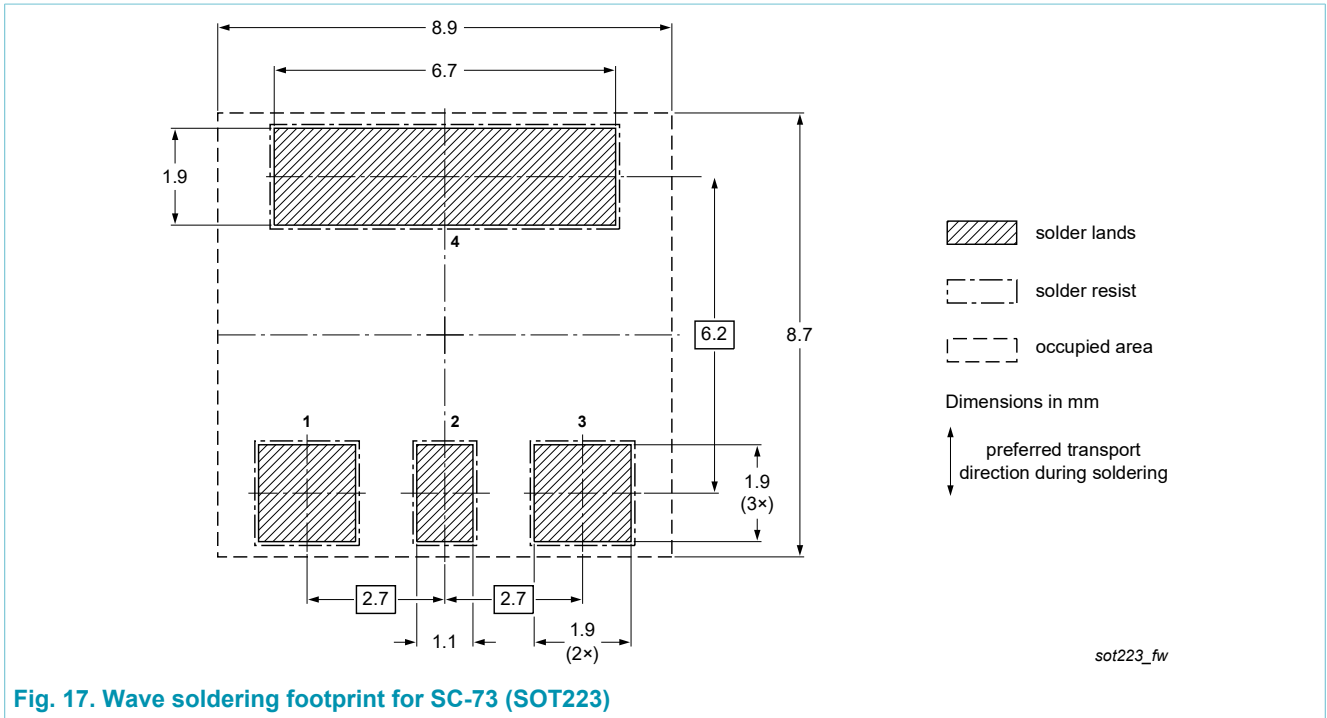


Fig. 16. Reflow soldering footprint for SC-73 (SOT223)



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|--------------------------------|--------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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