Picture cell driver for STN (LCD driver)
BU9716BK / BU9716BKV

The BU9716BK and BU9716BKV are man-machine interface ICs designed for applications such as multi-media portable terminals.
Specifically, these products are used as driver ICs for operating mode display LCD panels in portable terminals, household appliances, and other similar products. The number of display cells includes 32 segments and 3 commons, enabling drive of up to 96 cells.

●Applications
Multi-media portable terminals, POS terminals, ECR terminals, short wave radios, telephones, cameras, VCRs, movie projectors, car audio systems, and others

●Features
1) Up to 32 segment outputs and 3 common outputs can be displayed, for a total of 96 segments.
2) 1 / 3 duty display.
3) Either 1 / 2 or 1 / 3 can be selected for power supply for LCD display.

●Absolute maximum ratings (Ta = 25°C, V_{SS} = 0V)

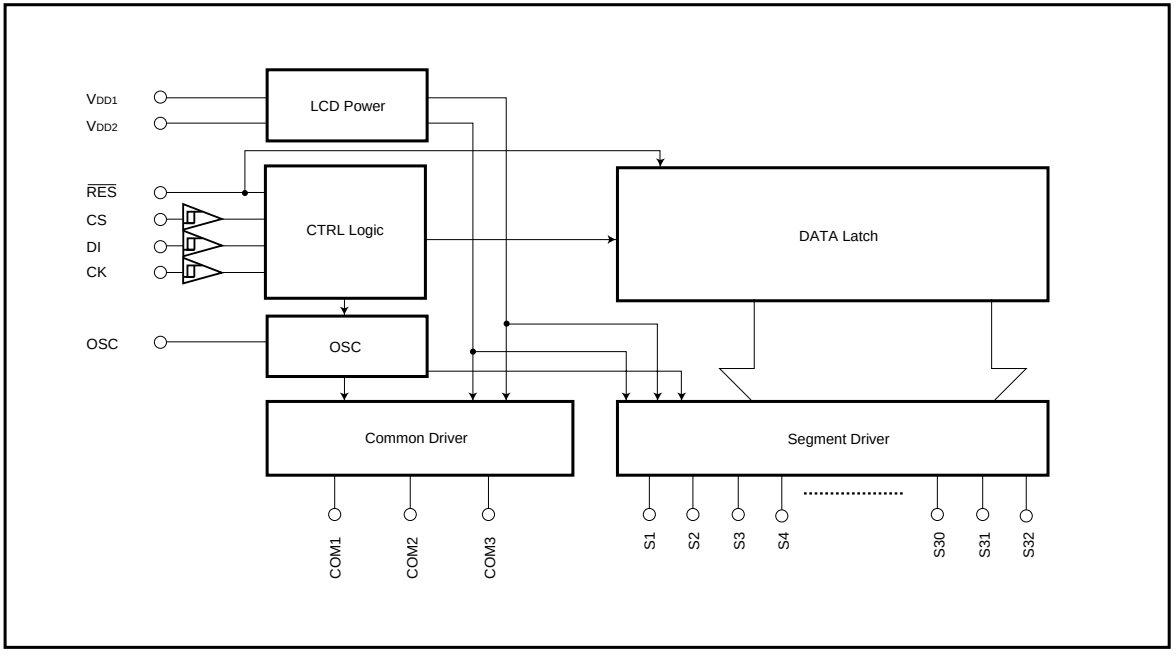
Parameter		Symbol	Limits	Unit
Power supply voltage		V_{DD}	– 0.3 ~ + 7.0	V
Power dissipation	BU9716BK	Pd	500*1	mW
	BU9716BKV		400*2	
Input voltage		V_{IN}	– 0.3 ~ V_{DD} + 0.3	V
Operating temperature		Topr	– 40 ~ + 85	°C
Storage temperature		Tstg	– 55 ~ + 125	°C

∗1 Reduced by 5mW for each increase in Ta of 1°C over 25°C .
∗2 Reduced by 4mW for each increase in Ta of 1°C over 25°C .

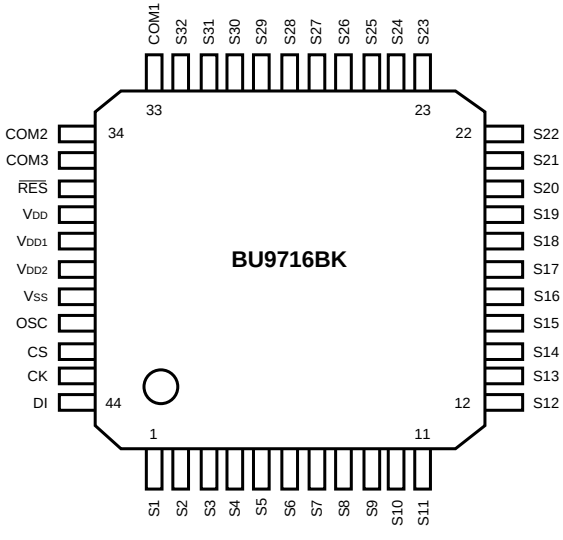
●Recommended operating conditions (Ta = 25°C, V_{SS} = 0V)

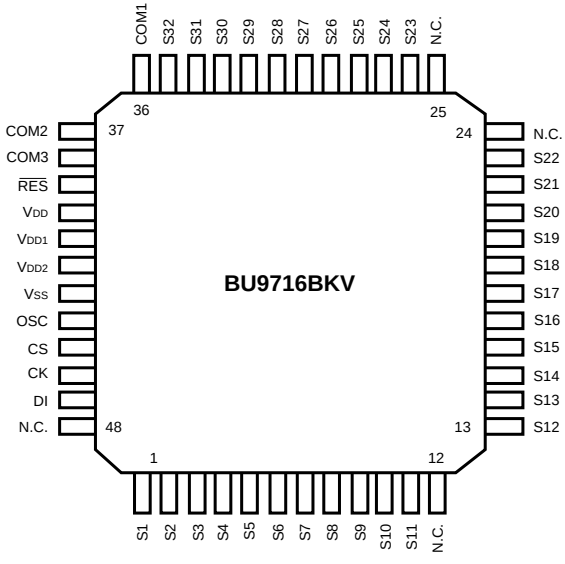
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.5	—	5.5	V
Input voltage	V_{DD1}	0	2 / 3V_{DD}	V_{DD}	V
	V_{DD2}	0	1 / 3V_{DD}	V_{DD}	V

●Block diagram



●Pin assignments





●Pin descriptions (BU9716BK)

Pin No.	Pin name	I / O	Function	Processing when not used
1 - 32	S1 - S32	O	Output pin for segment data. Outputs consistent LCD drive voltage to the data corresponding to COM1 to COM3.	OPEN
33 34 35	COM1 COM2 COM3	O	Common driver output. The frame frequency is $f_C = (f_{OSC} / 384)$ Hz	OPEN
36	$\overline{RES}$	I	Reset input. At $\overline{RES}$ = L, internal data (including control data) is reset.	V_{DD}
41	OSC	—	Oscillator pin (for common and segment alternating waveforms)	V_{SS}
42	CS	I	Chip select input. At CS = H, data can be transferred.	V_{SS}
43	CK	I	Synchronous clock input for serial data transfer	V_{SS}
44	DI	I	Serial data input	V_{SS}
38	V_{DD1}	—	Internal reference voltage for LCD drive. In 1 / 2 bias mode, this is connected to V_{DD2}.	OPEN
39	V_{DD2}	—	Internal reference voltage for LCD drive. In 1 / 2 bias mode, this is connected to V_{DD1}.	OPEN

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input high level voltage	V_{IH}	$0.8V_{DD}$	—	V_{DD}	V	CS, CK, DI, $\overline{RES}$
Input low level voltage	V_{IL}	0	—	$0.2V_{DD}$	V	CS, CK, DI, $\overline{RES}$
Input high level current	I_{IH}	0	—	6.0	µA	CS, CK, DI, $\overline{RES}$, $V_I = V_{DD}$
Input low level current	I_{IL}	0	—	6.0	µA	CS, CK, DI, $\overline{RES}$, $V_I = V_{SS}$
Output high level voltage	V_{SOH}	—	$V_{DD} – 1.0$	—	V	S1 ~ S32, I_O = – 20µA
	V_{COH}	—	$V_{DD} – 1.0$	—	V	COM1 ~ COM3, I_O = – 100µA
Output low level voltage	V_{SOL}	—	1.0	—	V	S1 ~ S32, I_O = – 20µA
	V_{COL}	—	1.0	—	V	COM1 ~ COM3, I_O = – 100µA
Intermediate output voltage	V_{CM1}	—	$1 / 2V_{DD} \pm 1.0$	—	V	COM1 ~ COM3, 1 / 2Bias
	V_{SM1}	—	$2 / 3V_{DD} \pm 1.0$	—	V	S1 ~ S32, 1 / 3Bias
	V_{CM2}	—	$2 / 3V_{DD} \pm 1.0$	—	V	COM1 ~ COM3, 1 / 3Bias
	V_{SM2}	—	$1 / 3V_{DD} \pm 1.0$	—	V	S1 ~ S32, 1 / 3Bias
	V_{CM3}	—	$1 / 3V_{DD} \pm 1.0$	—	V	COM1 ~ COM3, 1 / 3Bias
Power supply current	I_Q	—	30	70	µA	Low-power mode
	I_{DD}	—	100	300	µA	f_{OSC} = 38kHz

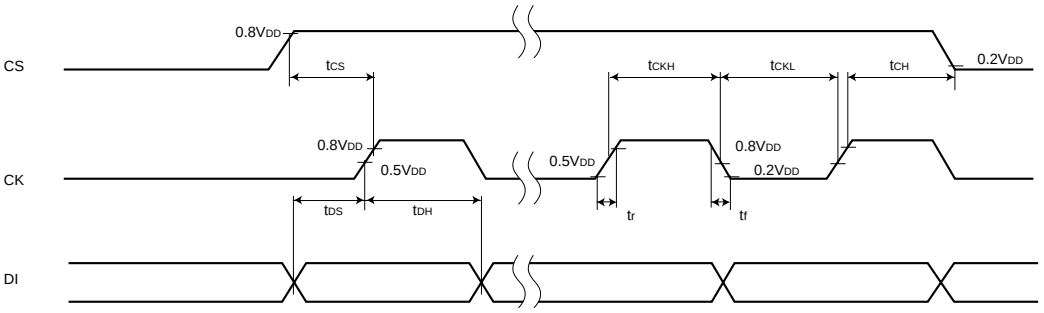
●Electrical characteristics

AC characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V)

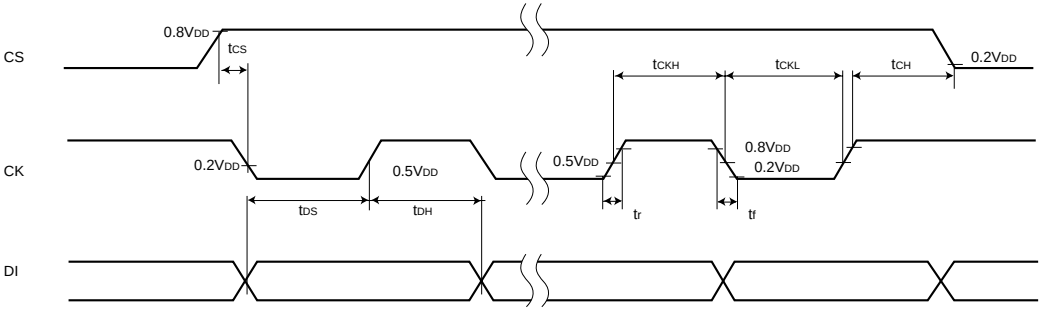
Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit
Recommended external resistance	R	OSC	—	47	—	kΩ
Recommended external capacitance	C	OSC	—	1000	—	pF
Guaranteed oscillation range	f_{OSC}	OSC	19	38	76	kHz
Data setup time	t_{DS}	CK, DI	100	—	—	ns
Data hold time	t_{DH}	CK, DI	100	—	—	ns
CS setup time	t_{CS}	CS, CK	100	—	—	ns
CS hold time	t_{CH}	CS, CK	100	—	—	ns
CK "H" pulse width	t_{CKH}	CK	100	—	—	ns
CK "L" pulse width	t_{CKL}	CK	100	—	—	ns
Rise time	t_r	CS, CK, DI	—	—	300	ns
Fall time	t_f	CS, CK, DI	—	—	300	ns

AC timing waveform

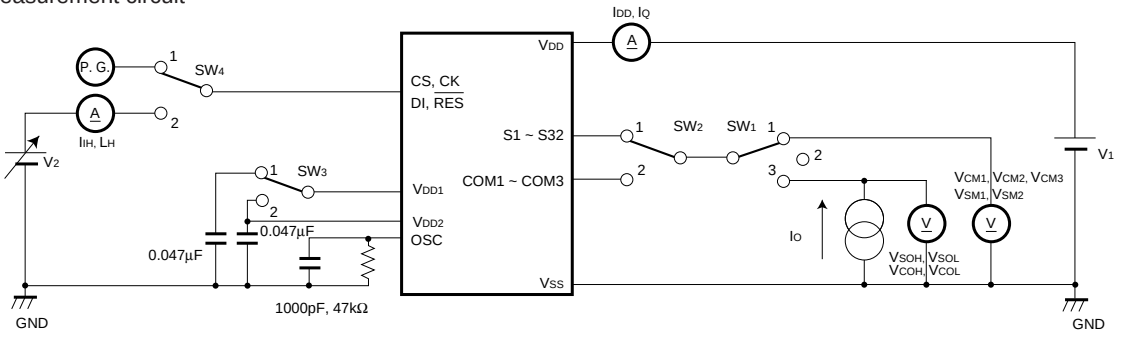
(1) When CK is stopped at “L”



(2) When CK is stopped at “H”



●Measurement circuit



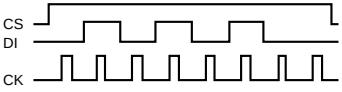
∗ P. G.: Control signal generator for programmable signal generator, etc.

Fig.1

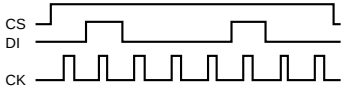
Measurement conditions

Parameter	Symbol	SW1	SW2	SW3	SW4	Conditions
Input high level voltage	V_{IH}	2	—	—	1	Set as P.G. input voltage; mode switching test
Input low level voltage	V_{IL}					
Input high level current	I_{IH}	2	—	—	2	$V_2 = V_{DD}$
Input low level current	I_{IL}					$V_2 = V_{SS}$
Output high level voltage	V_{SOH}	3	1	1	1	Pattern 1, I_O = – 20µA
	V_{COH}		2			Pattern 1, I_O = – 100µA
Output low level voltage	V_{SOL}	3	1	2	1	Pattern 2, I_O = 20µA
	V_{COL}		2			Pattern 2, I_O = 100µA
Intermediate output voltage	V_{CM1}	1	2	2	1	Pattern 3
	V_{SM1}		1	1		Pattern 4
	V_{CM2}		2			Pattern 4
	V_{SM2}		1			Pattern 5
	V_{CM3}		2			Pattern 5
Current dissipation	I_Q	2	—	—	1	Pattern 6
	I_{DD}					Test after power on
AC characteristics		2	—	—	1	Used as P.G. input condition

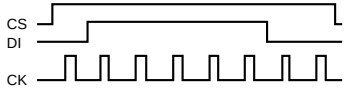
Measurement pattern



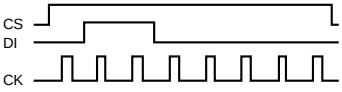
Pattern 1
Fig.2



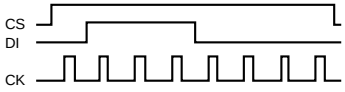
Pattern 2
Fig.3



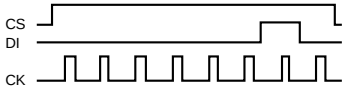
Pattern 3
Fig.4



Pattern 4
Fig.5



Pattern 5
Fig.6



Pattern 6
Fig.7

●Circuit operation

Timing charts

(1) When CK is stopped at “L”

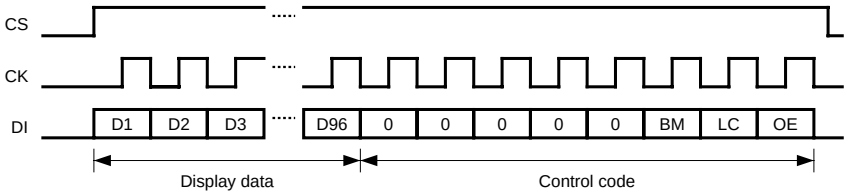


Fig.8

When CS is HIGH, data can be transferred. Data is sent to the shift register at the rising edge of CK. After all of the DI data has been transferred, CS should be set to LOW. The voltage corresponding to the display data transferred at the falling edge of CS is output.

(2) When CK is stopped at “H”

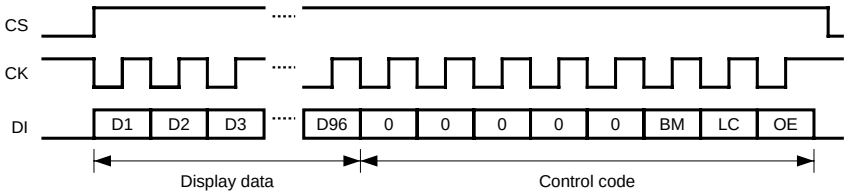


Fig.9

Control code table

OE	Output enable control
0	Normal operation
1	All display data is 0; no display (internal oscillation circuit is operating)

BM	Bias mode control
0	1 / 3 bias
1	1 / 2 bias

LC	Low power mode control
0	Normal operation
1	Low power mode = The internal oscillation circuit stops oscillating, and segment and common output = 0

Correspondence between display data input and segments

Segment	COM3	COM2	COM1
S1	D1	D2	D3
S2	D4	D5	D6
S3	D7	D8	D9
S4	D10	D11	D12
S5	D13	D14	D15
S6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48

Segment	COM3	COM2	COM1
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96

●Timing chart

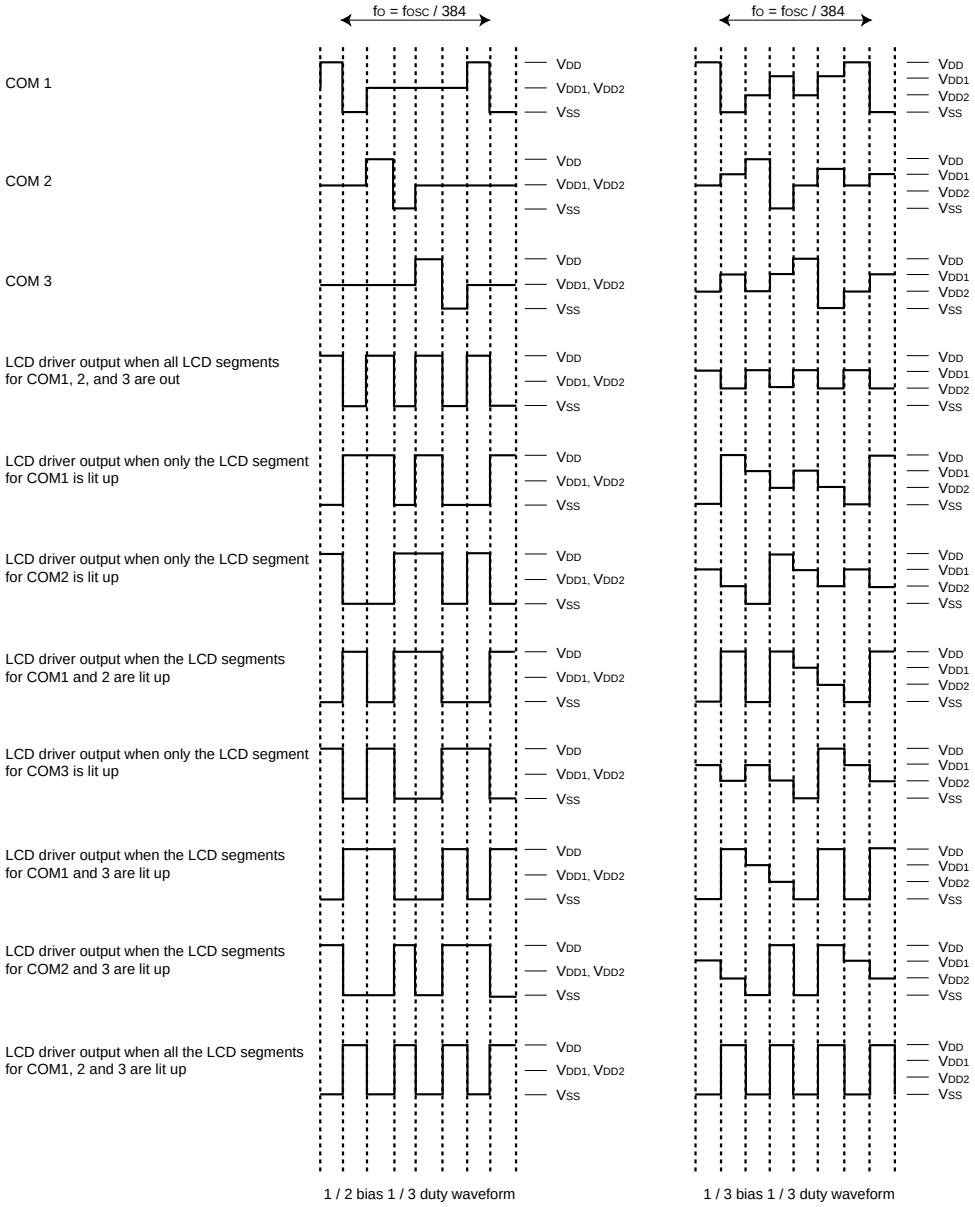
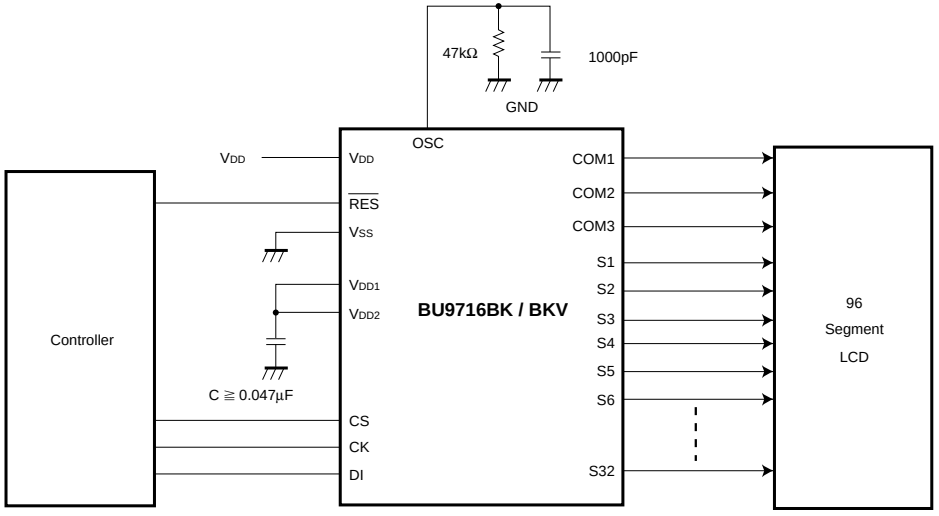


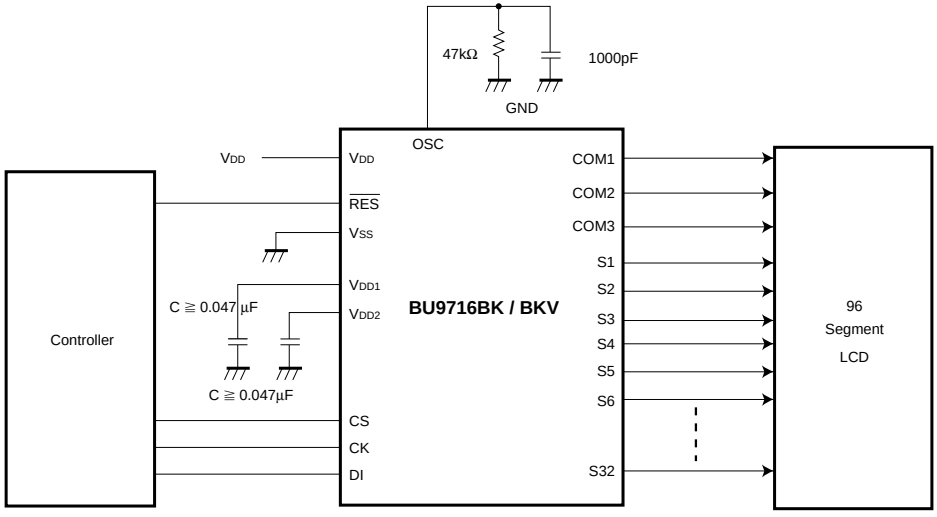
Fig.10

●Application example 1



1 / 2 bias mode

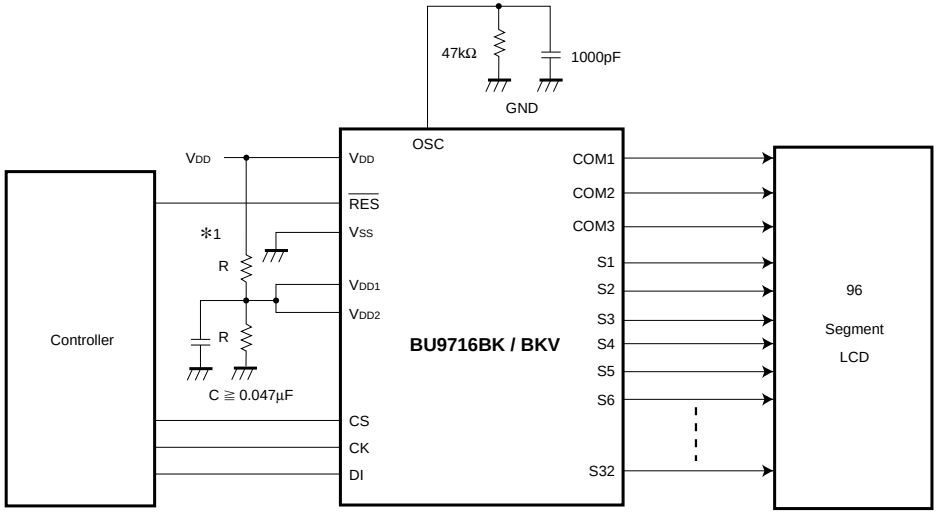
Fig.11



1 / 3 bias mode

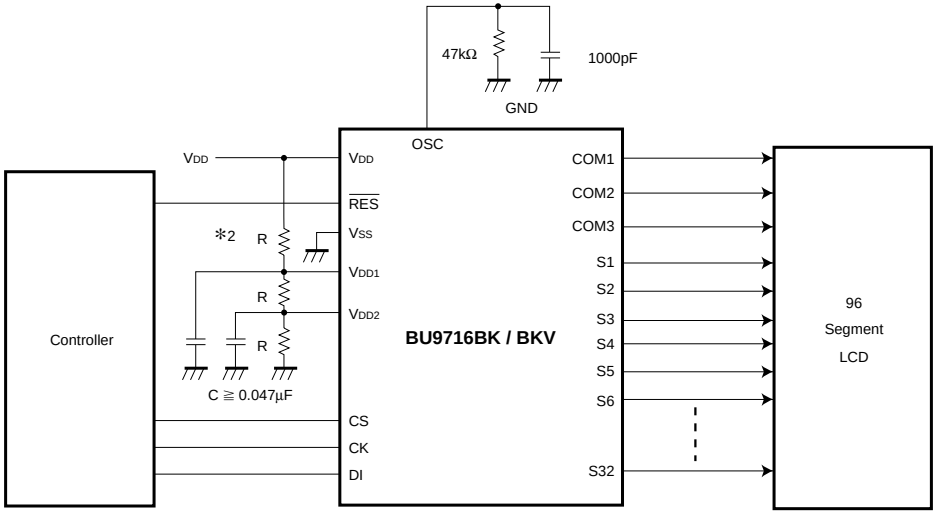
Fig.12

●Application example 2



1 / 2 bias mode

Fig.13



1 / 3 bias mode

Fig. 14

The resistance values and capacitance for*1 and *2 should be set to match the LCD panel, and should be checked using test operation.