Product data sheet

1. Product profile

1.1 General description

High-voltage, high-speed planar-passivated NPN power switching transistor in a SOT428 (D-PAK) surface mounted package.

1.2 Features and benefits

Low thermal resistance

Fast switching

1.3 Applications

- Electronic lighting ballast
- Inverters

- DC-to-DC converters
- Motor control systems

1.4 Quick reference data

- V_{CESM} ≤ 700 V
- Arr P_{tot} \leq 80 W

- $I_C \le 8 A$
- $\blacksquare h_{FEsat} = 11 (typ)$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	base	mb	
2	collector		2
3	emitter		
mb	mounting base; connected to collector	[]	1—
			3
		∐ 1 3	sym056
		DPAK (SOT428)	

^[1] It is not possible to make a connection to pin 2 of the SOT428 (D-PAK) package.

3. Ordering information

Table 2. Ordering information

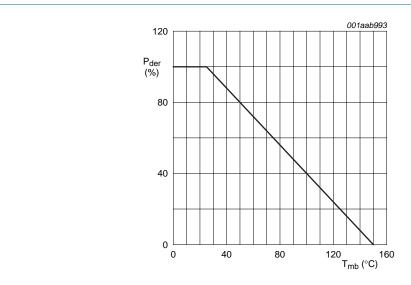
Type number	Package				
	Name	Description	Version		
BUJ105AD	D-PAK	plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT428		

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	peak collector-emitter voltage	$V_{BE} = 0 V$	-	700	V
V_{CEO}	collector-emitter voltage	open base	-	400	V
V_{CBO}	collector-base voltage	open emitter	-	700	V
I _C	collector current (DC)		-	8	Α
I _{CM}	peak collector current		-	16	Α
I _B	base current (DC)		-	4	Α
I_{BM}	peak base current		-	8	Α
P _{tot}	total power dissipation	$T_{mb} = \le 25 ^{\circ}C$; see Figure 1	-	80	W
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	150	°C



$$P_{der}(\%) = \frac{P_{tot}}{P_{tot(25 °C)}} \times 100\%$$

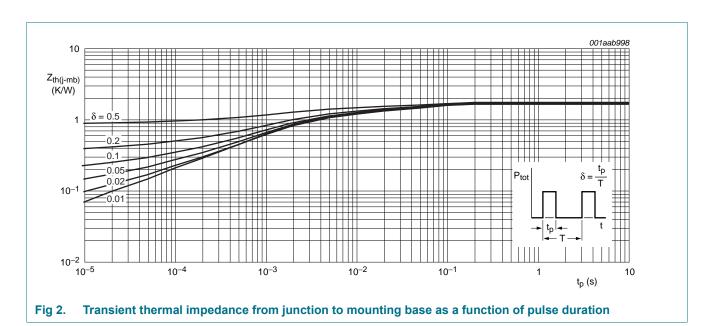
Fig 1. Normalized total power dissipation as a function of mounting base temperature

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 2	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		<u>[1]</u> -	75	-	K/W

[1] Device mounted on a printed-circuit board; minimum footprint



6. Characteristics

 Table 5.
 Characteristics

 T_{mb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
Static cha	Static characteristics						
I _{CES}	collector-emitter cut-off current	V _{BE} = 0 V; V _{CE} = V _{CESMmax}	<u>[1]</u> -	-	0.2	mΑ	
		$V_{BE} = 0 \text{ V}; V_{CE} = V_{CESMmax}; T_j = 125 ^{\circ}\text{C}$	<u>[1]</u> _	-	0.5	mA	
I _{CBO}	collector-base cut-off current	V _{BE} = 0 V; V _{CE} = V _{CESMmax}	<u>[1]</u> -	-	0.2	mA	
I _{CEO}	collector-emitter cut-off current	V _{CEO} = V _{CEOMmax} = 400 V	<u>[1]</u> -	-	0.1	mA	
I _{EBO}	emitter-base cut-off current	V _{EB} = 9 V; I _C = 0 A	-	-	1	mA	
V_{CEOsus}	collector-emitter sustaining voltage	$I_B = 0$ A; $I_C = 10$ mA; $L = 25$ mH; see Figure 3 and 4	400	-	-	V	
V _{CEsat}	collector-emitter saturation voltage	I _C = 4.0 A; I _B = 0.8 A; see <u>Figure 11</u>	-	0.3	1.0	V	
V _{BEsat}	base-emitter saturation voltage	$I_C = 4.0 \text{ A}$; $I_B = 0.8 \text{ A}$; see Figure 12	-	1.0	1.5	V	
h _{FE}	DC current gain	$I_C = 1 \text{ mA}; V_{CE} = 5 \text{ V}$	10	14	34		
		$I_C = 500 \text{ mA}$; $V_{CE} = 5 \text{ V}$; see Figure 10	13	23	36		
h _{FEsat}	DC saturation current gain	$I_C = 4.0 \text{ A}; V_{CE} = 5 \text{ V}$	8	11	15		

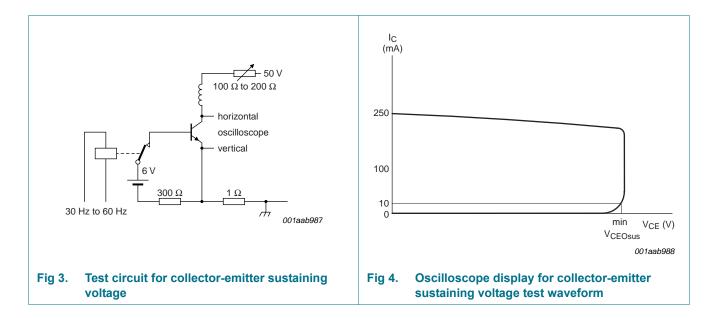


 Table 5.
 Characteristics ...continued

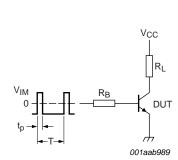
 T_{mb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic	characteristics					
Switching	times (resistive load); see Figure	<u>5</u> and <u>6</u>				
t _{on}	turn-on time	$I_{Con} = 5 \text{ A}; I_{Bon} = -I_{Boff} = 1 \text{ A}; R_{L} = 75 \Omega$	-	0.65	1	μS
t _{stg}	storage time		-	1.8	2.5	μS
t _f	fall time		-	0.3	0.5	μS
Switching	times (inductive load); see Figure	<u>7</u> and <u>8</u>				
t _{stg}	storage time	$I_{Con} = 5 \text{ A}; I_{Bon} = 1 \text{ A}; L_{B} = 1 \mu\text{H};$	-	1.2	1.7	μS
t _f	fall time	$V_{BB} = -5 \text{ V}$	-	20	50	ns
Switching times (inductive load); see Figure 7 and 8						
t _{stg}	storage time	$I_{Con} = 5 \text{ A}$; $I_{Bon} = 1 \text{ A}$; $L_{B} = 1 \mu \text{H}$;	-	1.4	1.9	μS
t _f	fall time	$V_{BB} = -5 \text{ V; } T_j = 100 ^{\circ}\text{C}$	-	25	100	ns

[1] Measured with half sine-wave voltage (curve tracer).



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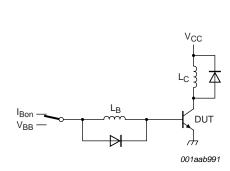


 V_{IM} = -6 V to +8 V; V_{CC} = 250 V; t_p = 20 $\mu s;$ δ = t_p/T = 0.01.

 R_{B} and R_{L} calculated from I_{Con} and I_{Bon} requirements.

Fig 6. Switching times waveforms for resistive load

Fig 5. Test circuit for resistive load switching



 V_{CC} = 300 V; V_{BB} = –5 V; L_{C} = 200 $\mu H; \ L_{B}$ = 1 $\mu H.$

Fig 7. Test circuit for inductive load switching

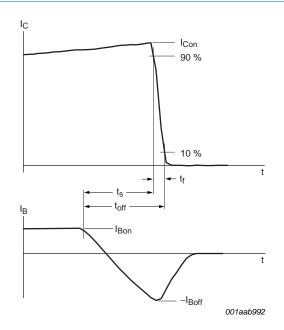


Fig 8. Switching times waveforms for inductive load



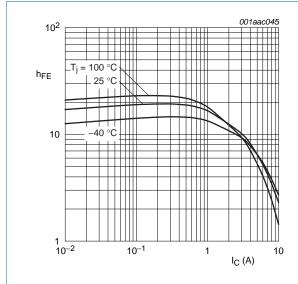


Fig 9. DC current gain as a function of collector current; typical values at $V_{CE} = 1 \text{ V}$

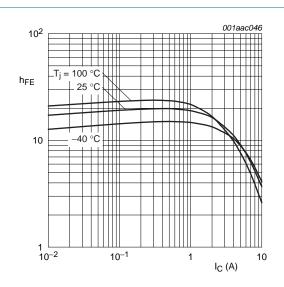


Fig 10. DC current gain as a function of collector current; typical values at V_{CE} = 5 V

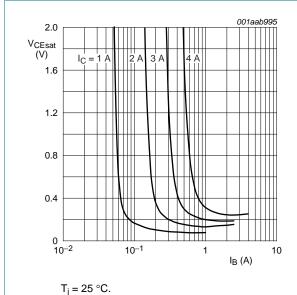


Fig 11. Collector-emitter saturation voltage as a function of base current; typical values

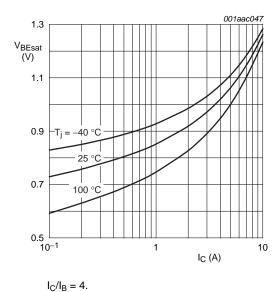


Fig 12. Base-emitter saturation voltage as a function of collector current; typical values

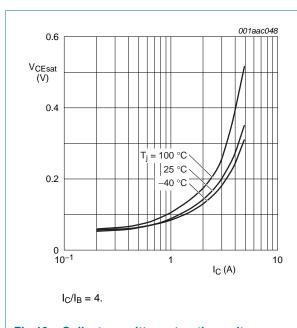
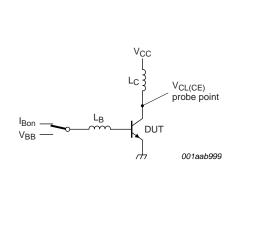
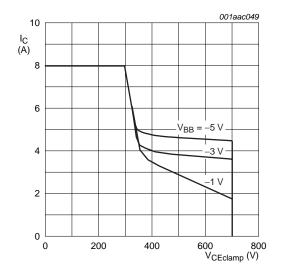


Fig 13. Collector-emitter saturation voltage as a function of collector current; typical values



 $V_{CEclamp}$ < 700 V; V_{CC} = 150 V; V_{BB} = -5 V, -3 V and -1 V; L_B = 1 $\mu H;$ L_C = 200 $\mu H.$

Fig 14. Test circuit for reverse bias safe operating area



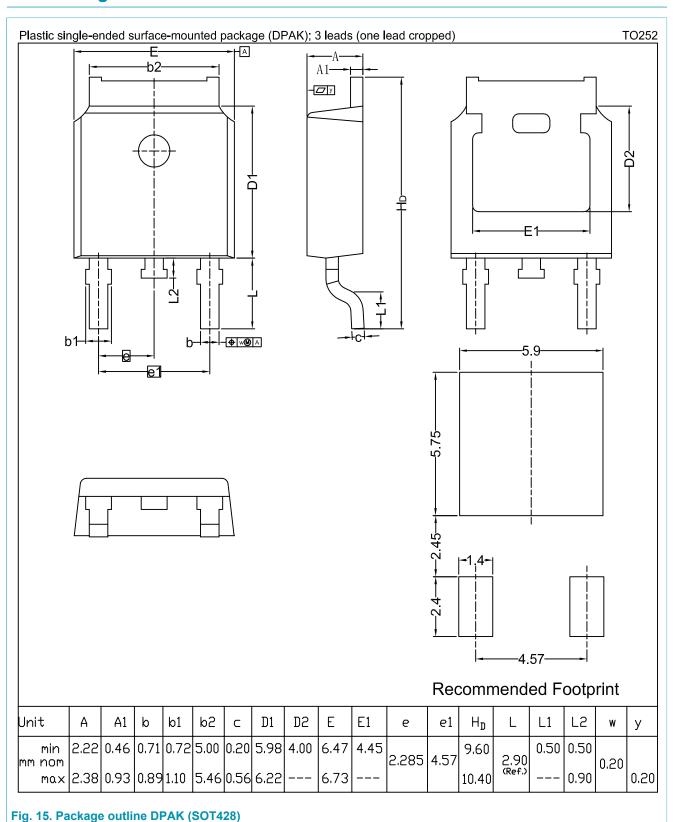
 $T_j < T_{j(max)}$.

Fig 15. Reverse bias safe operating area

7. Package information

Epoxy meets requirements of UL94 V-0 at ½ inch.

8. Package outline





9. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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