LUMISSIL MICROSYSTEMS

A Division of ISSI

C100 Subminiature Video Application Processor

DATA SHEET

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History

Version	Date	Author	Description
Rev 1.0			Initial

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Introduction

C100 is a subminiature video application processor targeting for video devices like medical equipment, mobile camera, webcam, domestic appliances and so on. This SoC introduces a kind of innovative architecture to fulfill both high performance computing and high quality image and video encoding requirements addressed by video devices. C100 provides high-speed CPU computing power, excellent image signal process, fluent 2k resolution video recording.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data L1 cache, and 128kB L2 cache, operating at 1.2GHz, and full feature MMU function performs OS related tasks At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is a video encoder engine designed to process video streams using the HEVC(ISO/IEC 23008-2 High Efficiency Video Coding) and AVC(ISO/IEC 14496-10 Advanced Video Coding) standards. It also supports still picture encoding using the JPEG standard(ITU T.81). Together with the on chip video accelerating engine and post image processing unit, C100 delivers high video performance. The maximum resolution of 2592x2048 in the format of AVC are supported in encoding. up to 40Mbit/s, 2592x1920@25fps.

The ISP (Image signal processor) core supports excellent image process with the image from raw sensors. It supports MIPI interface. With the functions, such as 3A, 2D and 3D denoise, WDR/HDR, lens shading, it can supply maximum resolution 2592x2048 resolution image for view or encoding to store or transfer.

For more quickly and easily to use C100, 1G bit DDR3L is integrated on chip.

On-chip modules such as audio CODEC, multi-channel SAR-ADC controller and camera interface offer designers a economical suite of peripherals for video application. WLAN, Bluetooth and expansion options are supported through MMC/SD/SDIO host controllers. Other peripherals such as USB, UART as well as general system resources provide enough computing and connectivity capability for many applications.

1 Overview

1.1 Block Diagram

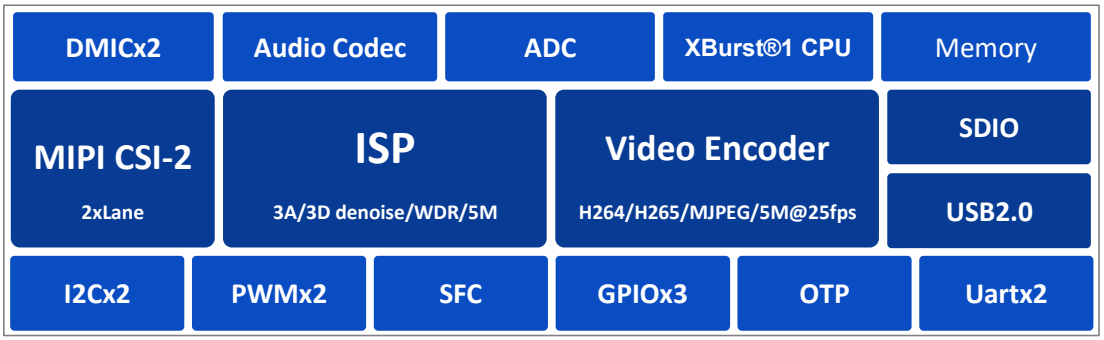


Figure1- 1 C100 Diagram

1.2 Features

1.2.1 CPU

- XBurst®-1 core 9-stage pipeline micro-architecture, the operating frequency is 1.2GHz

1.2.2 Video Processor Unit

- Support DVT HEVC/AVC/JPEG Encoder
- Support HEVC up to 20Mbit/s and AVC up to 40Mbit/s, maximum frame rate is 1920x1080@60fps or 2560x1920@25fps

1.2.3 Image Signal Processor

- Dynamic/Static Defect Pixel Correction
- Green Equalization
- Black Level Correction
- Lens Shading Correction
- 3A(Auto Exposure/Auto White Balance/Auto Focus)
- Support Statistical Information Output(3A)
- Adaptive Dynamic Range Compression
- Demosaic
- Sharpen
- Bayer Denoise
- 2D/3D Denoise
- Color Noise Suppression
- Lens Distortion Correction
- 2D Color Correction

- 3D Color Correction
- Gamma Correction
- Defog, WDR
- 3 Independent Image Scaler and Output
- Crop, Mirror and Flip
- Support Maximum Resolution:2592x2048

1.2.4 Audio System

- Integrated Audio codec
  - 24 bits DAC with 93dB SNR
  - 24 bits ADC with 92dB SNR
  - Support signal-ended and differential microphone input and line input
  - Automatic Level Control (ALC) for smooth audio recording
  - Pure logic process: no need for mixed signal layers and less mask cost
  - Programmable input and output analog gains
  - Digital interpolation and decimation filter integrated
  - Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K
- Low power DMIC Controller
  - 16bit data interface and 20bit precision internal controller
  - SNR:90dB,THD:-90dB@FS -20dB
  - Linear high pass filter include. Attenuation:-2.9dB@100Hz,22dB@27Hz,-36dB@10Hz
  - Low power voice trigger when waiting to start talking
  - 1/2 channel digital MIC support
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation
  - Sample frequency supported:8k,16k

1.2.5 System Functions

- Clock generation and power management
  - On-chip 12/24/27/50MHZ oscillator circuit
  - One three-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - MSC clock supports 100M clock
  - Functional-unit clock gating
  - Shut down power supply for P0, ISP, VPU, IPU
- Timer and counter unit with PWM output and/or input edge counter
  - Provide four separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflow
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB

Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer controller
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- PCLK, EXTAL and RTCCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SoC
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - one Channels
  - Resolution: 10-bit
  - Integral nonlinearity: ±1 LSB
  - Differential nonlinearity: ±0.5 LSB
  - Resolution/speed: up to 2MSPS
  - Max Frequency: 24MHz
  - Low power dissipation: 1.5mW(worst)
  - Support multi-touch detect
  - Support write control command by software
  - Single-end and Differential Conversion Mode
  - Support external touch screen controller
  - Pin Description
- OTP Slave Interface
  - Total 1024 bits. Lower 192bits are read only, other higher bits are read-able and write-able

1.2.6 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 3 interrupts, each interrupt corresponds to the group, to INTC

- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - 16-level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 2 independent SMB channels (SMB0, SMB1)

- One High Speed Synchronous serial interfaces (SFC)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - transmit-only or receive-only operation
  - MSB first for command and data transfer, and LSB first for address transfer
  - 64 entries x 32 bits wide data FIFO
  - one device select
  - Configurable sampling point for reception
  - Configurable timing parameters: t_{SLCH}, t_{CHSH} and t_{SHSL}
  - Configurable flash address wide are supported
  - 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
  - two data transfer mode: slave mode and DMA mode
  - Configurable 6 phases for software flow

- Two UARTs (UART0, UART1)
  - Full-duplex operation

- 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
- 64x8 bit transmit FIFO and 64x11bit receive FIFO
- Independently controlled transmit, receive (data ready or timeout), line status interrupts
- Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification

- One MMC/SD/SDIO controllers (MSC0)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit and 4bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes

- USB 2.0 interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer

1.2.7 Bootrom

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	22nm CMOS low power
Power supply voltage	General purpose I/O: 1.5~3.6V DDR I/O: 1.35V(DDR3) ± 0.1V EFUSE programming: 1.8V ± 10% Analog power supply 1: 1.8V ± 10% Analog power supply 2: 3.3V ± 10% Core: 0.8V ± 0.1V
Package	BGA85
Operating frequency	1.2GHz

2 Packaging and Pinout Information

2.1 Overview

C100 processor is offered in BGA85, show in Figure 2-2. The C100 pin to ball assignment is show in Figure 2-1.. The detailed pin description is listed in Table 2-1 ~ Table 2-14.

2.2 Solder Process

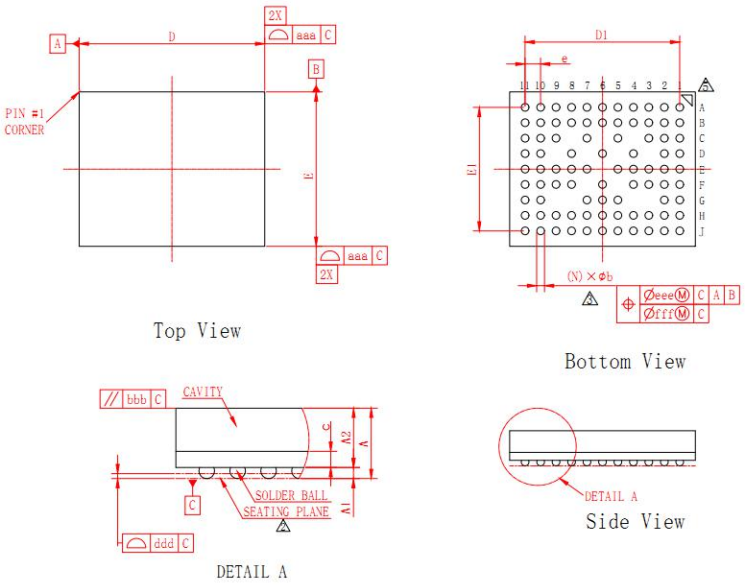
C100 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

C100 package moisture sensitivity is level 3.

2.4 C100 Package

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.240	---	---	0.0488
A1	0.130	0.180	0.230	0.005	0.0071	0.0091
A2	0.910	0.960	1.010	0.036	0.0378	0.0398
c	0.220	0.260	0.300	0.009	0.0102	0.0118
D	5.900	6.000	6.100	0.232	0.2362	0.2402
E	4.900	5.000	5.100	0.193	0.1969	0.2008
D1	---	5.000	---	---	0.1969	---
E1	---	4.000	---	---	0.1575	---
e	---	0.500	---	---	0.0197	---
b	0.200	0.250	0.300	0.008	0.0098	0.0118
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.250			0.010		
N	85			85		
MD/ME	11/9			11/9		



TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.230mm; [球形防焊开口: 0.230mm;]

⚠PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
[主要基准C和底面是锡球;]

⚠DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]

4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]

⚠THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
[PIN 1 标识仅供参考;]

6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
[禁止使用一级环境管理物质;]

Figure2- 1 C100 package outline drawing

Figure2- 2 C100 pin to ball assignment

2.5 Pin Description

2.5.1 I2Cx/MIPI

Table2- 1 I2Cx/MIPI Pins(3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB0_SDA PA12	IO IO	D2	2mA PU-rst	SMB0_SDA: I2C 0 serial data PA12: GPIO group A bit 12	VDDIO0
SMB0_SCK PA13	O IO	D1	2mA PU-rst	SMB0_SCK: I2C 0 serial clock PA13: GPIO group A bit 13	VDDIO0
MIPI_MCLK PA15	O IO	E1	2mA SR-rst*	MIPI_MCLK: MIPI main clock output PA15: GPIO group A bit 15	VDDIO0

2.5.2 SFC

Table2- 2 SFC Pins(6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SFC_DT PA23	IO IO	H9	8mA PU-rst SMT-rst	SFC_DT: high speed ssi transmit data PA23: GPIO group A bit 23	VDDIO1
SFC_DR PA24	IO IO	H11	8mA PU-rst	SFC_DR: high speed ssi receive data PA24: GPIO group A bit 24	VDDIO1
SFC_GPC PA25	IO IO	J11	8mA PU-rst	SFC_GPC: high speed ssi general-purpose control PA25: GPIO group A bit 25	VDDIO1
SFC_CE1 PA26	IO IO	G10	8mA PU-rst	SFC_CE1: high speed ssi chip 1 select PA26: GPIO group A bit 26	VDDIO1
SFC_CLK PA27	O IO	J10	8mA PU-rst	SFC_CLK: high speed ssi clock PA27: GPIO group A bit 27	VDDIO1
SFC_CE0 PA28	O IO	H10	8mA PU-rst	SFC_CE0: high speed ssi chip 0 select PA28: GPIO group A bit 28	VDDIO1

2.5.3 MSC0/PWMx/UARTx/I2C1/DMIC

Table2- 3 MSC0/GMAC/PWMx/UARTx/I2C1/DMIC Pins (18)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_D0 PB00	IO IO	F10	2mA	MSC0_D0: MSC (MMC/SD) 0 data bit 0 PB00: GPIO group B bit 00	VDDIO1
MSC0_D1 PB01	IO IO	G11	2mA	MSC0_D1: MSC (MMC/SD) 0 data bit 1 PB01: GPIO group B bit 01	VDDIO1
MSC0_D2 PB02	IO IO	D10	2mA	MSC0_D2: MSC (MMC/SD) 0 data bit 2 PB02: GPIO group B bit 02	VDDIO1
MSC0_D3 PB03	IO IO	E11	2mA	MSC0_D3: MSC (MMC/SD) 0 data bit 3 PB03: GPIO group B bit 03	VDDIO1
MSC0_CLK PB04	O IO	F11	2mA	MSC0_CLK: MSC (MMC/SD) 0 clock output PB04: GPIO group B bit 04	VDDIO1
MSC0_CMD PB05	IO IO	E10	2mA PU-rst	MSC0_CMD: MSC (MMC/SD) 0 command PB05: GPIO group B bit 05	VDDIO1
PWM0 PB17	O IO	A3	2mA PD-rst	PWM0: PWM channel 0 output PB17: GPIO group B bit 17.	VDDIO1
PWM1 PB18	O IO	B4	mA PD-rst	PWM1: PWM channel 1 output PB18: GPIO group B bit 18.	VDDIO1
UART0_RXD PB19	I IO	B10	2mA PU-rst	UART0_RXD: UART 0 data receive PB19: GPIO group B bit 19	VDDIO1
UART0_CTS PB20	I IO	A11	2mA	UART0_CTS: UART 0 clear-to-send handshaking PB20: GPIO group B bit 20	VDDIO1
UART0_RTS PB21	O IO	B11	2mA	UART0_RTS: UART 0 request-to-send handshaking PB21: GPIO group B bit 21	VDDIO1

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_TXD PB22	O IO	A10	2mA	UART0_TXD: UART 0 data transmit PB22: GPIO group B bit 22	VDDIO1
UART1_TXD PB23	O IO	A9	2mA	UART1_TXD: UART 1 transmit data PB23: GPIO group B bit 23	VDDIO1
UART1_RXD PB24	I IO	B9	2mA PU-rst	UART1_RXD: UART 1 receive data PB24: GPIO group B bit 24	VDDIO1
SMB1_SDA PB25	IO IO	B5	2mA PU-rst	SMB1_SDA: I2C 1 serial data PB25: GPIO group B bit 25	VDDIO1
SMB1_SCK PB26	O IO	A4	2mA PU-rst	SMB1_SCK: I2C 1 serial clock PB26: GPIO group B bit 26	VDDIO1
DMIC_CLK PB28	O IO	A5	2mA PD-rst	DMIC_CLK: digital microphone clock output PB28: GPIO group B bit 28	VDDIO1
DMIC_DAT0 PB29	I IO	A6	2mA PU-rst	DMIC_DAT0: digital microphone data bit 0 PB29: GPIO group B bit 29	VDDIO1

2.5.4 GPIO

Table2- 4 GPIO Pins (2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PB31	IO	B6	2mA PD-rst	PB31: GPIO group B bit 31	VDDIO1
PA18	IO	E2	2mA PD-rst	PA18: GPIO group A bit 18	VDDIO0

2.5.5 System Control

Table2- 5 Boot Select Pins(2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
(BOOT_SEL0) PC00	I IO	C10	2mA PU-rst	It is taken as BOOT select bit 0 by Boot ROM code PC00: GPIO group C bit 00	VDDIO1
(BOOT_SEL1) PC01	I IO	C11	2mA PD-rst	It is taken as BOOT select bit 1 by Boot ROM code PC01: GPIO group C bit 01	VDDIO1

2.5.6 Digital IO/core power/ground

Table2- 6 IO/Core power supplies Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDIO0	P	B2	-	VDDIO0: IO digital power for DVP power domain, 1.8V	-
VDDIO1	P	D11	-	VDDIO1: IO digital power for normal function Pad power domain, 1.8V/3.3V	-
VDDIO2	P	J6	-	VDDIO2: IO digital power for normal function Pad power domain, 1.8V/3.3V	-

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDD	P	C3,C9,E3,D9,F3 ,F9,G5,G6,G7	-	VDD: CORE digital power, 0.8V	-
VSS	P	D4,D6,D8,E4,E5 ,E7,E8,F4,F6,F8	-	VSS: IO digital ground for none DRAM and CORE digital ground, 0V	-

2.5.7 DDR power/ground

Table2- 7 DDR power/ground supplies Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DDR_VREF	P	B3	-	DDR_VREF: DDR reference voltage, (VREF = VDDMEM/2)	-
DDR_ZQ	AIO	B9	-	DDR_ZQ: DDR3 External reference which is connected to a 240Ω resister to VSS.	-
VDDMEM	P	C5,C7	-	VDDMEM: DDR supply(1.35V for DDR3)	-
DDRPLL_VCCD	P	A8	-	DDRPLL_VCCD: DDR PLL power supply for digital	-
DDRPLL_VCCA	P	A7	-	DDRPLL_VCCA: DDR PLL power supply for analog	-
DDRPLL_VSSA	P	B7	-	DDRPLL_VSSA: DDR PLL analog ground	-

2.5.8 Analog - USB 2.0

Table2- 8 USB 2.0 (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
USB0PP	AIO	H5	-	USB0PP: USB2.0 positive data line	USB_AVD33
USB0PN	AIO	J4	-	USB0PN: USB2.0 negative data line	USB_AVD33
USB_AVD33	P	J5	-	USB_VCC33: This is the analog supply that is used to support 3.3V signaling. This supply has both integrated IO pads and associated ESD. The expectation is that this supply is unique to the USB PHY. The PHY provides two pins for this power supply, but they can often be bonded out to a single package pin if the parasitic are low enough to support the current draw.	-
USB_AVD18	P	H4	-	USB_VCC18: This is the analog supply that is used to support 1.8V signaling. This supply has both integrated IO pads.	-

2.5.9 Analog - MIPI

Table2- 9 MIPI CSI Pins (7)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MIPI_DATAN0	AIO	F1	-	MIPI_DATAN0: In MIPI model is data lane 0 serial signal	MIPI_AV D_18

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MIPI_DATAP0	AIO	F2	-	MIPI_DATAP0: In MIPI model is data lane 0 serial signal	MIPI_AVD18
MIPI_CLKN	AIO	G1	-	MIPI_CLKN: In MIPI model is clock lane serial signal	MIPI_AVD18
MIPI_CLKP	AIO	G2	-	MIPI_CLKP: In MIPI model is clock lane serial signal	MIPI_AVD18
MIPI_DATAN1	AIO	H1	-	MIPI_DATAN1: In MIPI model is data lane 1 serial signal	MIPI_AVD18
MIPI_DATAP1	AIO	H2	-	MIPI_DATAP1: In MIPI model is data lane 1 serial signal	MIPI_AVD18
MIPI_AVD18	P	J1	-	MIPI_AVD18: PHY analog power, 1.8V	-

2.5.10 Analog – SARADC

Table2- 10 SARADC Pins (3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_AUX0	AI	J2	-	AUX0: SARADC channel 0 input	ADC_AVDD
ADC_AVDD	P	J3	-	ADC_AVDD: SARADC analog power, 1.8 V	-
ADC_AVSS	P	H3	-	ADC_AVSS: analog ground	-

2.5.11 Analog – SARADC

Table2- 11 SARADC Pins (3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_AUX0	AI	J2	-	AUX0: SARADC channel 0 input	ADC_AVDD
ADC_AVDD	P	J3	-	ADC_AVDD: SARADC analog power, 1.8 V	-
ADC_AVSS	P	H3	-	ADC_AVSS: analog ground	-

2.5.12 Analog - EFUSE

Table2- 12 EFUSE Pins (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EFUSE_AVD	P	B1	-	EFUSE: EFUSE programming power, 0V/1.8V	-

2.5.13 Analog - CLOCK/PLL

Table2- 13 CLOCK/PLL Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_XI	AI	A2	2~30 MHz Oscillator, OSC on/off	EXCLK_XI: external oscillator clock input or external 24MHz clock input	VDDIO0
EXCLK_XO	AO	A1		EXCLK_XO: external oscillator clock output	VDDIO0
VDDIO0	P	B2	-	VDDIO0: Oscillator power supply, 1.8V	-
PLL_VDDHV	P	C2	-	PLL_VDDHV:PLL analog supply power 1.8V	-
PLL_VDD	P	C1	-	PLL_VDD: PLL digital supply power 0.8V	-

NOTES:

1 All GPIO are programmable with multi-voltage (1.8V, 3.3V) general purpose, bi-directional I/O buffer with a selectable LVCMOS input or LVCMOS Schmitt trigger input and programmable pull-up / pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

2 The meaning of phases in IO cell characteristics are:

- 2/8mA out: The IO cell's output driving strength is about 2/8mA.
- PU: The IO cell contains a pull-up resistor and fixed pull up.
- PD: The IO cell contains a pull-down resistor and fixed pull down.
- PU-rst: The IO cell during reset and after the pull up function is enabled.
- PD-rst: The IO cell during reset and after the pull down function is enabled.
- SMT: The IO cell is Schmitt trigger input and fixed.
- SMT-rst: The IO cell during reset and after the Schmitt trigger input function is enabled.

SR-rst: The IO cell during reset and after the slew-rate function select fast mode

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table3- 1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDMEM power supplies voltage	-0.1	1.98	V
DDR_PLLVCCA power supplies voltage	-0.1	1.98	V
DDR_PLLVCCD power supplies voltage	-0.1	0.88	V
VDDIO0 power supplies voltage	-0.5	1.98	V
VDDIO1 power supplies voltage	-0.5	3.63	V
VDDIO2 power supplies voltage	-0.5	3.63	V
VDD power supplies voltage	-0.2	0.96	V
PLL_VDDHV power supplies voltage	-0.1	1.98	V
EFUSE_AVD power supplies voltage	-0.1	1.98	V
USB_AVD33 power supplies voltage	-0.1	3.63	V
USB_AVD18 power supplies voltage	-0.1	1.98	V
ADC_AVDD power supplies voltage	-0.1	1.98	V
CODEC_AVDD power supplies voltage	-0.1	1.98	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.	-	2000	V

3.2 Recommended operating conditions

Table3- 2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VDDMEM	VDD voltage for KGD	1.35	1.35	1.98	V
DDRPLL_VCCA	DDR PLL analog supplies voltage	1.62	1.8	1.98	V
DDRPLL_VCCD	DDR PLL digital supplies voltage	0.72	0.8	0.88	V
VDDIO0	GPIO power domain 0 supplies voltage	1.62	1.8	1.98	V
VDDIO1	GPIO power domain 1 supplies voltage	1.5	3.3	3.63	V
VDDIO2	GPIO power domain 2 supplies voltage	1.5	3.3	3.63	V
VDD	VDD core supplies voltage	0.72	0.8	0.88	V
PLL_VDDHV	APLL, MPLL and VPLL analog voltage	1.62	1.8	1.98	V
PLL_VDD	APLL, MPLL and VPLL digital voltage	0.72	0.8	0.88	V

Symbol	Description	Min	Typical	Max	Unit
EFUSE_AVD	EFUSE program supplies voltage	1.62	1.8	1.98	V
USB_AVD33	USB PHY VCCA3P3 analog voltage	3.0	3.3	3.6	V
USB_AVD18	USB PHY VCC18 analog voltage	1.62	1.8	1.98	V
ADC_AVDD	SARADC analog voltage	1.62	1.8	1.98	V
CODEC_AVDD	CODEC analog voltage	1.62	1.8	1.98	V
MIPI_AVD18	MIPI analog voltage	1.62	1.8	1.98	V

Table3- 3 Recommended operating conditions for VDDIO0/VDDIO1/VDDIO2 supplied pins

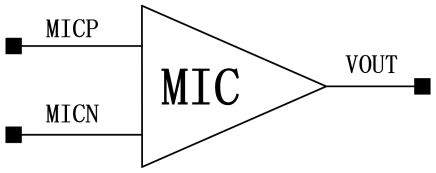
Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	*0.65	-	+0.3	V
V_{IL18}	Input low voltage for 1.8V I/O application	-0.3	-	*0.35	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7	-	+0.3	V
V_{IL25}	Input low voltage for 2.5V I/O application	-0.3	-	0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2	-	+0.3	V
V_{IL33}	Input low voltage for 3.3V I/O application	-0.3	-	0.8	V

Table3- 4 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	-20	25	+85	°C
T_J	Junction temperature	-40	25	+125	°C

3.3 Audio codec

3.3.1 Microphone input

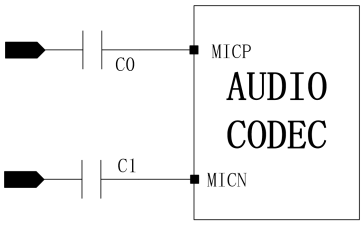


There are two inputs channels named left ADC channel and right ADC channel. In the each channel, there are one inputs which are configured as differential input by the microphone PGA(MICL).

The signal of microphone output should be input to AUDIO CODEC through DC-blocking capacitor, as shown in following figure. The capacitance and input resistance form a high pass filter. For example, when the gain of the MIC module is 20dB, the input resistance is 45KΩ and 0.1uF DC-blocking capacitor is used, the lower cut-off frequency is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 45 \times 10^{3} \times 0.1 \times 10^{-6}} = 35.4Hz$$

The capacitance of the DC-blocking capacitor should be determined by the minimum input impedance and application requirements.



If the output of microphone is single-ended, the AUDIO ADC input should be connected as following figure.

Microphone PGA has four gains to amplify the input signal, that is, 0dB, 20dB, 30dB and 40dB.

3.3.2 ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC_L and ALC_R) gain according to the comparison result.

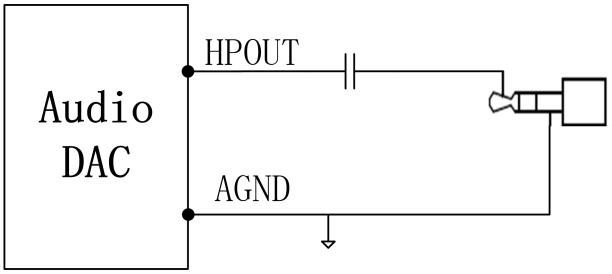
The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

3.3.3 Headphone output

Audio codec DAC output can drive 16 Ω or 32 Ω headphone load through DC-blocking capacitor.
In the configuration using DC-blocking capacitor, shown in following figure, the headphone ground is connected to the real ground. The capacitance and the load resistance determine the lower cut-off frequency. For instance, if 16 Ω headphone and 100uF DC-blocking capacitor are used, the lower cut-off frequency is

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 16 \times 100 \times 10^{-6}} = 99.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.



The headphone driver chooses DAC output as input. It has a gain rang from -39dB to +6dB with a tuning step of 1.5dB.

3.3.4 Microphone bias

Microphone bias output is used to bias external microphones. The bias voltage can varies from 0.8*CODEC_AVDD to 0.975* CODEC_AVDD with a step of 0.025* CODEC_AVDD.

3.4 Power On, Reset and BOOT

3.4.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the C100 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-5 gives the timing parameters. Following are the name of the power.

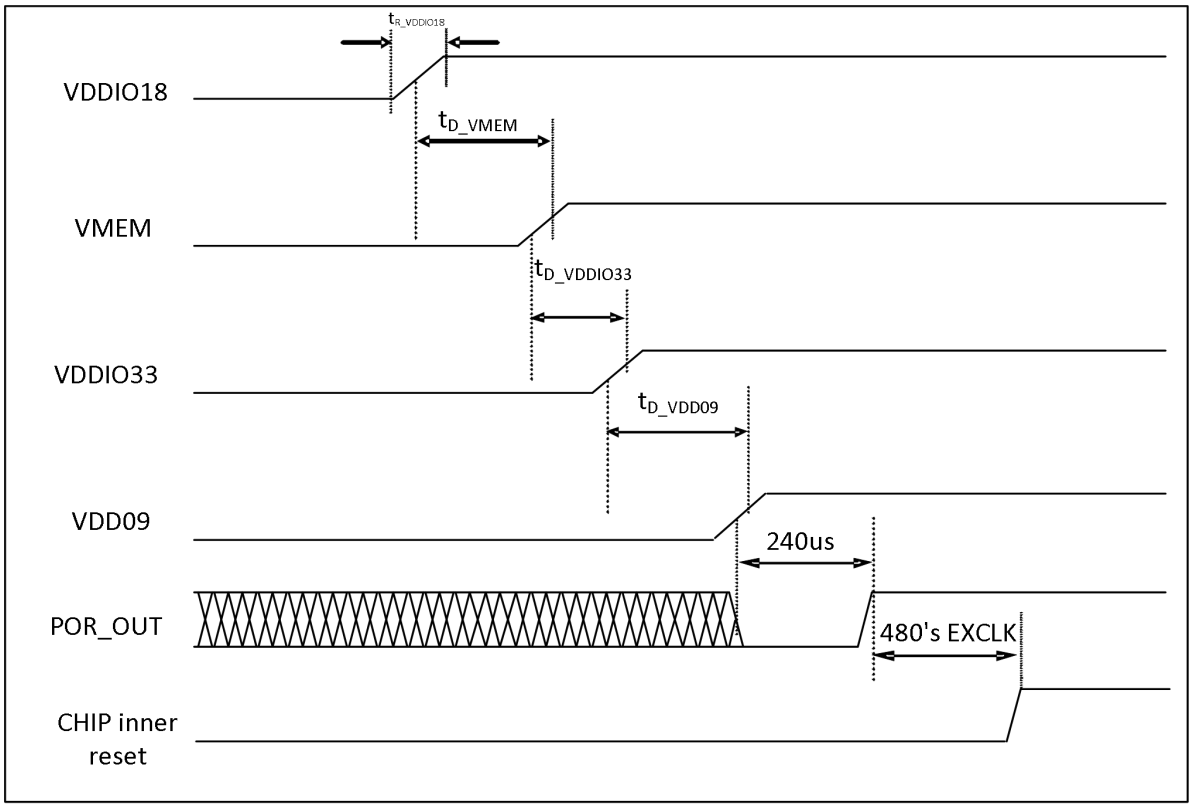
- VDD08: all 0.8V power supplies, VDD, DDR_PLLVCCD, PLL_VDD
- VMEM: VDDMEM
- VDD18: VDDIO0,DDR_PLLVCCA,PLL_VDDHV,VDDIO_OSC, USB_AVD18, MIPI_AVD18, ADC_AVDD, CODEC_AVDD
- VDD33: VDDIO1,VDDIO2,USB_AVD33

Table3- 5 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDD18}	VDD18 rise time[1]	0	-	ms
t_{D_VMEM}	Delay between VDD18 arriving 50% to VMEM arriving 50%	0	-	ms
t_{D_VDD33}	Delay between VMEM arriving 50% to VDD33 arriving 50%	0	-	ms
t_{D_VDD08}	Delay between VDD33 arriving 50% to VDD08 arriving 50%	0	-	ms

NOTES:

- The power rise time is defined as 10% to 90%.



POR reset mode

Figure3- 1 Power-On Timing Diagram

3.4.2 Reset procedure

There are 3 reset sources: 1. POR hardware reset;2. WDT timeout reset; and 3. hibernating reset when exiting hibernating mode. After reset, program start from boot.

- POR(Power-On-Reset) hardware reset.
  The chip POR circuit provides reliable reset function for general applications. Powered by 1.8V analog supply and monitors 0.8V digital and 1.8V analog supply. It generates reset signal to digital logic. Set low if analog supply or digital supply is below the threshold voltage(typical 1.35V threshold for 1.8V supply and 0.6V threshold for 0.8V supply), and will be set high if both of analog supply and digital supply exceed the threshold voltage.
- WDT reset.
  This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.
- Hibernating reset.
  This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description” for details. The oscillators are on. The USB 2.0 PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.4.3 BOOT

The boot sequence of the C100 is controlled by boot_sel[1:0]. The configuration is shown as follow:

Table3- 6 Boot Configuration of C100

boot_sel[1:0]	Boot method
00	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B)
01	SFC boot @ CS4 (SPI boot)
10	NOR boot @ CS2 (just for FPGA testing)
11	USB boot @ USB 2.0 device, EXTCLK=24MHz

Note:

1. When SFC boot start failure, the program in bootrom will go into MSC0 boot, if it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it.

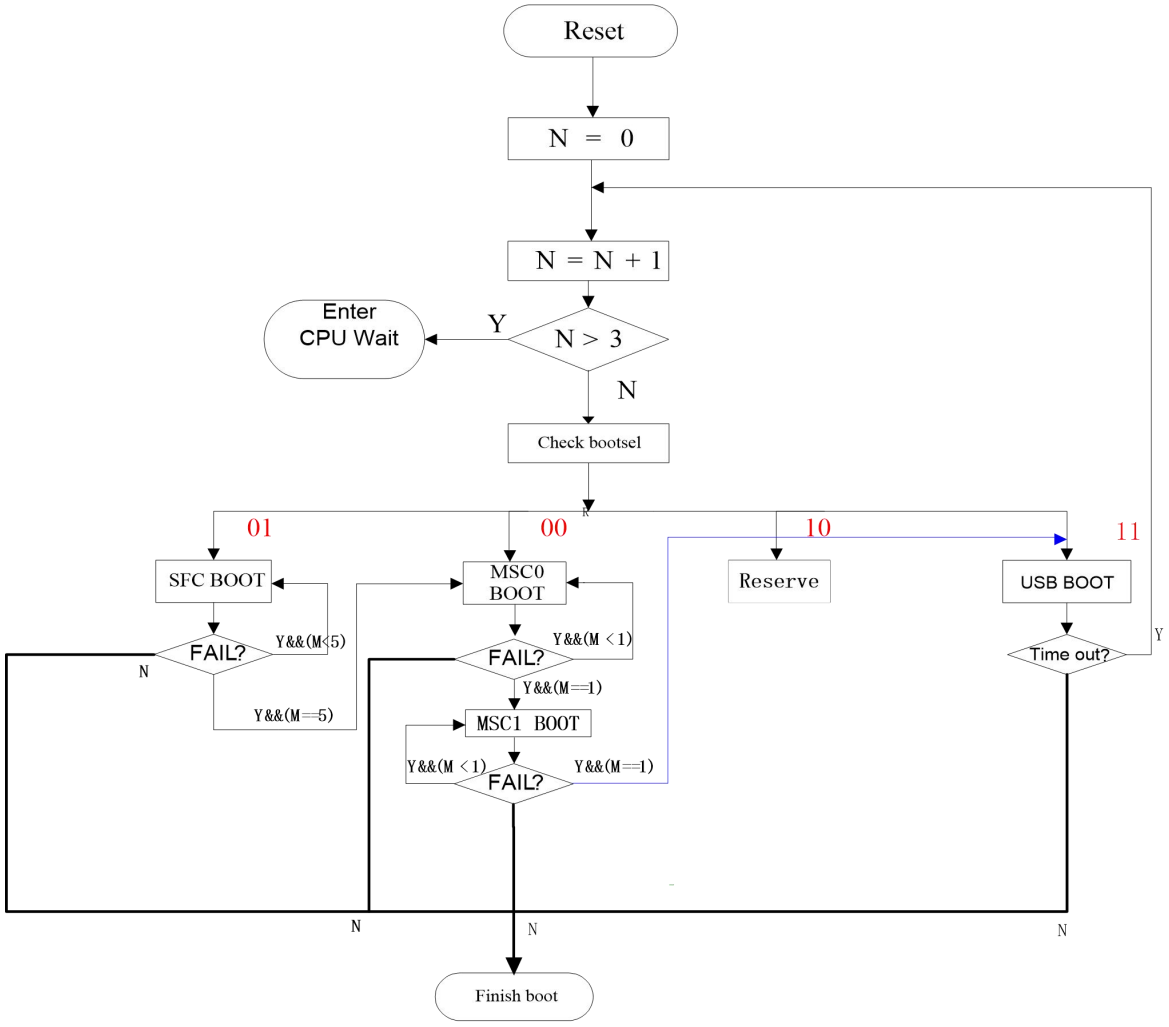


Figure3- 2 Boot sequence diagram of C100