

C3M0045065J1

Silicon Carbide Power MOSFET

C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

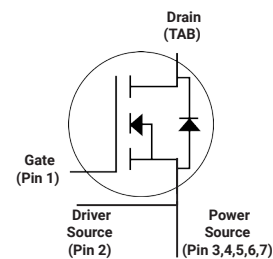
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Datacenter and Telecom Power Supplies
- EV Battery Chargers
- High voltage DC/DC converters
- Energy Storage Systems
- Solar Inverters

Package



Part Number	Package	Marking
C3M0045065J1	TO-263-7L XL	C3M0045065J1

Maximum Ratings ($T_c=25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Value	Unit	Note
V_{DSmax}	Drain - Source Voltage	650	V	
V_{GSmax}	Gate - Source voltage	-8/+19	V	Note 1
I_D	Continuous Drain Current, $V_{GS} = 15\text{ V}$, $T_c = 25^\circ\text{C}$	47	A	Fig. 19
	Continuous Drain Current, $V_{GS} = 15\text{ V}$, $T_c = 100^\circ\text{C}$	31		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_p limited by T_{jmax}	132	A	
P_D	Power Dissipation, $T_c=25^\circ\text{C}$, $T_j = 150^\circ\text{C}$	147	W	Fig. 20
T_j, T_{stg}	Operating Junction and Storage Temperature	-40 to +150	$^\circ\text{C}$	
T_L	Solder Temperature, 1.6mm (0.063") from case for 10s	260	$^\circ\text{C}$	

Note (1): Recommended turn off / turn on gate voltage $V_{GS} = -4V...0V / +15V$

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$		
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.6	3.6	V	$V_{DS} = V_{GS}, I_D = 4.84\ \text{mA}$	Fig. 11	
			2.3		V	$V_{DS} = V_{GS}, I_D = 4.84\ \text{mA}, T_J = 150^\circ\text{C}$		
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$		
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$		
$R_{DS(on)}$	Drain-Source On-State Resistance		45	60	m Ω	$V_{GS} = 15\ \text{V}, I_D = 17.6\ \text{A}$	Fig. 4, 5, 6	
			54			$V_{GS} = 15\ \text{V}, I_D = 17.6\ \text{A}, T_J = 150^\circ\text{C}$		
g_{fs}	Transconductance		12		S	$V_{DS} = 20\ \text{V}, I_{DS} = 17.6\ \text{A}$	Fig. 7	
			11			$V_{DS} = 20\ \text{V}, I_{DS} = 17.6\ \text{A}, T_J = 150^\circ\text{C}$		
C_{iss}	Input Capacitance		1621		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V to } 400\ \text{V}$ $F = 1\ \text{Mhz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18	
C_{oss}	Output Capacitance		101					
C_{rss}	Reverse Transfer Capacitance		8					
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		126					Note: 2
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		178					Note: 2
E_{oss}	C_{oss} Stored Energy		10		μJ	$V_{DS} = 400\ \text{V}, F = 1\ \text{Mhz}$	Fig. 16	
E_{ON}	Turn-On Switching Energy (Body Diode)		36		μJ	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 17.6\ \text{A}, R_{G(ext)} = 2.5\ \Omega, L = 99\ \mu\text{H}, T_J = 25^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25	
E_{OFF}	Turn Off Switching Energy (Body Diode)		7					
$t_{d(on)}$	Turn-On Delay Time		8		ns	$V_{DD} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 17.6\ \text{A}, R_{G(ext)} = 2.5\ \Omega, L = 99\ \mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 26	
t_r	Rise Time		10					
$t_{d(off)}$	Turn-Off Delay Time		19					
t_f	Fall Time		6					
$R_{G(int)}$	Internal Gate Resistance		3		Ω	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$		
Q_{gs}	Gate to Source Charge		21		nC	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 17.6\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12	
Q_{gd}	Gate to Drain Charge		16					
Q_g	Total Gate Charge		61					

Note (2): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 400V

$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 400V

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	$V_{GS} = -4\text{ V}, I_{SD} = 8.8\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2		V	$V_{GS} = -4\text{ V}, I_{SD} = 8.8\text{ A}, T_J = 150^\circ\text{C}$	
I_S	Continuous Diode Forward Current		26	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
$I_{S,pulse}$	Diode pulse Current		132	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recover time	10		ns	$V_{GS} = -4\text{ V}, I_{SD} = 17.6\text{ A}, V_R = 400\text{ V}$ $dif/dt = 5420\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	206		nC		
I_{rrm}	Peak Reverse Recovery Current	36		A		
t_{rr}	Reverse Recover time	13		ns	$V_{GS} = -4\text{ V}, I_{SD} = 17.6\text{ A}, V_R = 400\text{ V}$ $dif/dt = 1915\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	103		nC		
I_{rrm}	Peak Reverse Recovery Current	14		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.85	$^\circ\text{C}/\text{W}$		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

Typical Performance

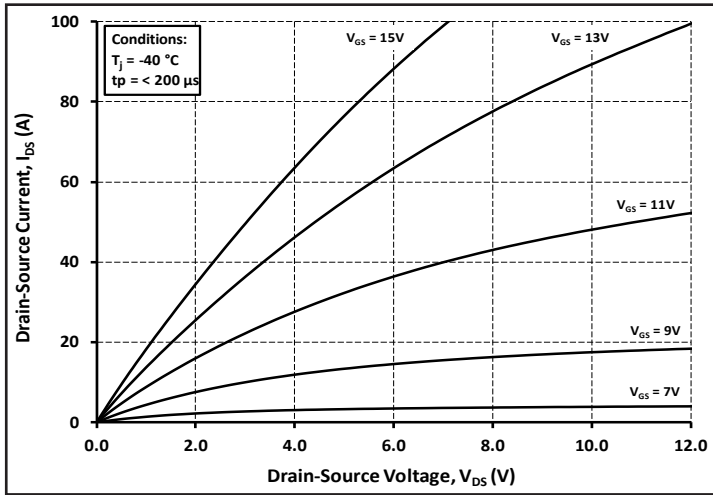


Figure 1. Output Characteristics $T_J = -40\text{ }^\circ\text{C}$

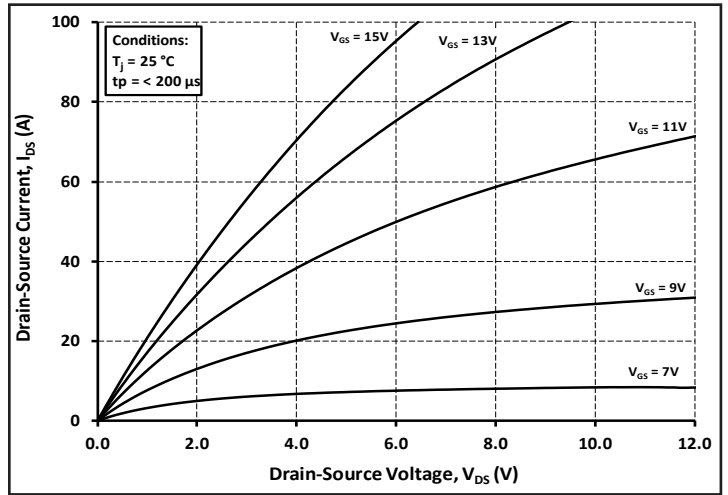


Figure 2. Output Characteristics $T_J = 25\text{ }^\circ\text{C}$

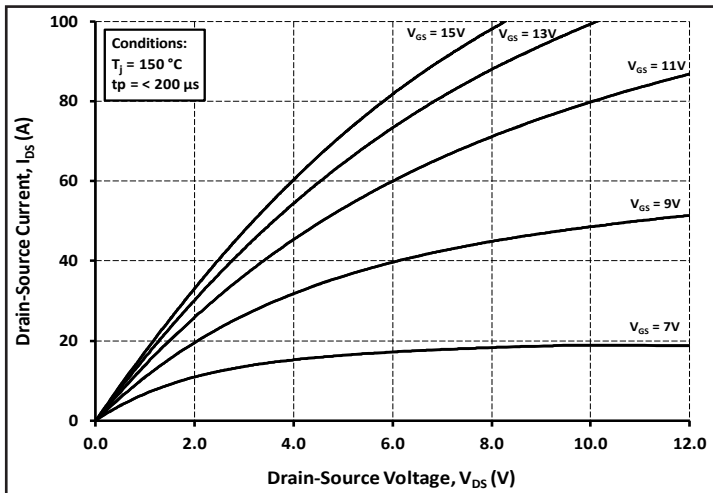


Figure 3. Output Characteristics $T_J = 150\text{ }^\circ\text{C}$

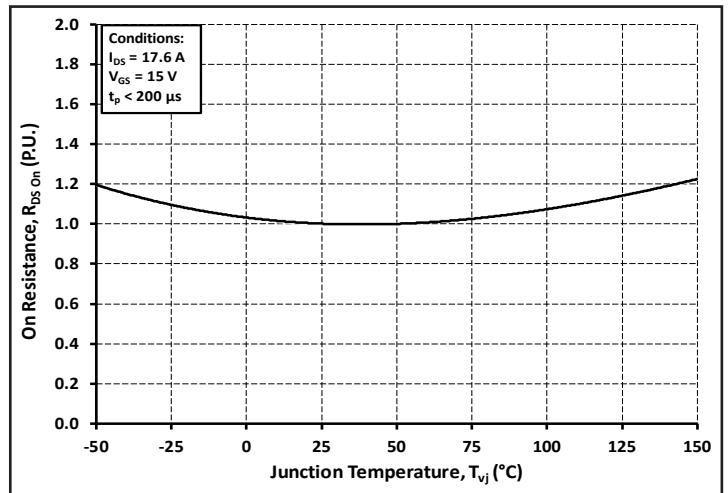


Figure 4. Normalized On-Resistance vs. Temperature

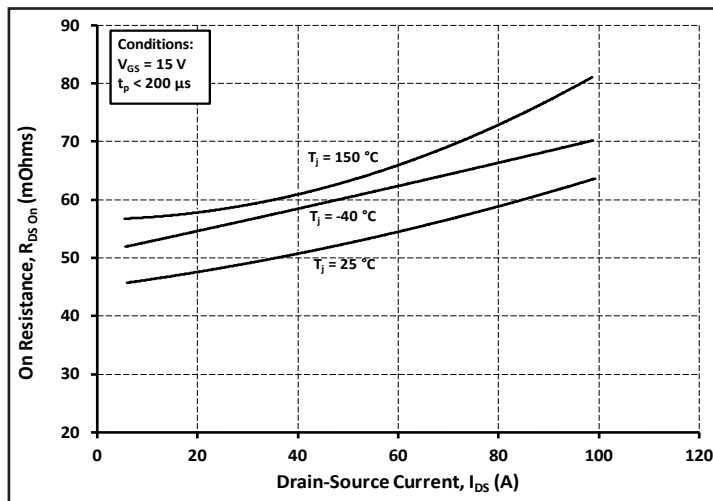


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

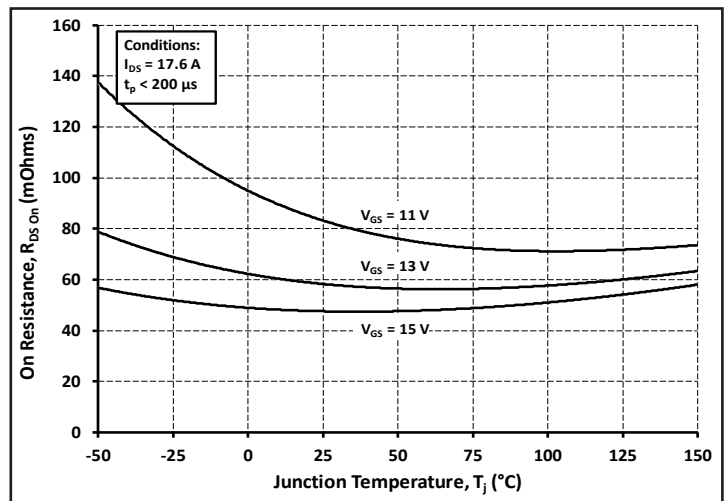


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

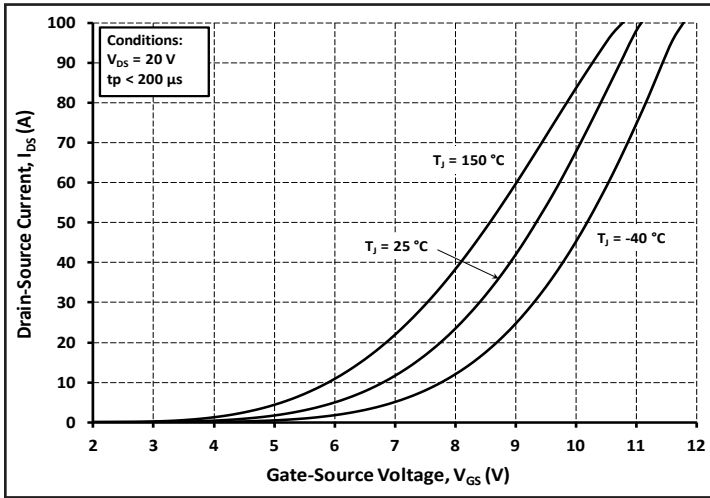


Figure 7. Transfer Characteristic for Various Junction Temperatures

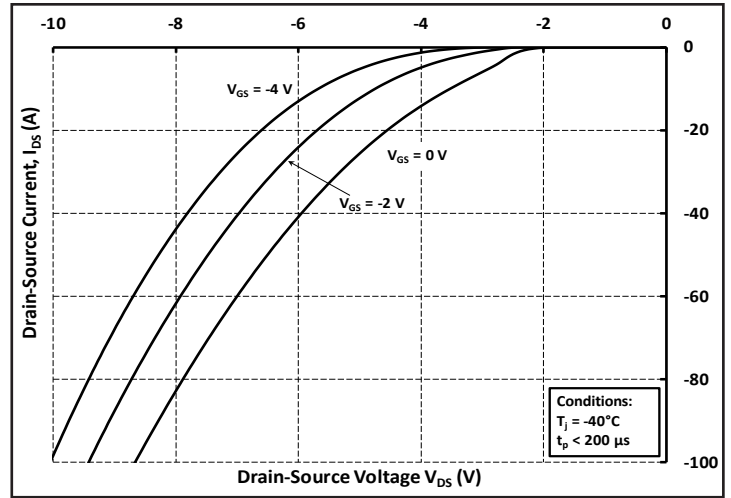


Figure 8. Body Diode Characteristic at -40 °C

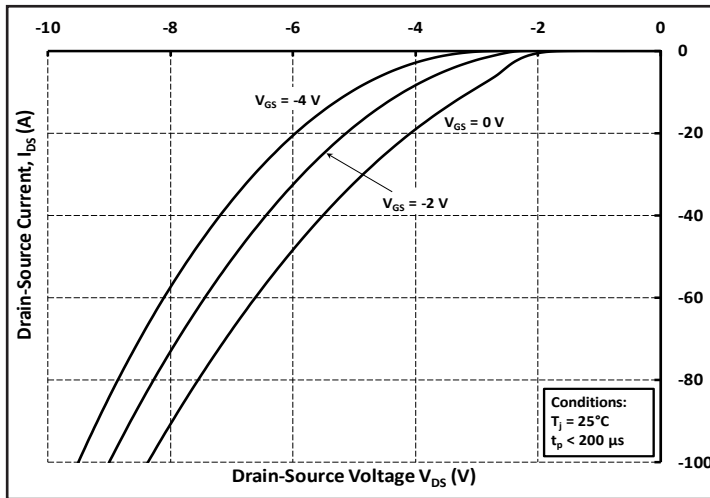


Figure 9. Body Diode Characteristic at 25 °C

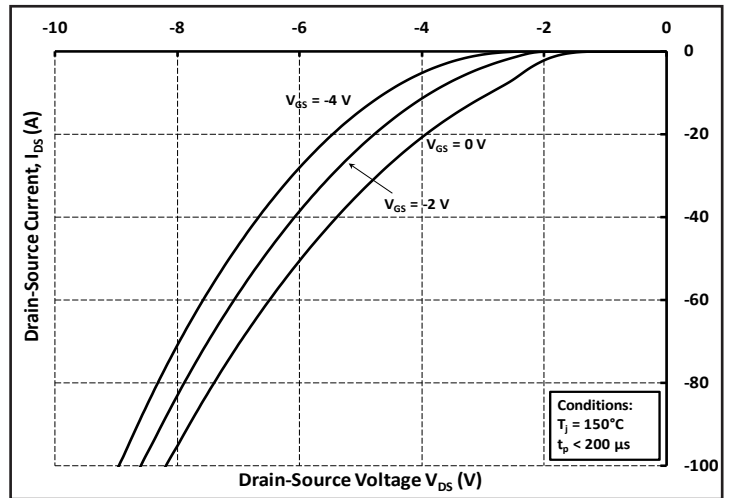


Figure 10. Body Diode Characteristic at 150 °C

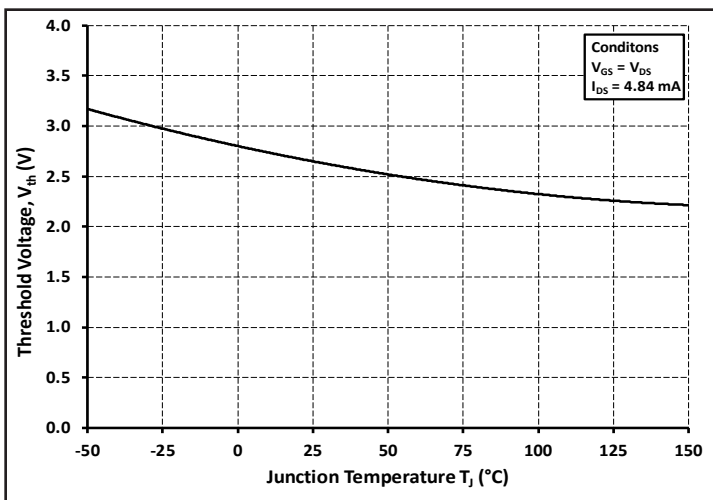


Figure 11. Threshold Voltage vs. Temperature

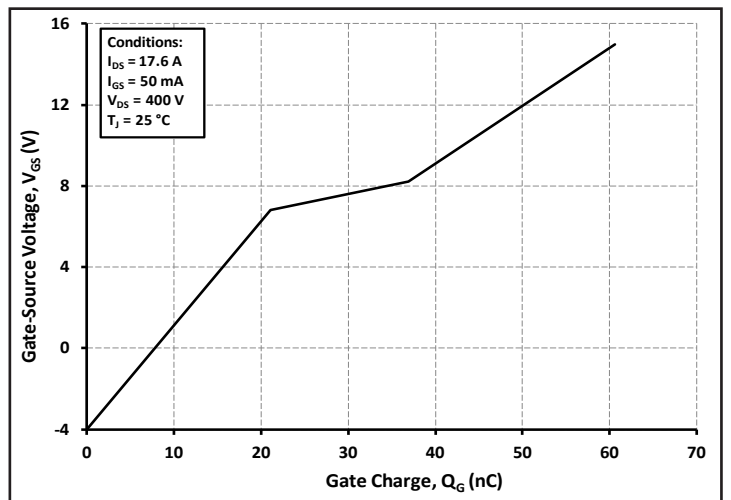


Figure 12. Gate Charge Characteristics

Typical Performance

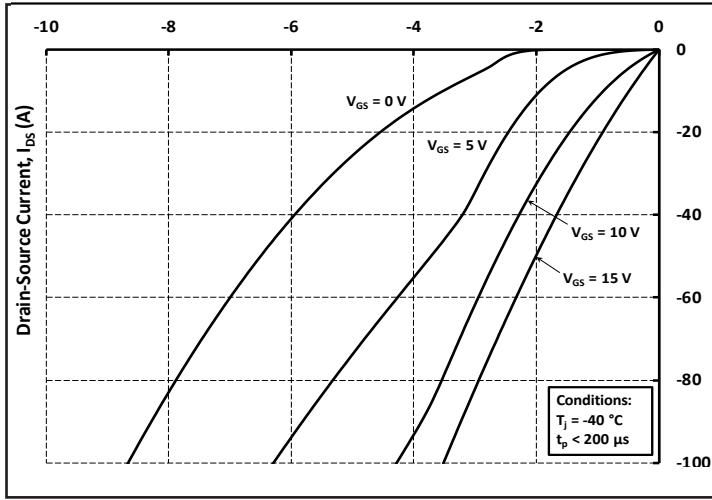


Figure 13. 3rd Quadrant Characteristic at $-40\text{ }^{\circ}\text{C}$

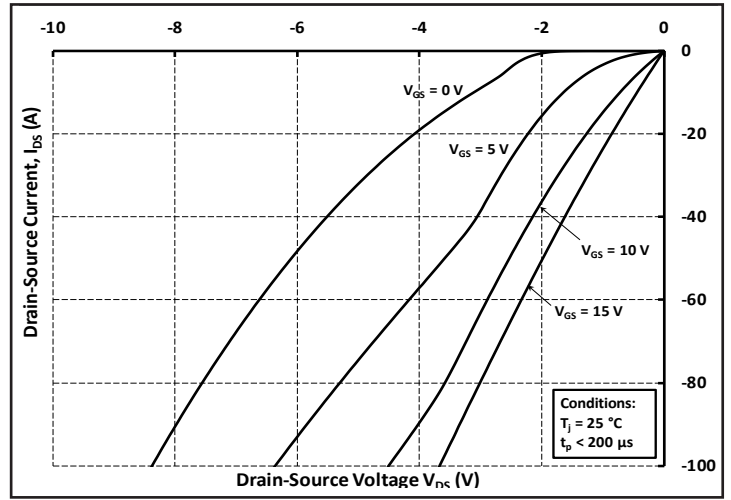


Figure 14. 3rd Quadrant Characteristic at $25\text{ }^{\circ}\text{C}$

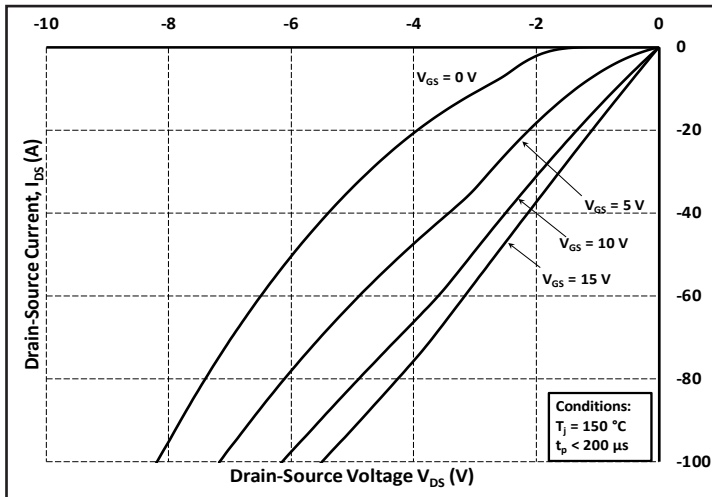


Figure 15. 3rd Quadrant Characteristic at $150\text{ }^{\circ}\text{C}$

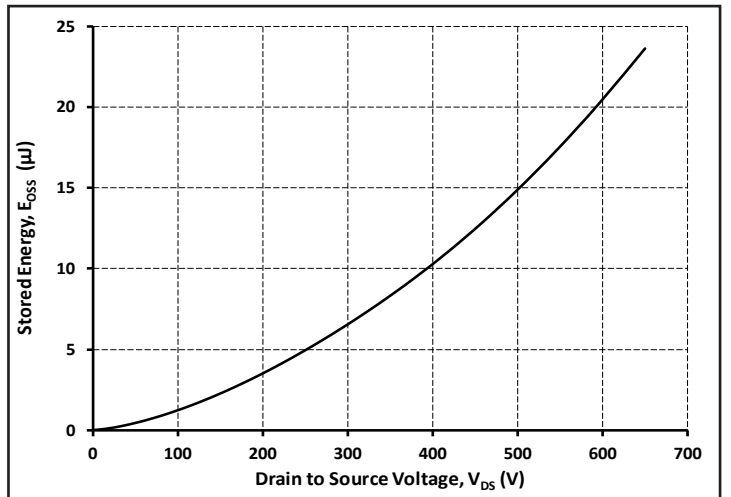


Figure 16. Output Capacitor Stored Energy

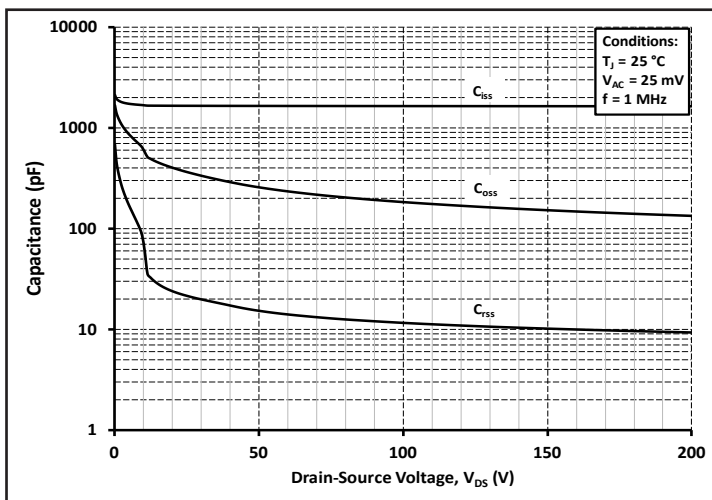


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

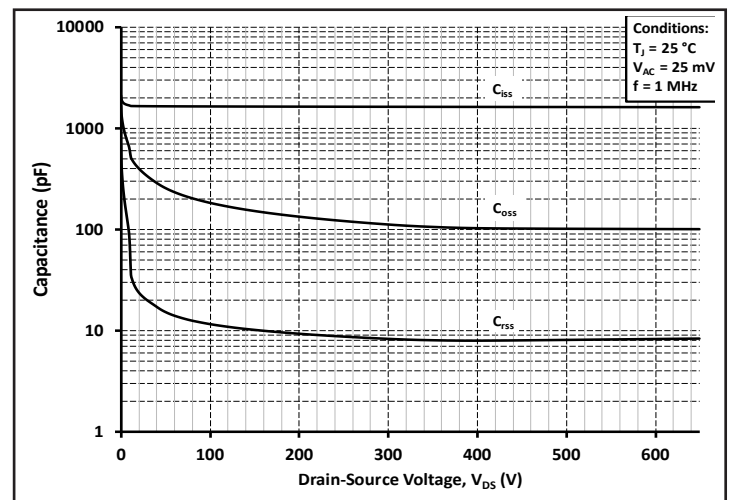


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 600V)

Typical Performance

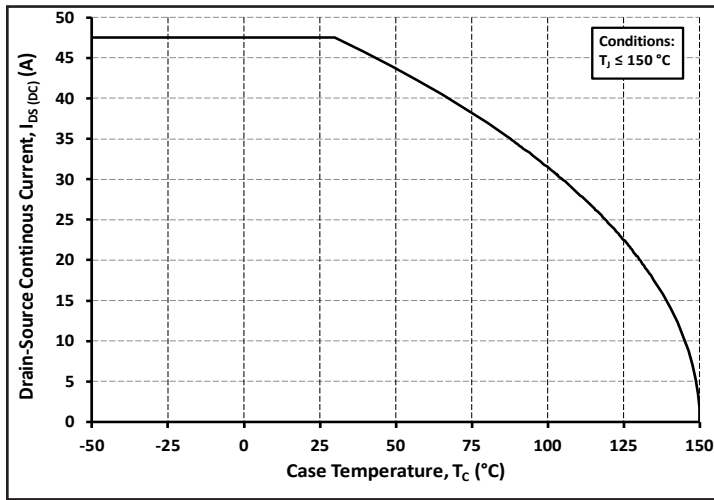


Figure 19. Continuous Drain Current Derating vs. Case Temperature

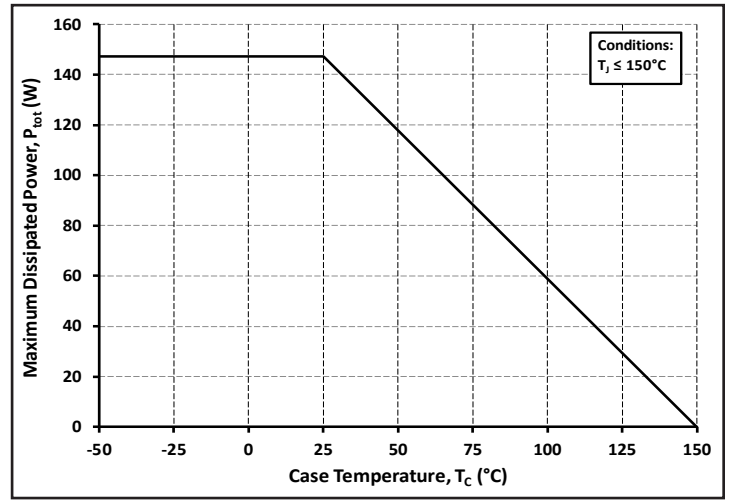


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

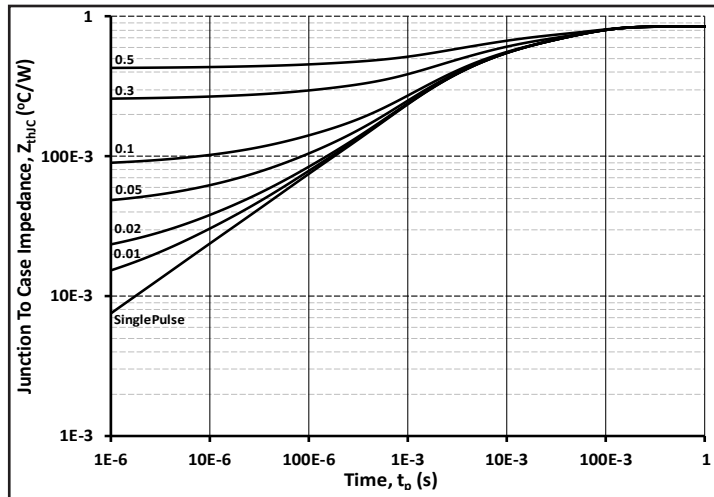


Figure 21. Transient Thermal Impedance (Junction - Case)

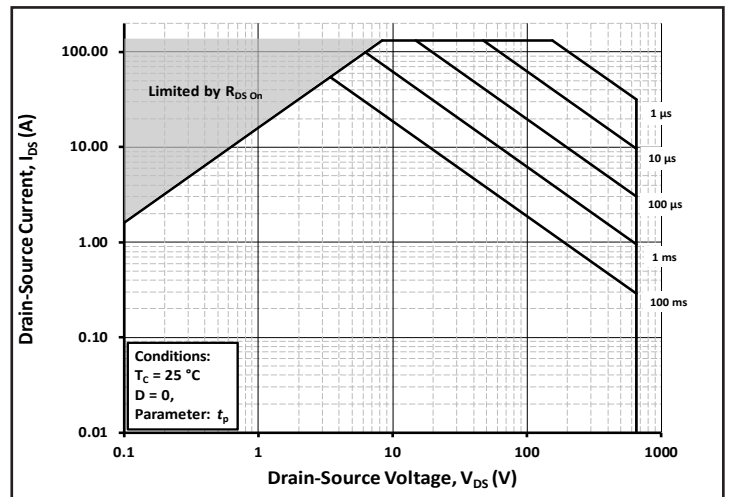


Figure 22. Safe Operating Area

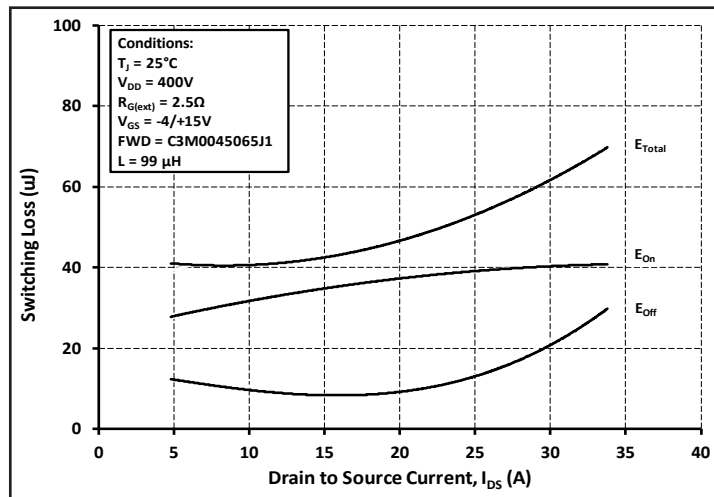


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

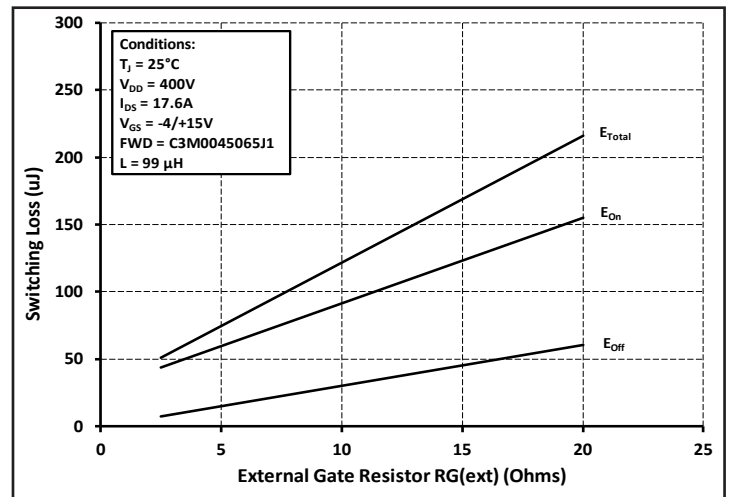


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

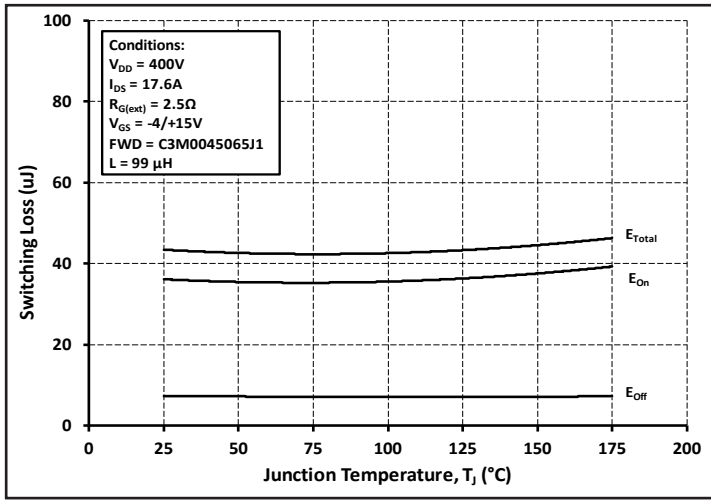


Figure 25. Clamped Inductive Switching Energy vs. Temperature

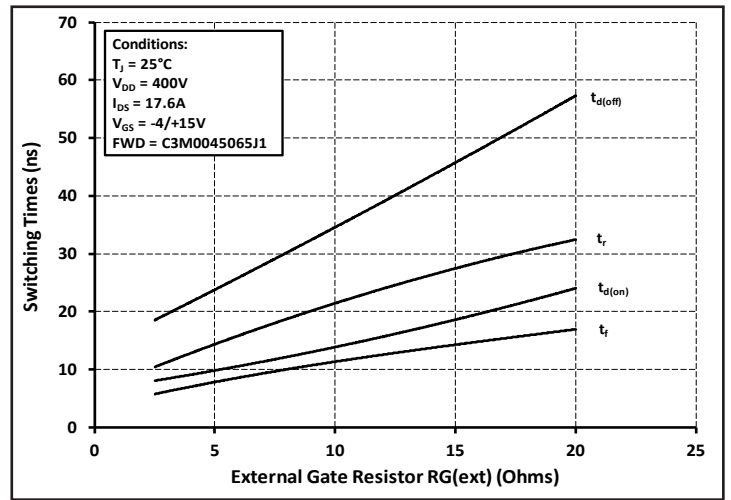


Figure 26. Switching Times vs $R_{G(ext)}$

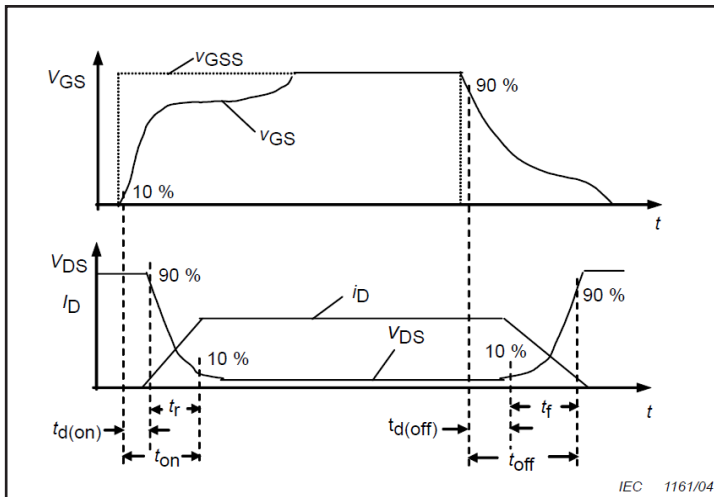


Figure 27. Switching Times Definition

Test Circuit Schematic

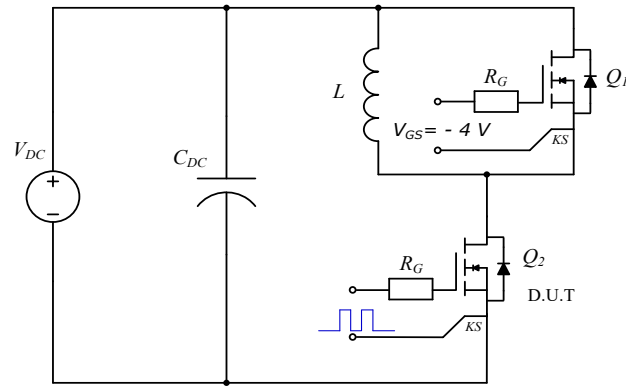
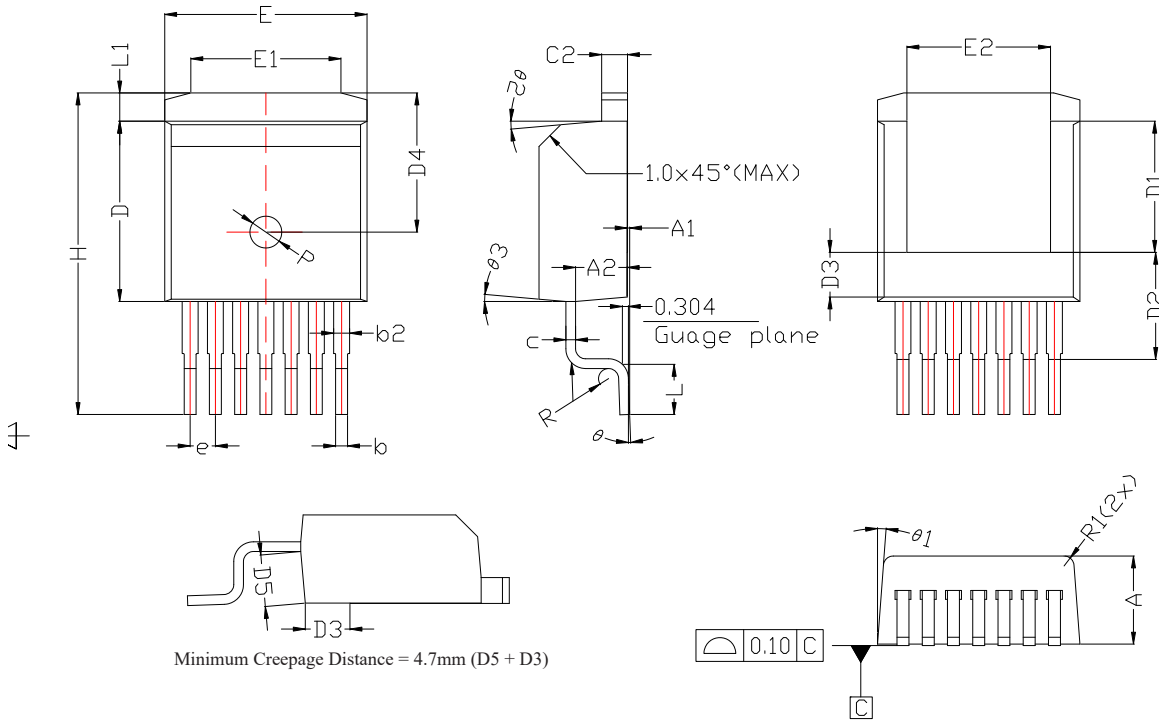


Figure 28. Clamped Inductive Switching
Waveform Test Circuit

Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

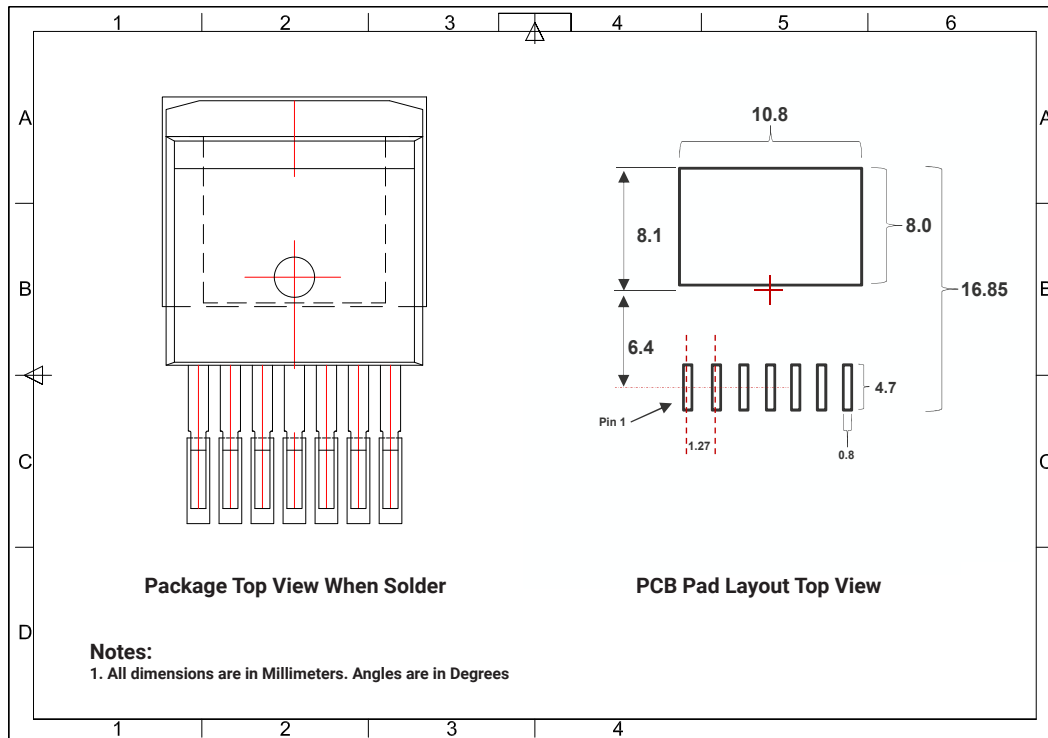
Package Dimensions

TO-263-7L XL



DIM	MIN	MAX	TYP
D	9.025	9.125	9.075
E	10.13	10.23	10.18
A	4.30	4.57	4.435
H	15.043	17.313	16.178
D1	6.50	6.70	6.60
E1	6.50	8.60	7.55
D2	5.39 REF.		
E2	6.778	7.665	7.223
D3	2.148	2.248	
D4	7.00 REF.		
D5	2.555	2.605	
A1	0	0.25	0.125
A2	2.595 REF.		
e	1.27 TYP.		
L	2.324	2.70	2.512
b	0.50	0.70	0.60
L1	0.968	1.868	1.418
b2	0.60	1.00	0.80
C2	1.17	1.37	1.27
c	0.281	0.481	0.381
R	0.506 REF.		
R1	0.50 REF.		
P	ø1.60 REF.		
θ	0°	8°	4°
θ1	4.5°	5.5°	5°
θ2	4°	6°	5°
θ3	4°	6°	5°

- NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER. ANGLES ARE IN DEGREE.
 2. DIMENSION "D" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH SHALL NOT EXCEED 0.50 MM PER SIDE. DIMENSION "E" DOES NOT INCLUDE MOLD FLASH, GATE BURRS, THE GATE BURRS SHALL NOT EXCEED 0.30MM.
 3. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 4. "b2" DIMENSION DON'T INCLUDE DAMBAR PROTRUSION.
 5. THE VOID SHOULD BE CONTROL WITHIN 0.25MM.



- Notes:
1. All dimensions are in Millimeters. Angles are in Degrees