C3M0045065L

Silicon Carbide Power MOSFET

C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

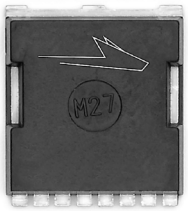
Benefits

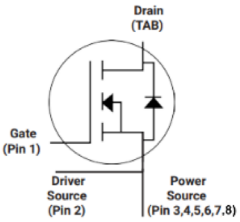
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Datacenter Power Supplies
- Telecom Power Supplies
- Energy Storage Systems
- Solar (PV) inverters
- High Voltage DC/DC converters

Package





Part Number	Package	Marking
C3M0045065L	TOLL	C3M0045065L

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter		Value	Unit	Note
V_{DSmax}	Drain - Source Voltage		650	V	
V_{GSmax}	Gate - Source Voltage		-8/+19	V	Note: 1
I_D	Continuous Drain Current, V_{GS} = 15 V	T_C = 25˚C	49	A	Fig. 19 Note: 2
		T_C = 100˚C	33		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_P limited by T_{jmax}		132	A	Fig. 22
P_D	Power Dissipation, T_C=25˚C, T_J = 175 ˚C		164	W	Fig. 20 Note: 2
T_J	Junction Temperature		-40 to +175	˚C	
T_C , T_{stg}	Case Temperature and Storage Temperature		-40 to +150	˚C	
T_L	Solder Temperature, 1.6mm (0.063”) from case for 10s		260	˚C	

Note (1): Recommended turn off / turn on gate voltage V_{GS} - 4V...0V / +15V
Note (2): Verified by design

4600 Silicon Drive | Durham, NC 27703 | Tel: +1.919.313.5300 | wolfspeed.com/power

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.6	3.6	V	V_{DS} = V_{GS}, I_D = 4.84 mA	Fig. 11
			2.2		V	V_{DS} = V_{GS}, I_D = 4.84 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		45	60	mΩ	V_{GS} = 15 V, I_D = 17.6 A	Fig. 4, 5, 6
			61			V_{GS} = 15 V, I_D = 17.6 A, T_J = 175ºC	
g_{fs}	Transconductance		12		S	V_{DS}= 20 V, I_{DS}= 17.6 A	Fig. 7
			11			V_{DS}= 20 V, I_{DS}= 17.6 A, T_J = 175ºC	
C_{iss}	Input Capacitance		1621		pF	V_{GS} = 0 V, V_{DS} = 400 V F = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		101				
C_{rss}	Reverse Transfer Capacitance		8				
E_{oss}	C_{oss} Stored Energy		20		µJ	V_{DS} = 600 V, F = 1 Mhz	
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		126		pF	V_{GS} = 0 V, V_{DS} = 0... 400V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		178		pF		
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		53		µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 17.6A, $R_{G(ext)}$ = 2.5 Ω, L= 99 µH, T_J = 25ºC FWD = Internal Body Diode	Fig. 23
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		10				
$t_{d(on)}$	Turn-On Delay Time		7		ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 17.6 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 26
t_r	Rise Time		9				
$t_{d(off)}$	Turn-Off Delay Time		17				
t_f	Fall Time		6				
$R_{G(int)}$	Internal Gate Resistance		3		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		20		nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 17.6 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		16				
Q_g	Total Gate Charge		59				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 400V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	V_{GS} = -4 V, I_{SD} = 8.8 A, T_J = 25 °C	Fig. 8, 9, 10
		4.2		V	V_{GS} = -4 V, I_{SD} = 8.8 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		28	A	V_{GS} = -4 V, T_C = 25˚C	
$I_{S,\ pulse}$	Diode pulse Current		132	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	10		ns	V_{GS} = -4 V, I_{SD} = 17.6 A, V_R = 400 V dif/dt = 6580 A/µs, T_J = 25 °C	
Q_{rr}	Reverse Recovery Charge	207		nC		
I_{rrm}	Peak Reverse Recovery Current	38		A		
t_{rr}	Reverse Recover time	12		ns	V_{GS} = -4 V, I_{SD} = 17.6 A, V_R = 400 V dif/dt = 2260 A/µs, T_J = 25 °C	
Q_{rr}	Reverse Recovery Charge	94		nC		
I_{rrm}	Peak Reverse Recovery Current	14		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.64	°C/W		Fig. 21

Typical Performance

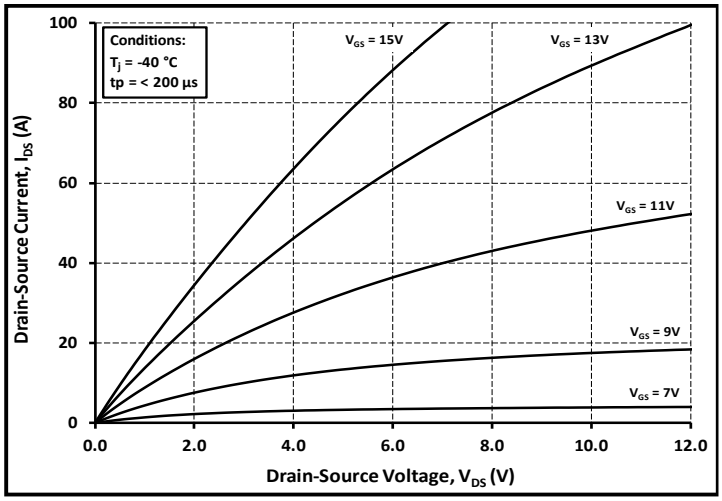


Figure 1. Output Characteristics T_J = -40 ºC

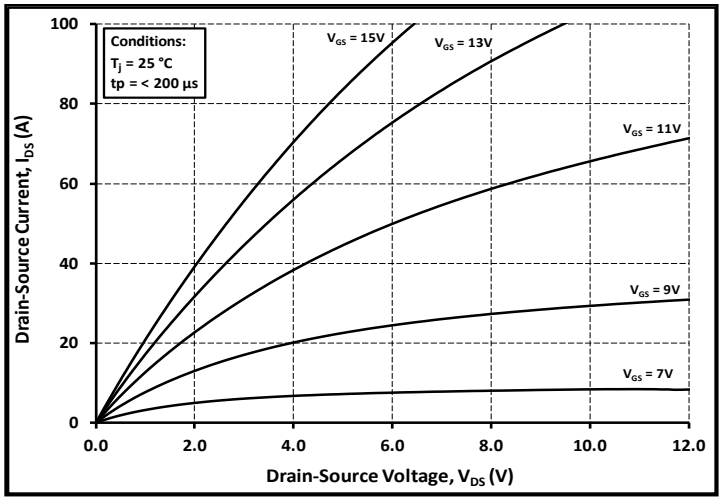


Figure 2. Output Characteristics T_J = 25 ºC

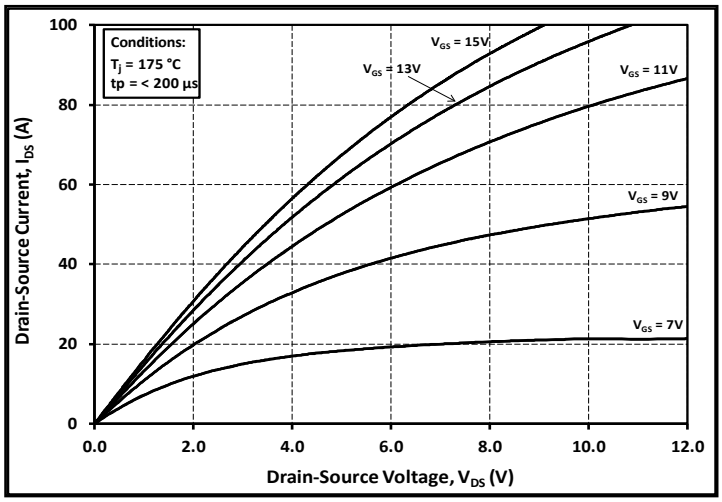


Figure 3. Output Characteristics T_J = 175 ºC

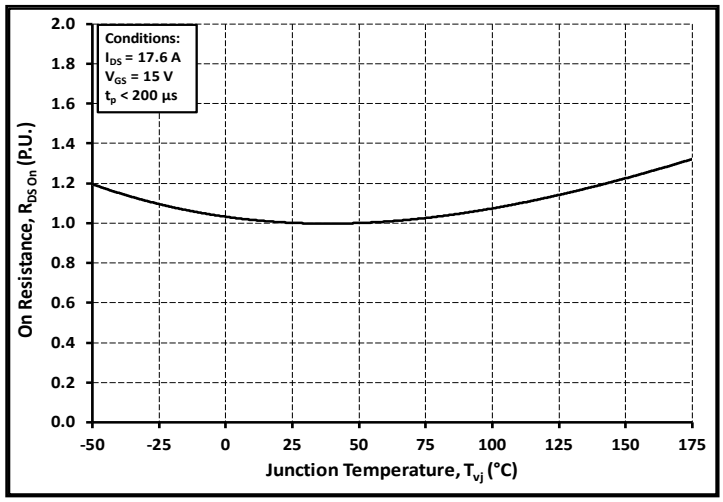


Figure 4. Normalized On-Resistance vs. Temperature

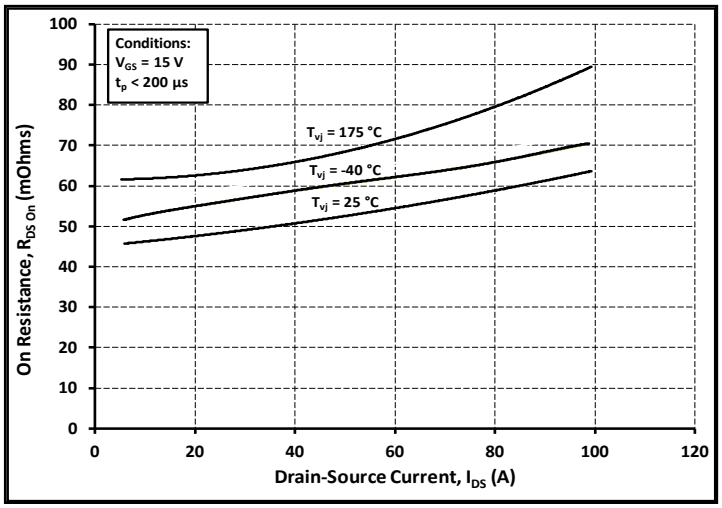


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

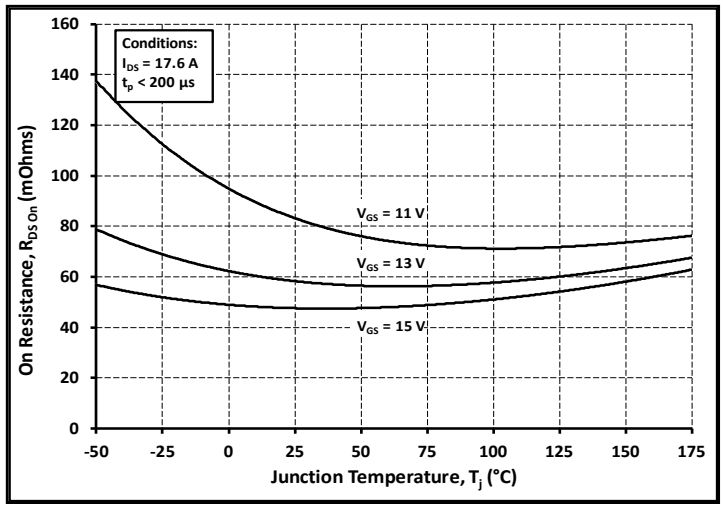


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

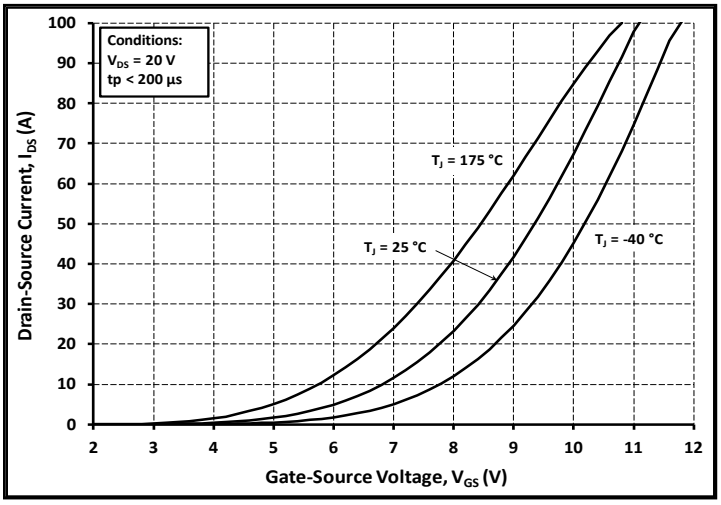


Figure 7. Transfer Characteristic for Various Junction Temperatures

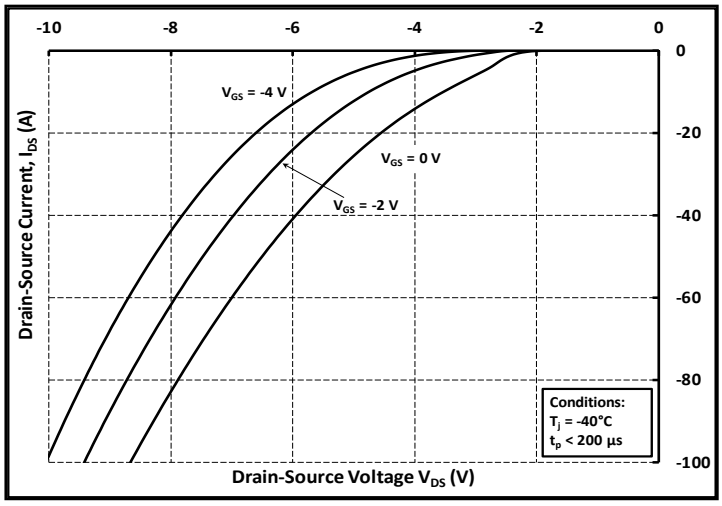


Figure 8. Body Diode Characteristic at -40 °C

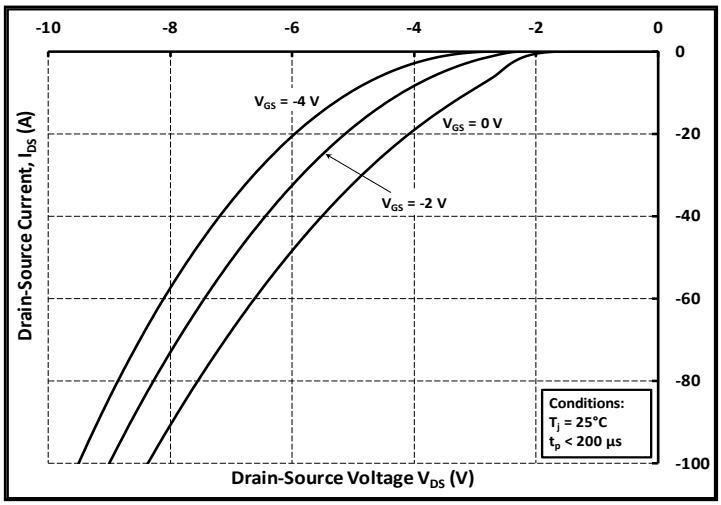


Figure 9. Body Diode Characteristic at 25 °C

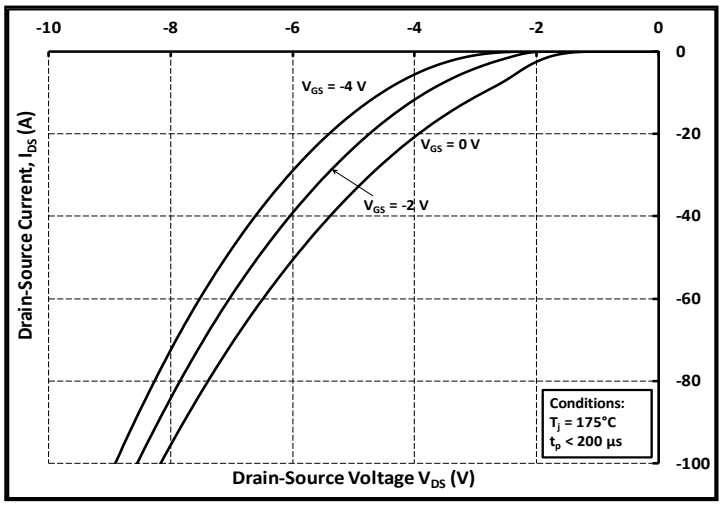


Figure 10. Body Diode Characteristic at 175 °C

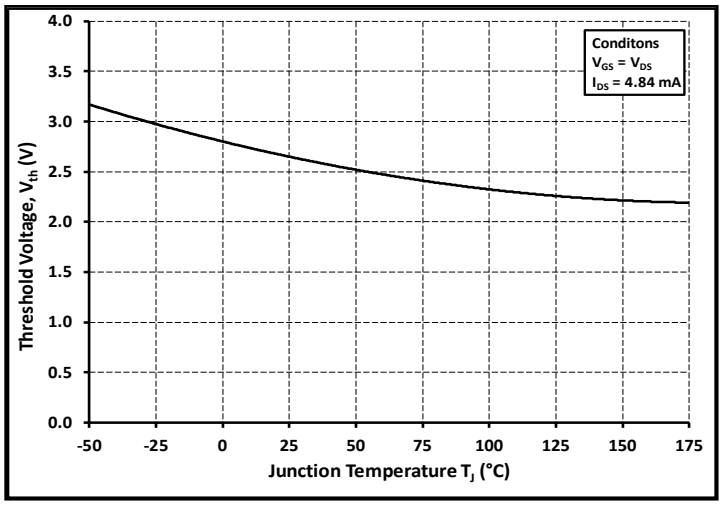


Figure 11. Threshold Voltage vs. Temperature

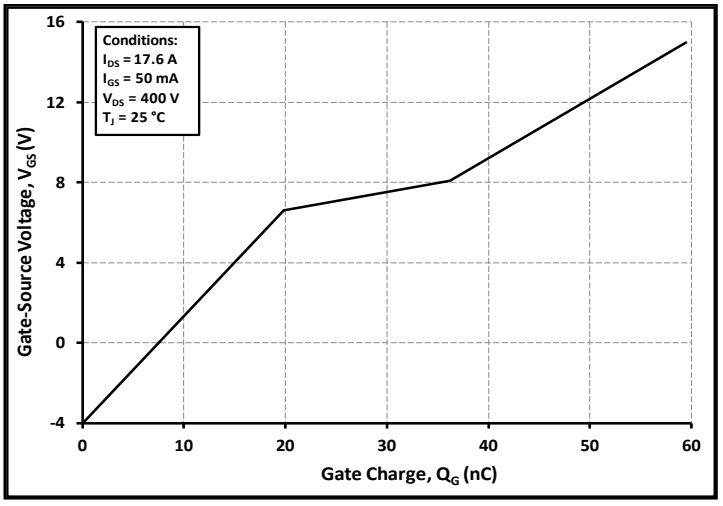


Figure 12. Gate Charge Characteristics

Typical Performance

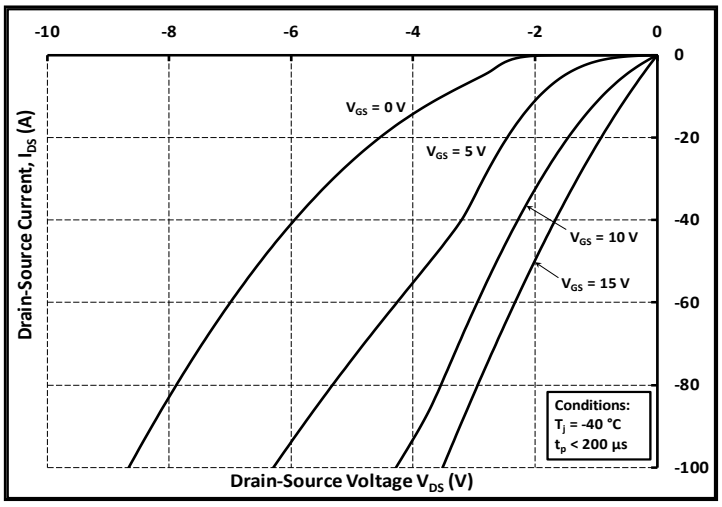


Figure 13. 3rd Quadrant Characteristic at -40 ºC

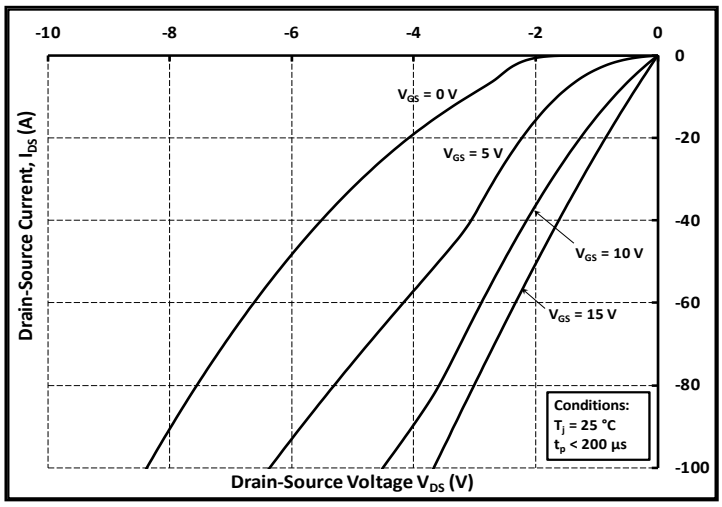


Figure 14. 3rd Quadrant Characteristic at 25 ºC

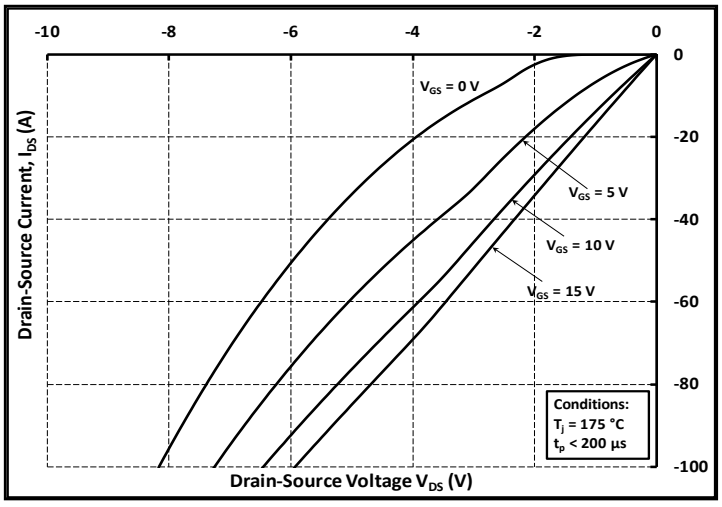


Figure 15. 3rd Quadrant Characteristic at 175 ºC

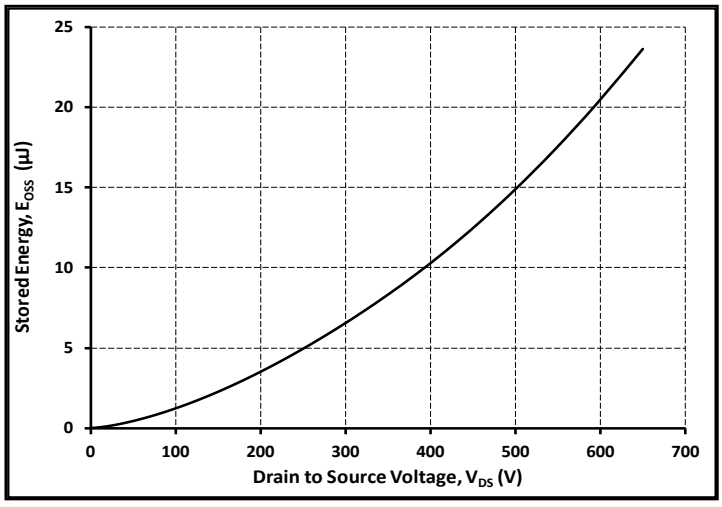


Figure 16. Output Capacitor Stored Energy

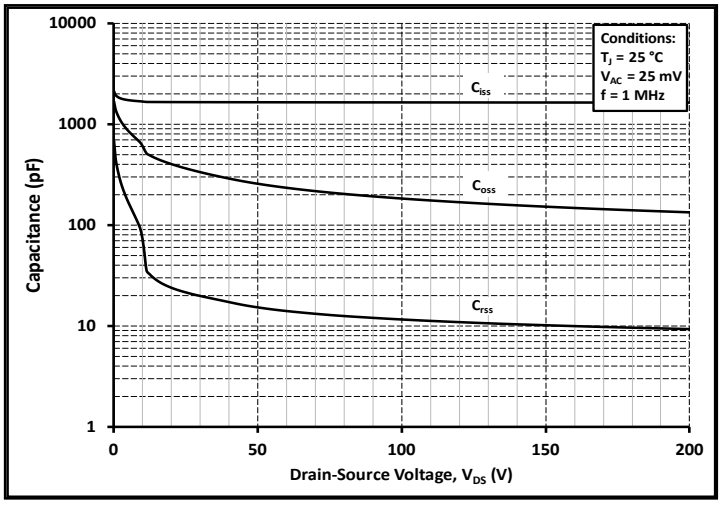


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

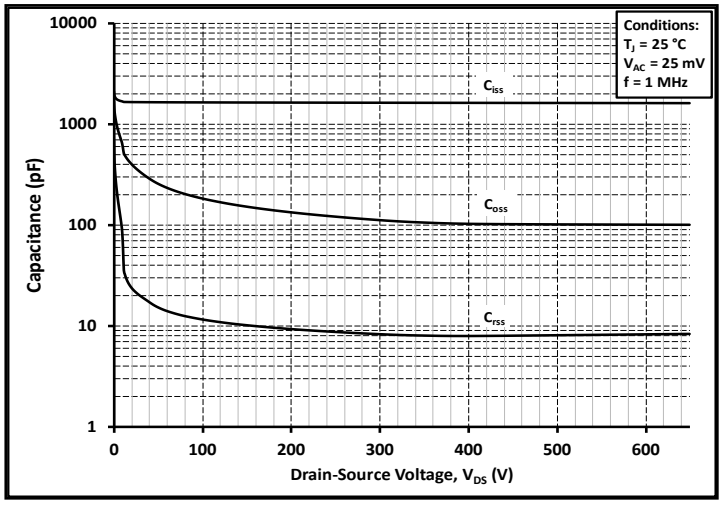


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

Typical Performance

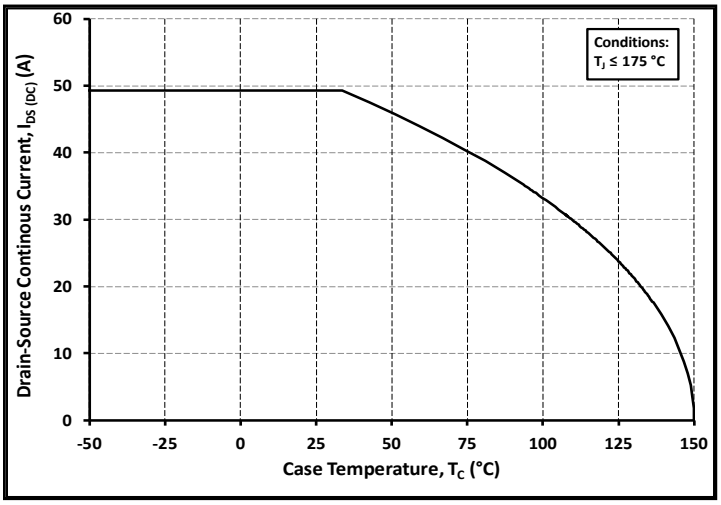


Figure 19. Continuous Drain Current Derating vs. Case Temperature

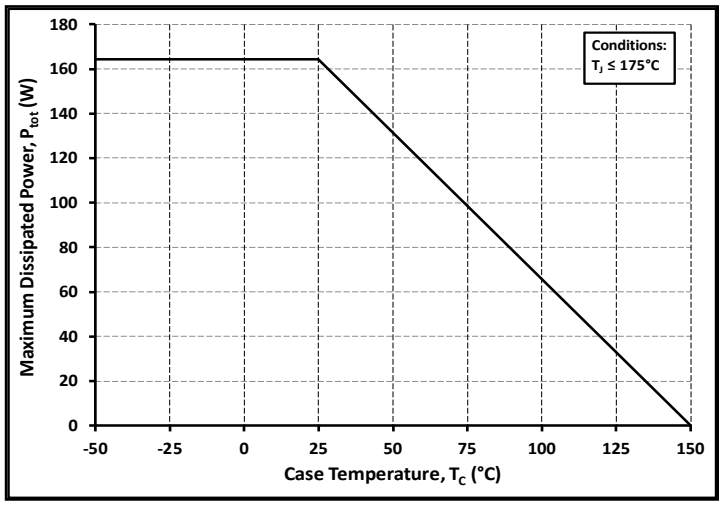


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

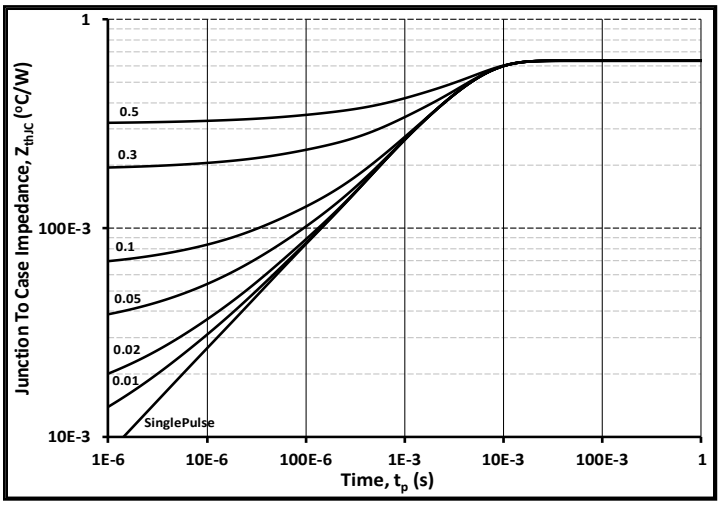


Figure 21. Transient Thermal Impedance (Junction - Case)

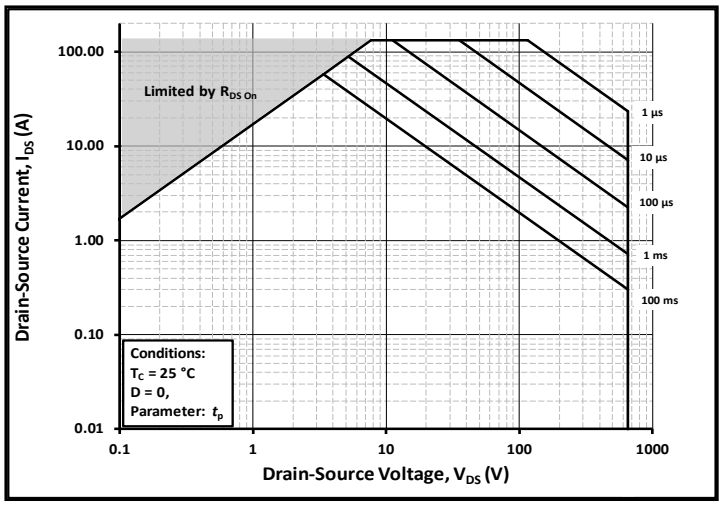


Figure 22. Safe Operating Area

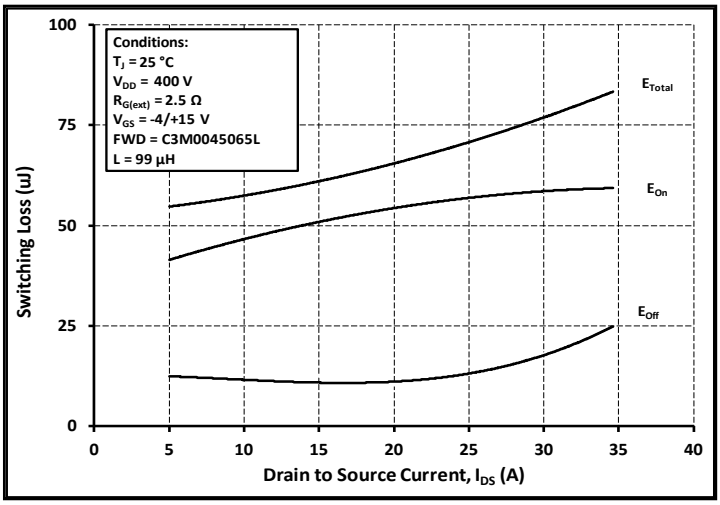


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400V)

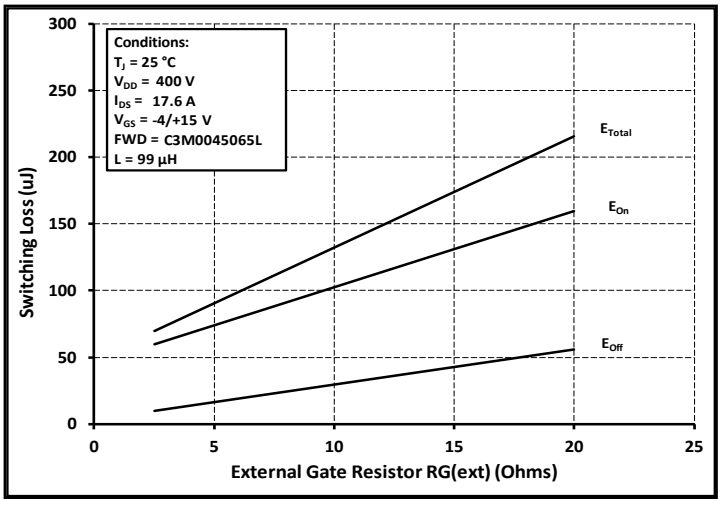


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

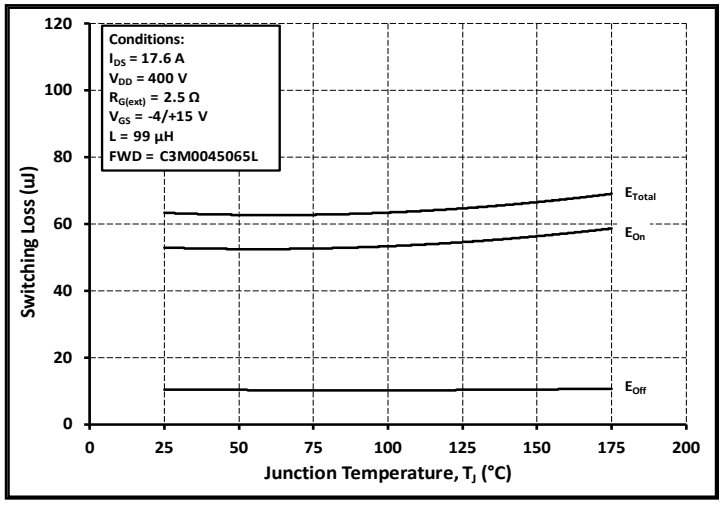


Figure 25. Clamped Inductive Switching Energy vs. Temperature

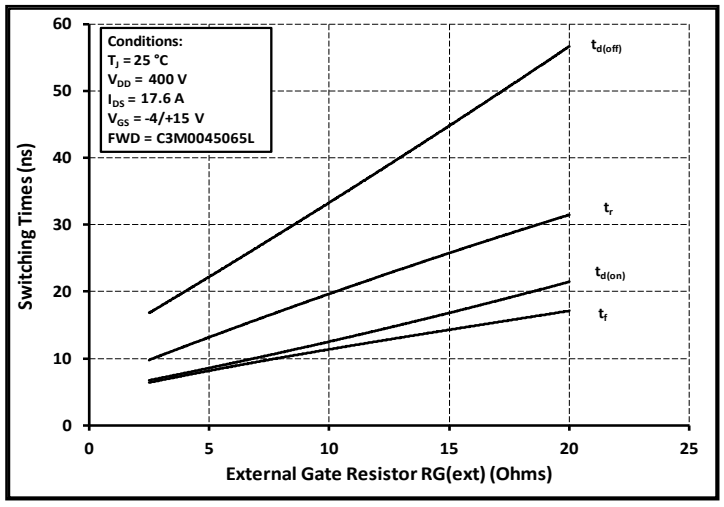


Figure 26. Switching Times vs. $R_{G(ext)}$

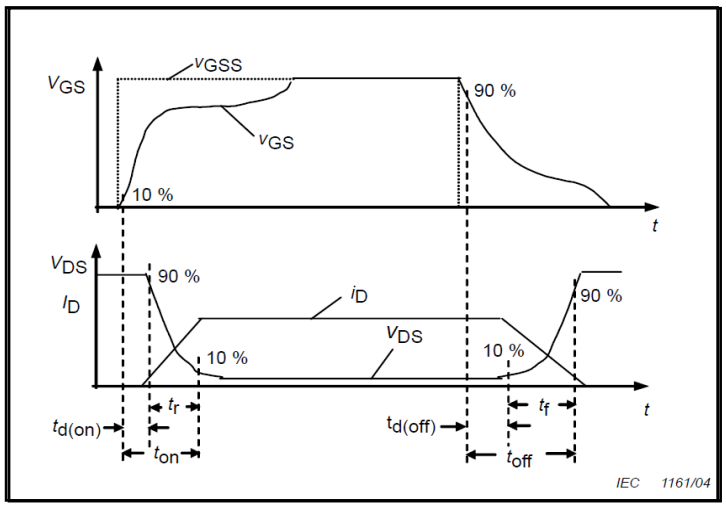


Figure 27. Switching Times Definition

Test Circuit Schematic

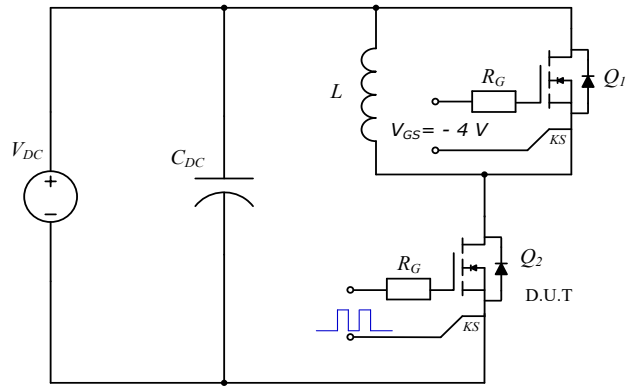
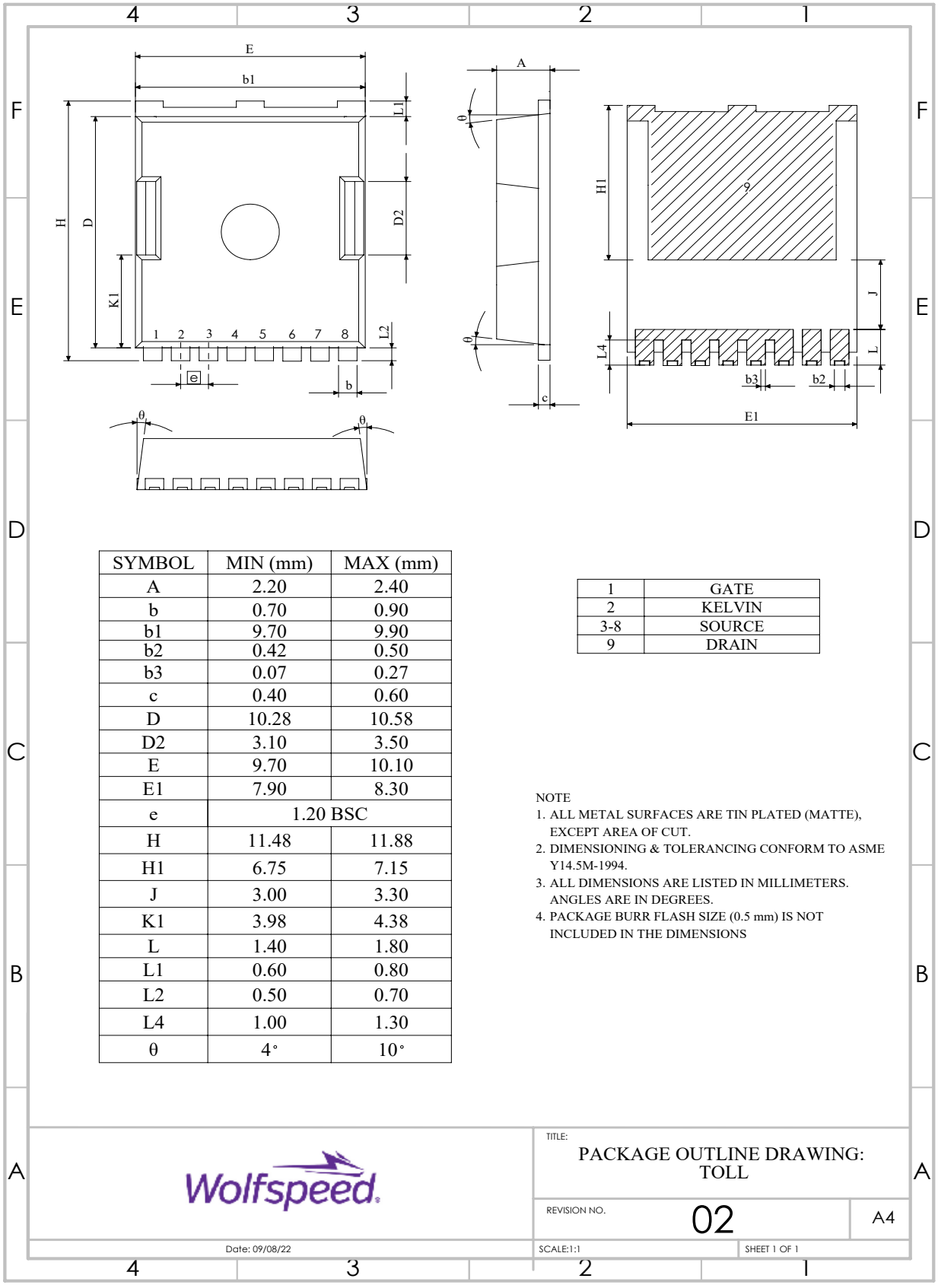


Figure 28. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
b3	0.07	0.27
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20 BSC	
H	11.48	11.88
H1	6.75	7.15
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°

1	GATE
2	KELVIN
3-8	SOURCE
9	DRAIN

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

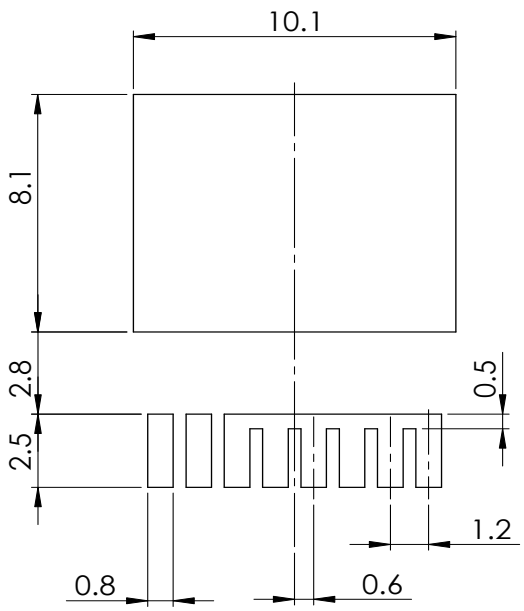
TITLE: PACKAGE OUTLINE DRAWING: TOLL

REVISION NO. 02 | A4

Date: 09/08/22 | SCALE:1:1 | SHEET 1 OF 1

Recommended Solder Pad Layout

(Note: All Dimensions are listed in Millimeters)



Revision history

Document Version	Date of release	Descriptiion of changes
1.0	September-2022	Initial datasheet