

C3M0060065J

Silicon Carbide Power MOSFET

C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- 3rd Generation SiC MOSFET technology
- Low inductance package with driver source pin
- 7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Qrr)
- Halogen free, RoHS compliant

Benefits

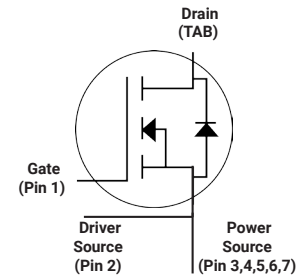
- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Applications

- EV charging
- Server power supplies
- Solar PV inverters
- UPS
- DC/DC converters

V_{DS}	650 V
$I_D @ 25^\circ\text{C}$	36 A
$R_{DS(on)}$	60 mΩ

Package



Part Number	Package	Marking
C3M0060065J	TO-263-7	C3M0060065J

Maximum Ratings

Symbol	Parameter	Value	Unit	Note
V_{DSS}	Drain - Source Voltage, $T_c = 25^\circ\text{C}$	650	V	
V_{GS}	Gate - Source voltage (Under transient events < 100 ns)	-8/+19	V	Fig. 28
I_D	Continuous Drain Current, $V_{GS} = 15\text{ V}$, $T_c = 25^\circ\text{C}$	36	A	Fig. 19
	Continuous Drain Current, $V_{GS} = 15\text{ V}$, $T_c = 100^\circ\text{C}$	26		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_p limited by T_{jmax}	99	A	
P_D	Power Dissipation, $T_c = 25^\circ\text{C}$, $T_j = 175^\circ\text{C}$	136	W	Fig. 20
T_j, T_{stg}	Operating Junction and Storage Temperature	-40 to +175	$^\circ\text{C}$	
T_L	Solder Temperature, 1.6mm (0.063") from case for 10s	260	$^\circ\text{C}$	

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
V_{GSon}	Gate-Source Recommended Turn-On Voltage		15		V	Static	Fig. 28
V_{GSoff}	Gate-Source Recommended Turn-Off Voltage		-4		V		
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3	3.6	V	$V_{DS} = V_{GS}, I_D = 5\ \text{mA}$	Fig. 11
			1.9		V	$V_{DS} = V_{GS}, I_D = 5\ \text{mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance	42	60	79	m Ω	$V_{GS} = 15\ \text{V}, I_D = 13.2\ \text{A}$	Fig. 4, 5, 6
			80			$V_{GS} = 15\ \text{V}, I_D = 13.2\ \text{A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		10		S	$V_{DS} = 20\ \text{V}, I_{DS} = 13.2\ \text{A}$	Fig. 7
			9			$V_{DS} = 20\ \text{V}, I_{DS} = 13.2\ \text{A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		1020		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 600\ \text{V}$ $f = 1\ \text{MHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		80				
C_{rss}	Reverse Transfer Capacitance		9				
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		95		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V to } 400\ \text{V}$	Note 1
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		132				
E_{oss}	C_{oss} Stored Energy		15		μJ	$V_{DS} = 600\ \text{V}, 1\ \text{MHz}$	Fig. 16
E_{ON}	Turn-On Switching Energy (Body Diode)		41		μJ	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 13.2\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 135\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
E_{OFF}	Turn Off Switching Energy (Body Diode)		5				
$t_{d(on)}$	Turn-On Delay Time		9		ns	$V_{DD} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 13.2\ \text{A}, R_{G(ext)} = 2.5\ \Omega, L = 135\ \mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 26
t_r	Rise Time		8				
$t_{d(off)}$	Turn-Off Delay Time		17				
t_f	Fall Time		6				
$R_{G(int)}$	Internal Gate Resistance		3		Ω	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$	
Q_{gs}	Gate to Source Charge		14		nC	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 13.2\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		14				
Q_g	Total Gate Charge		46				

Note (1): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 400V
 $C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 400V

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	$V_{GS} = -4\text{ V}, I_{SD} = 6.6\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.8		V	$V_{GS} = -4\text{ V}, I_{SD} = 6.6\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		21	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
$I_{S, pulse}$	Diode pulse Current		99	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recover time	8		ns	$V_{GS} = -4\text{ V}, I_{SD} = 13.2\text{ A}, V_R = 400\text{ V}$ $dif/dt = 3600\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	75		nC		
I_{rrm}	Peak Reverse Recovery Current	15		A		
t_{rr}	Reverse Recover time	10		ns	$V_{GS} = -4\text{ V}, I_{SD} = 13.2\text{ A}, V_R = 400\text{ V}$ $dif/dt = 2300\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	62		nC		
I_{rrm}	Peak Reverse Recovery Current	10		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.1	$^\circ\text{C}/\text{W}$		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

Typical Performance

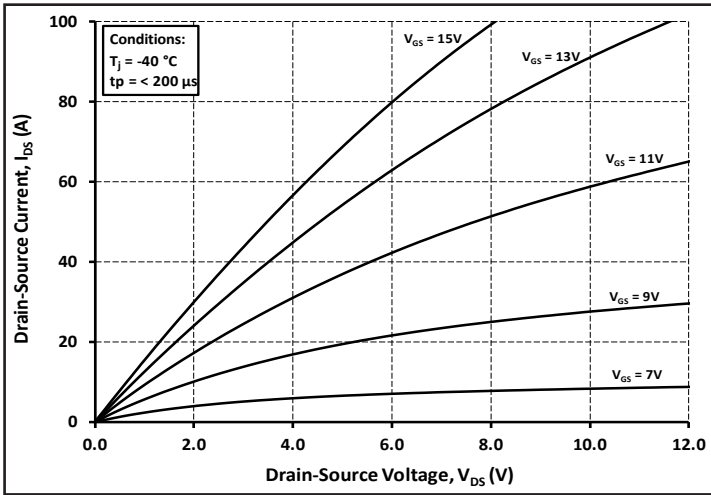


Figure 1. Output Characteristics $T_J = -40\text{ }^\circ\text{C}$

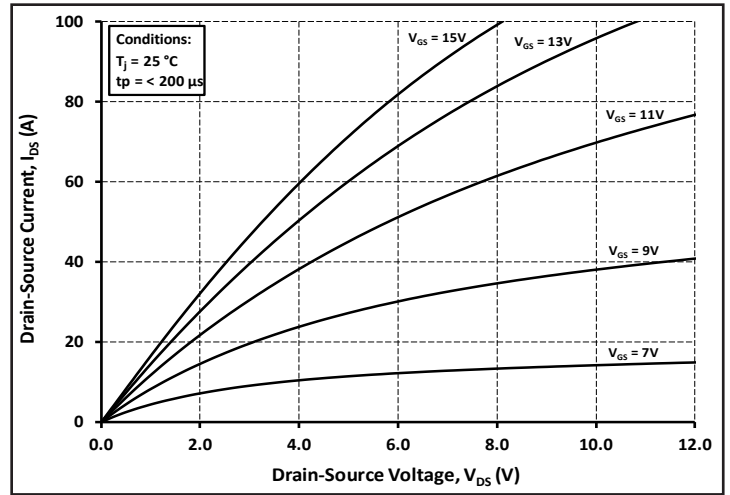


Figure 2. Output Characteristics $T_J = 25\text{ }^\circ\text{C}$

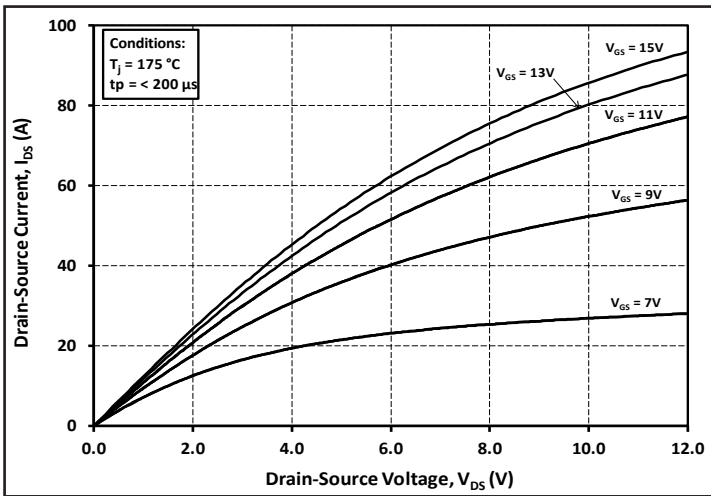


Figure 3. Output Characteristics $T_J = 175\text{ }^\circ\text{C}$

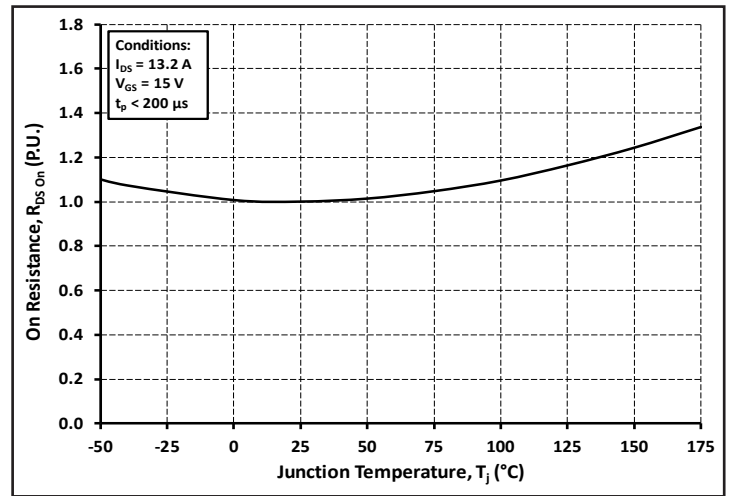


Figure 4. Normalized On-Resistance vs. Temperature

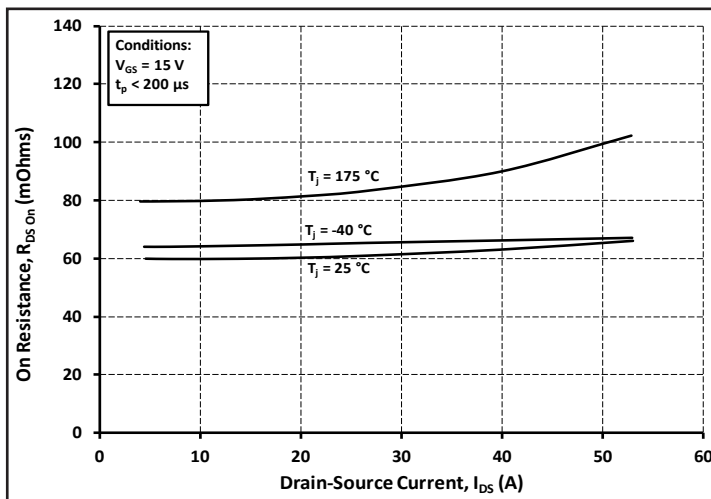


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

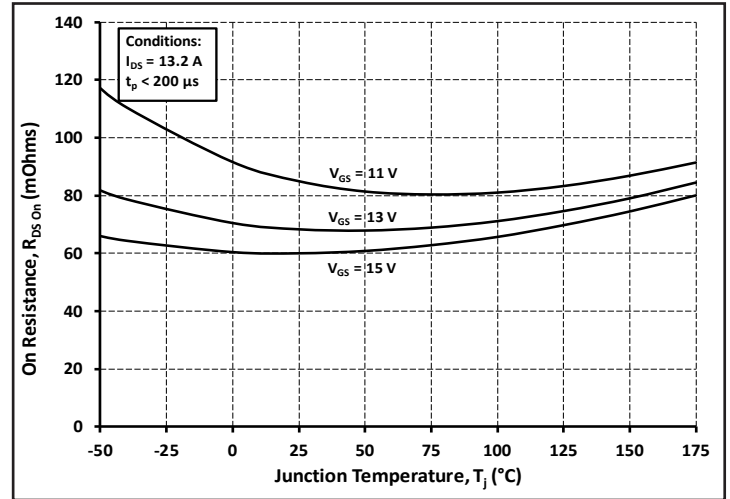


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

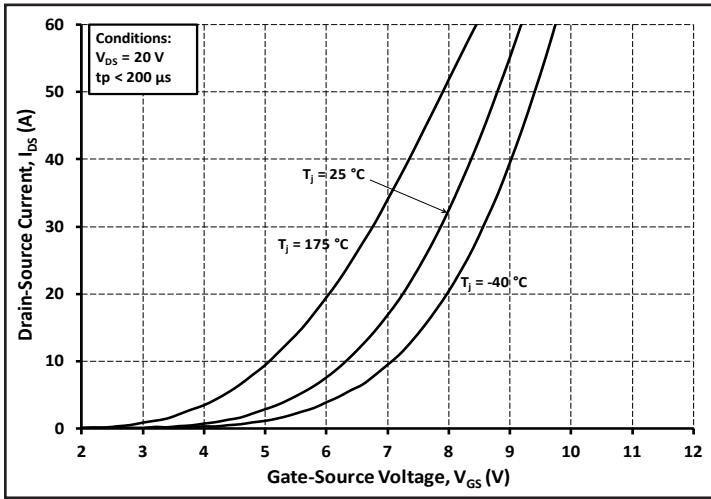


Figure 7. Transfer Characteristic for Various Junction Temperatures

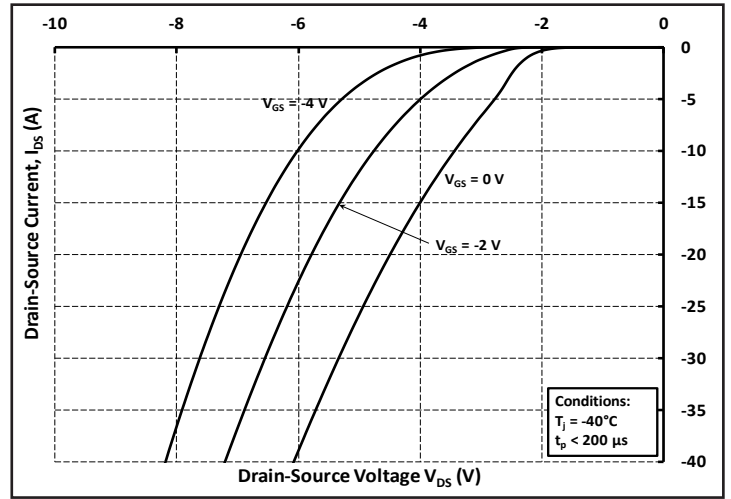


Figure 8. Body Diode Characteristic at $-40\text{ }^\circ\text{C}$

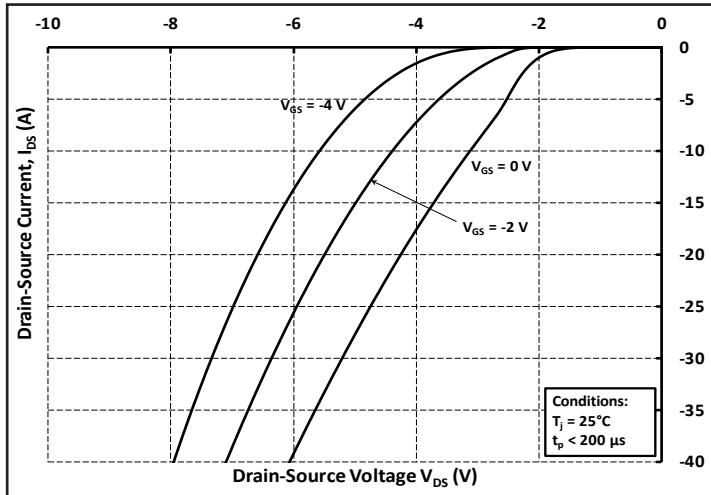


Figure 9. Body Diode Characteristic at $25\text{ }^\circ\text{C}$

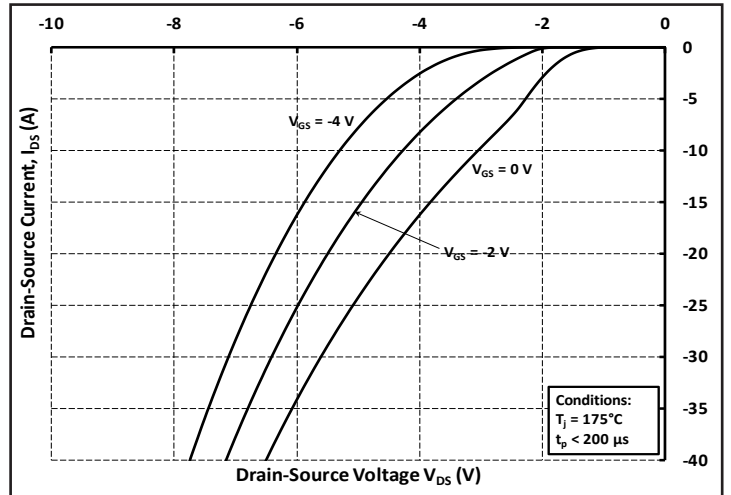


Figure 10. Body Diode Characteristic at $175\text{ }^\circ\text{C}$

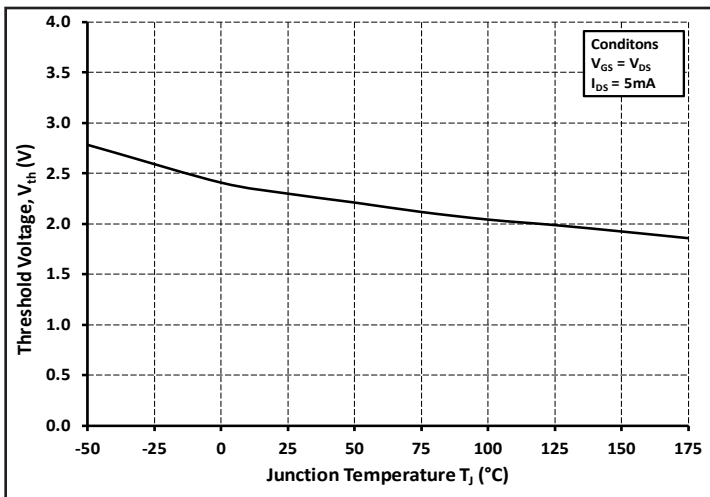


Figure 11. Threshold Voltage vs. Temperature

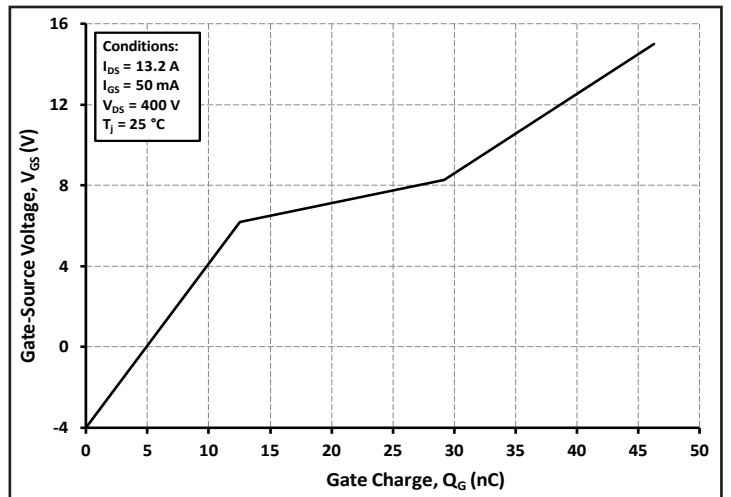


Figure 12. Gate Charge Characteristics

Typical Performance

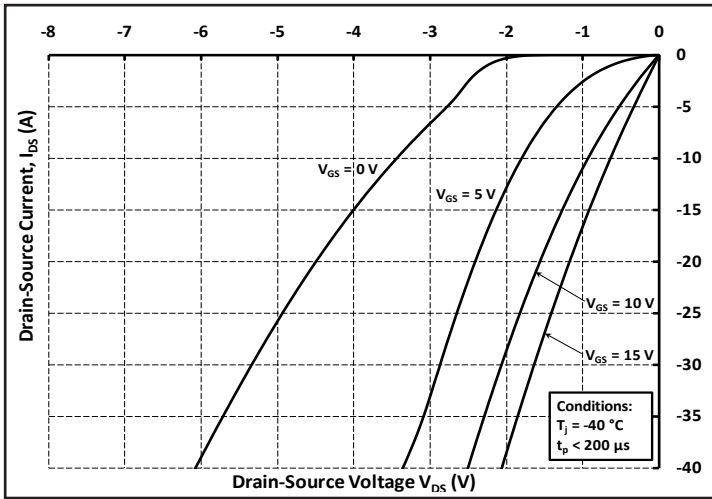


Figure 13. 3rd Quadrant Characteristic at -40 °C

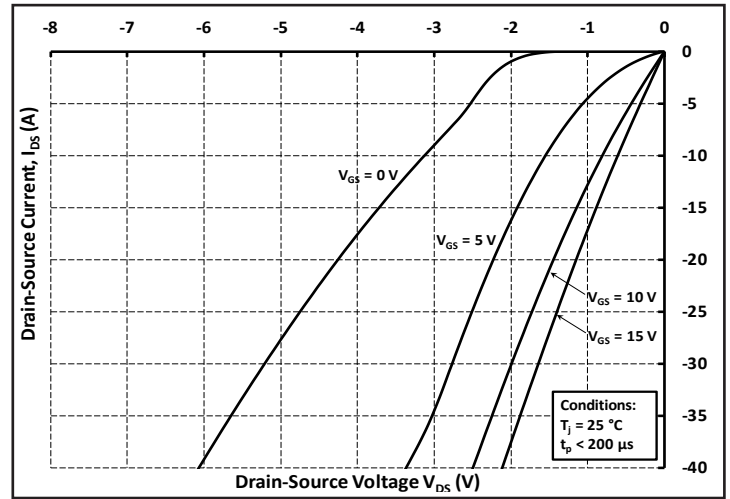


Figure 14. 3rd Quadrant Characteristic at 25 °C

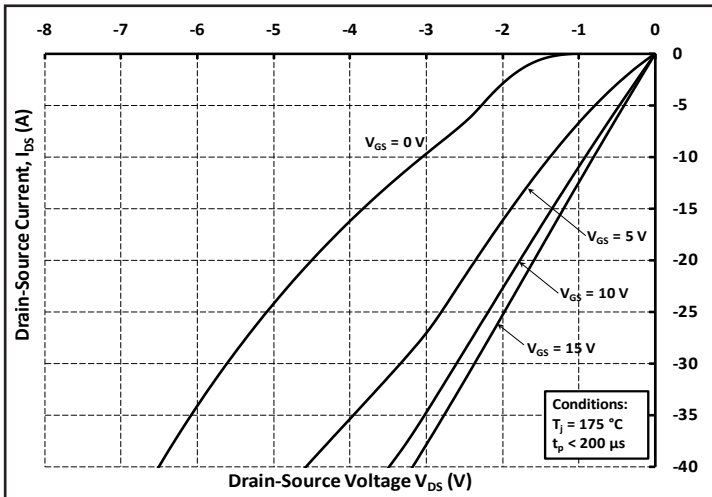


Figure 15. 3rd Quadrant Characteristic at 175 °C

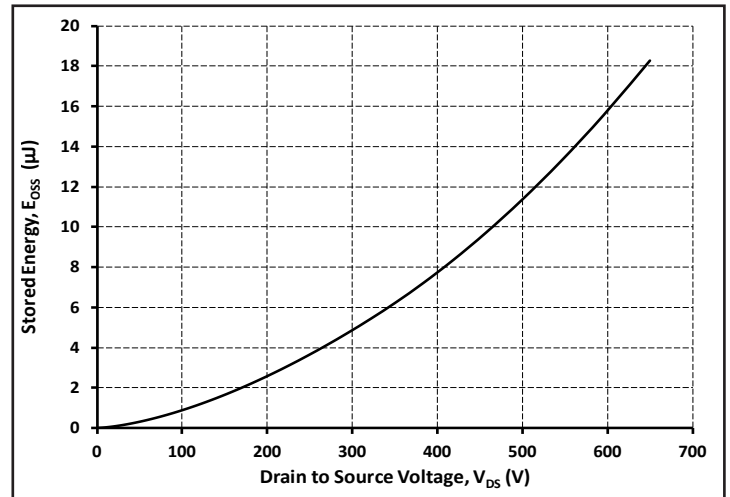


Figure 16. Output Capacitor Stored Energy

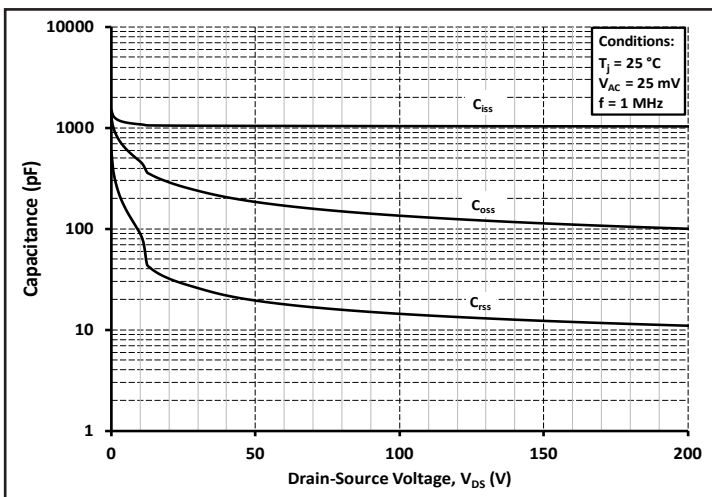


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

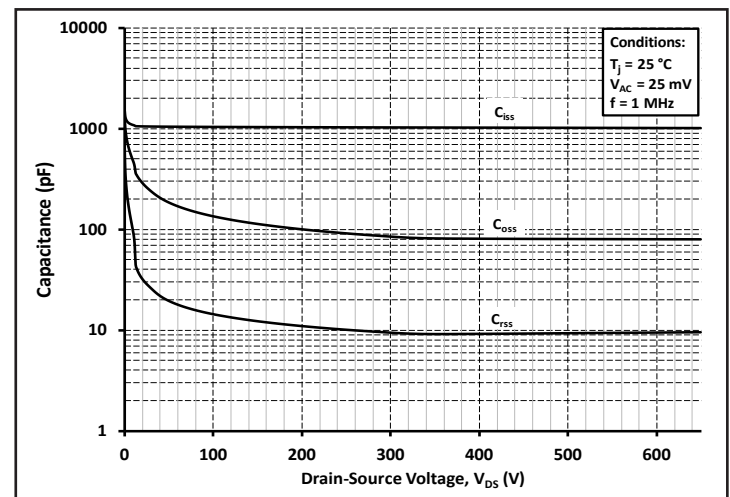


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

Typical Performance

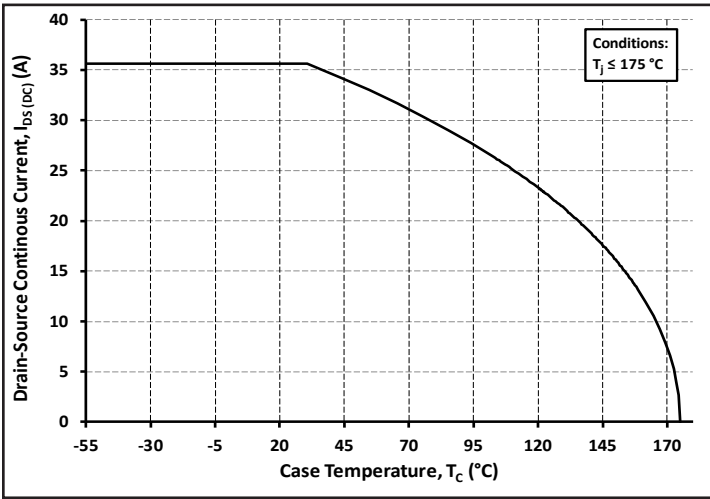


Figure 19. Continuous Drain Current Derating vs. Case Temperature

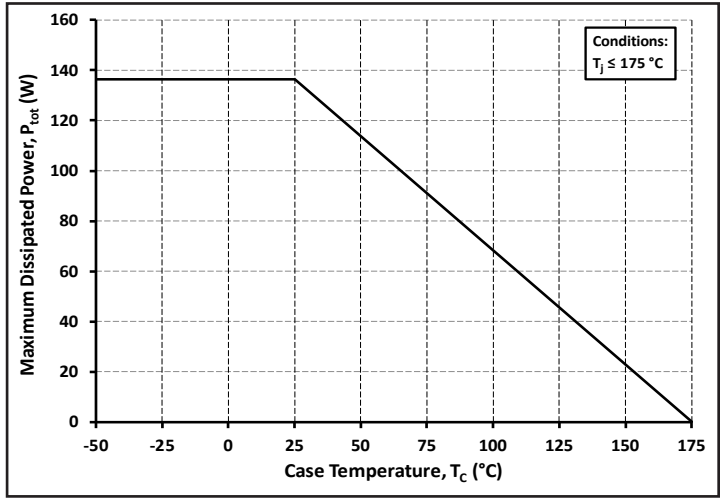


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

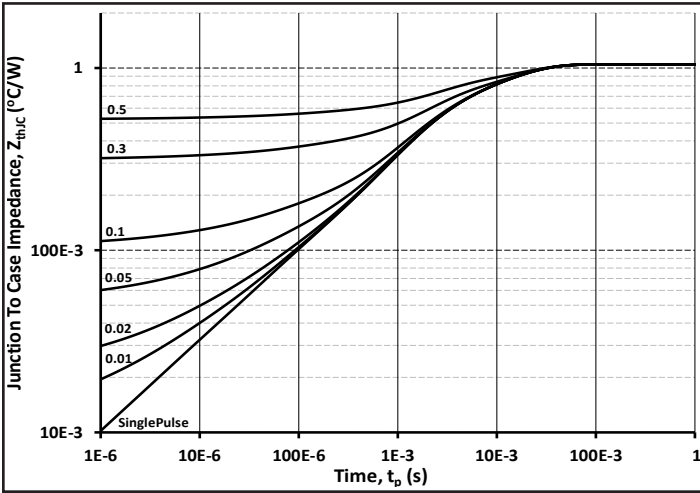


Figure 21. Transient Thermal Impedance (Junction - Case)

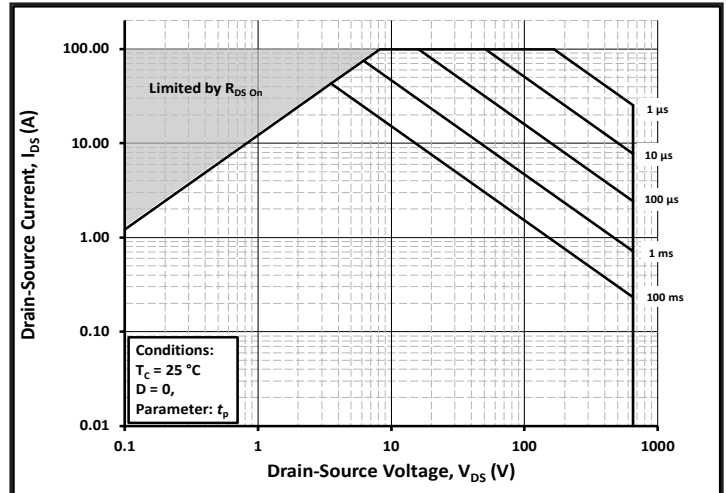


Figure 22. Safe Operating Area

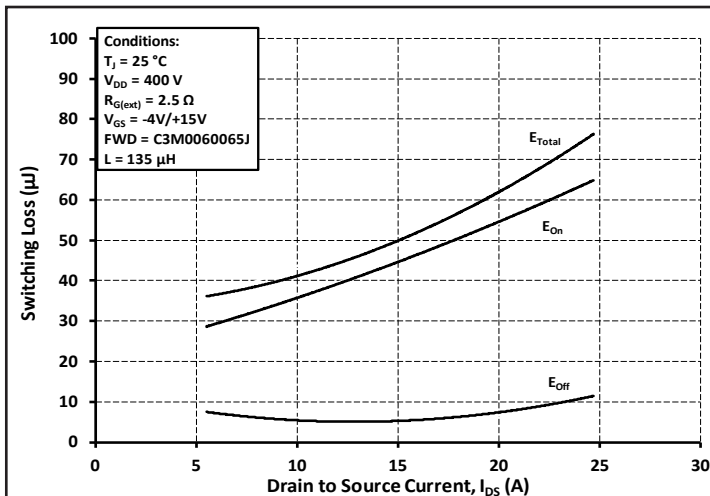


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

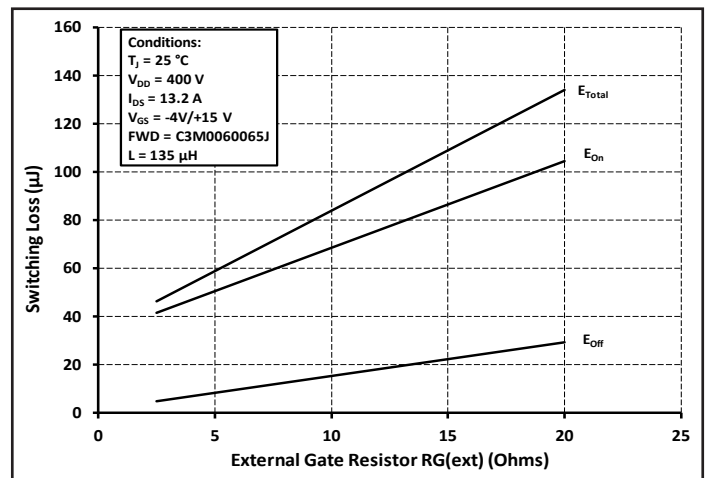


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

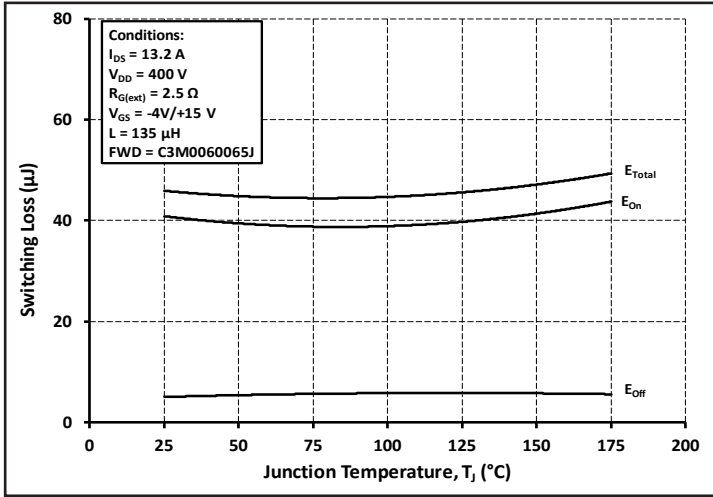


Figure 25. Clamped Inductive Switching Energy vs. Temperature

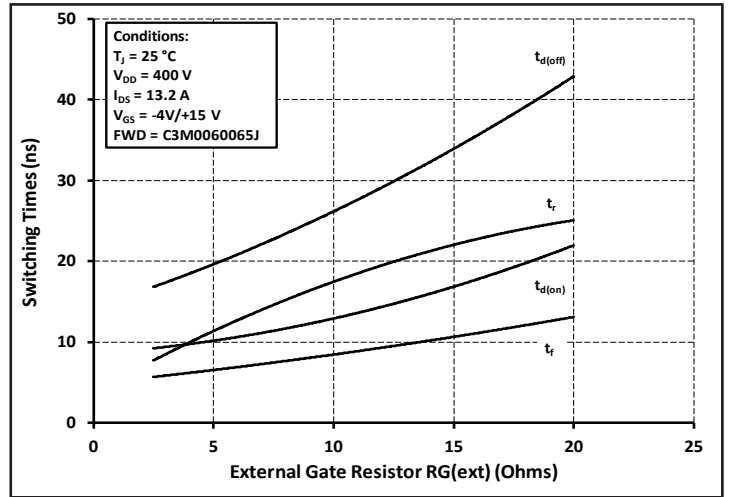


Figure 26. Switching Times vs. $R_{G(ext)}$

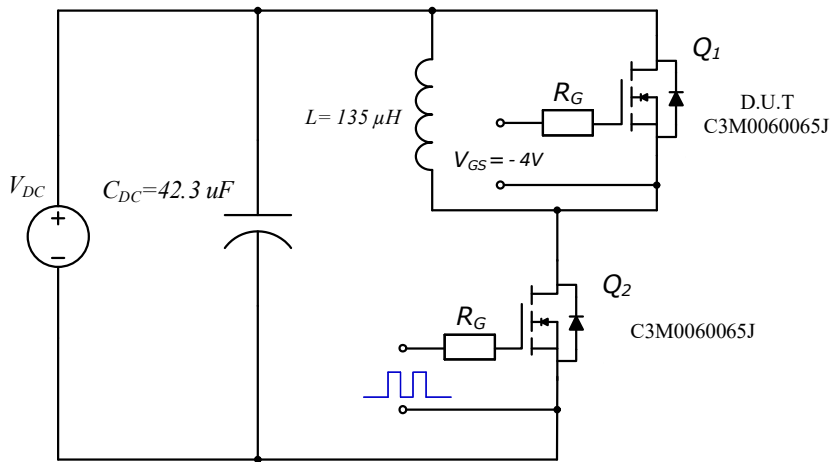


Figure 27. Clamped Inductive Switching Waveform Test Circuit

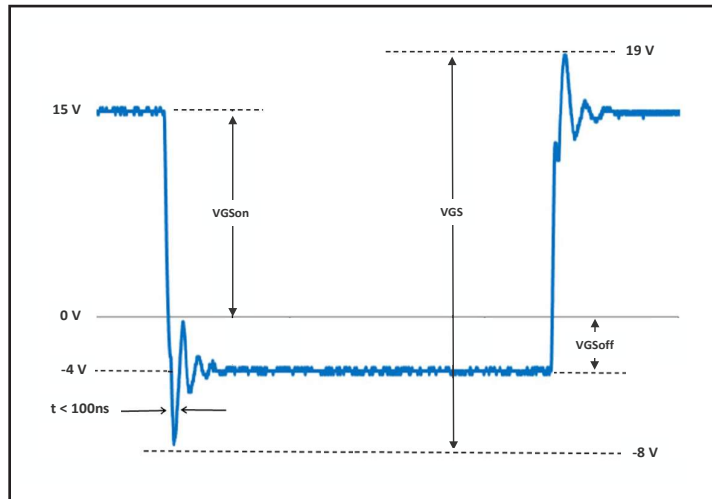
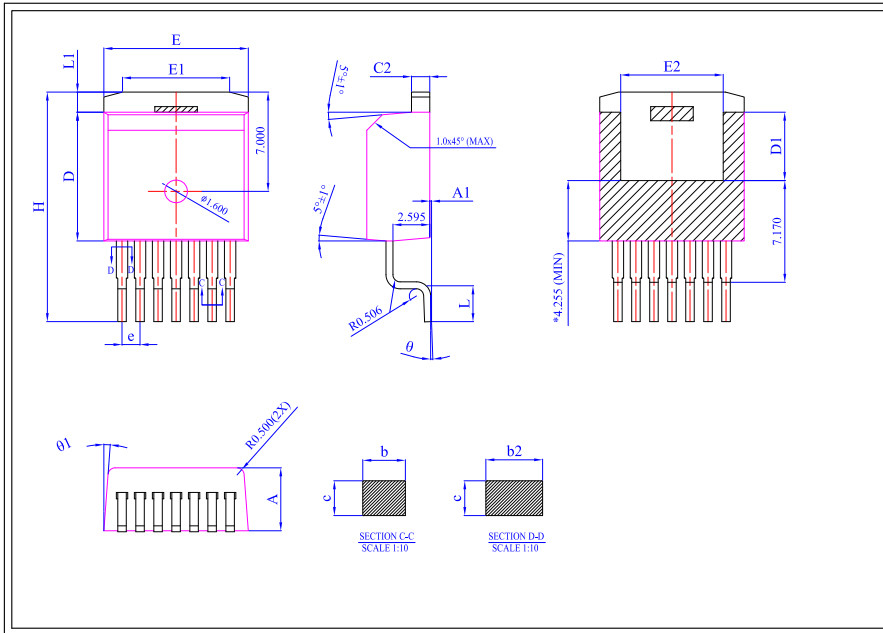


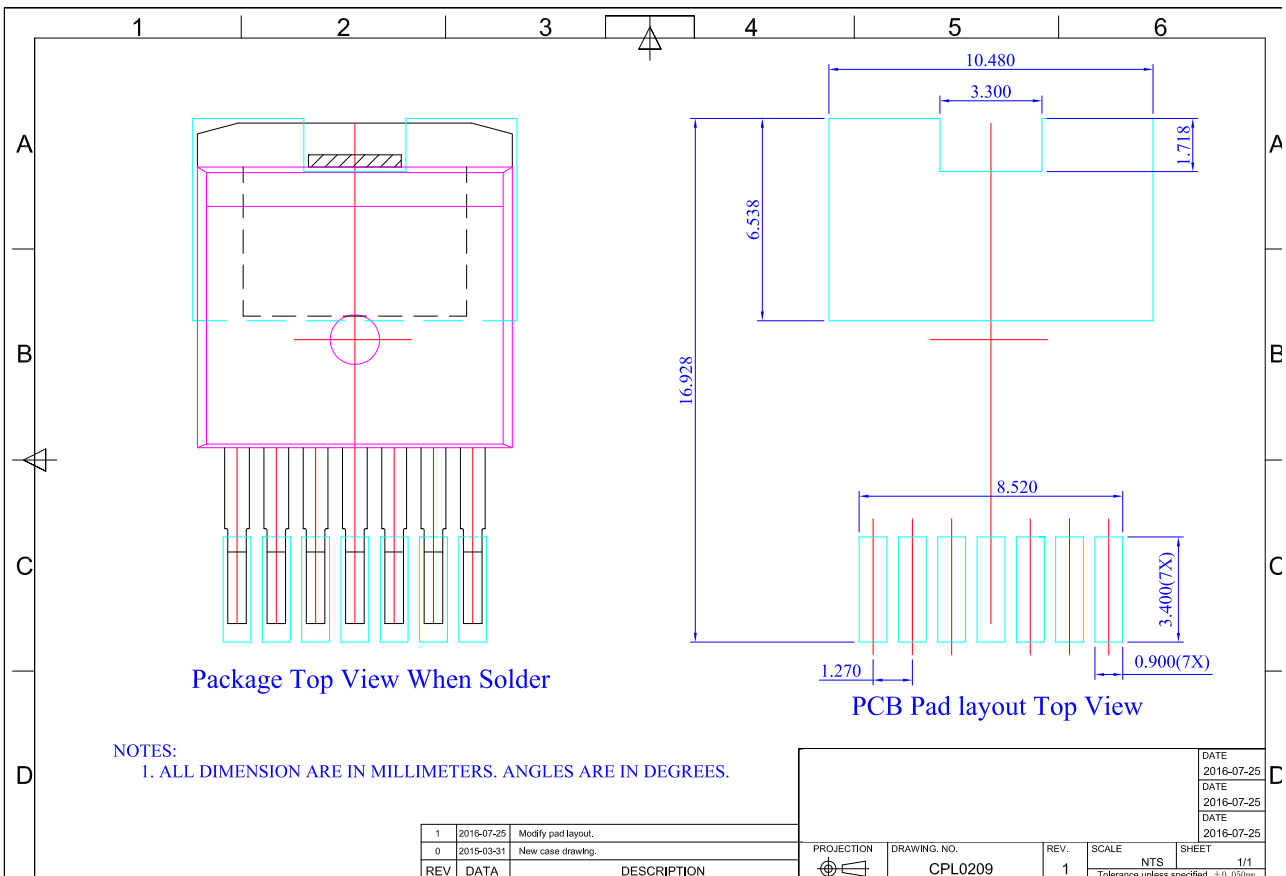
Figure 28. V_{GS} Waveform Example

Package Dimensions

Package 7L D2PAK



Dim	All Dimensions in Millimeters		
	Min	typ	Max
A	4.300	4.435	4.570
A1	0.00	0.125	0.25
b	0.500	0.600	0.700
b2	0.600	0.800	1.000
c	0.330	0.490	0.650
C2	1.170	1.285	1.400
D	9.025	9.075	9.125
D1	4.700	4.800	4.900
E	10.130	10.180	10.230
E1	6.500	7.550	8.600
E2	6.778	7.223	7.665
e	1.27		
H	15.043	16.178	17.313
L	2.324	2.512	2.700
L1	0.968	1.418	1.868
Ø	0°	4°	8°
Ø1	4.5°	5°	5.5°



NOTES:
1. ALL DIMENSION ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

REV	DATA	DESCRIPTION
1	2016-07-25	Modify pad layout.
0	2015-03-31	New case drawing.



PROJECTION
DRAWING NO.
CPL0209

REV.
1

SCALE
NTS
Tolerance unless specified ±0.050mm

DATE
2016-07-25
DATE
2016-07-25
DATE
2016-07-25

SHEET
1/1