

C3M0075120J

Silicon Carbide Power MOSFET

C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Low impedance package with driver source pin
- 7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Benefits

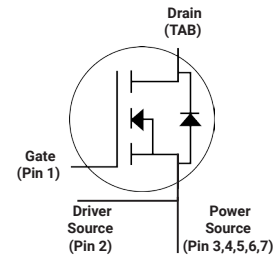
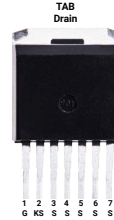
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch Mode Power Supplies

V_{DS}	1200 V
$I_D @ 25^\circ\text{C}$	30 A
$R_{DS(on)}$	75 m Ω

Package



Part Number	Package	Marking
C3M0075120J	TO-263-7	C3M0075120J

Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
V_{GSmax}	Gate - Source Voltage (dynamic)	-8/+19	V	AC ($f > 1\text{ Hz}$)	Note: 1
V_{GSop}	Gate - Source Voltage (static)	-4/+15	V	Static	Note: 2
I_D	Continuous Drain Current	30	A	$V_{GS} = 15\text{ V}, T_C = 25^\circ\text{C}$	Fig. 19
		19.7		$V_{GS} = 15\text{ V}, T_C = 100^\circ\text{C}$	
$I_{D(pulse)}$	Pulsed Drain Current	80	A	Pulse width t_p limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	113.6	W	$T_C = 25^\circ\text{C}, T_J = 150^\circ\text{C}$	Fig. 20
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$		
T_L	Solder Temperature	260	$^\circ\text{C}$	1.6mm (0.063") from case for 10s	

Note (1): When using MOSFET Body Diode $V_{GSmax} = -4\text{V}/+19\text{V}$

Note (2): MOSFET can also safely operate at $0/+15\text{ V}$

Electrical Characteristics (T_c = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V _{(BR)DSS}	Drain-Source Breakdown Voltage	1200			V	V _{GS} = 0 V, I _D = 100 μA	
V _{GS(th)}	Gate Threshold Voltage	1.8	2.5	3.6	V	V _{DS} = V _{GS} , I _D = 5 mA	Fig. 11
			2.2		V	V _{DS} = V _{GS} , I _D = 5 mA, T _J = 150°C	
I _{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V _{DS} = 1200 V, V _{GS} = 0 V	
I _{GSS}	Gate-Source Leakage Current		10	250	nA	V _{GS} = 15 V, V _{DS} = 0 V	
R _{DS(on)}	Drain-Source On-State Resistance		75	90	mΩ	V _{GS} = 15 V, I _D = 20 A	Fig. 4, 5, 6
			100			V _{GS} = 15 V, I _D = 20 A, T _J = 150°C	
g _{fs}	Transconductance		12		S	V _{DS} = 20 V, I _{DS} = 20 A	Fig. 7
			13			V _{DS} = 20 V, I _{DS} = 20 A, T _J = 150°C	
C _{iss}	Input Capacitance		1390		pF	V _{GS} = 0 V, V _{DS} = 1000 V f = 1 MHz V _{AC} = 25 mV	Fig. 17, 18
C _{oss}	Output Capacitance		58				
C _{rss}	Reverse Transfer Capacitance		2				
E _{oss}	C _{oss} Stored Energy		33		μJ		Fig. 16
E _{ON}	Turn-On Switching Energy (Body Diode FWD)		200		μJ	V _{DS} = 800 V, V _{GS} = -4 V/15 V, I _D = 20 A, R _{G(ext)} = 0 Ω, L = 156 μH, T _J = 150°C	Fig. 26, 29
E _{OFF}	Turn-Off Switching Energy (Body Diode FWD)		90				
t _{d(on)}	Turn-On Delay Time		7		ns	V _{DD} = 800 V, V _{GS} = -4 V/15 V I _D = 20 A, R _{G(ext)} = 0 Ω, Timing relative to V _{DS} Inductive load	Fig. 27, 28, 29
t _r	Rise Time		15				
t _{d(off)}	Turn-Off Delay Time		24				
t _f	Fall Time		8				
R _{G(int)}	Internal Gate Resistance		9		Ω	f = 1 MHz, V _{AC} = 25 mV	
Q _{gs}	Gate to Source Charge		18		nC	V _{DS} = 800 V, V _{GS} = -4 V/15 V I _D = 20 A Per IEC60747-8-4 pg 21	Fig. 12
Q _{gd}	Gate to Drain Charge		12				
Q _g	Total Gate Charge		48				

Reverse Diode Characteristics (T_c = 25°C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V _{SD}	Diode Forward Voltage	4.5		V	V _{GS} = -4 V, I _{SD} = 10 A	Fig. 8, 9, 10
		4.0		V	V _{GS} = -4 V, I _{SD} = 10 A, T _J = 150 °C	
I _S	Continuous Diode Forward Current		22.4	A	V _{GS} = -4 V	Note 1
I _{S, pulse}	Diode pulse Current	80		A	V _{GS} = -4 V, pulse width t _p limited by T _{Jmax}	Note 1
t _{rr}	Reverse Recover time	25		ns	V _{GS} = -4 V, I _{SD} = 20 A, V _R = 800 V dif/dt = 1925 A/μs, T _J = 25 °C	Note 1, Fig. 29
Q _{rr}	Reverse Recovery Charge	109		nC		
I _{rrm}	Peak Reverse Recovery Current	11		A		

Thermal Characteristics

Symbol	Parameter	Max.	Unit	Test Conditions	Note
R _{θJC}	Thermal Resistance from Junction to Case	1.1	°C/W		Fig. 21
R _{θJA}	Thermal Resistance From Junction to Ambient	40			

Typical Performance

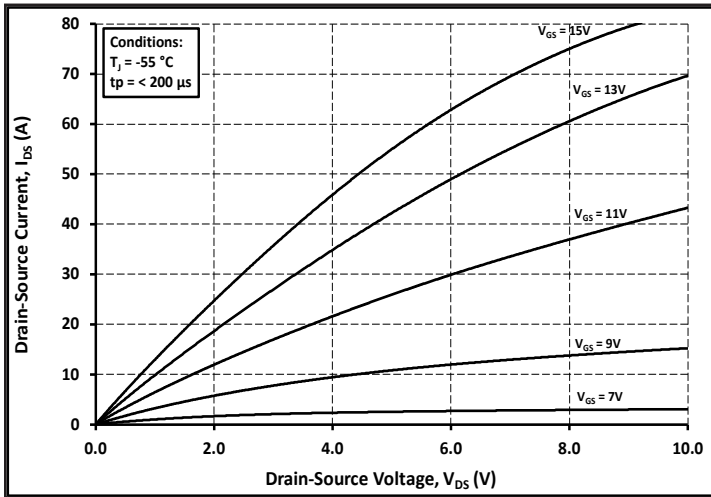


Figure 1. Output Characteristics $T_J = -55\text{ }^\circ\text{C}$

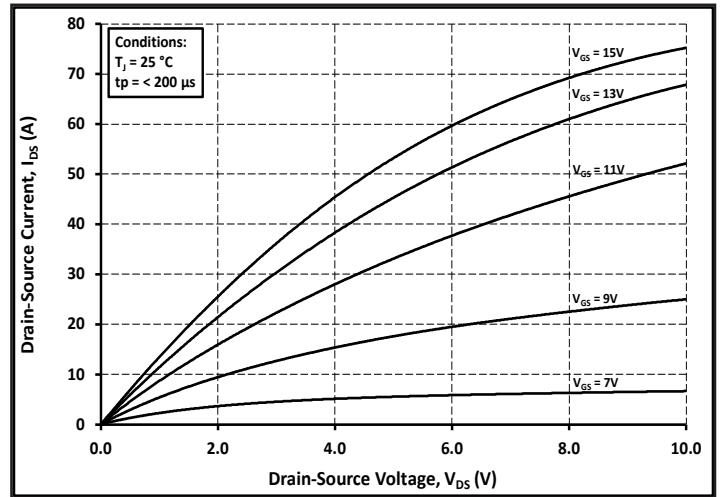


Figure 2. Output Characteristics $T_J = 25\text{ }^\circ\text{C}$

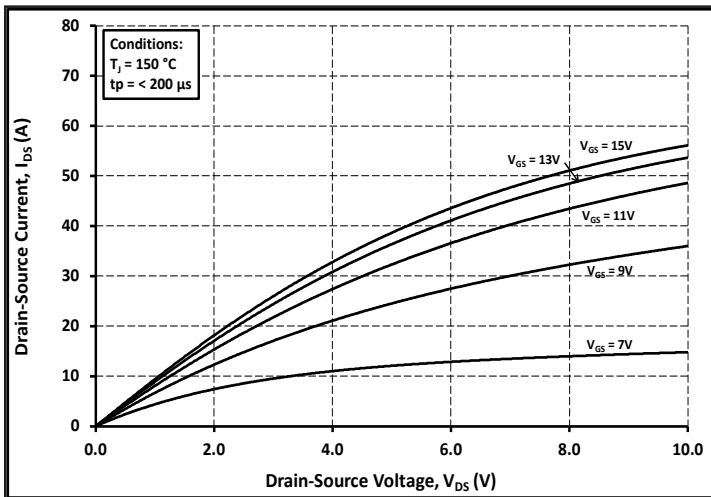


Figure 3. Output Characteristics $T_J = 150\text{ }^\circ\text{C}$

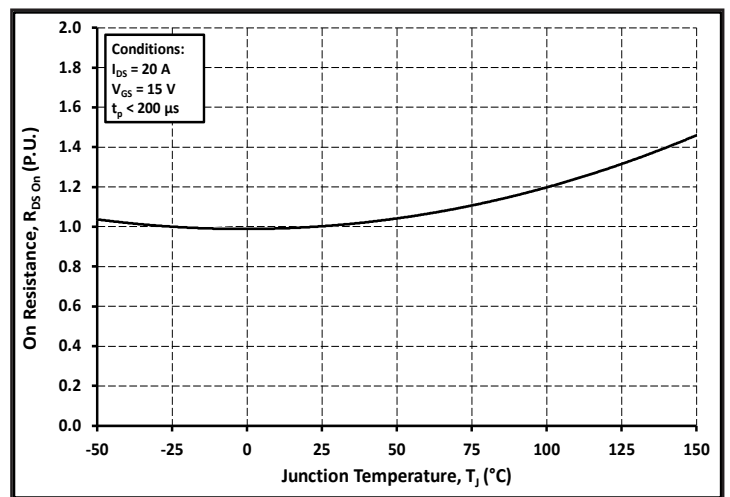


Figure 4. Normalized On-Resistance vs. Temperature

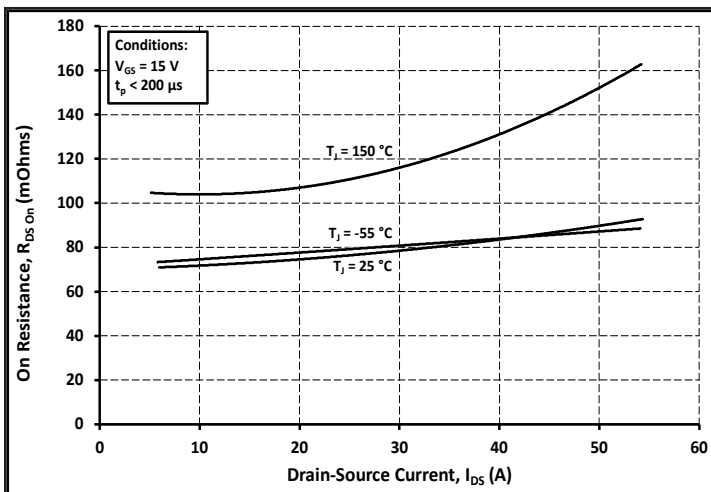


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

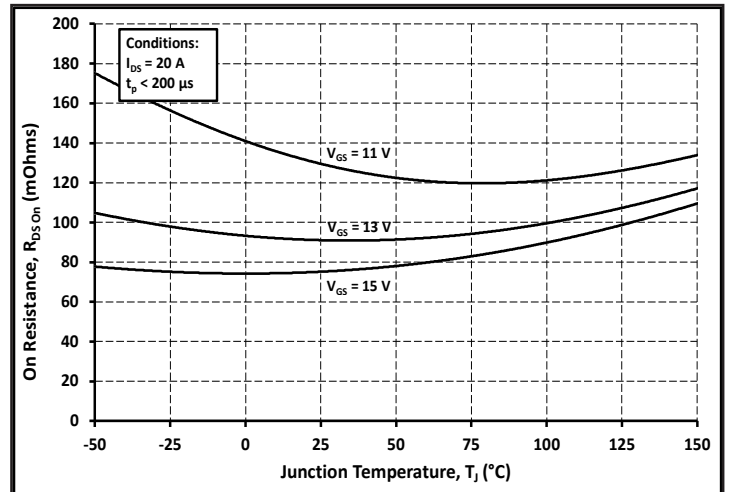


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

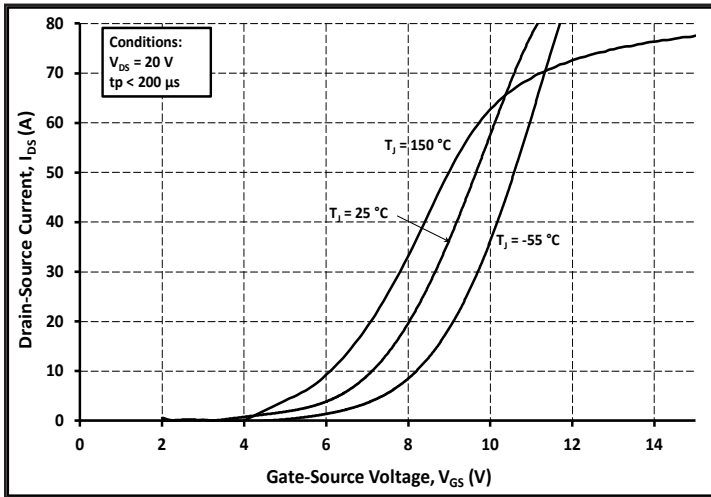


Figure 7. Transfer Characteristic for Various Junction Temperatures

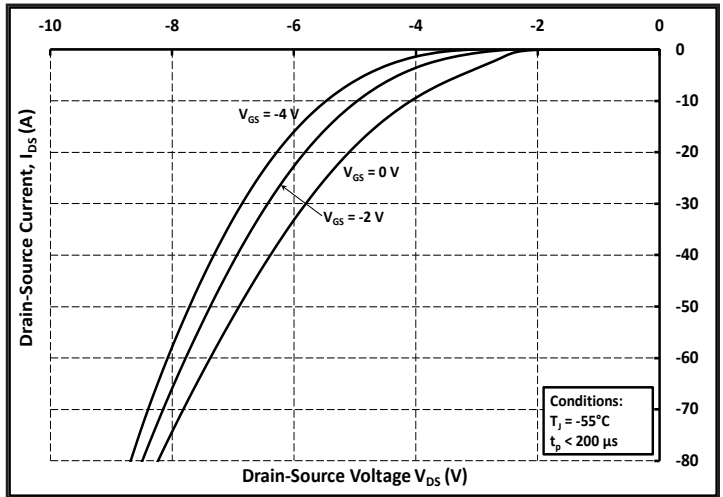


Figure 8. Body Diode Characteristic at $-55\text{ }^\circ\text{C}$

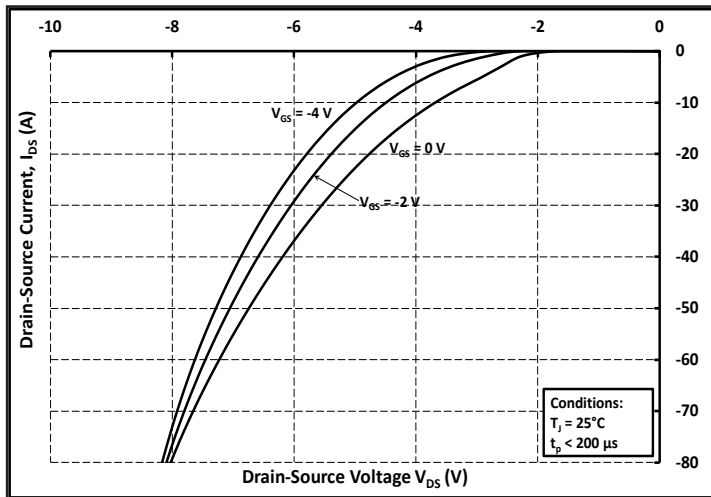


Figure 9. Body Diode Characteristic at $25\text{ }^\circ\text{C}$

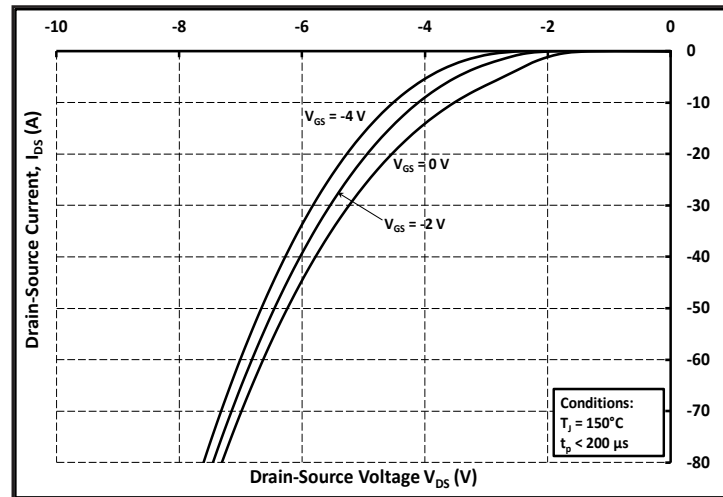


Figure 10. Body Diode Characteristic at $150\text{ }^\circ\text{C}$

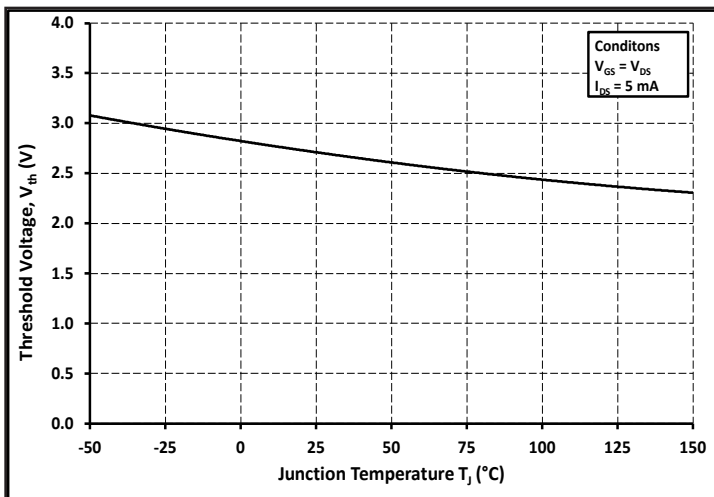


Figure 11. Threshold Voltage vs. Temperature

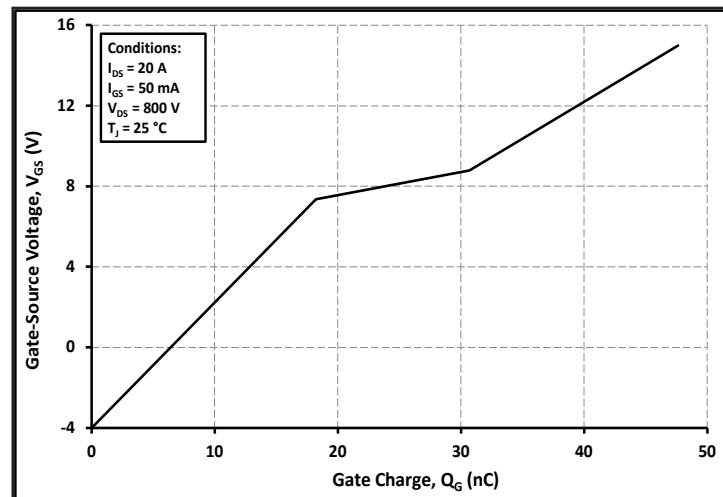


Figure 12. Gate Charge Characteristics

Typical Performance

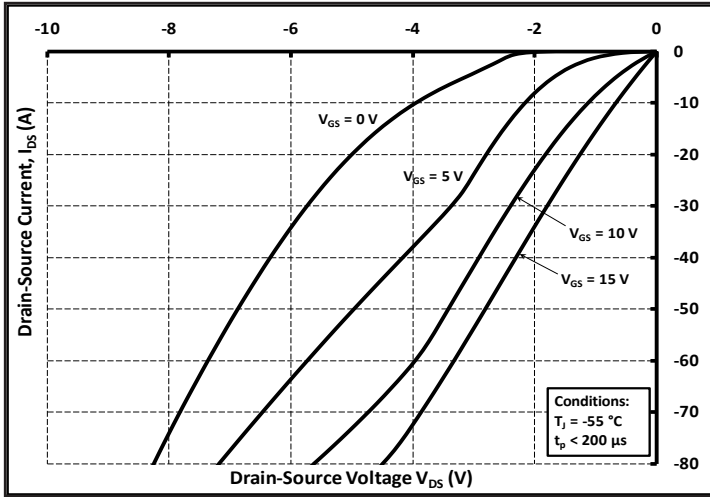


Figure 13. 3rd Quadrant Characteristic at -55 °C

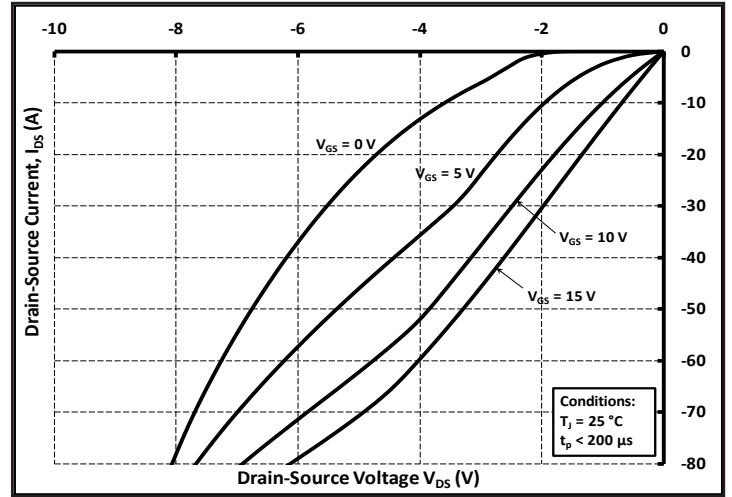


Figure 14. 3rd Quadrant Characteristic at 25 °C

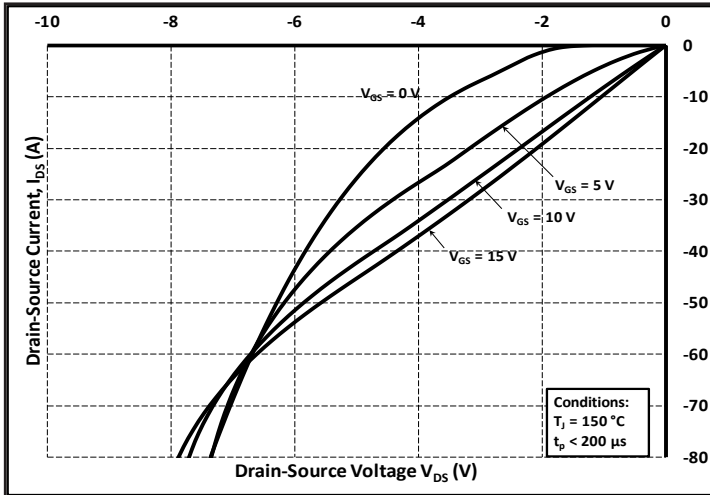


Figure 15. 3rd Quadrant Characteristic at 150 °C

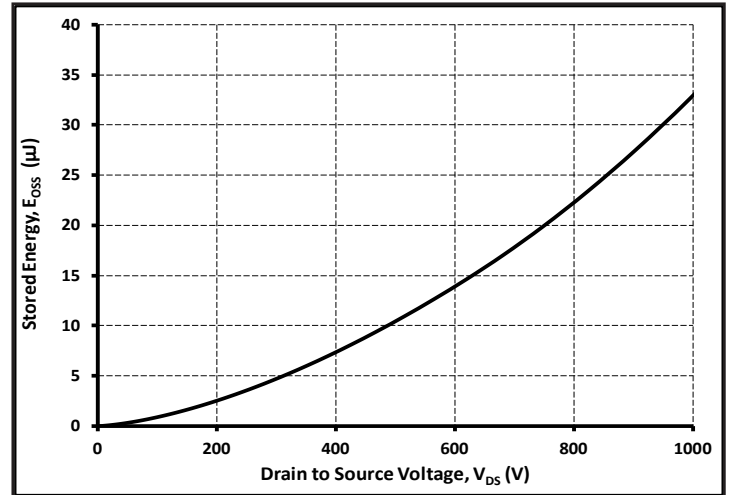


Figure 16. Output Capacitor Stored Energy

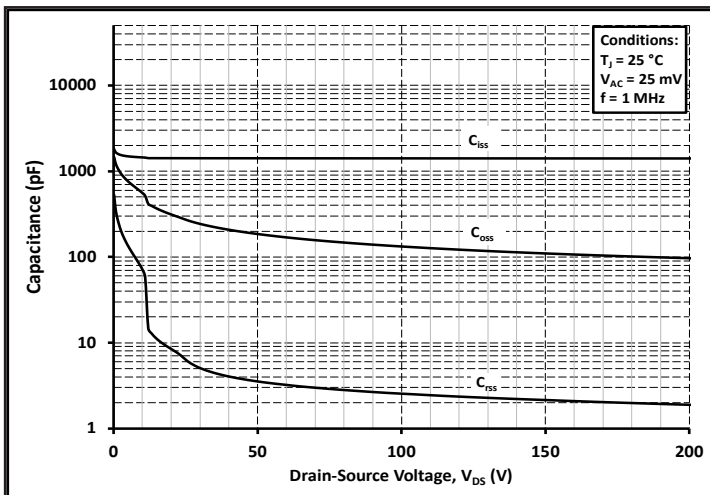


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

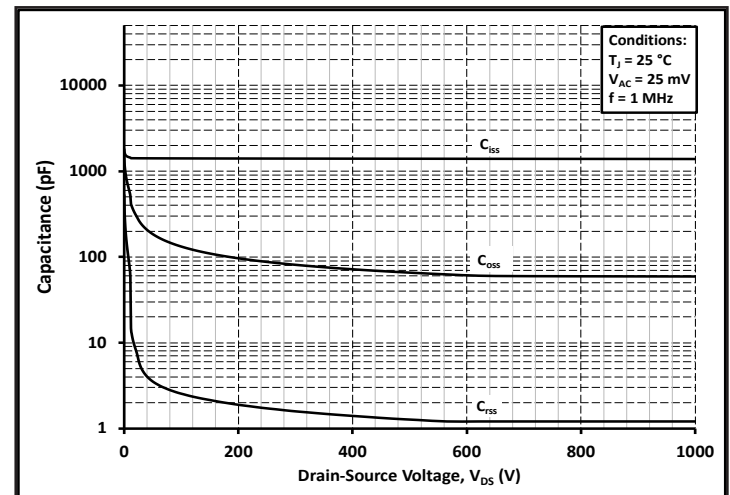


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000V)

Typical Performance

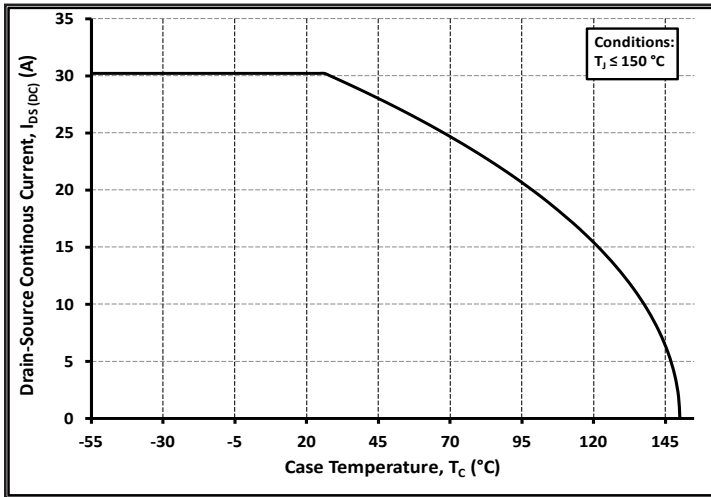


Figure 19. Continuous Drain Current Derating vs. Case Temperature

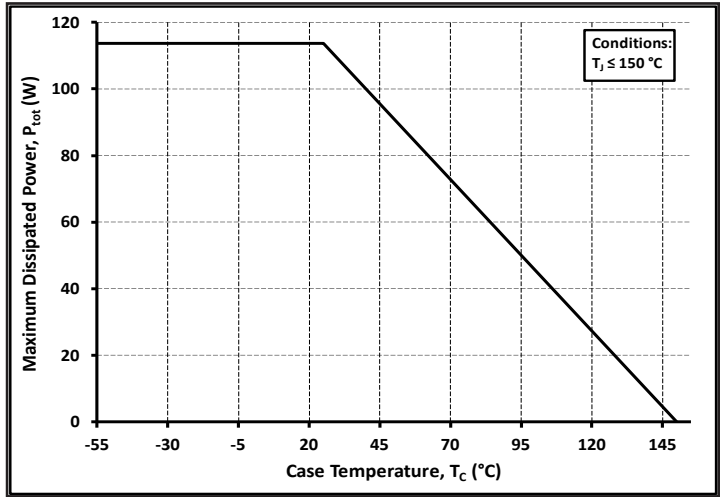


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

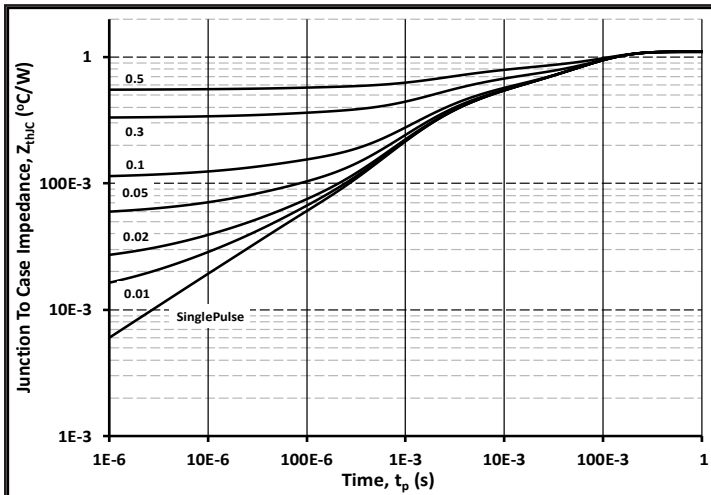


Figure 21. Transient Thermal Impedance (Junction - Case)

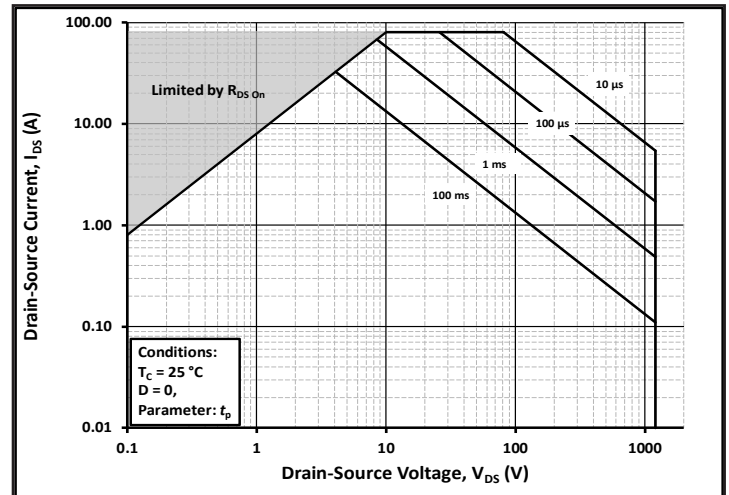


Figure 22. Safe Operating Area

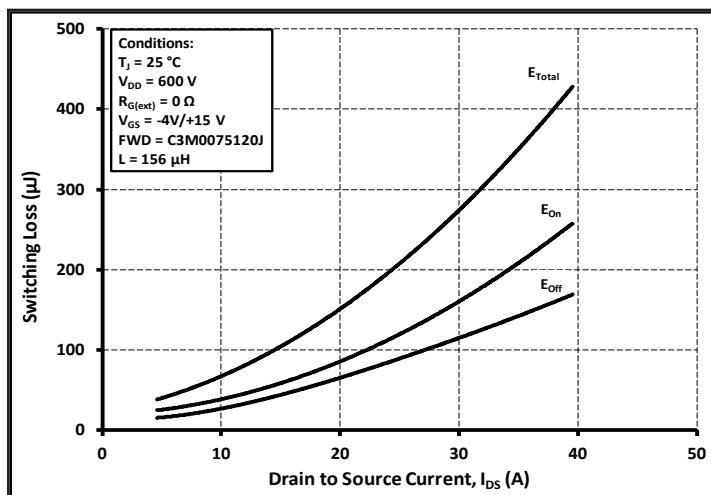


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600V$)

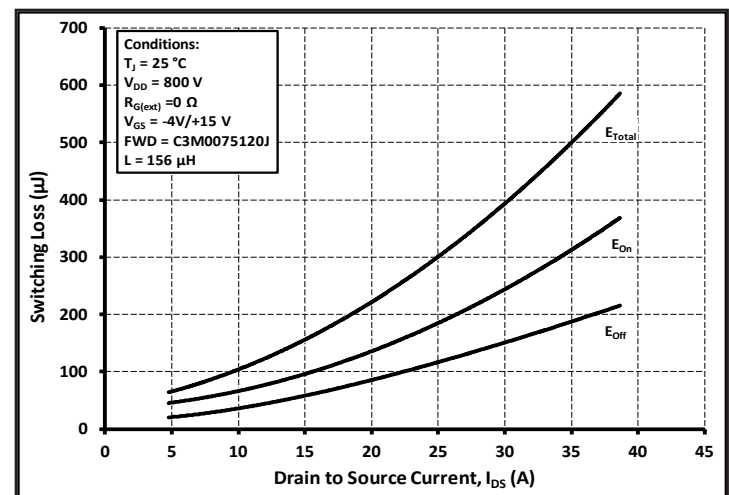


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800V$)

Typical Performance

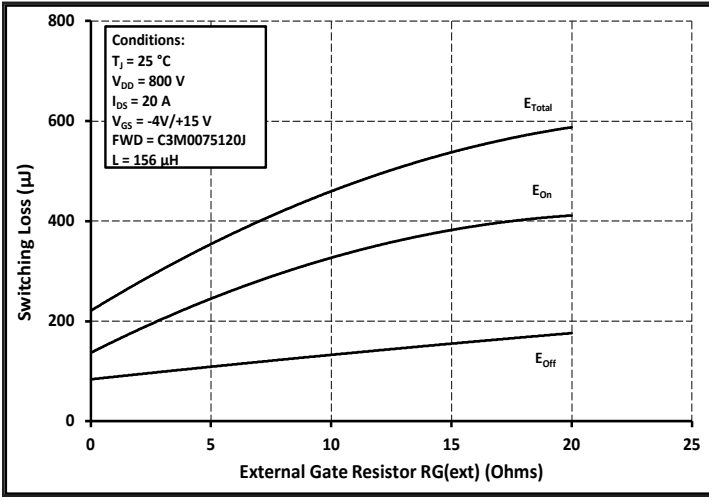


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

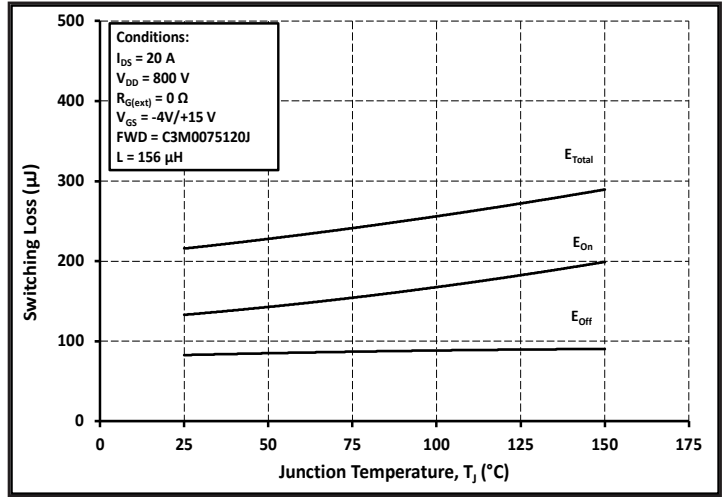


Figure 26. Clamped Inductive Switching Energy vs. Temperature

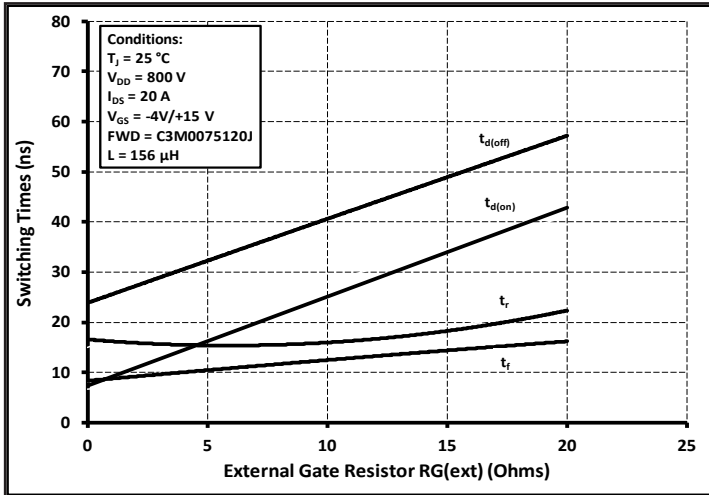


Figure 27. Switching Times vs. $R_{G(ext)}$

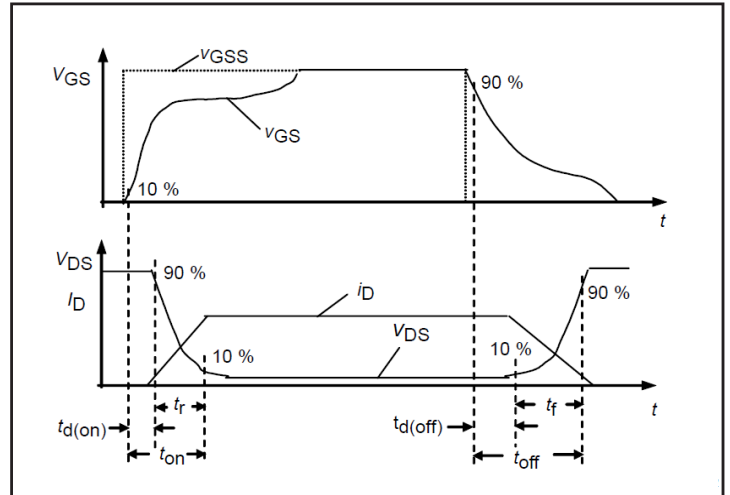


Figure 28. Switching Times Definition

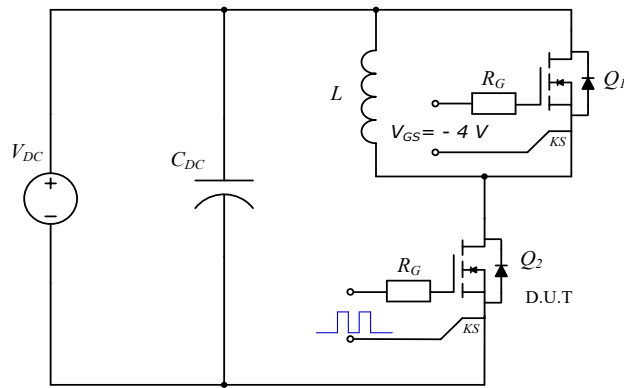
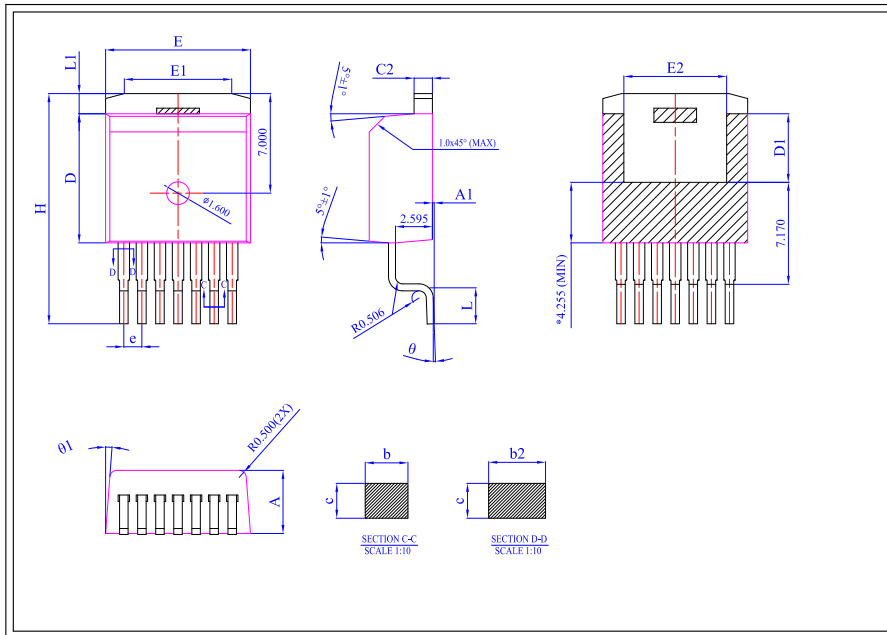


Figure 29. Clamped Inductive Switching
Waveform Test Circuit

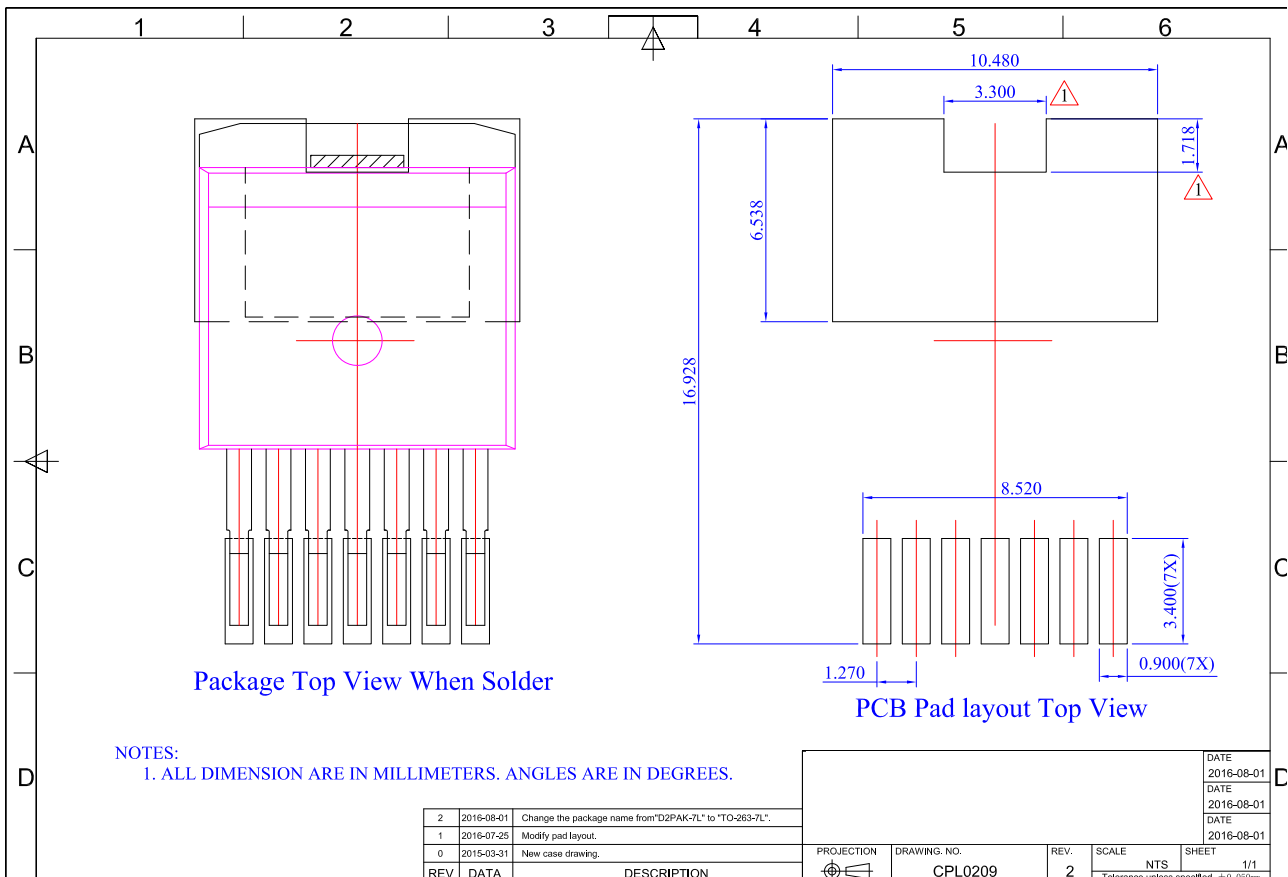
Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

Package Dimensions

Package 7L D2PAK




Dim	All Dimensions in Millimeters		
	Min	typ	Max
A	4.300	4.435	4.570
A1	0.00	0.125	0.25
b	0.500	0.600	0.700
b2	0.600	0.800	1.000
c	0.330	0.490	0.650
C2	1.170	1.285	1.400
D	9.025	9.075	9.125
D1	4.700	4.800	4.900
E	10.130	10.180	10.230
E1	6.500	7.550	8.600
E2	6.778	7.223	7.665
e	1.27		
H	15.043	16.178	17.313
L	2.324	2.512	2.700
L1	0.968	1.418	1.868
Ø	0°	4°	8°
Ø1	4.5°	5°	5.5°



NOTES:
1. ALL DIMENSION ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

REV	DATA	DESCRIPTION
2	2016-08-01	Change the package name from "D2PAK-7L" to "TO-263-7L".
1	2016-07-25	Modify pad layout.
0	2015-03-31	New case drawing.

PROJECTION	DRAWING NO.	REV.	SCALE	SHEET
	CPL0209	2	NTS	1/1
Tolerance unless specified ±0.050mm				