C8051F410-GDI

Tested Flash MCU Die in Wafer Form

Analog Peripherals
- **12-Bit ADC**
  - ±1 LSB INL; no missing codes
  - Programmable throughput up to 200 ksps
  - Up to 24 external inputs
  - Data dependent windowed interrupt generator
  - Built-in temperature sensor (±3 °C)
- **Two 12-Bit Current Mode DACs**
- **Two Comparators**
  - Programmable hysteresis and response time
  - Configurable as wake-up or reset source
- **POR/Brownout Detector**
- **Voltage Reference—1.5, 2.2 V (programmable)**

On-Chip Debug
- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

Supply Voltage 2.0 to 5.25 V
- Built-in LDO regulator: 2.1 or 2.5 V

High Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- Expanded interrupt handler

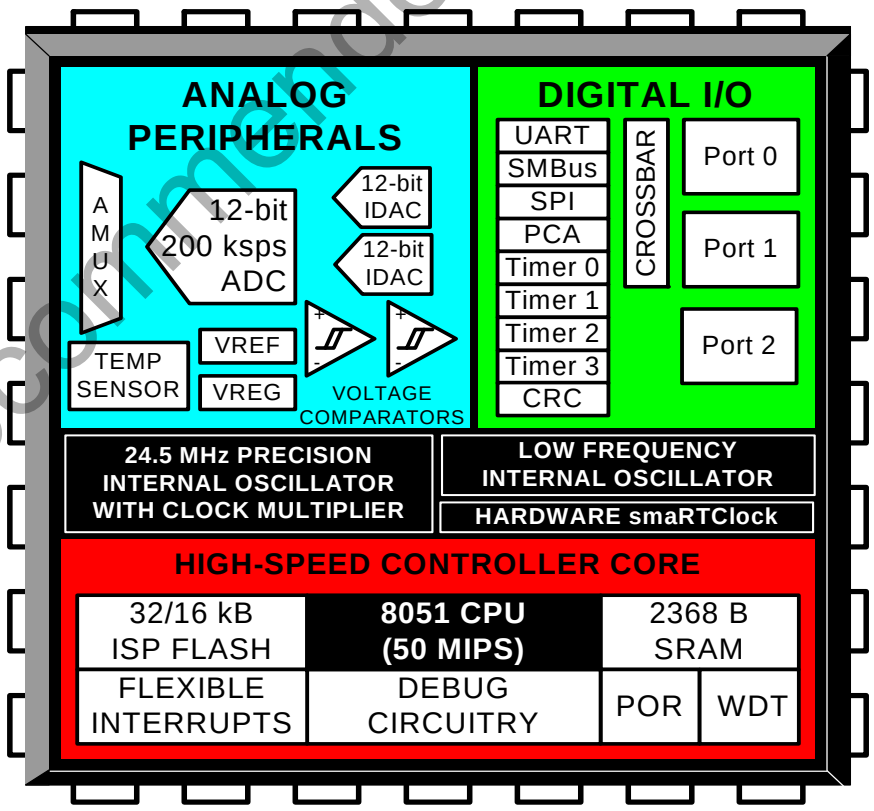
Memory
- 2304 bytes internal data RAM (256 + 2048)
- 32/16 kB Flash; In-system programmable in 512 byte sectors
- 64 bytes battery-backed RAM (smaRTClock)

Digital Peripherals
- 24 port I/O; push-pull or open-drain, up to 5.25 V tolerance
- Hardware SMBus™ (I2C™ Compatible), SPI™, and UART serial ports available concurrently
- Four general purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- Hardware smaRTClock operates down to 1 V with 64 bytes battery-backed RAM and backup voltage regulator

Clock Sources
- Internal oscillators: 24.5 MHz 2% accuracy supports UART operation; clock multiplier up to 50 MHz
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- smaRTClock oscillator: 32 kHz Crystal or self-resonant oscillator
- Can switch between clock sources on-the-fly

Temperature Range: –40 to +85 °C

Full Technical Data Sheet
- C8051F410/1/2/3



1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (Bytes)	SmaRTClock Real Time Clock	SMBus/I^2C	UART	SPI	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	12-Bit ADC	Two 12-bit Current Output DACs	Internal Voltage Reference	Temperature Sensor	Analog Comparators	Lead-Free (RoHS-Compliant)	Package	Wafer Thickness
C8051F410-GDI	50	32	2368	✓	1	1	1	4	✓	24	✓	✓	10	✓	1	✓	Tested Die in Wafer Form	12 mil
C8051F410-G1DI	50	32	2368	✓	1	1	1	4	✓	24	✓	✓	10	✓	1	✓	Tested Die in Wafer Form	No back-grind

2. Pin Definitions

Table 2.1 lists the pin definitions for the C8051F410-GDI. For a full description of each pin, refer to the C8051F410/1/2/3 data sheet.

Table 2.1. Pin Definitions for C8051F410-GDI

Name	Physical Pad Number	Type	Description
V_{DD}	10, 11		Core Supply Voltage.
V_{IO}	1, 41		I/O Supply Voltage.
GND	8, 9		Ground.
$V_{RTC-BACKUP}$	5		SmaRTClock Backup Supply Voltage.
V_{REGIN}	12, 13		On-Chip Voltage Regulator Input.
$\overline{RST}$/ C2CK	2	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. A 1 kΩ pullup to V_{IO} is recommended. Clock signal for the C2 Debug Interface.
P2.7/ C2D	39	D I/O D I/O	Port 2.7. Bi-directional data signal for the C2 Debug Interface.
XTAL3	7	A In	smaRTClock Oscillator Crystal Input.
XTAL4	6	A Out	smaRTClock Oscillator Crystal Input.
P0.0/ IDAC0	23	D I/O or A In A Out	Port 0.0. IDAC0 Output.
P0.1/ IDAC1	24	D I/O or A In A Out	Port 0.1. IDAC1 Output.
P0.2	25	D I/O or A In	Port 0.2.
P0.3	26	D I/O or A In	Port 0.3.

Table 2.1. Pin Definitions for C8051F410-GDI (Continued)

Name	Physical Pad Number	Type	Description
P0.4/ TX	27	D I/O or A In D Out	Port 0.4. UART TX Pin.
P0.5/ RX	28	D I/O or A In D In	Port 0.5. UART RX Pin.
P0.6/ CNVSTR	29	D I/O or A In D In	Port 0.6. External Convert Start Input for ADC0, IDA0, and IDA1.
P0.7	30	D I/O or A In	Port 0.7.
P1.0/ XTAL1	14	D I/O or A In A In	Port 1.0. External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P1.1/ XTAL2	15	D I/O or A In A O or D In	Port 1.1. External Clock Output. This pin is the excitation driver for an external crystal or resonator, or an external clock input for CMOS, capacitor, or RC oscillator configurations.
P1.2 V_{REF}	16	D I/O or A In A In	Port 1.2. External V_{REF} Input.
P1.3	17	D I/O or A In	Port 1.3.
P1.4	18	D I/O or A In	Port 1.4.
P1.5	19	D I/O or A In	Port 1.5.
P1.6	20	D I/O or A In	Port 1.6.
P1.7	21	D I/O or A In	Port 1.7.

Table 2.1. Pin Definitions for C8051F410-GDI (Continued)

Name	Physical Pad Number	Type	Description
P2.0	31	D I/O or A In	Port 2.0.
P2.1	32	D I/O or A In	Port 2.1.
P2.2	33	D I/O or A In	Port 2.2.
P2.3	34	D I/O or A In	Port 2.3.
P2.4	36	D I/O or A In	Port 2.4.
P2.5	37	D I/O or A In	Port 2.5.
P2.6	38	D I/O or A In	Port 2.6.

3. Bonding Instructions

Table 3.1. Bond Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (LQFP32)	Package Pin Name	Physical Pad X (um)	Physical Pad Y (um)
1	1	VIO	-1099.49	1063.135
2	2	\RST/C2CK	-1099.49	923.875
3	NA	Reserved*	-1099.49	794.055
4	NA	Reserved*	-1099.49	719.055
5	3	VRTC-BACKUP	-1099.49	232.125
6	4	XTAL4	-1099.49	42.685
7	5	XTAL3	-1099.49	-97.695
8	6	GND	-1099.49	-230.665
9	6	GND	-1099.49	-344.135
10	7	VDD	-1099.49	-445.735
11	7	VDD	-1099.49	-519.735
12	8	VREGIN	-1099.49	-957.615
13	8	VREGIN	-1099.49	-1031.615
14	9	P1.0/XTAL1	-863.93	-1211.435
15	10	P1.1/XTAL2	-430.55	-1211.435
16	11	P1.2/VREF	-244.03	-1211.435
17	12	P1.3	-76.39	-1211.435
18	13	P1.4	290.13	-1211.435
19	14	P1.5	457.77	-1211.435
20	15	P1.6	644.29	-1211.435
21	16	P1.7	811.93	-1211.435
22	NA	Reserved*	951.19	-1211.435
23	17	P0.0/IDAC0	1099.49	-1001.495
24	18	P0.1/IDAC1	1099.49	-833.855
25	19	P0.2	1099.49	-618.575
26	20	P0.3	1099.49	-450.935
27	21	P0.4/TX	1099.49	450.935
28	22	P0.5/RX	1099.49	618.575
29	23	P0.6/CNVSTR	1099.49	833.855

***Note:** Pins marked “Reserved” should not be connected.

Table 3.1. Bond Pad Coordinates (Relative to Center of Die) (Continued)

30	24	P0.7	1099.49	1001.495
31	25	P2.0	903.93	1211.435
32	26	P2.1	736.29	1211.435
33	27	P2.2	535.39	1211.435
34	28	P2.3	367.75	1211.435
35	NA	Reserved*	-29.77	1211.435
36	29	P2.4	-198.13	1211.435
37	30	P2.5	-365.77	1211.435
38	31	P2.6	-552.29	1211.435
39	32	P2.7/C2D	-719.93	1211.435
40	NA	Reserved*	-859.19	1211.435
41	1	VIO	-951.19	1211.435

***Note:** Pins marked “Reserved” should not be connected.

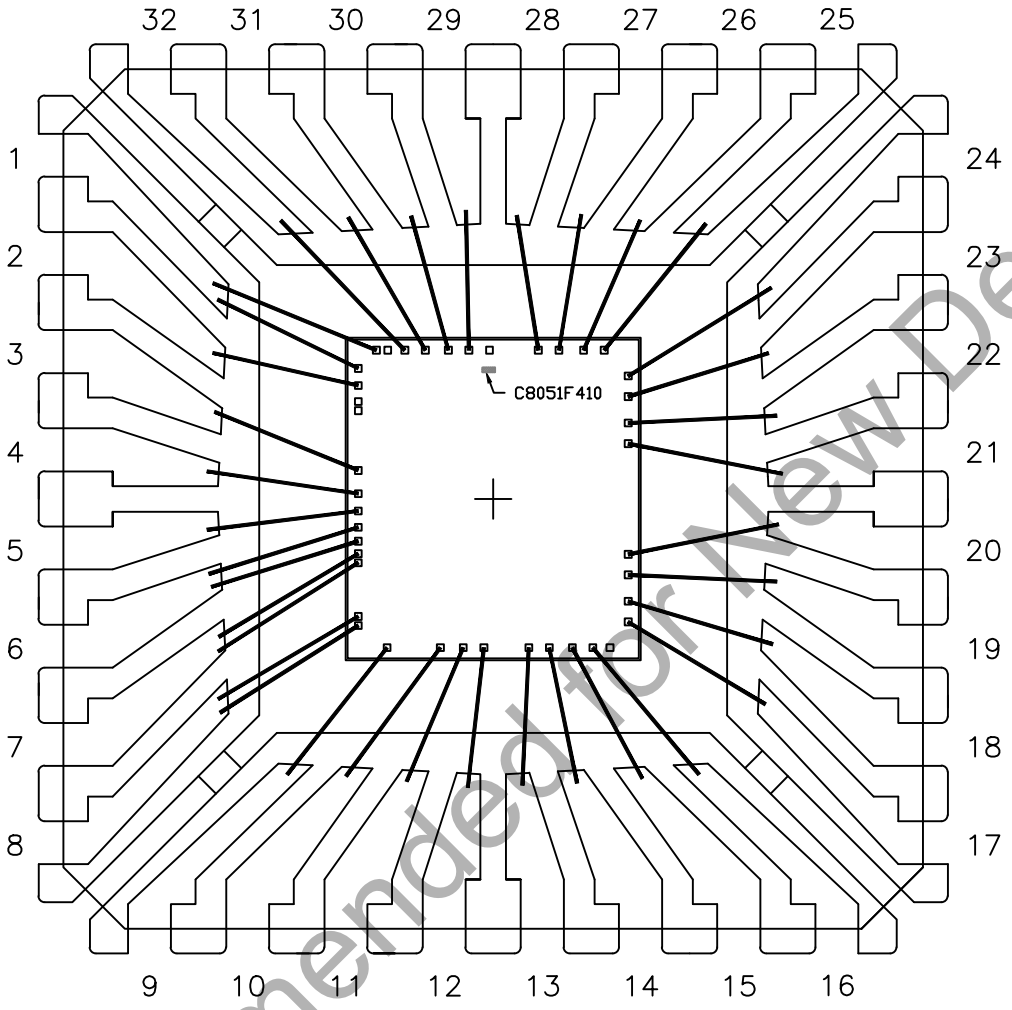


Figure 3.1. Die Bonding (LQFP-32)

Table 3.2. Wafer and Die Information

Wafer Dimensions	8 in
Die Dimensions	2.4 mm x 2.63 mm
Wafer Thickness	12 mil ±1 mil (C8051F410-GDI) No backgrind (C8051F410-G1DI)
Wafer Identification	Notch
Scribe Line Width	80 µm
Die Per Wafer*	Contact Sales for info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 µm x 60 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	75 µm
***Note:** This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

Document Change List

Revision 1.0 to Revision 1.1

- Changed Wafer Packaging Detail to “Wafer Jar” in Table 3.2 on page 9.

Revision 1.1 to Revision 1.2

- Added C8051F410-G1DI option in Table 1.1 and Table 3.2.