C8051F850-GDI

Tested 25 MIPS 8 kB Flash Mixed-Signal MCU Die in Wafer Form

Memory
- Up to 8 kB flash
- Flash is in-system programmable in 512-Byte sectors
- Up to 512 Bytes RAM (256 + 256)

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers

12-Bit Analog-to-Digital Converter
- Up to 16 input channels
- Up to 200 ksps 12-bit mode or 800 ksps 10-bit mode
- Internal VREF or external VREF supported

Internal Low-Power Oscillator
- Calibrated to 24.5 MHz
- Low supply current
- ±2% accuracy over supply and temperature

Internal Low-Frequency Oscillator
- 80 kHz nominal operation
- Low supply current
- Independent clock source for watchdog timer

2 Analog Comparators
- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current

Additional Support Peripherals
- Independent watchdog timer clocked from LFO
- 16-bit CRC engine

High-Speed CIP-51 µC Core
- Efficient, pipelined instruction architecture
- Up to 25 MIPS throughput with 25 MHz clock
- Uses standard 8051 instruction set
- Expanded interrupt handler

General-Purpose I/O
- Up to 18 pins
- 5 V-Tolerant
- Crossbar-enabled

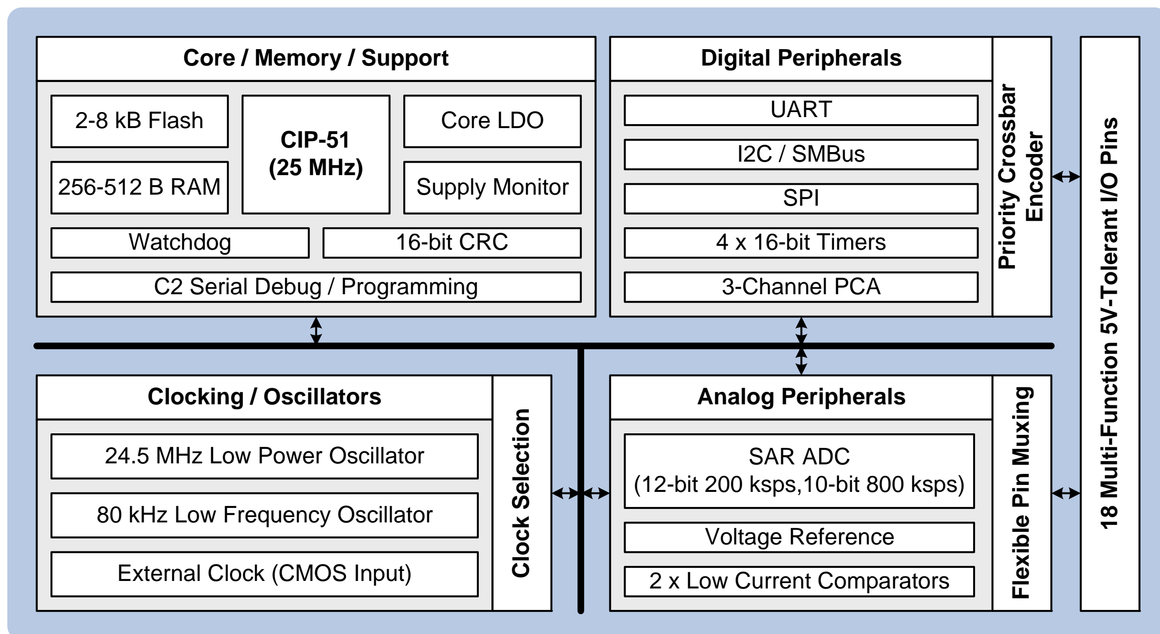
Communication Peripherals
- UART
- I^2C / SMBus™
- SPI™

Timer/Counters and PWM
- 4 General-Purpose 16-bit Timer/Counters
- 16-bit programmable counter array (PCA) with three channels of PWM, capture/compare, or frequency output capability, and hardware kill/safe state capability

Temperature Range
- –40 to +85 °C

Supply Voltage
- 2.2 to 3.6 V

Full Technical Data Sheet
- C8051F85x-86x



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1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (Bytes)	RAM (Bytes)	24.5 MHz Internal Oscillator	80 kHz Internal Oscillator	SMBus/I^2C	UART	SPI	Timers (16-bit)	PWM / PCA Channels	Digital Port I/Os (Total)	Number of ADC0 Channels	I/O with Comparator 0/1 Inputs	Wafer Thickness
C8051F850-C-G1DI	25	8k	512	1	1	1	1	1	4	3	18	16	16	28.5433 mil / 725 µm (No backgrind)

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2. Pin Definitions

Table 2.1 lists the pin definitions for the C8051F850-GDI. For a full description of each pin, refer to the C8051F85x-C8051F86x data sheet.

Table 2.1. Pin Definitions for C8051F850-GDI

Pin Name	Type	Pad Number	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	22			
VDD	Power	23			
$\overline{RST}$ / C2CK	Active-low Reset / C2 Debug Clock	24			
P0.0	Standard I/O	21	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0 VREF
P0.1	Standard I/O	20	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1 AGND
P0.2	Standard I/O	19	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
P0.3 / EXTCLK	Standard I/O / External CMOS Clock Input	17	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
P0.4	Standard I/O	16	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CP0P.4 CP0N.4

Table 2.1. Pin Definitions for C8051F850-GDI (Continued)

Pin Name	Type	Pad Number	Crossbar Capability	Additional Digital Functions	Analog Functions
P0.5	Standard I/O	15	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CP0P.5 CP0N.5
P0.6	Standard I/O	13	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP0P.6 CP0N.6
P0.7	Standard I/O	12	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CP0P.7 CP0N.7
P1.0	Standard I/O	11	Yes	P1MAT.0	ADC0.8 CP1P.0 CP1N.0
P1.1	Standard I/O	9	Yes	P1MAT.1	ADC0.9 CP1P.1 CP1N.1
P1.2	Standard I/O	8	Yes	P1MAT.2	ADC0.10 CP1P.2 CP1N.2
P1.3	Standard I/O	6	Yes	P1MAT.3	ADC0.11 CP1P.3 CP1N.3
P1.4	Standard I/O	5	Yes	P1MAT.4	ADC0.12 CP1P.4 CP1N.4
P1.5	Standard I/O	3	Yes	P1MAT.5	ADC0.13 CP1P.5 CP1N.5

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Table 2.1. Pin Definitions for C8051F850-GDI (Continued)

Pin Name	Type	Pad Number	Crossbar Capability	Additional Digital Functions	Analog Functions
P1.6	Standard I/O	2	Yes	P1MAT.6	ADC0.14 CP1P.6 CP1N.6
P1.7	Standard I/O	1	Yes		ADC0.15 CP1P.7 CP1N.7
P2.0 / C2D	Standard I/O / C2 Debug Data	25			
P2.1	Standard I/O	4			

3. Bonding Instructions

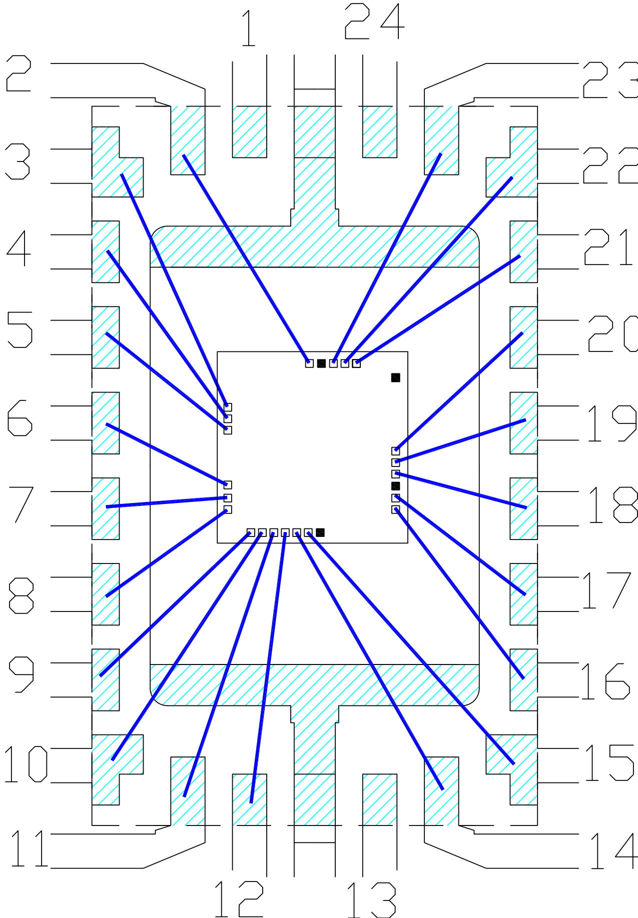

Figure 3.1. Die Bonding Example (QSOP-24)

Table 3.1. Bond Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (QSOP-24)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
1	9	P1.7	–451	–627
2	10	P1.6	–366	–627
3	11	P1.5	–281	–627
5	12	P2.1	–196	–627
6	14	P1.4	–111	–627
7	15	P1.3	–26	–627
4	Reserved*	—	63	–627
8	16	P1.2	622	–456
9	17	P1.1	622	–371
10	Reserved*	—	622	–282
11	18	P1.0	622	–193
12	19	P0.7	622	–108
13	20	P0.6	622	–23
14	Reserved*	—	622	522
15	21	P0.5	331	627
16	22	P0.4	246	627
17	23	P0.3	161	627
18	Reserved*	—	72	627
19	2	P0.2	–17	627
20	3	P0.1	–622	302
21	4	P0.0	–622	217
22	5	GND	–622	132
23	6	VDD	–622	–274
24	7	RST/C2CK	–622	–371
25	8	P2.0/C2D	–622	–456

***Note:** Pins marked “Reserved” should not be connected.

Table 3.2. Wafer and Die Information

Wafer ID	C8051F850C
Wafer Dimensions	8 in
Die Dimensions	1399.94 µm x 1409.22 µm
Wafer Thickness (No backgrind)	28.5433 mil ±1 mil (725 µm)
Wafer Identification	Notch
Scribe Line Width	60 µm
Die Per Wafer*	Contact Sales For Info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	57.12 µm x 57.12 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	75 µm

***Note:** This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).

4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g., nitrogen or clean, dry air).

5. Failure Analysis (FA) Guidelines

Certain conditions must be met for Silicon Laboratories to perform Failure Analysis on devices sold in wafer form.

- In order to conduct failure analysis on a device in a customer-provided package, Silicon Laboratories must be provided with die assembled in an industry standard package that is pin compatible with existing packages Silicon Laboratories offers for the device. Initial response time for FA requests that meet this requirements will follow the standard FA guidelines for packaged parts.
- If retest of the entire wafer is requested, Silicon Laboratories must be provided with the whole wafer. Silicon Laboratories cannot retest any wafers that have been sawed, diced, backgrind or are on tape. Initial response time for FA requests that meet this requirements will be 3 weeks.