1. General description

The CBTD3384 is a dual 5-pole, single-throw bus switch. The device features two output enable inputs ($n\overline{OE}$) that each control five switch channels. The switches are disabled when the associated $n\overline{OE}$ input is HIGH. CBTD3384 is specifically designed for 5 V to 3.3 V level shifting applications. This device is fully specified for partial power down applications using I_{OFE} .

2. Features and benefits

- Designed to be used in 5 V to 3.3 V level shifting applications with internal diode
- 5 Ω switch connection between two ports
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - CDM JESD22-C101C exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

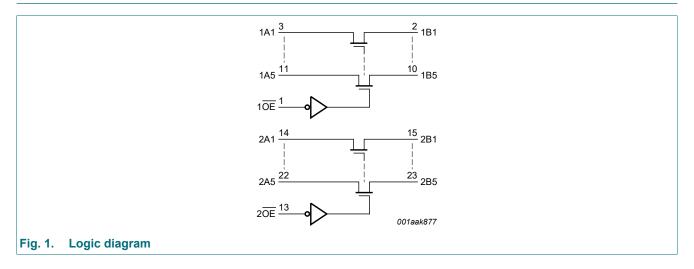
Table 1. Ordering information

Type number	Package	ckage										
	Temperature range	Name	Description	Version								
CBTD3384D	-40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1								
CBTD3384PW	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1								



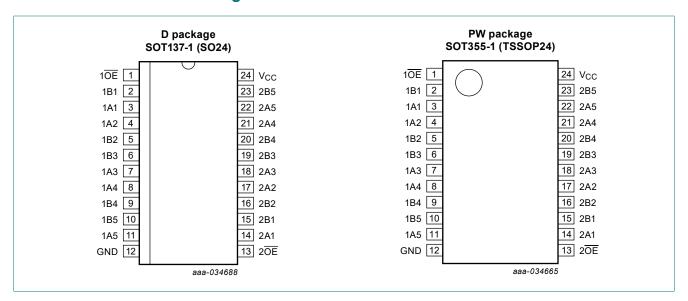
10-bit level shifting bus switch with 5-bit output enables

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description		
10E, 20E	1, 13	output enable input (active LOW)		
1A1, 1A2, 1A3, 1A4, 1A5	3, 4, 7, 8, 11	data input/output (A port)		
2A1, 2A2, 2A3, 2A4, 2A5	14, 17, 18, 21, 22	data input/output (A port)		
1B1, 1B2, 1B3, 1B4, 1B5	2, 5, 6, 9, 10	data input/output (B port)		
2B1, 2B2, 2B3, 2B4, 2B5	15, 16, 19, 20, 23	data input/output (B port)		
GND	12	ground (0 V)		
V _{CC}	24	positive supply voltage		

10-bit level shifting bus switch with 5-bit output enables

6. Functional description

Table 3. Function selection

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ Z = high-impedance \ OFF-state.$

Input		Input/output				
1 OE	2 OE	1An, 1Bn	2An, 2Bn			
L	L	1An = 1Bn	2An = 2Bn			
L	Н	1An = 1Bn	Z			
Н	L	Z	2An = 2Bn			
Н	Н	Z	Z			

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

 T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-0.5	+7.0	V
I _O	output current	V _O < 0 V	-	±128	mA
I _{IK}	input clamping current	V _{I/O} = 0 V	-50	-	mA
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
T _{amb}	ambient temperature	operating in free air	-40	-	+85	°C

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9. Static characteristics

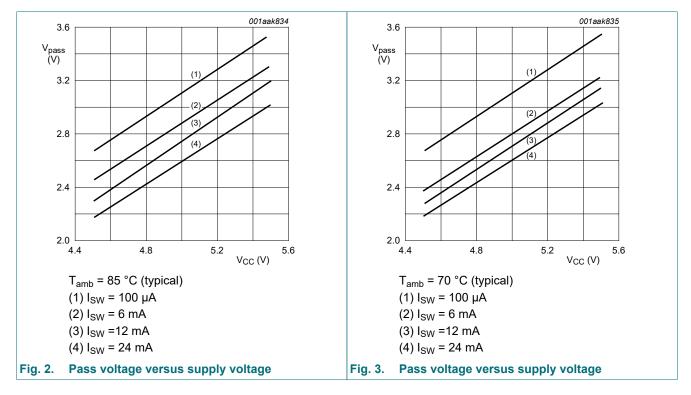
Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

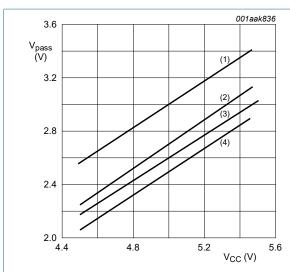
Symbol	Parameter	Conditions		T _{amb} =	+85 °C	Unit	
				Min	Typ[1]	Max	
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _I = -18 mA		-	-	-1.2	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V		-	-	±1	μΑ
I _{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND		-	-	1.5	mA
ΔI _{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	2]	-	-	2.5	mA
V _{pass}	pass voltage	see Fig. 2 to Fig. 6		-	-	-	V
Cı	input capacitance	control pins; V _I = 3 V or 0 V		-	3.2	-	pF
C _{io(off)}	off-state input/output capacitance	port off; $V_I = 3 \text{ V or } 0 \text{ V; } n\overline{OE} = V_{CC}$		-	6.0	-	pF
R _{ON}	ON resistance	$V_{CC} = 4.5 \text{ V}; V_I = 0 \text{ V}; I_I = 64 \text{ mA}$	3]	-	5	7	Ω
		$V_{CC} = 4.5 \text{ V}; V_I = 0 \text{ V}; I_I = 30 \text{ mA}$	3]	-	5	7	Ω
		$V_{CC} = 4.5 \text{ V}; V_I = 2.4 \text{ V}; I_I = -15 \text{ mA}$	3]	-	17	50	Ω

- [1] All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
- [2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
- [3] Measured by the voltage drop between the nAn and the nBn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nAn or nBn) terminals.

9.1. Typical pass voltage graphs



10-bit level shifting bus switch with 5-bit output enables



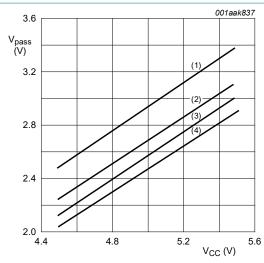
(1)
$$I_{SW} = 100 \mu A$$

(2)
$$I_{SW} = 6 \text{ mA}$$

(3)
$$I_{SW}$$
 =12 mA

(4)
$$I_{SW} = 24 \text{ mA}$$

Fig. 4. Pass voltage versus supply voltage

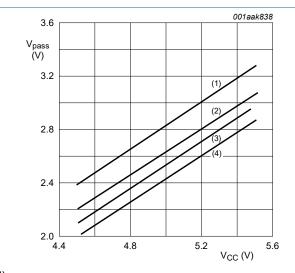


(1)
$$I_{SW} = 100 \mu A$$

(2)
$$I_{SW} = 6 \text{ mA}$$

(4)
$$I_{SW} = 24 \text{ mA}$$

Fig. 5. Pass voltage versus supply voltage



T_{amb} = -40 °C (typical)

(1) $I_{SW} = 100 \mu A$

(2) $I_{SW} = 6 \text{ mA}$

(3) I_{SW} = 12 mA

(4) $I_{SW} = 24 \text{ mA}$

Fig. 6. Pass voltage versus supply voltage;

10-bit level shifting bus switch with 5-bit output enables

10. Dynamic characteristics

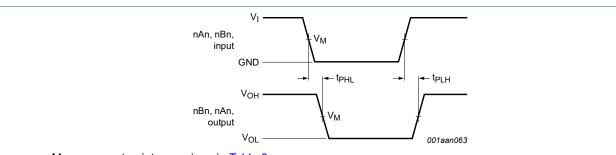
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

Symbol	Parameter	Conditions	T _{amb}	Unit		
			Min	Тур	Max	
t _{pd}	propagation delay	nAn, nBn to nBn, nAn; see Fig. 7 [1]				
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	0.25	ns
t _{en}	enable time	nOE to nAn or nBn; see Fig. 8 [2]				
		V _{CC} = 5.0 V ± 0.5 V	1.2	4.3	7.0	ns
t _{dis}	disable time	nOE to nAn or nBn; see Fig. 8 [2]				
		V _{CC} = 5.0 V ± 0.5 V	1.7	3.0	5.3	ns

^[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

10.1. Waveforms and test circuit



Measurement points are given in <u>Table 8</u>.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times

^[2] t_{pd} is the same as t_{PLH} and t_{PHL} . t_{en} is the same as t_{PZL} and t_{PZH} . t_{dis} is the same as t_{PLZ} and t_{PHZ} .

10-bit level shifting bus switch with 5-bit output enables

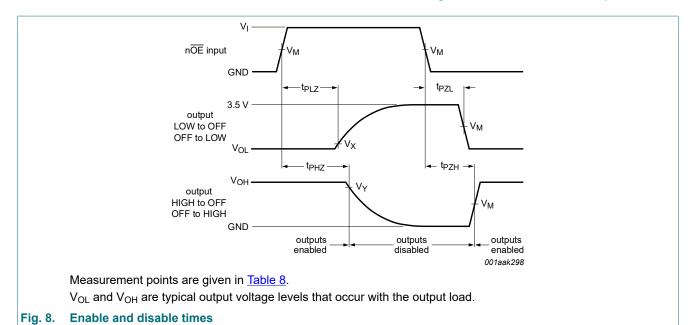
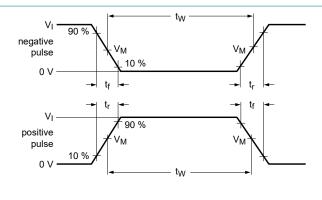
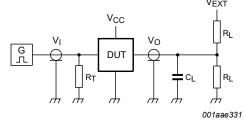


Table 8. Measurement points

Supply voltage	Input		Output					
V _{CC} V _I		V _M	V _M	V _X	V _Y			
$V_{CC} = 5.0 V \pm 0.5 V$	GND to 3.0 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V			

10-bit level shifting bus switch with 5-bit output enables





Test data is given in Table 9.

All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz; $Z_o = 50 \Omega$.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

 V_{EXT} = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

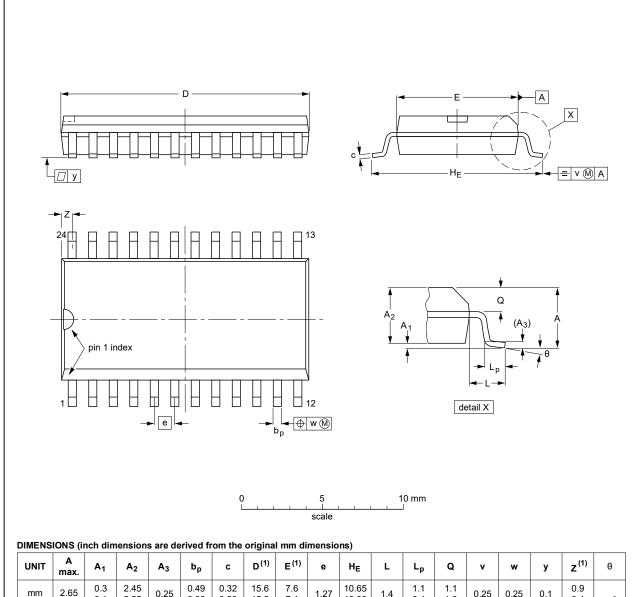
Supply voltage	Input		Load		V _{EXT}			
	V_{l} t_{r}, t_{f}		CL	R_L	t _{PLH} , t _{PHL} t _{PLZ} , t _{PZL} t		t _{PHZ} , t _{PZH}	
$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open	

10-bit level shifting bus switch with 5-bit output enables

11. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



U	NIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
r	nm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
ine	ches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

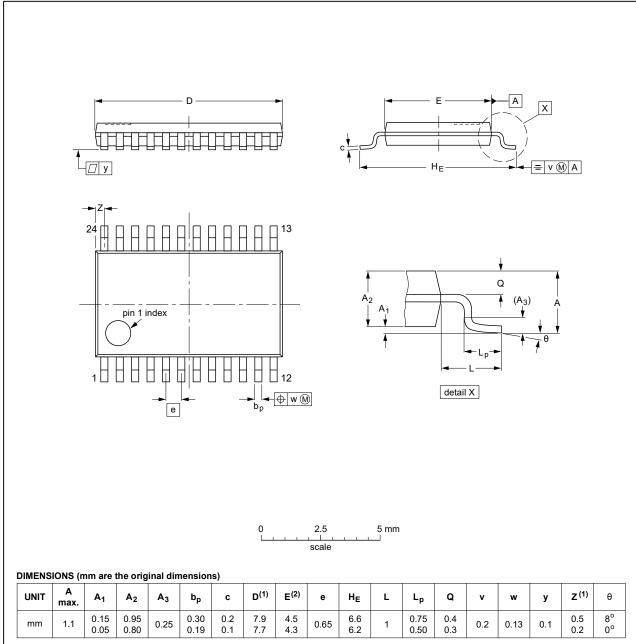
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT137-1	075E05	MS-013				99-12-27 03-02-19	

Fig. 10. Package outline SOT137-1 (SO24)

10-bit level shifting bus switch with 5-bit output enables

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT355-1		MO-153				99-12-27 03-02-19	

Fig. 11. Package outline SOT355-1 (TSSOP24)

10-bit level shifting bus switch with 5-bit output enables

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
НВМ	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
CBTD3384 v.11	20231020	Product data sheet	-	CBTD3384 v.10	
Modifications:	<u>Section 1</u> and <u>Section 2</u> updated.				
CBTD3384 v.10	20210312	Product data sheet	-	CBTD3384 v.9	
Modifications:	Type number CBTD3384DB (SOT340-1 / SSOP24) removed.				
CBTD3384 v.9	20190306	Product data sheet	-	CBT3384 v.8	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number CBTD3384DK (SOT556-1) removed. 				
CBTD3384 v.8	20121212	Product data sheet	-	CBT3384 v.7	
Modifications:	• Table 1: changed +125 °C into +85 °C (errata).				
CBTD3384 v.7	20121119	Product data sheet	-	CBT3384 v.6	
Modifications:	• Table 1: changed +85 °C into +125 °C (errata).				
CBTD3384 v.6	20111121	Product data sheet	-	CBTD3384 v.5	
Modifications:	Legal pages updated.				
CBTD3384 v.5	20101119	Product data sheet	-	CBTD3384 v.4	
CBTD3384 v.4	20011220	Product specification		CBTD3384 v.3	
CBTD3384 v.3	20000830	Product specification	-	CBTD3384 v.2	
CBTD3384 v.2	20000830	Product specification	-	-	

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10-bit level shifting bus switch with 5-bit output enables

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- 2] The term 'short data sheet' is explained in section "Definitions".
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