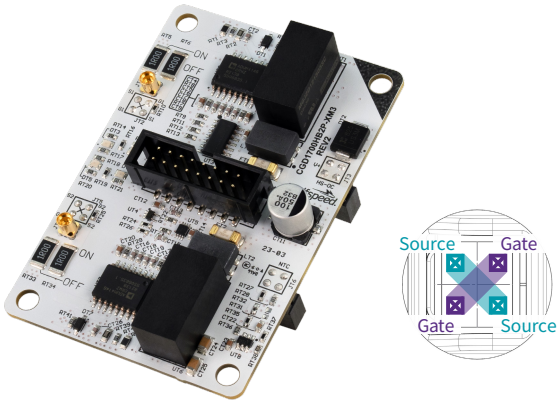
CGD1700HB2P-XM3

Dual Channel Isolated Gate Driver for XM Half-Bridge Modules up to 1700 V

Technical Features

- Optimized for use with Wolfspeed's Cross-Pin XM3 Half-Bridge Power Modules
- High-Frequency Operation, Ultra-Fast Switching Operation
- Secondary UVLO with Hysteresis
- Onboard 2 W Isolated Power Supplies
- Primary OVLO and Reverse Polarity Protection
- Differential Inputs for Increased Noise Immunity
- Increased overcurrent trip level versatility
- Reduced soft-shutdown resistance for faster turn-off during fault



Compatible with Cross-Pin XM Modules

Applications

- DC Bus Voltage up to 1500 V

System Benefits

- Onboard Overcurrent, Shoot-Through, and Reverse Polarity Protection
- Single-Ended to Differential Daughter Board Available (CGD12HB00D)

Maximum Parameters (Verified by Design)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DC}	-0.5 to 13.2	V
Logic Level Input	V_I	-0.5 to 5.5	
Output Peak Current (T_A = 25 °C)	I_o	±10	A
Output Power per Channel (T_A = 25 °C)	P_{Drive}	2	W
Maximum Switching Frequency (Module & MOSFET Dependent, see Power Estimate Section)	f_S	80	kHz
Ambient Operating Temperature	T_{OP}	-40 to 85	°C
Storage Temperature	T_{STG}	-40 to 85	

Rev. 1, January 2023

4600 Silicon Drive | Durham, NC 27703 | Tel: +1.919.313.5300 | wolfspeed.com/power

Gate Driver Electrical Characteristics (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V_{DC}	10.8	12	13.2	V	
Secondary Under Voltage Lockout	V_{UVLO}		11.5	12		
Secondary UVLO Hysteresis	V_{HYS}		0.06			
Over Voltage Clamping	V_{OVLO}	18	20	22		
High Level Logic Input Voltage	V_{IH}	3.5		5.5		Single-Ended Inputs
Low Level Logic Input Voltage	V_{IL}	0		1.5		
Differential Input Common Mode Range	V_{IDCM}		± 2.5	± 7		Differential Inputs
Positive-going input threshold voltage, differential input	V_{IT+}			0.2	V	$V_{ID} = V_{Pos\text{-}Line} - V_{Neg\text{-}Line}$
Negative-going input threshold voltage, differential input	V_{IT-}	-0.2				
Differential Output Magnitude	V_{OD}	2	3.7		V	R_L = 100 Ω
High level Output Voltage	$V_{GATE, HIGH}$		+15			
Low level Output Voltage	$V_{GATE, LOW}$		-4			
Working Isolation Voltage	V_{IOWM}		1500			V_{RMS}
Isolation Capacitance	V_{ISO}		4.9		pF	Per Channel
Common Mode Transient Immunity	CMTI	100			kV/µs	V_{CM} = 1500 V
Output Resistance[1]	$R_{G(IC)-ON}$		0.48	0.98	Ω	Gate Driver Buffer Tested at 1 A
	$R_{G(IC)-OFF}$		0.47	0.81		
External Turn-On Resistance[2]	$R_{G(EXT)-ON}$		1			External SMD Resistor 2512 (6432 Metric)
External Turn-Off Resistance[2]	$R_{G(EXT)-OFF}$		1			
Output Rise Time	t_{ON}		223		ns	$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF From 10% to 90%
Output Fall Time	t_{OFF}		208			
Propagation Delay (Turn-Off)	t_{PHL}		120			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 0 nF From 50 % to 50 %
Propagation Delay (Turn-On)	t_{PHL}		125			
Over-current Blanking Time	t_{Blank}		600			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Over-current Propagation Delay to FAULT Signal Low	$t_{PD-FAULT}$		1.3		µs	Does Not Include Blanking
Soft-Shutdown Time	t_{SS}		1.3			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Soft-Shutdown Resistance[3]	R_{SS}		5		Ω	Tested at 25 mA
Miller Clamp Resistance	R_{MC}		1.1	2.75		Tested at 100 mA
Miller Clamp Voltage Threshold	V_{MC}	1.75	2	2.25	V	Referenced to Source

1 Output resistance of gate driver IC.

2 Additional output resistance is added with SMD resistors. Separate resistors to turn-on and turn-off allowing

3 Soft-Shutdown network will safely turn off the gate in the event an over current is detected

Input Connector Information

Pin Number	Parameter	Description
1	V_{DC}	Power supply input pin (+12 V Nominal Input)
2	Common	Common
3	HS-P (*)	Positive line of 5 V differential high-side PWM signal pair. Terminated Into 120 Ω.
4	HS-N (*)	Negative line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
5	LS-P (*)	Positive line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
6	LS-N (*)	Negative line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
7	$\overline{\text{FAULT-P}}$ (*)	Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA. A low state on FAULT indicates when a desaturation fault has occurred. The presence of a fault precludes the gate drive output from going high.
8	$\overline{\text{FAULT-N}}$ (*)	Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA.
9	RTD-P (*)	Positive line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via frequency.
10	RTD-N (*)	Negative line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via frequency.
11	$\overline{\text{PS-Dis}}$	Pull down to disable power supply. Pull up or leave floating to enable. Gate and source are connected with 10 kΩ when disabled.
12	Common	Common
13	PWM-EN	Pull down to disable PWM input logic. Pull up or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled.
14	Common	Common
15	Reset	When a fault exists, bring this pin high to clear the fault.
16	Common	Common

* Inputs 3-10 are different differential pairs

Signal Description

- **PWM Signals:** High-side and low-side PWM are RS-422 compatible differential inputs. The termination impedance of the differential receiver is 120 Ω. Overlap protection is provided to prevent both the high-side and low-side gates from turning on simultaneously. The overlap protection should not be used as a dead time generator.

- **FAULT Signal:** The fault signal is a RS-422 compatible differential output with a maximum drive strength of 20 mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. This signal will be low if an over-current fault or UVLO fault condition is detected on either channel. A red LED will indicate a fault condition. The LED, DT4, indicates a high-side fault and DT6 indicates a low-side fault.

- **UVLO Fault:** The UVLO circuit detects when the output rails of the isolated DC/DC converter fall below safe operating conditions for the gate driver. A UVLO fault indicates that the potential between the split output rails has fallen below the UVLO active level. The gate for the channel where the fault occurred will be pulled low through R_G for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. There is hysteresis for this fault to ensure safe operating conditions. The UVLO faults for both channels are combined along with the over-current fault in the FAULT output signal. When there is no UVLO fault present, a green LED indicates a power good state. The LED, DT3, indicates a high-side power good status and DT5 indicates a low-side power good status.

- **Over-Current Fault:** An over-current fault is an indication of an over-current event in the SiC power module. The over-current protection circuit measures the drain-source voltage, and the fault will indicate if this voltage has risen above a level corresponding to the safe current limit. When a fault has occurred the corresponding gate driver channel will be disabled, and the gate will be pulled down through a soft-shutdown resistor, R_{SS}. The drain-source limit can be configured through on-board resistors. The over-current fault is latched upon detection and must be cleared by the user with a high pulse of at least 500 ns on the RESET signal.

- **RTD (NTC):** RTD output is a differential signal that returns the resistance of the temperature sensor (NTC) integrated into XM3 modules. The signal is a frequency modulated signal that encodes the resistance of the temperature sensor. The approximate temperature of the module can be determined from this resistance. See the section RTD (NTC) Temperature Feedback for further details.

- **PS-DIS:** The PS-DIS signal disables the output of the isolated DC/DC converters for the two channels. It is a single-ended input that must be pulled low to turn off the power supplies. With the power supplies disabled the gate will be held low with a 10 kΩ resistor. This signal can be used for startup sequencing.

- **PWM-EN:** This is a single-ended input that enables the PWM inputs for both channels. When this signal is pulled down the differential receivers for both channels are disabled and the gates will both be pulled low through $R_{GEXT-OFF}$. All protection circuitry and power supplies will continue to operate including FAULT and RTD outputs.

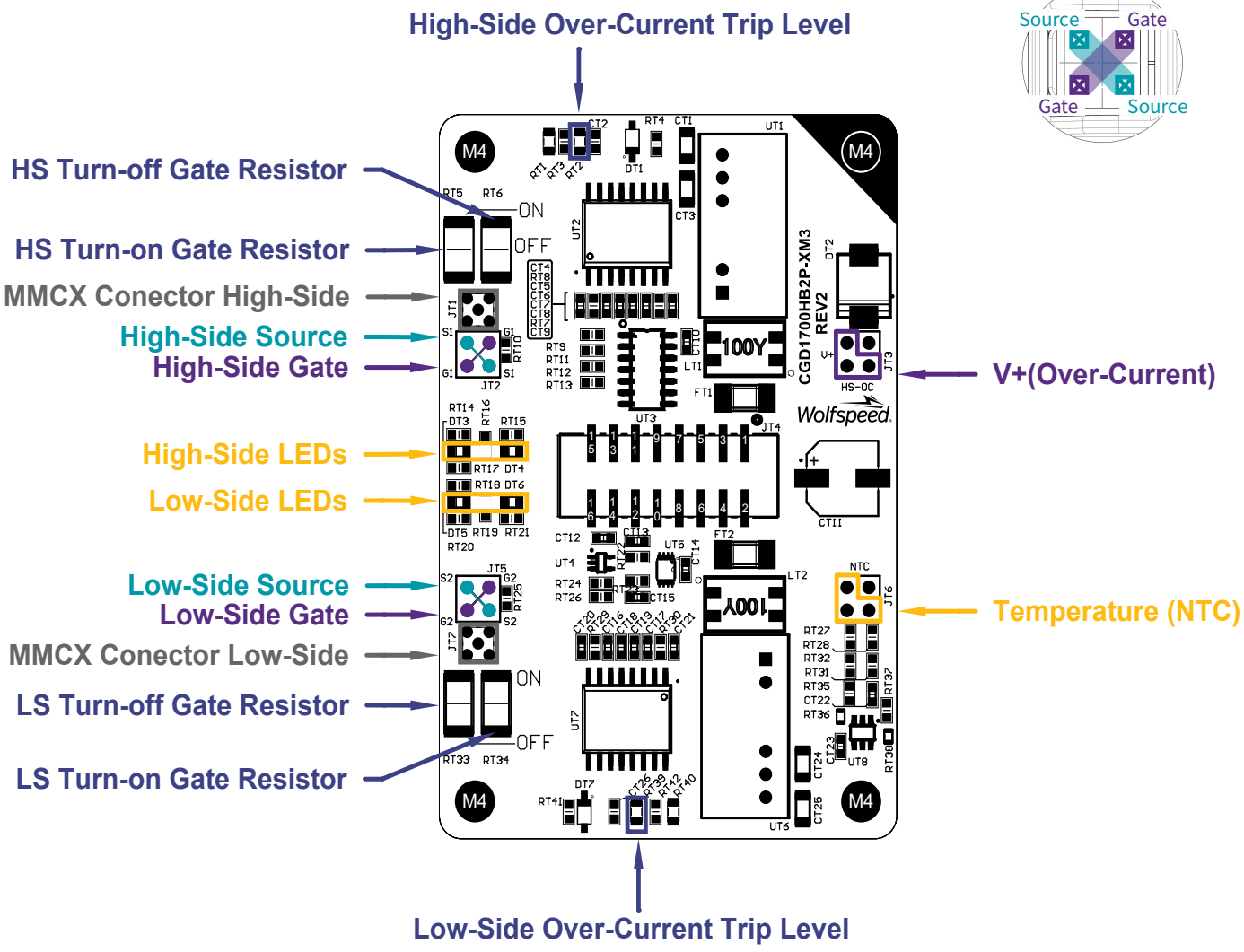
- **Over-Voltage and Reverse Polarity Protection:** Power input on pin 1 of gate driver connector features a power management IC to protect the gate driver from damage by connecting a power source that exceeds the voltage rating of the gate driver or if the current limit is exceeded. There is also a diode and MOSFET in-line with the power input to protect against connecting a power source with positive and negative polarity reversed.

Truth Table

PWM	$\overline{\text{PWM-EN}}$	PS-DIS	RESET	Overcurrent/ UVLO	$\overline{\text{FAULT}}$	Output
H	H or Z	H or Z	L	No	H	H
L	H or Z	H or Z	L	No	H	L
X	L	H or Z	L	No	H	L
X	X	L	X	No	L	Z
X	H or Z	H or Z	L	Yes	L	L

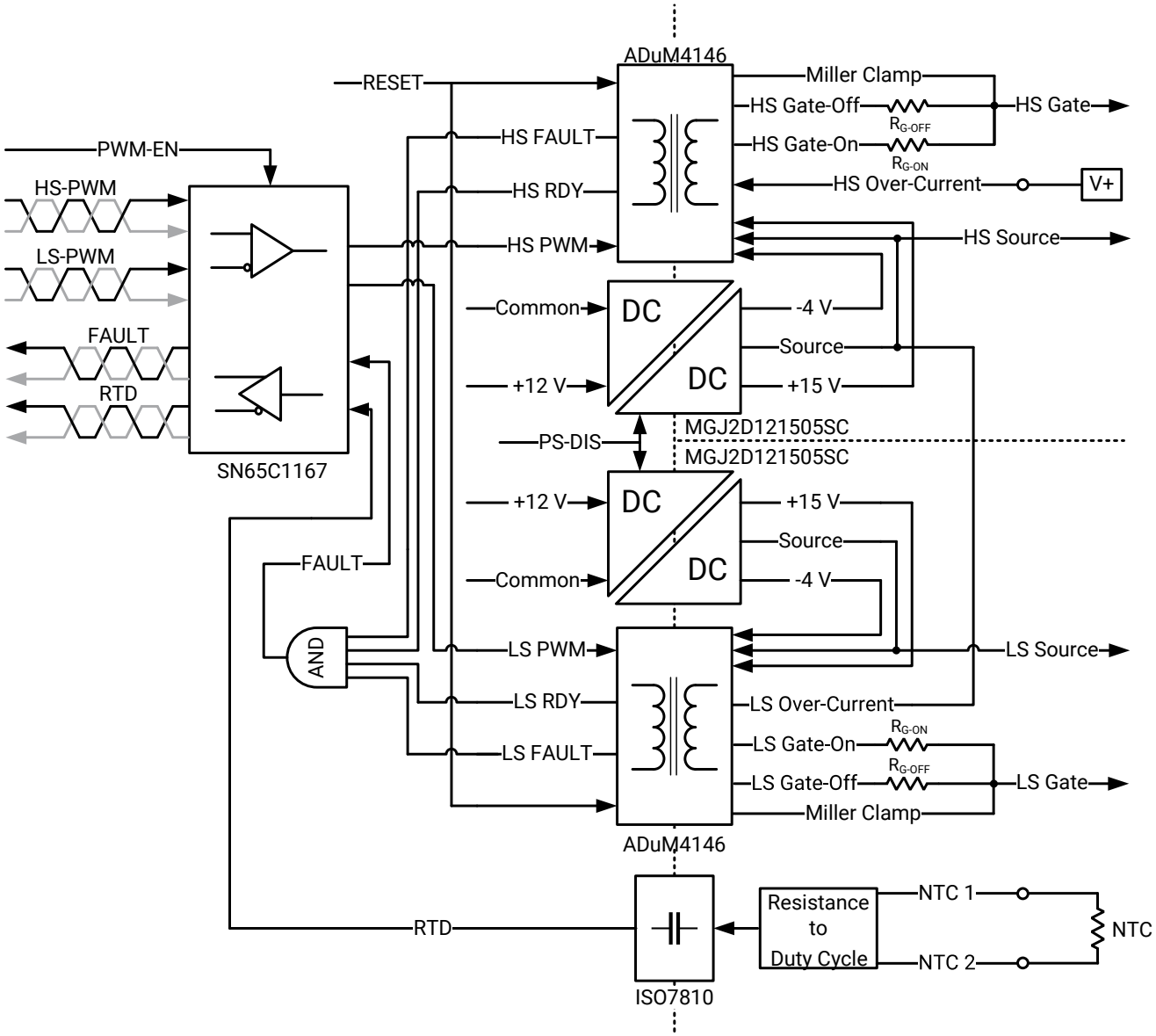
H = High | L = Low | X = Irrelevant | Z = High Impedance

Gate Driver Interface



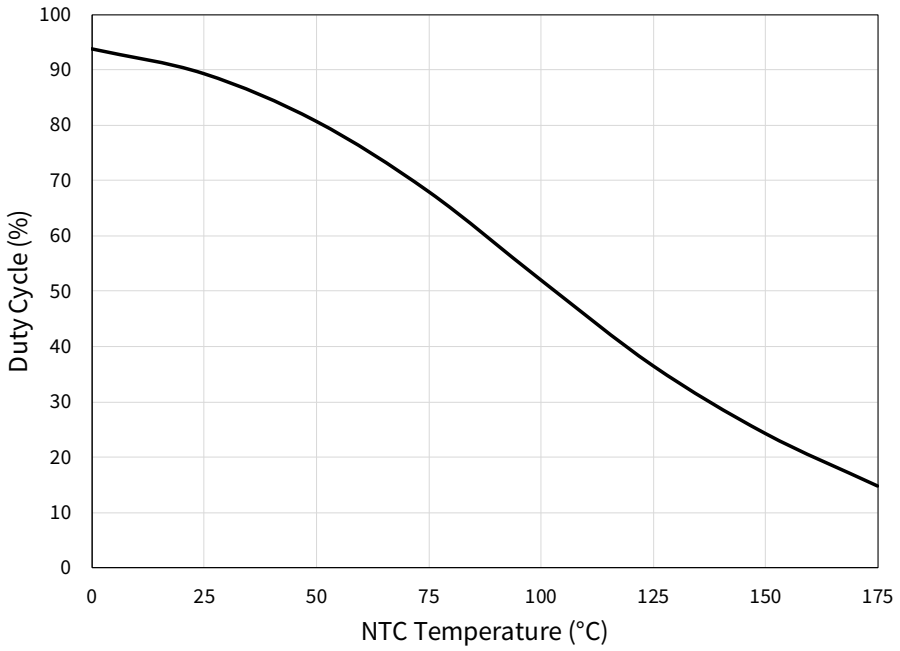
Zoom View of Signal Pinout

Function Block Diagram



RTD (NTC) Temperature Feedback

The resistance measurement of the XM3 power module's NTC is available on the input connector of the gate driver as a differential pair on pins 9 and 10. The NTC resistance is converted to a pulse width modulated (PWM) square. The temperature to duty cycle relationship is displayed in the table below. The NTC measurement circuit is located on the low-side gate drive channel, and a digital isolator is used to transmit the duty cycle-encoded signal back to the primary side of the driver. For this reason, the NTC signal does not need any additional isolation, and can be included in the same ribbon cable as the rest of the gate driver's signals. The temperature reported by the NTC differs largely from the junction temperature of the SiC MOSFETs and should not be used as an accurate junction temperature measurement.



NTC Temperature vs. Duty Cycle

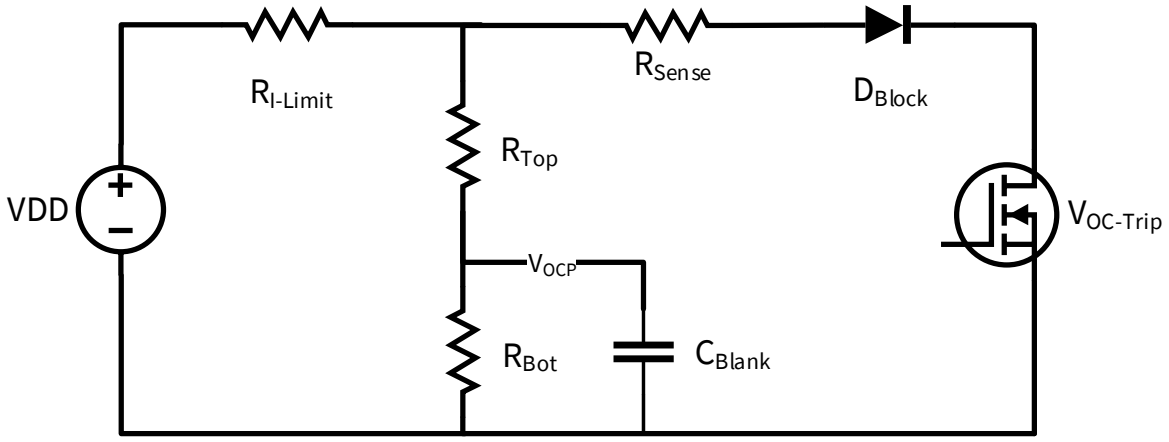
NTC Temperature (°C)	NTC Resistance (Ω)	Duty Cycle (%)
0	13,491	93.8
25	4,700	89.3
50	1,928	80.7
75	898	68.0
100	464	52.0
125	260	36.5
150	156	24.3
175	99	14.8

Over-Current Trip Level

The over-current (OC) fault detection circuit measures the on-state V_{DS} voltage across each switch position and triggers a fault condition if the voltage rises above a set level. The internal comparator trip voltage in the ADuM4146C gate driver IC is 3.5 V. Considering the forward voltage of the high-voltage blocking diodes, the over-current trip level can be approximated with the following equation:

$$V_{OC\text{-}Trip} = (3.5V - 2V_F) * (R_{Bot}/(R_{Top} + R_{Bot}))$$

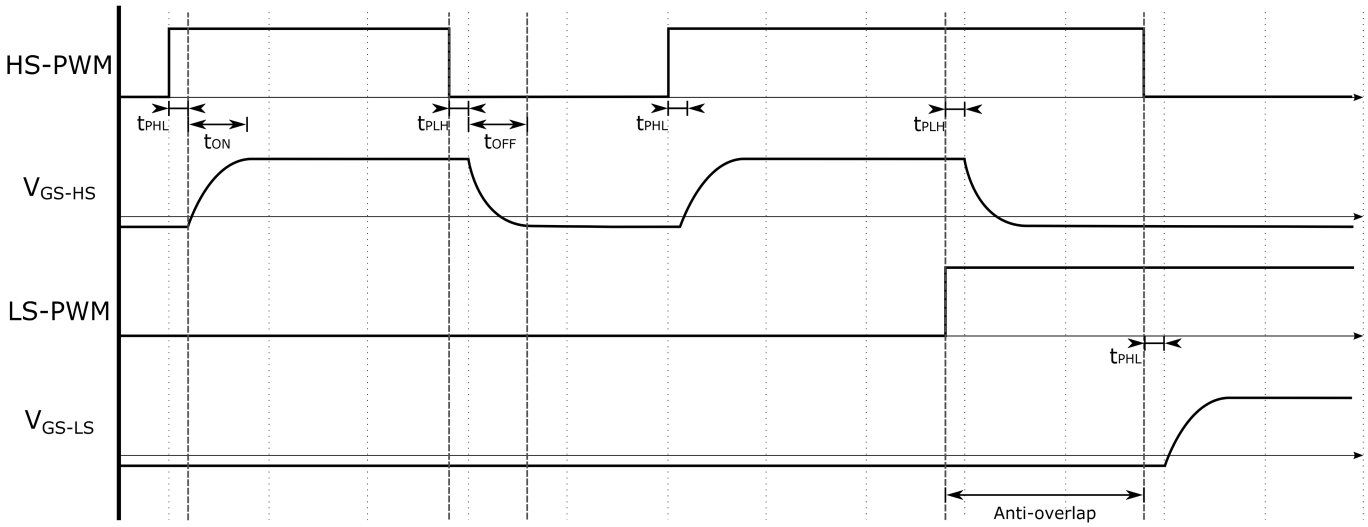
where the forward voltage of the high-voltage diodes, V_F, is approximately 0.5 V. As shipped, the over-current trip level is 5.1 V.



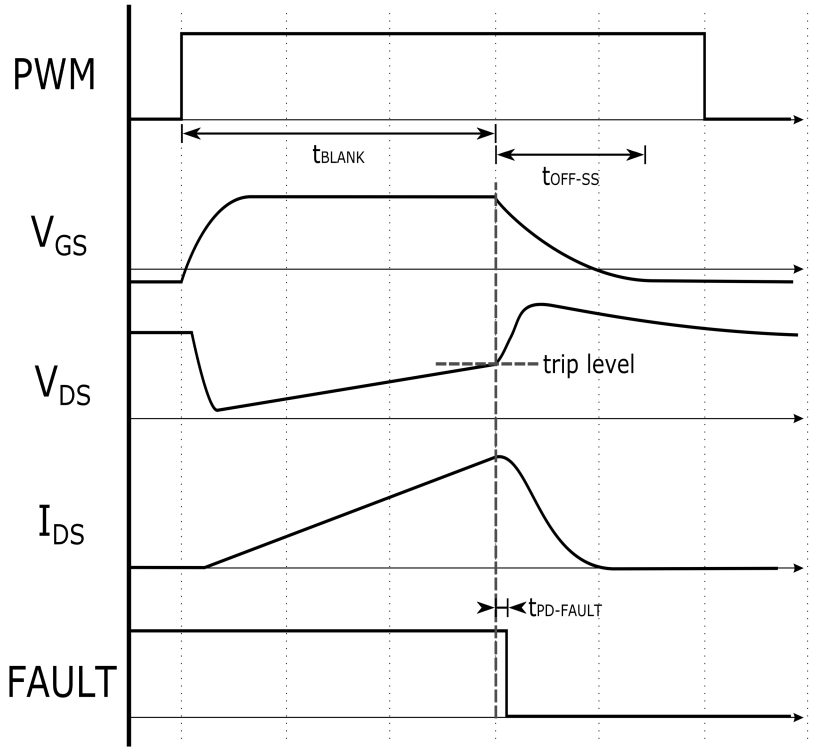
To select an appropriate over-current trip level, refer to the I_D vs. V_{DS} output characteristic curves in the module datasheet. As an example, the pulse-current rating of the CAB320M17XM3 is 640 A; therefore, an over-current trip point of 600 A at 175 °C is selected. On the I_D vs. V_{DS} curve, the drain-to-source voltage at the 600 A operating condition is approximately 5.1 V. Hence, the over-current trip voltage, $V_{OC\text{-}Trip}$, should be approximately 5.1 V, which can be used to calculate the required resistor values with the equation above.

The HS-OC connector, JT3, cannot be left floating as the over-current fault will trip immediately when the high-side gate is actuated. If bench-top testing of the gate driver is required, it is acceptable to short the HS-OC connection to the high-side source to prevent the over-current fault from tripping. The same phenomenon exists for the low-side, and it is acceptable to short the high-side source (low-side drain) to the low-side source for bench-top testing. The over-current fault condition must be acknowledged with the Reset signal to remain normal operation of the gate driver.

Timing Information



Gate Timing Diagram



Over-Current Protection Timing Diagram

Input Connector Information

- 16 Positions Header, 0.100” (2.54 mm) Pitch, Through Hole, Gold (SBH11-PBPC-D08-ST-BK)

Suggesting Mating Parts

- 16 Position Rectangular Header, IDC, Gold, 28 AWG (SFH210-PPPC-D08-ID-BK)
- 16 Position Header, 0.100” (2.54 mm) Pitch, Through Hole, Gold (SFH11-PBPC-D08-RA-BK)
- 16 Position Header, 0.100” (2.54 mm) Pitch, Through Hole, Right Angle, Gold (SFH11-PBPC-D08-RA-BK)

Output Connector Information

- 4 Positions Header, 0.100” (2.54 mm) Pitch, Through Hole, Gold (Samtec® ESQ-102-33-L-D)

Power Estimates

The gate driver power required is calculated using the formula below. The gate charge is dependent on the datasheets of the module being driven. Once the required gate driver power is calculated, the required input power can be calculated from the efficiency curves on the power supplies datasheet. This calculation is for one channel of the gate driver.

$$P_{SW} = Q_G * F_{SW} * \Delta V_{PS}$$

P_{SW}: gate driver power (per channel)

Q_G: total gate charge (MOSFET gate charge × number of MOSFETs per switch position)

F_{SW}: switching frequency

ΔV_{PS}: difference in isolated power supply voltage rails ($V_{PS,HIGH}$ - $V_{PS,LOW}$)

Example:

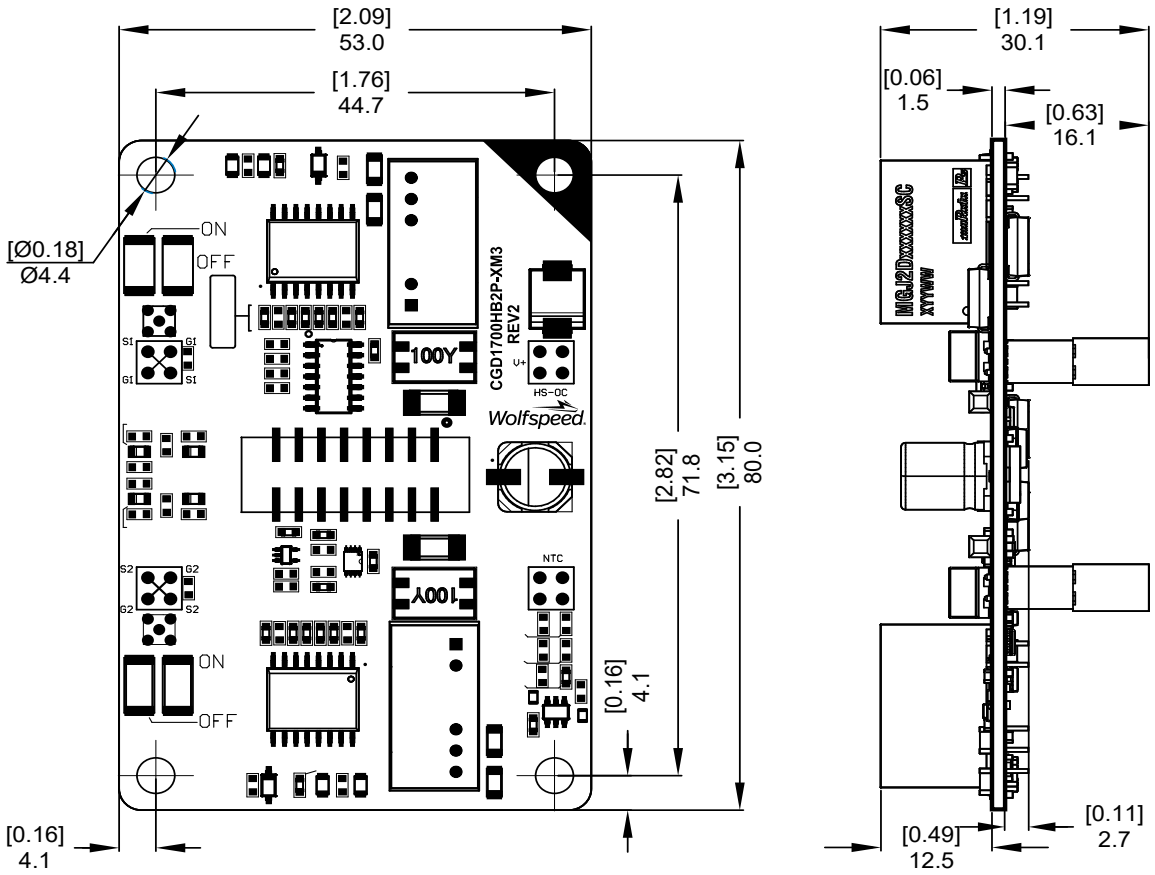
Calculate the maximum switching frequency for CAB320M17XM3.

P_{SW}	2 W (rated output power of isolated power supply on gate driver)
Q_G	1245 nC (provided in CAB320M17XM3 datasheet)
$V_{PS,HIGH}$	15 V (isolated power supply’s positive output voltage)
$V_{PS,LOW}$	-5 V (isolated power supply’s negative output voltage)
ΔV_{PS}	20 V

$$2\ W = 1245\ nC * F_{SW} * 20\ V$$

$F_{SW\text{-}Max} \approx$ 80 kHz with margin

Dimensions



Dimensions ([in] mm)

Supporting Links & Tools

Evaluation Tools & Support

- XM Module Product Family
- KIT-CRD-CIL17N-XM: Dynamic Performance Evaluation Board for the XM Modules
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum

Dual-Channel Gate Driver Board

- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- PRD-04814: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies